
Proceedings Paper:
Hoang, K.D. orcid.org/0000-0001-7463-9681 and Wang, J. orcid.org/0000-0003-4870-3744 (2012) Design Optimization of High Frequency Transformer for Dual Active Bridge DC-DC Converter. In: XXth International Conference on Electrical Machines (ICEM). XXth International Conference on Electrical Machines, 02 - 05 September, 2012, Marseille, France. IEEE , pp. 2311-2317. ISBN 978-1-4673-0142-8

https://doi.org/10.1109/ICElMach.2012.6350205

Design Optimization of High Frequency Transformer for Dual Active Bridge DC-DC Converter

K. D. Hoang and J. Wang

***Abstract* -- This paper presents a design optimization procedure for high frequency transformer (HFT) employed in bidirectional dual active bridge (DAB) isolated DC-DC converter. It is shown that leakage inductance, phase-shifted angle, skin and proximity effects have to be taken into account together with the HFT voltage-ampere rating to minimize total losses. It is also demonstrated that the leakage inductance required for zero voltage switching operation can be realized under the proposed design procedure without employing extra inductor. The proposed design methodology is experimentally validated by measurements on a prototype HFT.**

***Index Terms*--AC losses, converter losses, design optimization, dual active bridge DC-DC converter, eddy current effects, high frequency transformer, Litz-wire, MOSFET, zero voltage switching operation.**

I. Introduction

RECENTLY, investigations in high-power DC-DC conversion have been significantly increased due to its essential role in electric vehicle applications and battery based energy storage systems [1], [2]. Among DC-DC converter topologies, bidirectional dual active bridge (DAB) isolated DC-DC converter [3], [4] shown in Fig. 1(a) is often considered as a preferred candidate for such applications because of its advantages on galvanic isolation, switching loss reduction, electromagnetic interference (EMI) improvement, and efficiency gain. Generally, this topology consists of two voltage source active bridges linked by a galvanically isolated high-frequency transformer (HFT). Each bridge is controlled to produce a high-frequency square wave voltage at its transformer terminals and the power flow from one DC source to the other is regulated via appropriately controlling the phase-shifted angle between these two square wave voltages [4].

It is desirable for a DAB isolated DC-DC converter to operate at high switching frequency to achieve high-power density and light-weight. However, it is essential that soft-switching techniques with zero or low switching losses are employed. In [4], it was demonstrated that leakage inductance value of the isolated HFT needs to be carefully selected for zero voltage switching (ZVS). As leakage inductance under the HFT design is normally minimized for conducting loss reduction, additional inductors were utilized [4] which results in increase in HFT size and weight.

On the other hand, based on the primary referred equivalent circuit of the DAB isolated DC-DC converter shown in Fig. 1(b) [3], it is evident that the power transfer via the HFT in the DC-DC converter relies on both its leakage inductance and the phase-shifted angle between its terminal square wave voltages. As a result, there is always a trade-off between the leakage inductance and the phase-shifted angle when maximizing the power conversion.

Additionally, at high switching frequency, high AC losses in the HFT windings are inevitable due to the skin- and proximity-effects [5], [6], and [7]. The leakage inductance and the magnitude of the AC loss are influenced by the transformer geometry and winding layout. Therefore, the leakage inductance, phase-shifted angle, and the skin and proximity effects need to be taken into consideration in the HFT design procedure for minimizing electrical losses.

In [8], [9], [10], [11], and [12], design procedures for high frequency transformer (HFT) were presented. However, all these proposed methods start with the core dimensions being determined based on voltage-ampere (VA) rating of the transformer. The winding arrangement based on selected core dimensions is subsequently suggested. As a result, the influence of leakage inductance and phase-shifted angle on the design are neglected under these conventional design methodologies.

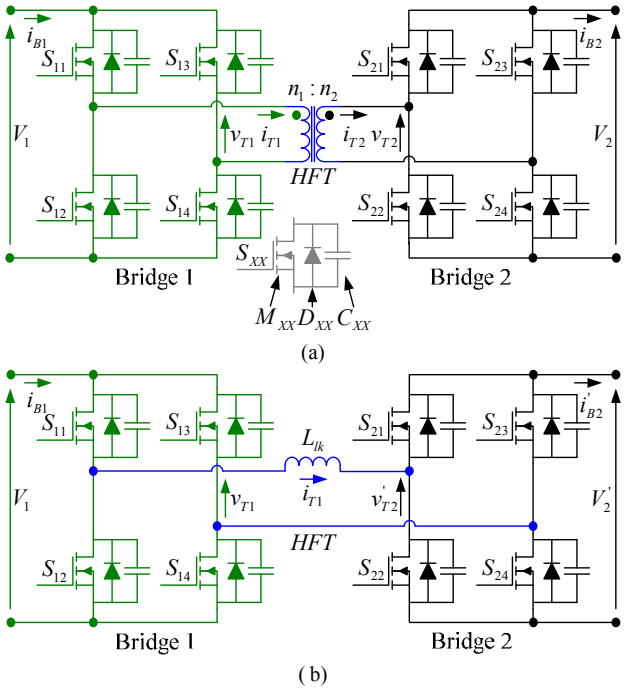

Fig. 1. DAB DC-DC converter [3]; each switch S_{XX} is implemented by a power MOSFET M_{XX}, a diode D_{XX}, and a snubber capacitor C_{XX}; i_{B1}-V_1 and i_{B2}-V_2 are, respectively, the primary and secondary DAB current-voltage; i_{T1}-v_{T1} and i_{T2}-v_{T2} are, respectively, the primary and secondary HFT current-voltage. (a) Topology. (b) Primary referred equivalent circuit.

This paper presents a design optimization procedure for HFT which takes into consideration the leakage inductance, phase-shifted angle, skin and proximity effects for minimizing total losses of DAB isolated DC-DC converter. The proposed design method is experimentally validated by measurements on a prototype HFT.

This work was supported in part by the European Commission under Grant No. 260087.

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II. PRINCIPLES OF DAB DC-DC CONVERTER OPERATION

A. Operation of DAB DC-DC Converter

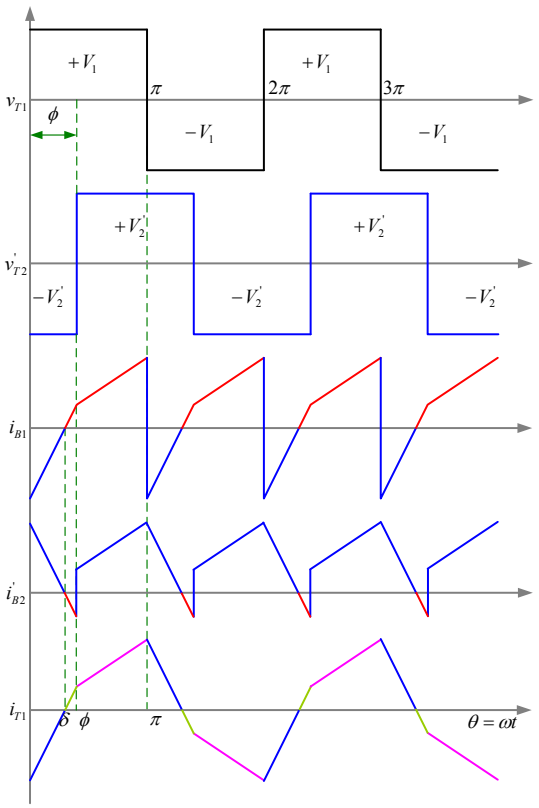


Fig. 2. Idealized operating waveforms for DAB DC-DC converter [3]; ω is the angular frequency; δ is the current zero-crossing angle; and ϕ is the phase-shifted angle.

TABLE I CONDUCTION MODE OF DAB DC-DC CONVERTER

$0 < \theta \le \delta$		$\delta < \theta \le \phi$		$\phi < \theta \le \pi$	
Bridge 1	Bridge 2	Bridge 1	Bridge 2	Bridge 1	Bridge 2
D_{11-14}	D_{22-23}	M_{11-14}	M_{22-23}	M_{11-14}	D_{21-24}

Assuming that the power is transferred from bridge 1 to bridge 2 as denoted in Fig. 1(b), idealized operating waveforms and conduction mode of a DAB isolated DC-DC converter [3] can be illustrated in Fig. 2 and Table I, respectively. Based on these operating waveforms, instantaneous value of HFT current, $i_{T1}=i(\theta)$, can be computed from the current slope associated with the conducting modes $A=\frac{V_1+V_2'}{\omega L_{lk}}$; $B=\frac{V_1-V_2'}{\omega L_{lk}}$ as follows.

For $0 < \theta \le \delta$ (mode 1)

$$i(\theta) = A\theta + I_0 \tag{1}$$

$$I_{rms1}^2 = \frac{1}{2\pi}\left(\frac{A^2}{3}\delta^3 + AI_0\delta^2 + I_0^2\delta\right) \tag{2}$$

$$I_{av1} = \frac{1}{2\pi}\left(\frac{A}{2}\delta^2 + I_0\delta\right) \tag{3}$$

For $\delta < \theta \le \phi$ (mode 2)

$$i(\theta) = A(\theta - \delta) \tag{4}$$

$$I_{rms2}^2 = \frac{1}{2\pi}\left[\frac{A^2}{3}(\phi^3 - \delta^3) - A^2\phi\delta(\phi - \delta)\right] \tag{5}$$

$$I_{av2} = \frac{1}{2\pi}\frac{A}{2}(\phi - \delta)^2 \tag{6}$$

For $\phi < \theta \le \pi$ (mode 3)

$$i(\theta) = B(\theta - \phi) + I_\phi \tag{7}$$

$$I_{rms3}^2 = \frac{1}{2\pi}\left[\frac{B^2}{3}(\pi^3 - \phi^3) + (I_\phi - \phi B)(\pi - \phi)(I_\phi + \pi B)\right] \tag{8}$$

$$I_{av3} = \frac{1}{2\pi}\left[\frac{B}{2}(\pi^2 - \phi^2) + (I_\phi - \phi B)(\pi - \phi)\right] \tag{9}$$

$$I_{T1rms} = \sqrt{2(I_{rms1}^2 + I_{rms2}^2 + I_{rms3}^2)} \tag{10}$$

$$I_0 = -\frac{V_1}{2\omega L_{lk}}[\pi + d(2\phi - \pi)] = -I_\pi \tag{11}$$

$$P_O = \frac{V_1'^2}{\omega L_{lk}} d\phi\left(1 - \frac{\phi}{\pi}\right) \tag{12}$$

$$d = \frac{V_2'}{V_1} = N\frac{V_2}{V_1};\ N = \frac{n_1}{n_2};\ \delta = -\frac{I_0}{A} \tag{13}$$

where d is the conversion ratio; $i(\theta)$ is the instantaneous HFT current at the angular θ; I_0 and I_π is, respectively, the HFT current at $\theta = 0$ and $\theta = \pi$; I_{avi} and I_{rmsi} is, respectively, the average and rms values of HFT current associated with the ith conduction mode; I_{T1rms} is the total rms value of HFT current; L_{lk} is the leakage inductance; N is the turn ratio; n_1 and n_2 is, respectively, the primary turn number and secondary turn number; P_O is the transferred power; V_1 and V_2' is, respectively, the primary voltage value and secondary voltage referred primary.

Zero voltage switching occurs when an active switch in the DAB is turned on while its anti-parallel diode is free-wheeling. Thus the condition for ZVS operation is given by:

$$I_0 < 0;\ I_\phi > 0 \tag{14}$$

B. Conduction and Switching Losses of DAB DC-DC Converter

Due to its fast switching characteristics, MOSFET is often selected for DAB isolated DC-DC converters. According to [9] and [13], the conduction and switching losses of one MOSFET device of the converter can be expressed as:

For $0 < \theta \le \delta$ (mode 1)

$$P_{Dpri.1} = V_D I_{Fav} + R_D I_{Frms}^2 + f_s E_{Doff} \tag{15}$$

$$P_{D\sec.1} = V_D N I_{Fav} + R_D N^2 I_{Frms}^2 + f_s E_{Doff} \tag{16}$$

For $\delta < \theta \le \phi$ (mode 2)

$$P_{Mpri.2} = R_M I_{Mrms}^2 + f_s E_{Mon} \tag{17}$$

$$P_{M\sec.2} = R_M N^2 I_{Mrms}^2 + f_s (E_{Mon} + E_{Moff}) \tag{18}$$

For $\phi < \theta \le \pi$ (mode 3)

$$P_{Mpri.3} = R_M I_{Mrms}^2 + f_s E_{Moff} \tag{19}$$

$$P_{D\sec.3} = V_D N I_{Fav} + R_D N^2 I_{Frms}^2 \tag{20}$$

$$E_{Mon} = \frac{(t_{ri} + t_{fv})}{2} V_{DSon} I_{Mon} + V_{DSon} Q_{rr} \tag{21}$$

$$E_{Moff} = \frac{(t_{rv} + t_{fi})}{2} V_{DSoff} I_{Moff} \tag{22}$$

$$E_{Doff} = V_{DSon} Q_{rr} \tag{23}$$

$$P_{S.Loss\Sigma} = 4(P_{Dpri.1} + P_{Mpri.2} + P_{Mpri.3} + P_{D\sec.1} + P_{M\sec.2} + P_{D\sec.3}) \tag{24}$$

where E_{Doff} is the reverse recovery charge energy of free-wheeling diode; E_{Mon} and E_{Moff} is, respectively, the switch-

on and switch-off energy of the MOSFET; f_s is the switching frequency; I_{Fav} and I_{Frms} is, respectively, the average and rms forward current of the free-wheeling diode; I_{Mon} and I_{Moff} is, respectively, the MOSFET current at on-state and off-state; I_{Mrms} is the rms value of the MOSFET current; P_D and P_M is, respectively, the switching losses of the free-wheeling diode and MOSFET; $P_{S.Loss\Sigma}$ is the total conduction and switching losses; Q_{rr} is the reverse recovery charge; R_D and R_M is, respectively, the free-wheeling diode and the MOSFET on-state resistance; t_{ri}, t_{fi}, and t_{rv}, t_{fv} is, respectively, the MOSFET current and voltage rise-time and fall-time; V_D is the freewheeling diode forward voltage drop; V_{DSon} and V_{DSoff} is, respectively, the MOSFET Drain-Source voltage at on-state and off-state.

For completeness, aforementioned definitions for switching loss calculation are diagrammatically represented in Fig. 3 [13]. Appropriate currents expressed in (1) to (11) are employed to compute the converter conduction and switching losses. It is worth noting that for the ZVS operation, E_{Doff} and E_{Mon} become zero.

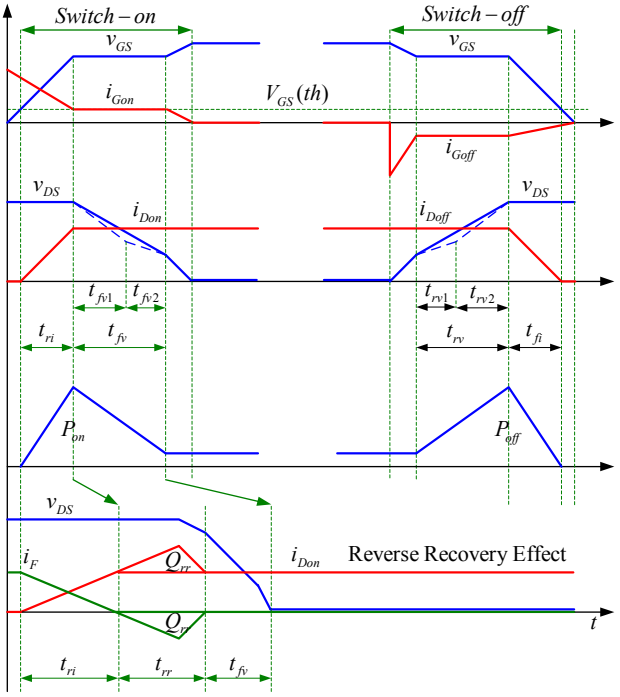


Fig. 3. Switching losses of power MOSFET [13].

In the next section, the conduction and switching loss model is utilized for optimizing HFT design with particular emphasis on minimizing the total losses in the HFT and DAB.

III. OPTIMIZED HFT DESIGN

The objective of the HFT design is to find the optimal values of the leakage inductance, phase-shifted angle, core dimensions, turn ratio, and winding information in order to minimize the total converter losses, $P_{C.Loss\Sigma}$, (conduction and switching losses, winding losses, and core losses) of the DAB isolated DC-DC converter. Normally, for high switching frequency applications, ferrite core should be selected to eliminate eddy current loss in the core [14]. The design specification of the HFT is shown in Table II. The output voltage range from 90V to 140V corresponds to the variation of battery voltage when the converter is used as a bidirectional battery charger. The chosen switching device is a power MOSFET (STW55NM60ND) which is recommended for bridge topologies, in particular, ZVS phase-shifted converters [15]. The design process can be categorized into 4 steps as follows.

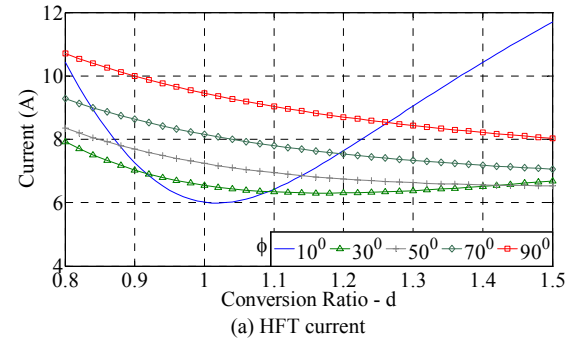
TABLE II DESIGN SPECIFICATION OF HFT

Output power	2.2kW
Input voltage	380V
Output voltage	90-140V
Nominal output voltage	120V
Switching frequency	40kHz
Flux density in the core, Bmax	0.25T
Switching device	STW55NM60ND [15]

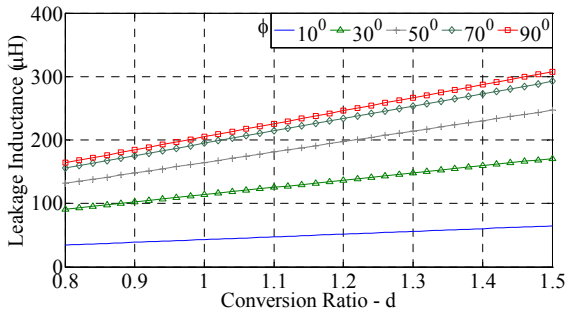
A. Step 1: Optimal Phase-shifted Angle

The phase-shifted angle of the DAB isolated DC-DC converter varies from 0 to 90 degrees [4], Fig. 2. Therefore, for the given design specification P_O = 2.2kW, V_1 = 380V, and f_s = 40kHz, the phase-shifted angle ϕ is varied from 0 to 90 degrees to minimize HFT current associated with a given output voltage. Since the output voltage varies from 90V to 140V, which corresponds to the conversion ratio d varies from 0.8 to 1.5. For each value of ϕ, the resultant leakage inductance for the power transfer and the HFT current are computed, respectively, using (12) and (10).

Fig. 4(a) shows that a phase-shifted angle around 30 degrees can result in minimum HFT current for a full-range conversion ratio from 0.8 to 1.5. Fig. 4(b) illustrates the variation of the leakage inductance from 90µH to 170µH when d varies from 0.8 to 1.5 for the phase-shifted angle of 30 degrees.



(a) HFT current



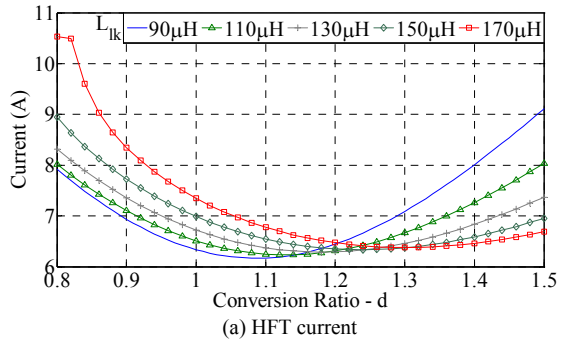
(b) Leakage inductance

Fig. 4. Variation HFT current and leakage inductance with phase-shifted angle and conversion ratio.

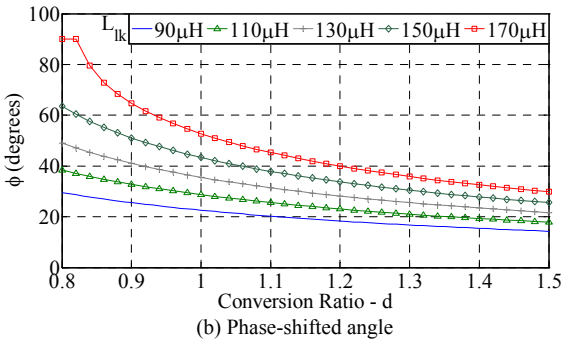
B. Step 2: Optimal Leakage Inductance and Conversion Ratio

In step 2, for a given leakage inductance value between 90µH and 170µH, P_O = 2.2kW, V_1 = 380V, and f_s = 40kHz, the variations of phase-shifted angle, HFT current, and ZVS operation range with the conversion ratio d (0.8~1.5) are investigated according to (12), (10), and (14).

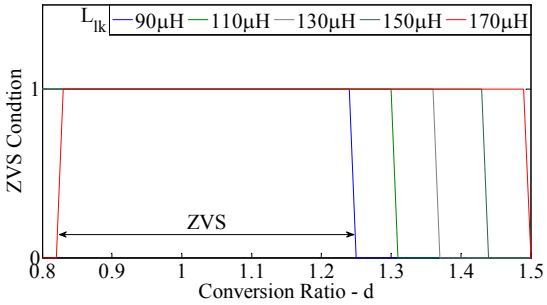
Fig. 5(a) shows that when the leakage inductance is around 90μH, the HFT current becomes minimum for a conversion ratio of 1.07. Fig. 5(b) shows that the phase-shifted angle associated with L_{lk} = 90μH and d = 1.07 is around 22 degrees, whilst Fig. 5(c) illustrates the ZVS operation range, where "1" indicates ZVS, and "0" otherwise. It can be seen that d = 1.07 satisfies the ZVS requirement for the design specification given in Table II.



(a) HFT current



(b) Phase-shifted angle



(c) ZVS operation range

Fig. 5. Variation HFT current and phase-shifted angle and ZVS range with leakage inductance and conversion ratio.

C. *Step 3: Optimal Core Dimensions*

In this step, core dimensions are optimized for minimum HFT weight and electrical losses with P_O = 2.2kW; L_{lk} = 90μH; d = 1.07; and ϕ = 22 degrees.

Assuming the chosen core is an EE ferrite core with dimensions shown in Fig. 6, the leakage inductance and maximum flux density, B_{max}, can be computed by [9]:

$$L_{lk} = \frac{1}{3}\mu_0 n_1^2 MLT \frac{h}{b} \tag{25}$$

$$B_{\max} = \Delta B = \frac{V_1}{4A_{core} f_s n_1} \tag{26}$$

where A_{core} is the core area; MLT is the mean-length per turn which is estimated by assuming that bobbin occupies 20% of window area.

$$A_{core} = d_T a \; ; MLT = 2(a + d_T) + 0.8b(2 + \pi) \tag{27}$$

It is worth noting that the top-bottom winding arrangement is chosen for the designed HFT in order to maximize the attainable leakage inductance [16].

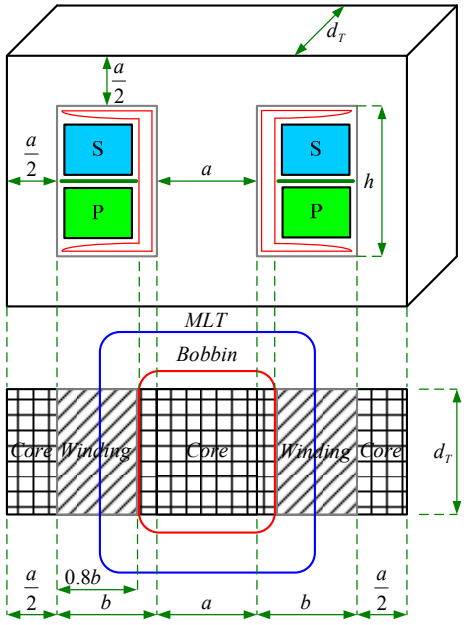


Fig. 6. Core dimensions used in HFT design investigation.

By defining two factors K_1 and K_2 as

$$K_1 = \frac{d_T}{a}; K_2 = \frac{h}{b} \tag{28}$$

Substituting (28) into (25) and (26) gives

$$n_1 K_1 a^2 4B_{\max} f_s = V_1 \tag{29}$$

$$n_1^2 \mu_0 K_2 MLT = 3L_{lk} \tag{30}$$

In addition, the relation between the core window area, A_w, and the primary conductor area [9] can be expressed as

$$A_w = K_2 b^2 = n_1 \frac{2}{k_f} \frac{I_{T1rms}}{J_{\max}} \tag{31}$$

where k_f is the filling factor chosen as 0.3 for Litz-wire and J_{max} is the current density given as 5.5 A.m^{-2} according to the thermal dissipation [9].

Equations (29), (30), and (31) can be used to study the optimized core dimensions for minimizing both core weight, C_W, and winding weight, W_W.

$$C_W = \rho_{Fe} C_V = \rho_{Fe} a K_1 [2(a+b)(a+K_2 b) - 2K_2 b^2] \tag{32}$$

$$W_W = \rho_{Cu} k_f A_W MLT \tag{33}$$

where ρ_{Fe} and ρ_{Cu} is, respectively, the ferrite mass density and copper mass density; C_V is the core volume.

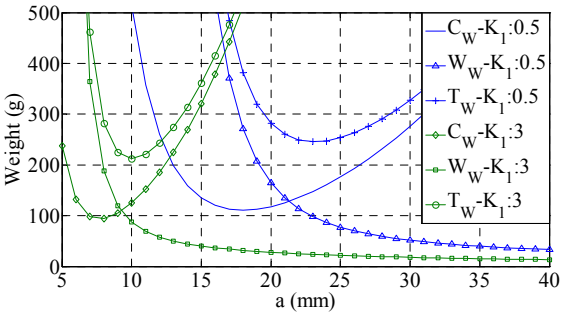


Fig. 7. Variations of HFT weight with a and K_1.

Fig. 7 shows the variations of the core weight, the winding weight, and the total HFT weight ($T_W = C_W + W_W$) with a for K_1 = 0.5 and 3. As can be seen, minimum total HFT weight can be achieved when a is between 10mm and 23mm. Fig. 8 shows variations of the other core dimensions, b and K_2, the mean length per turn, MLT, and the number of turns of primary winding n_1 with a and K_1.

When an optimal a for a given K_1 which minimize the total HFT losses can be determined, then the other dimensions, MLT and n_1 are found from Fig. 8.

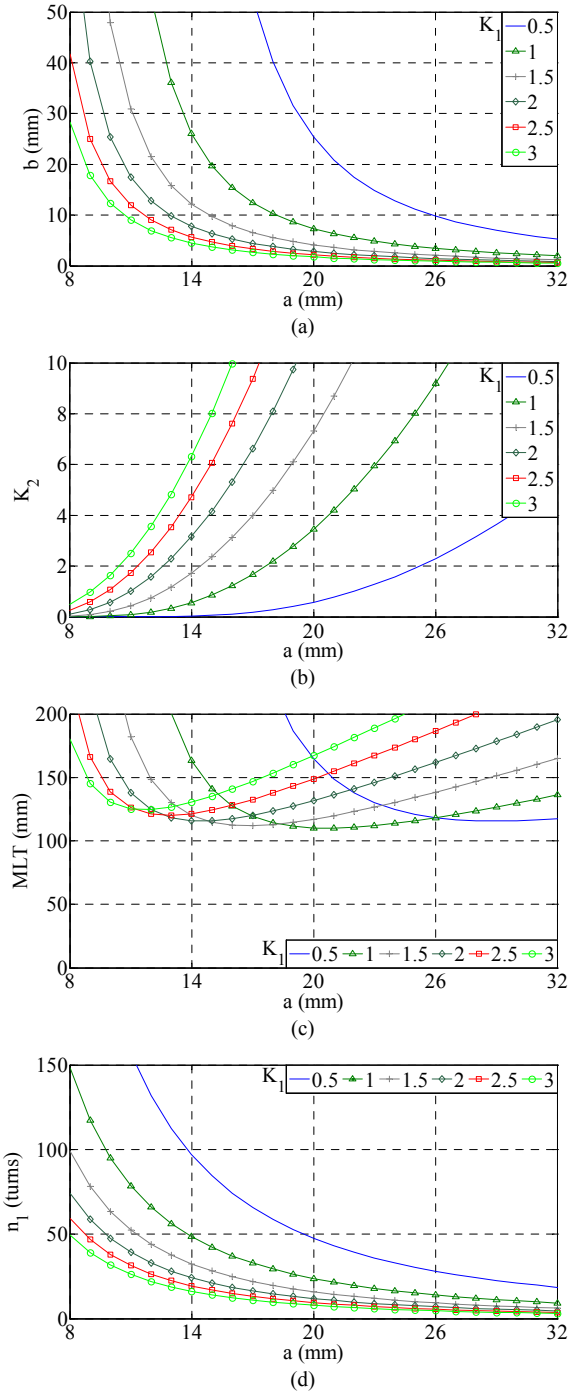


Fig. 8. Variations of core dimensions, MLT and n_1 with a.

Further, optimal round Litz-wire design needs to be determined to minimize the total winding losses. According to [17] and [18], optimal number of Litz-wire strands should be chosen to have its AC resistance, R_{AC}, being around 2 times of its DC resistance. This optimal AC resistance in per unit length can be computed as follows:

$$\beta = -2.4128d_c^2 + 1.5113d_c + 0.3535 \tag{34}$$

$$\delta_s = \frac{0.075}{\sqrt{f_s}};\ d_0 = \sqrt{\frac{-b_1 + \sqrt{b_1^2 + 12\delta_s^4}}{2}} \tag{35}$$

$$b_1 = \frac{\pi^2\beta^2}{24}(16m^2 - 1 + \frac{24}{\pi^2})d_c^2 \tag{36}$$

$$\zeta = 4\sqrt[4]{\frac{3}{1 + \frac{\pi^2 n_0\beta}{24}(16m^2 - 1 + \frac{24}{\pi^2})}} \tag{37}$$

$$\psi_1(\zeta) = 2\sqrt{2}\left(\frac{1}{\zeta} + \frac{1}{3}\frac{1}{2^8}\zeta^3 - \frac{1}{3}\frac{1}{2^{14}}\zeta^5\right) \tag{38}$$

$$\psi_2(\zeta) = \frac{1}{\sqrt{2}}\left(-\frac{1}{2^5}\zeta^3 + \frac{1}{2^{12}}\zeta^7\right) \tag{39}$$

$$R_{AC} = \frac{\sqrt{2}\rho_{Cu}n_1}{\pi\delta_s n_0 d_0}[\psi_1(\zeta) - \frac{\pi^2 n_0\beta}{24}(16m^2 - 1 + \frac{24}{\pi^2})\psi_2(\zeta)] \tag{40}$$

where d_c is the conductor diameter [9] computed from core window dimensions, HFT current, and current density; d_0 is the optimized strand diameter; m is the number of winding layers; n_0 is the number of strands per Litz-wire conductor; β is the Litz-wire packing factor; δ_s is the skin depth.

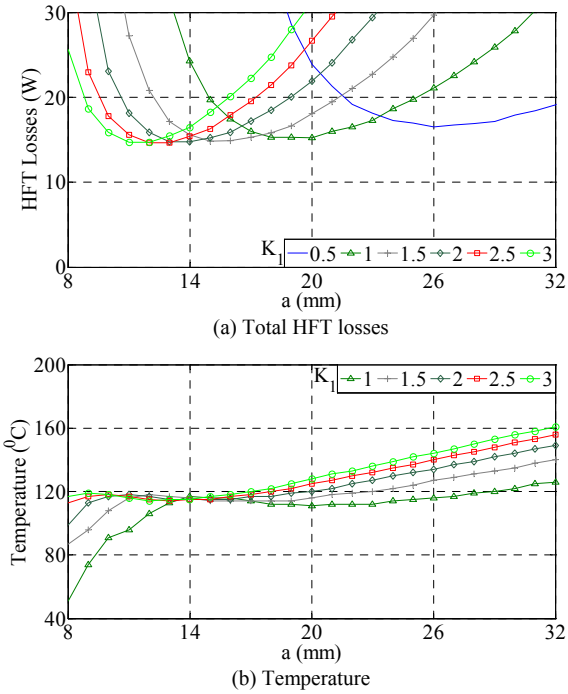


Fig. 9. Variation of HFT losses and temperature with a and K_1.

Based on the AC loss model of (40), the variations of total HFT losses, including DC and AC losses and core loss with the core dimension a and K_1 is shown in Fig. 9(a). The resultant temperature rise [9] can be determined as follows:

$$R_{\theta,rad} = \frac{10^8\Delta T}{5.1A_{CR}[(T_s + 273.15)^4 - (T_a + 273.15)^4]} \tag{41}$$

$$R_{\theta,conv} = \frac{(d_{vert})^{0.25}}{1.34A_{CR}(\Delta T)^{0.25}};\ R_{\theta,sa} = \frac{R_{\theta,rad}R_{\theta,conv}}{R_{\theta,rad} + R_{\theta,conv}} \tag{42}$$

$$P_{HFT\Sigma} = \frac{\Delta T}{R_{\theta,sa}} = P_{AC} + P_C;\ P_{AC} = R_{AC}I_{T1rms}^2;\ P_C = P_V C_V \tag{43}$$

$$A_{CR} = \begin{bmatrix} 4K_1a(a+b) + 2K_1a(K_2b+a) \\ +4(a+b)(K_2b+a) - 2\pi K_2b^2 + 2\pi b^2 + 4ab \end{bmatrix} \tag{44}$$

where A_{CR} is the crossectional area; d_{vert} is the HFT vertical height; P_{AC} is the winding loss; P_C and P_V is, respectively, the core loss and the relative core loss; $P_{HFT\Sigma}$ is the total HFT losses; $R_{\theta,conv}$ and $R_{\theta,rad}$ are the thermal resistances due to convective and radiative heat transfer, respectively; $R_{\theta,sa}$ is the total thermal resistance; T_a and T_s is the ambient and surface temperature in ^{0}C, respectively; $\Delta T = T_s - T_a$.

Fig. 9(b) shows the resultant temperature variations with

a and K_1 assuming $T_a = 25^0$C. From Fig. 9(b), it can be seen that the surface temperature is minimized when a is between 14mm to 17mm. This results together with the relevant K_1 presented in Fig. 9(a) and the minimum MLT value shown in Fig. 8(c) are utilized to determine the suitable ferrite core (E55/28/21). Table III compares the dimensions of optimized design and that of the selected core. It is evident that the proposed design optimization procedure leads to appropriate selection of available cores.

TABLE III COMPARISON BETWEEN OPTIMIZED DESIGN AND CHOSEN CORE

Optimized design	E55/28/21 (N87)
a = 17 (mm), K_1 = 1.25	a = 17.2 (mm), K_1 = 1.22
MLT = 112 (mm)	MLT = 124 (mm)
K_2 = 2.78	K_2 = 3.645
b = 8.63 (mm)	b = 10.1 (mm)
n_1 = 27 (turns)	n_1 = 27 (turns)

D. Step 4: Optimal Number of Turns of the Secondary Winding

Fig. 10 shows the numerical results of the total converter losses ($P_{C.Loss\Sigma} = P_{S.Loss\Sigma} + P_{HFT\Sigma}$) with the output voltage and transformer turn ratio when d = 1.07, L_{lk} = 90μH realized with E55/28/21 core; ϕ = 22 degrees, and P_O = 2200W. For the purpose of illustration, ZVS range at 90V (dashed blue line with crosses) and 140V (dashed grey line with circles) are also shown. As will be seen, the total losses decrease with the increases in turn ratio, but ZVS operation at 140V is lost when the turn ratio is greater than 3.4. Thus the optimal turn ratio for minimum total converter losses and full ZVS operation over the 90V-140V output voltage range is 3.4. The resultant number of turns of the secondary winding is n_2 = 8. Fig. 11 shows the variations of minimum leakage inductance for ZVS operation according to (14) with the output voltage for P_O = 2200W and 500W with n_2 = 8. It is obvious that ZVS operation is achieved for full range output voltage at P_O = 2200W with L_{lk} = 90μH. At lower output power, modified modulation techniques should be considered [2] to facilitate ZVS operation.

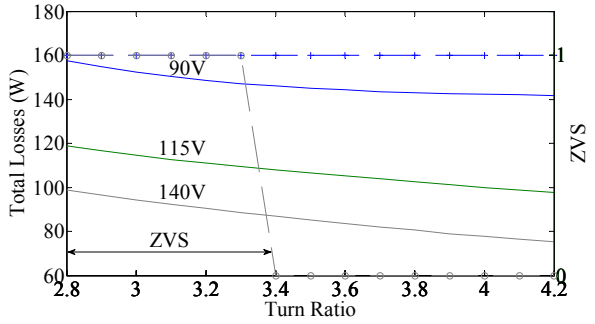


Fig. 10. Variation of total converter losses and ZVS range with turn ratio and output voltage.

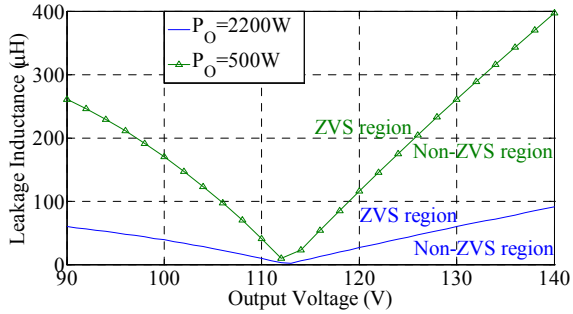


Fig. 11. Variation of minimum leakage inductance for ZVS with output voltage for P_O = 2200W and 500W with n_2 = 8.

IV. PROTOTYPE AND MEASUREMENTS

The outcomes of the proposed HFT design optimization, which is realized with core E55/28/21, are summarized in Table IV. It is worth noting that leakage inductance computed from (25) should be rescaled by a factor 0.7 due to three-dimensional and high frequency effects [19]. The winding arrangement for the HFT design is shown in Fig. 12(a). A prototype transformer has been constructed as per the optimal design, Fig. 12(b). The magnetizing and leakage inductances seen on both the primary and secondary sides are measured using an impedance analyzer. Fig. 13 shows the variations of resultant total converter losses with output voltage and power. As can be seen, the maximum total losses occur at 90V and P_O = 2200W is about 6.59% of the rated output power. At the nominal output voltage, the total losses are reduced to less than 5%. The measurement results are shown in Fig. 14 and validate the predicted magnetizing and leakage inductance, Table IV. This implies that ZVS operation can be ensured with the proposed design method without employing extra inductor.

TABLE IV OPTIMIZED DESIGN OF HFT

B_{max}	0.24848 (T)
Primary winding	27 turns, 162 strads-AWG38
Secondary winding	8 turns, 300 strands-AWG35
Magnetizing inductance Pri./Sec.	5.231/0.46 (mH)
Leakage inductance Pri./Sec.	90/10.5 (μH)

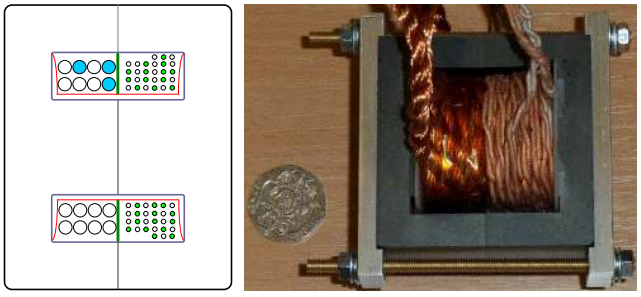


Fig. 12. HFT design. (a) Winding arrangement. (b) Prototype.

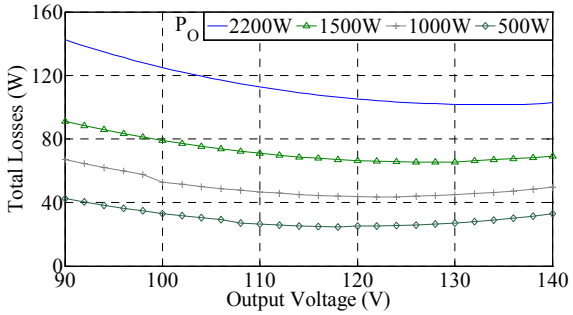
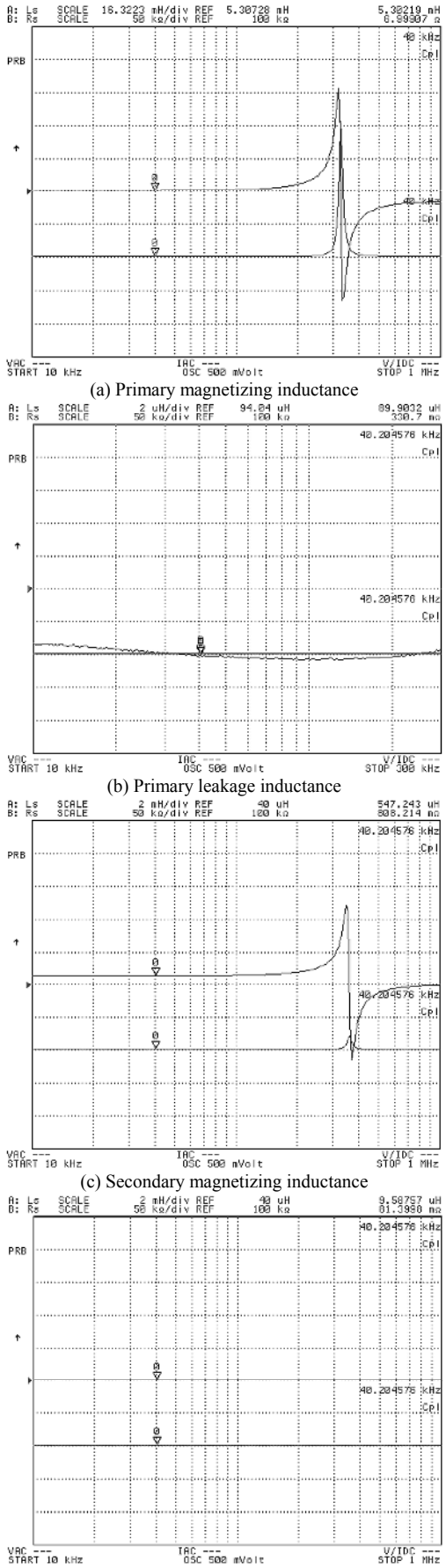


Fig. 13. Variation of total converter losses with output voltage and power.

V. CONCLUSION

In this paper, a design optimization procedure for the HFT employed in DAB isolated DC-DC converter has been described and experimentally validated. It has been shown that by considering leakage inductance, phase-shifted angle together with HFT VA rating, essential design equations for minimizing total losses of the DAB isolated DC-DC converter can be derived. It also has been demonstrated that leakage inductance requirement for ZVS operation can be achieved under the proposed design method without employing an extra inductor. Comparative study of DAB HFT design with conventional and the proposed design

methods will be performed in the near future.



(a) Primary magnetizing inductance

(b) Primary leakage inductance

(c) Secondary magnetizing inductance

(d) Secondary leakage inductance

Fig. 14. Measured inductances of prototype HFT.

VI. ACKNOWLEDGMENT

The authors gratefully acknowledge the European Commission for financial support and the P-MOB project partners for permission of the publication of this paper.

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