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Design procedure of 25.8 Gbps/lane re-timer IC regarding power integrity

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Abstract: A transceiver for a 25.8 Gbps/lane with a re-timer IC has been developed for information and communication equipment. Since a 1-unit interval (UI) is very narrow at 38.8 ps at 25.8 Gbps, power integrity (PI) jitter due to power supply fluctuation cannot be ignored. In this paper, we proposed a decoupling-capacitors (Decaps) placement technique to reduce power distribution network impedance (Zpdn) and a circuit design procedure regarding power supply fluctuation. The re-timer IC adopted from the proposed procedure achieved a bit error rate (BER) lower than 1×10^{-12} on backplane transmission with an insertion loss (IL) of 40 dB.

Keywords: power integrity, high-speed, multi-channel, low jitter, power distribution network impedance, on package decap

Classification: Integrated circuits

References

[1] Y. Doi, *et al.*: "A 32 Gb/s data-interpolator receiver with 2-tap DFE in 28 nm CMOS," ISSCC Dig. Tech. Papers (2013) 36 (DOI: 10.1109/ISSCC.2013.6487626).

[2] T. Kawamoto, *et al.*: "Multi-standard 185 fsrms 0.3-to-28 Gb/s 40 dB backplane signal conditioner with adaptive pattern-match 36-Tap DFE and data-rate-adjustment PLL in 28 nm CMOS," ISSCC Dig. Tech. Papers (2015) 54 (DOI: 10.1109/ISSCC.2015.7062922).

[3] M. Chandana, *et al.*: "Power integrity analysis for high performance design," 2015 ICCEREC (2015) 48 (DOI: 10.1109/ICCEREC.2015.7337052).

[4] K. Kogo, *et al.*: "Power signal integrity for 25 Gbps 40 dB compensation signal conditioner for backplane architecture," 2015ICSJ (2015) 212 (DOI: 10.1109/ICSJ.2015.7357400).

[5] W. Li-xin, *et al.*: "Power integrity analysis for high-speed PCB," 2010 First International Conference on Pervasive Computing, Signal Processing and Applications (2010) 414 (DOI: 10.1109/PCSPA.2010.106).

[6] B. Hassan and S. Mouloud: "Analysis and optimization of power integrity issues from high speed CMOS integrated circuit interactions in aeronautic systems," 2016 IEEE, 13th International Multi-Conference on Systems, Signals & Devices (2016) 636 (DOI: 10.1109/SSD.2016.7473674).

[7] R. Sjiariel, *et al.*: "Power integrity simulation of power delivery network system," 2015 IMOC (2015) 1 (DOI: 10.1109/IMOC.2015.7369185).

[8] Y. Uematsu, *et al.*: "Chip-package-PCB co-simulation for power integrity

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Accepted November 2, 2017
Publicized November 21, 2017
Copyedited December 10, 2017

design at the early design stage," 2015 APCAP (2015) 451 (DOI: 10.1109/APCAP.2015.7374446).
[9] M. J. Patil, *et al.*: "Techniques for detection of package issues in chip power integrity closure," 2016 EPEPS (2016) 79 (DOI: 10.1109/EPEPS.2016.7835422).
[10] H. Kimura, *et al.*: "28 Gb/s 560 mW multi-standard SerDes with single-stage analog front-end and 14-tap decision-feedback equalizer in 28 nm CMOS," ISSCC Dig. Tech. Papers (2014) 38 (DOI: 10.1109/ISSCC.2014.6757327).
[11] B. Zhang, *et al.*: "A 28 Gb/s multi-standard serial-link transceiver for backplane applications in 28 nm CMOS," ISSCC Dig. Tech. Papers (2015) 1 (DOI: 10.1109/ISSCC.2015.7062921).

1 Introduction

The throughput of information and amount of communication equipment has been increasing in data centers due to the expansion in needs, such as huge data analysis. Current transmission rates need to be higher between large scale integration circuits (LSI). Thus, a 25.8 Gbps/lane transceiver with an 8-lane re-timer integrated circuit (IC) was developed [1, 2]. Fig. 1 shows a backplane structure with this re-timer IC. The structure consisted of three boards and two connectors, and the insertion loss between the two re-timer ICs was 40 dB. However, transmission is very difficult because the transmission lines had impedance mismatch caused by the through holes (TH) and the connectors, and because the lines were contaminated. Therefore, it is essential to suppress each jitter element. Fig. 2 shows a jitter budget to achieve the 40 dB compensation. Since a 1-unit interval (UI) is very narrow at 38.8 ps at 25.8 Gbps, it is necessary to reduce the jitter. Generally, total jitter consists of the following: inter-symbol-interference (ISI) jitter, caused by transmission loss; reflection jitter, caused by impedance mismatching; power integrity (PI) jitter, caused by power supply fluctuations; and crosstalk jitter, caused by leakage signals from the other lanes. To support the IEEE 100GBASE-KR4 (802.3bj) standard, it is necessary to suppress transmission jitter. Therefore, to suppress PI jitter to 2.5 ps, we examined it. A method of reducing the PI jitter has already been reported [3, 4, 5, 6, 7, 8, 9]. These reports examined only the outside of the chip, and characteristics of inside of the chip such as a power supply rejection ratio (PSRR) and capacity of decoupling-capacitors (Decaps) were not considered. Therefore, larger

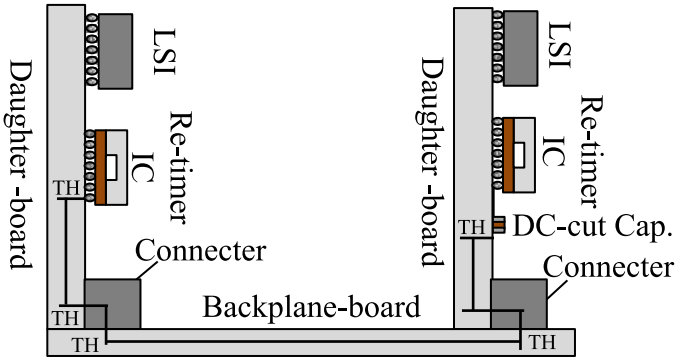

Fig. 1. Backplane structure assuming re-timer IC use

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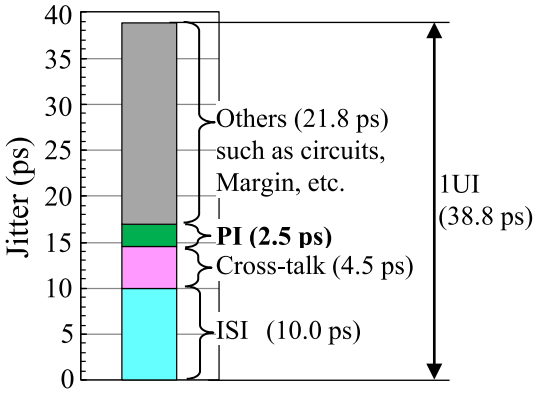

Fig. 2. Jitter budget to achieve 40 dB compensation

size Decaps were required on the outside of the chip, increasing both cost and area. In this paper, we have implemented effective countermeasures against PI jitter, considering both the inside and outside of the chip. Furthermore, we proposed a circuit-design procedure regarding power supply fluctuation. As a result, the developed re-timer IC achieved a bit error rate (BER) lower than 1×10^{-12} under actual conditions where there is impedance mismatch by connecters with an insertion loss (IL) of 40 dB.

2 Overview of PI jitter

Fig. 3 shows a schematic diagram of the power supply fluctuation and PI jitter. During the circuit's operation, a current fluctuation (ΔI) occurs. The wiring from the power supply to the circuit has power distribution network impedance (Zpdn). The supply voltage noise (ΔV) could be obtained by the following equation.

$$\Delta V = Zpdn \times \Delta I \tag{1}$$

We defined PI jitter as the jitter difference between the reference jitter when Zpdn is not considered (Zpdn = 0) and practical jitter when Zpdn is considered. Since PI jitter is proportional to ΔV, a reduction of Zpdn and ΔI is necessary to improve PI jitter. As ΔI is a design factor of the circuit, any reduction of it may deteriorate circuit performance. Therefore, as it is difficult to reduce ΔI only, lowering Zpdn is possible.

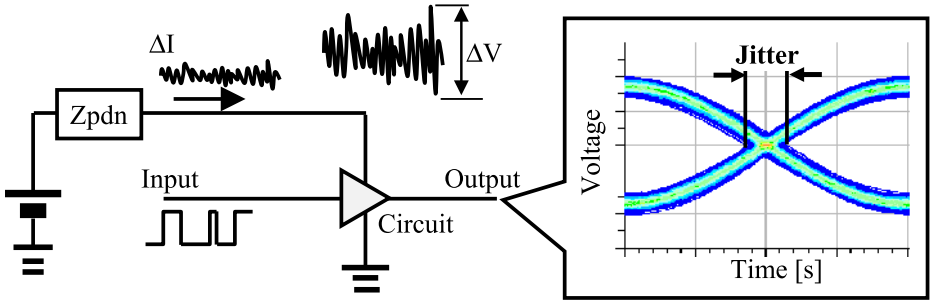

Fig. 3. Outline diagram of PI jitter

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3 Proposed circuit design procedure

Fig. 4 shows the proposed flow of the circuit design procedure regarding the power supply fluctuation. In Step 1, Zpdn and ΔI of the circuits under consideration are calculated. In Step 2, ΔV is calculated on the basis of the calculation from Step 1. In Step 3, the circuit characteristic using ΔV in calculated. In Step 4, if the circuit characteristic satisfies the PSRR specification of the circuits, the design is finished, but if it does not, the suppression of Zpdn will be redesigned until the specification is satisfied.

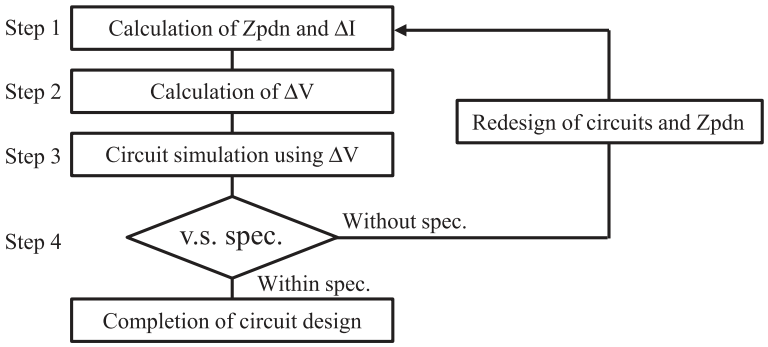
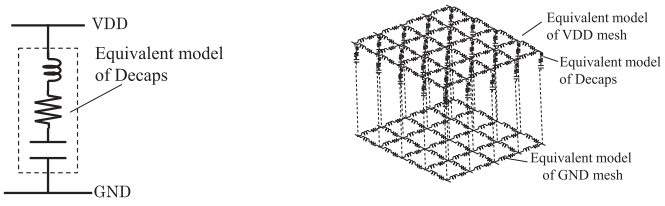


Fig. 4. Circuit design procedure regarding the fluctuation of power supply

4 Optimization of Zpdn

(i) Inside the chip

We first examined the relationship between Decaps placement inside the chip and Zpdn. To supply voltage to the transistors arranged in various places in the chip, the VDD and GND were arranged with a mesh on the whole chip. Decaps inside the chip were used as a countermeasure against Zpdn levels above the GHz band. The distance between the circuits where the current fluctuation occurs and the Decaps were examined. Fig. 5 shows the model used for the study, (a) is a zero-dimensional (0D) model in which the power mesh is not considered, and (b) is a two-dimensional (2D) model regarding the power mesh. Fig. 6(a) shows the calculated result of the frequency response of Zpdn from the center of a 400 μm × 400 μm power mesh region. The 0D and 2D Zpdns models coincided in the low frequency band, but there is a clear difference at 2 GHz or more. This difference is the deterioration of the Decaps caused by the parasitic inductance of the power mesh. Therefore, we proposed an index of Decap effects (IF(Zpdn)). The



(a) 0D model (b) 2D model

Fig. 5. Power mesh model for reviewing Zpdn in the chip

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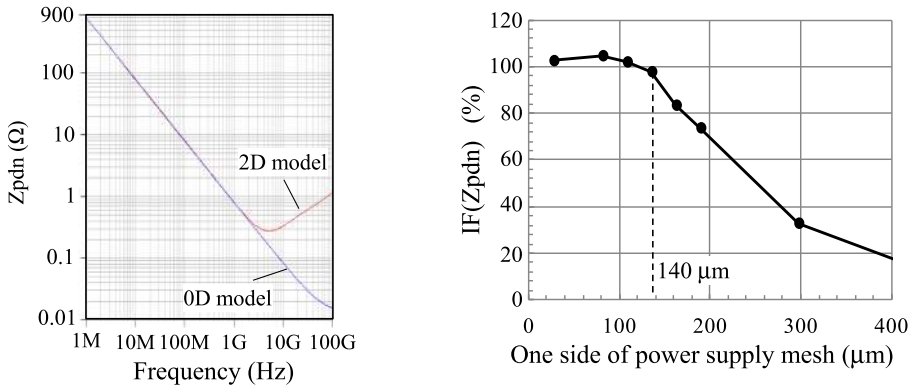
index was calculated from the ratio of the 0D- and 2D-model Zpdns, as shown in the following equation.

$$IF(Zpdn) = \frac{\text{0D Zpdn}}{\text{2D Zpdn}} \quad (2)$$

Fig. 6(b) shows the calculated results of IF(Zpdn) at 12.9 GHz, which was the Nyquist frequency of 25.8 Gbps. When IF(Zpdn) = 100%, the impedance of the 0D model and that of the 2D model are in agreement, indicating that all Decaps in the area are effective. However, when IF(Zpdn) < 100%, the effect of Decaps, which is located far from the noise source, decreases. As a result, we found that Decaps are effective in a circuit that is 140 µm × 140 µm, and the wider the area, the lower the Zpdn is due to the effect of the parasitic inductance. From this result, the chip to be developed has Decaps uniformly arranged in 140 µm × 140 µm areas as one block. This result is for the IC specification designed in this paper. For ICs with different operating frequencies, current consumptions, and capacitance densities of Decaps, it is necessary to calculate IF(Zpdn) for each the IC.



(a) Frequency response of Zpdn

(b) Effective area of Decap in chip @12.9GHz

Fig. 6. Calculated result of examination on Decaps placement inside chip

(ii) Outside the chip

We then examined the relationship between Decaps placement outside the chip and Zpdn. Since the re-timer IC of this development requires low Zpdn in wideband, we applied a flip chip-ball grid array (FC-BGA) package (PKG), which can place Decaps inside of the PKG. Fig. 7(a) shows the structure of the FC-BGA and (b) shows the equivalent circuit model of Zpdn. In this circuit, the GND trace and the self inductance of Decaps are much smaller than the trace inductance, and are thus ignored. A parasitic inductance is caused by the traces between Decaps. Therefore, the Decaps arranged in the chip and on the PCB differ in terms of effective frequency bands. Fig. 8 shows the calculated frequency response of Zpdn. In the band where the impedance decreases as the frequency increases, the capacitance due to Decaps is the main component band. On the other hand, in the band where the impedance increases with the frequency, the inductance due to the parasitic inductance is the main component band. From this calculation result, the Chip Decaps (Cc) are effective in bands over 100 MHz and the PCB Decaps

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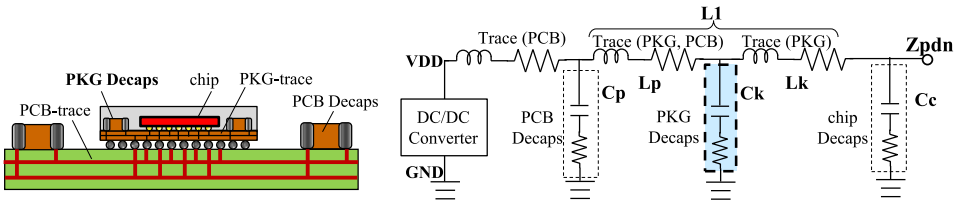
(Cp) are effective in band under 2 MHz. Also, as the frequency band switched between capacitive and inductive, a peak of Zpdn, called anti-resonance, occurs. A peak impedance of Zpdn without PKG Decaps occurs at anti-resonance (Fa) due to the parasitic inductance (L1) between Cc and Cp, and frequency is around 40 MHz. The Cc is the frequency band in which the Zpdn cannot be reduced. On the other hand, increased Cc require an expansion in the chip area, which leads to an increase in cost, which is not realistic. Therefore, the Cc and Cp cannot reduce Zpdn, and PKG Decap (Ck), which is effective at 40 MHz, is necessary. Cc are much smaller than Cp, so it is equivalent to GND. To suppress the peak impedance of Zpdn, the frequency of series resonance generated by Ck and trace (Lk) needed to be matched with the Fa. Fa can be represented by the following equation.

$$Fa \approx \frac{1}{2\pi\sqrt{L1 \times Cc}} = \frac{1}{2\pi\sqrt{Lk \times Ck}} \tag{3}$$

As a result, the peak impedance of Zpdn was suppressed by approximately 60% from 0.38 Ω to 0.15 Ω. On the basis of this result, reduction of PI jitter could be expected.



(a) FC-BGA of mounting structure (b) Equivalent circuit of the Zpdn

Fig. 7. Comparison of mounting structure

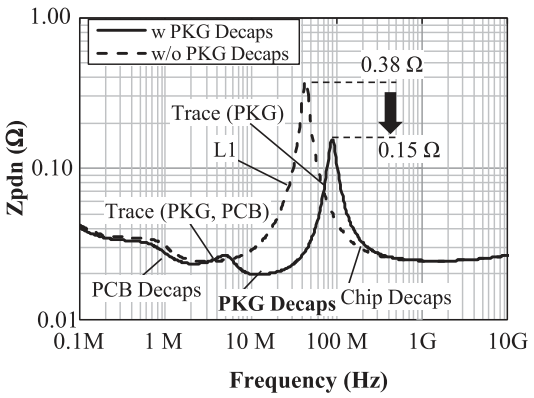


Fig. 8. Calculated frequency response of Zpdn showing effect of PKG Decaps

5 Circuit design regarding power supply fluctuation

Fig. 9(a) shows the current waveform of a re-timer IC when an ideal power supply has no voltage fluctuation. The current of the re-timer IC fluctuates at 0.2 App around 3.8 A. We calculated the voltage waveform at Step 2. The current waveform and the calculated waveform of the voltage from Zpdn are shown in Fig. 9(b). The

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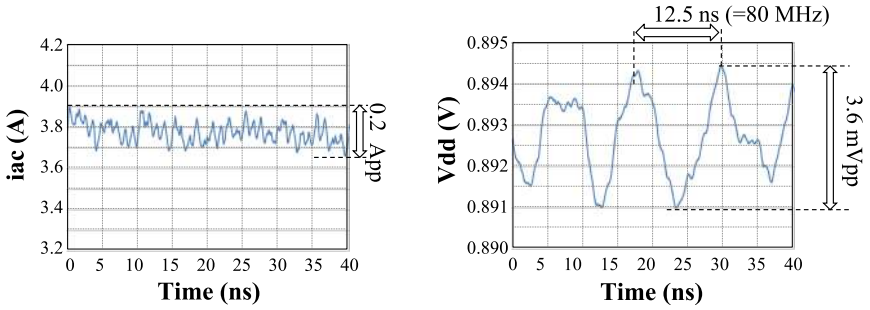
voltage waveform continued to fluctuate at 3.6 mVpp at 80 MHz of the peak frequency of Zpdn. Fig. 10 shows a schematic diagram of the circuit design regarding the proposed power supply fluctuation in Step 3. By connecting the calculated voltage waveform to the power supply, it is possible to design such a circuit.



(a) Current waveform for ideal power supply (b) Voltage waveform regarding Zpdn

Fig. 9. Simulated waveform of power supply

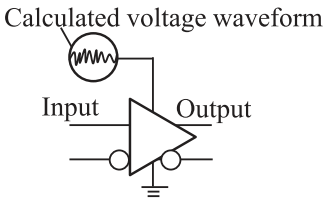
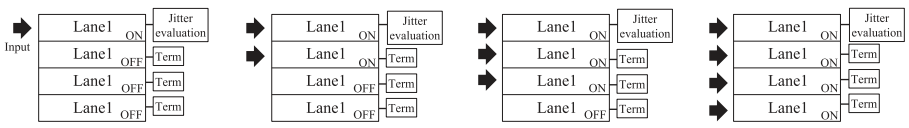


Fig. 10. Schematic diagram of circuit design procedure regarding proposed power supply fluctuation

6 Confirm the accuracy of proposed calculation method

To confirm the accuracy of this calculation method, measurement and simulation results were compared with a test element group (TEG). As the number of operations of the circuit increased, both the current and voltage fluctuations increased. Fig. 11 shows the structure of the TEG and the evaluation method. TEG was implemented with 4 lanes. As shown in (a), (b), (c), and (d), the number of operating lanes increased, and the jitter at that time was evaluated. Fig. 12 shows the measurement and simulation results of jitter, in which both are in very good agreement. This result supports the accuracy of our calculation method.



(a) Standard (b) 2-lane operation (c) 3-lane operation (d) 4-lane operation

Fig. 11. Structure of TEG and evaluation method to confirm proposed calculation method accuracy

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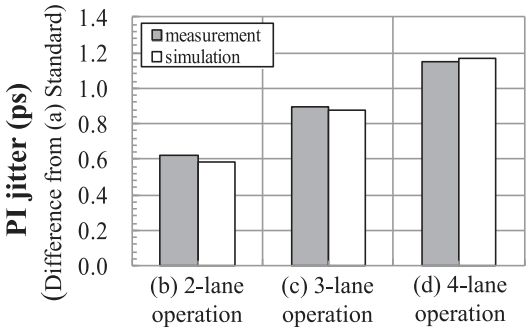


Fig. 12. Jitter comparison result of measurement and simulation

7 Measurement result

Fig. 13 shows the measurement result of PI jitter. We selected 1 lane to be the victim lane and evaluated the jitter increase when operating 7 aggressor lanes. As a result, the PI jitter was 1.6 ps, suppressed to less than 2.5 ps. The result obtained met the target specification. Next, we evaluated the transmission performance of an IL of 40 dB using the developed re-timer IC. Fig. 14(a) shows the transmission system, and (b) shows the measurement result of the bathtub. As a result, a BER lower than 1×10^{-12} was achieved. In the 40 dB transmission of the backplane structure, a positive result was obtained that enables 25.8 Gbps/lane transmission.

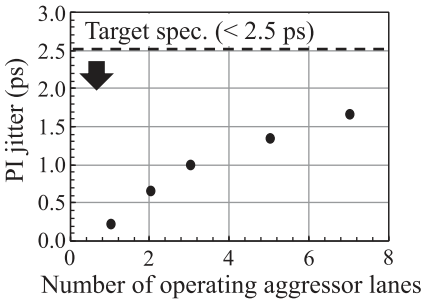
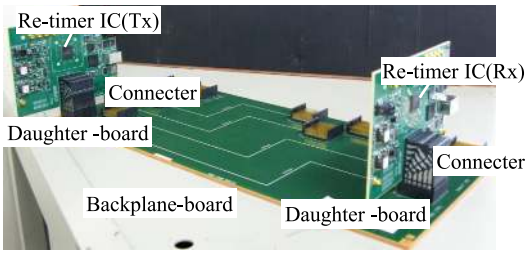
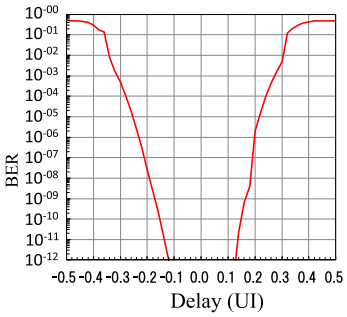


Fig. 13. Measurement result of PI jitter



(a) Transmission system



(b) Measurement result of bathtub

Fig. 14. Measurement result of transmission with 8 lanes

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8 Performance comparison

Table I shows the performance comparison of the re-timer IC at more than 25 Gbps/lane. The other ICs have their equivalent compensation performances, but as this is a result of transmitting inside the same board, the trace quality is ideal, which is not practical. As a result, jitter, due to impedance mismatch, is added to the actual condition of the trace, making transmission more difficult. However, the developed IC can transmit with the same loss under actual trace conditions where there is impedance mismatch of the connecters.

Table I. Performance comparison for over 25 Gbps re-timer IC

	LSI [10]	**Broadcom[11]**	**This work**
Technology	28-nm CMOS	28-nm CMOS	28-nm CMOS
Data rate (Gbps)	28.0	25.8	25.8
IL (dB)	34	40	40
Number of connectors	0	0	2
Year	2014	2015	2016

9 Conclusion

In response to the PI countermeasure only from the outside of the conventional chip, this report implemented PI countermeasures including the Decaps placement inside the chip. Furthermore, we proposed a circuit design procedure regarding power supply fluctuation. As a result, the developed re-timer IC designed using these procedures suppressed the PI jitter to 1.6 ps, and achieved a BER lower than 1×10^{-12} under actual conditions where there is impedance mismatch of connecters with an IL of 40 dB.

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