Global Journal of Researches in Engineering
Electrical and Electronics Engineering
Volume 13 Issue 15 Version 1.0 Year 2013
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 2249-4596 & Print ISSN: 0975-5861

Design, Simulation & Performance Evaluation of OFDM System to Reduce PAPR using SLM & LCM with FPGA

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GJRE-F Classification : *FOR Code: 290903p*

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Design, Simulation & Performance Evaluation of OFDM System to Reduce PAPR using SLM & LCM with FPGA

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I. Introduction

The root of Orthogonal Frequency Division Multiplexing (OFDM) scheme is traced back to 1960's when it was first proposed by Chang in 1968 . Since then, there has been a vigorous research effort in developing OFDM-based wireless communication systems. Over the years, OFDM has become to be the most popular transmission scheme for broadband communication systems that require high-speed 4G communication with 100 mbps data rate. Its increasing popularity is due to its spectral efficiency and inherent ro-bustness to channel impairments. In addition, the OFDM waveforms offer substantial improvements in performance over traditional single carrier approaches.[2]

Various applications of OFDM are Digital Audio Broadcast-ing (DAB) and Digital Video Broadcasting (DVB) in Europe, and for Asymmetric Digital Subscriber Line (ADSL) high data rate wired links. OFDM has also been standardized as the physical layer for the wireless networking standard 'HIPERLAN2' in Europe and as the IEEE 802.11a, g standard in the US, promising raw data rates of between 6 and 54Mbp[14]. Orthogonal Frequency Division Multiplexing (OFDM) is a multicarrier-based technique for mitigating ISI to improve capacity in the wireless system with spectral efficiency.[1]

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The paper aims at successful implementation of the transceiver on a FPGA which would pave a way towards developing an OFDM system which resolves the issue of high PAPR. Simulation results using System Generator and Matlab/Simulink and XILINX tools have been given in the paper."Low Crest Method" which is the selected technique of PAPR reduction is given in thi spaper. Finally it aims at development of a complete system which then results in robust, maximum throughput, highly scalable wireless LAN network.[2]

II. OFDM and PAPR

a) General OFDM Block Diagram Description

i. OFDM Transmitter

The model considered for the implementation of the OFDM transmitter is the shown above and basically consist of the following blocks:[13]

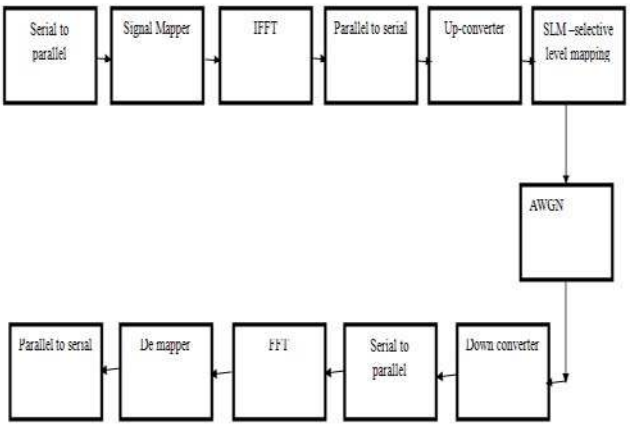

Figure 2.1 : Block diagram of an OFDM system

Serial to parallel converter, Constellation modulator, IFFT block, Parallel to serial converter, Digital to Analog converter, Selective Level Mapping.

ii. OFDM Receiver

The blocks of the OFDM Receiver are detailed below:

Analog to digital converter, Serial to parallel converter, Cyclic prefix removal, FFT block, M-QAM decoder, Parallel to serial converter.

b) Peak to average Power ratio

The major disadvantage of using several subcarriers in parallel using IFFT is the highly non-constant envelope of the transmit signal, making OFDM

very sensitive to nonlinear components in the transmission path. A key component is the high power amplifier (HPA). Due to cost, design and most importantly power efficiency considerations, the HPA cannot resolve the dynamics of the transmit signal and inevitably cuts off the signal at some point causing additional in-band distortions and adjacent channel interference. The power efficiency penalty is certainly the major obstacle to implement OFDM in low-cost applications. Moreover, in power-limited regimes determined by regulatory bodies, the average power is reduced compared to single-carrier systems reducing in turn the range of transmission. The power control problem motivates further research since it touches on many of the advantages that originally made OFDM transmission popular, i.e. spectral efficiency and implementation issues.

In OFDM systems, a fixed number of successive input data samples are modulated and then jointly correlated together by use of IFFT at the transmitter side. IFFT processes signals to produce orthogonal data sub-carriers. Mathematically, IFFT combines all the input signals to produce each one of the output symbols.

The signal processing by IFFT in the OFDM transmitter changes the statistical distribution of signals from uniform-to-Gaussian. Therefore, the dynamic range of the OFDM output envelope is most often higher than that of the single-carrier systems. However, PAPR is widely used to evaluate the dynamic range of the output envelope. The PAPR (in dB) is defined by the following equation [14].

$$\text{PAPR}=10log_{10}\left\{\frac{P_{peak}}{P_{avg}}\right\}=10log_{10}\frac{max[|x(n)|^2]}{E[|x_n|^2]} \quad (1)$$

where Ppeak represents peak output power, Paverage means average output power. E[•] denote the expected value, xn represents the transmitted OFDM signals which are obtained by taking IFFT operation on modulated input symbols Xk . xn is also expressed as[12]

$$x_n = \frac{1}{\sqrt{N}}\sum_{K=0}^{N-1} X_k W_N^{nk} \quad (2)$$

c) Selective Level Mapping

Selective level Mapping (SLM) was first proposed in 1996 to reduce PAPR in OFDM systems. The system block diagram of SLM is shown below.

At first, the input information is divided into OFDM data block X, which consists of N symbols, by the serial-toparallel (S/P) conversion and then data block X is multiplied carrier-wise with each one of the U different phase sequences B(u), resulting in a set of U different OFDM data.

In the SLM algorithm the data source denoted as X, is multiplied by the U different sets of phase factors/masks, element-wise to produce U different copies of X,

$$Xu = BuX \quad u= 1, 2, ...,U \quad (3)$$

where U is the design parameter in SLM. In general, more reduction in PAPR is likely to achieved when U in-creases.[12]

In addition, Bu is defined as:

$$Bu=[Bu,1\ Bu,2\ Bu,3...\ Bu,(N-1)] \quad (4)$$

Then all U alternative data blocks (one of the alternative sub-carrier sequences can be the unchanged original one) are transformed into time domain to get transmit OFDM symbol where N represents the number of subcarriers in IFFT and Bu,k is given by:

$$Bu,k = e^{j\phi u,k} \quad k = 0, 1, 2, ...,N - 1 \quad (5)$$

After multiplying X with the phase factors, each Xu is processed by IFFTs and its PAPR is then computed and compared with the others. The resulting signal that yields the lowest PAPR is subsequently chosen for transmission. In addition, the Bopt which implies the optimal Bu that produces the lowest PAPR has to be transmitted to receiver as a side information[14]. The receiver will then use Bopt to recover the data source, X[6].

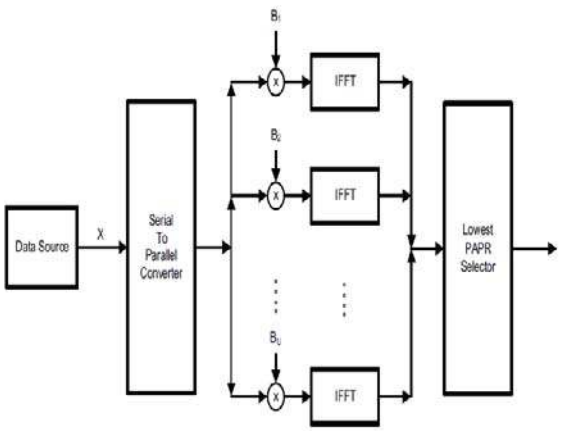

Figure 2.2 : Block diagram of SLM

III. Designed OFDM Model

The top level design contains simulink blocks for input, signal display and output. Input to the design is given from a sine wave generator or from a sound input stored in the workspace. The inputs are passed through a gateway in block to convert from floating point numbers to fixed point numbers compatible to Xilinx blockset. The data is then serialized using a parallel to serial converter and given to the OFDM transmitter. The transmitter is explained in detail in the later section. The

output of the transmitter, which is PAPR reduced serial data stream is given to the receiver to decode it. Also a certain amount of noise is added to the data stream. The receiver then decodes the stream. The final output is given from the receiver. This data is displayed and compared on the scope and also output on the workspace for comparison. Also the BER is calculated by comparing the data before and after decoding.

a) Transmitter Design

In the design presented, block length of 8 points and 4 different phase sequences are used. Transmitter subsystem design contains 4 independent OFDM modulators. In the modulator, the input data is multiplied by a look-up table from ROM before giving it to actual OFDM modulation process. This lookup table holds the phase sequences for each block. The output of each block is given to a PAPR calculator and selector. It transmits the data block with lowest PAPR and also transmits the selected block number.

b) Receiver Design

The receiver is a normal OFDM receiver with a phase sequence selector block. The data stream is first given to FFT block for decoding. Then the data stream is passed to a lookup table multiplier which multiplies data with a phase sequence as indicated by the selected block number from transmitter.

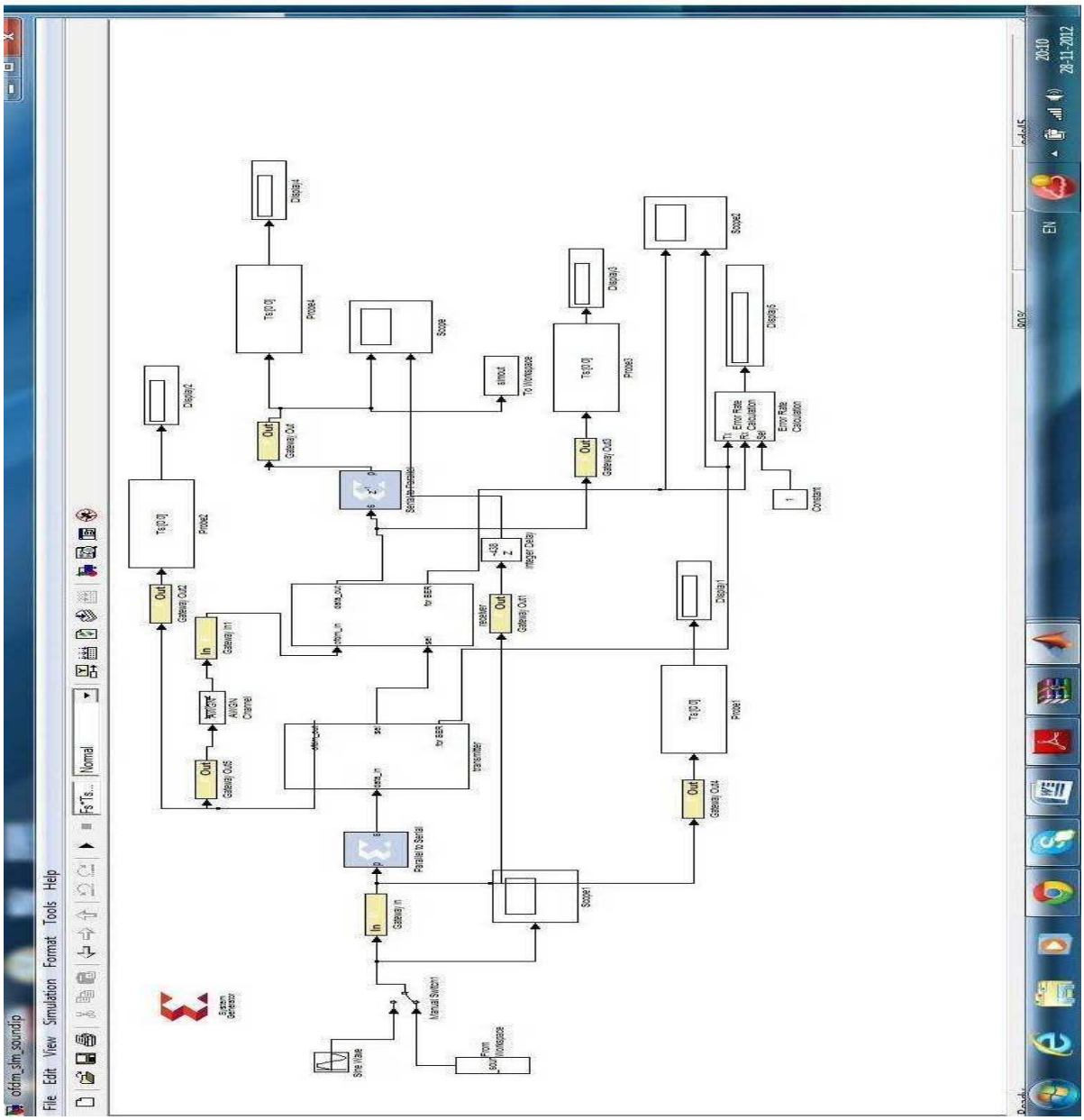

Figure 3.1 : Block diagram of the designed system

c) Transmitter Subsystem

- *Encoder*

The Figure 3.2 indictes the encoder module where there are two shift registers and two X-OR gates. Initially the shift registers have a zero bit stored in it. For the first X-OR gate there are three inputs. The first input is as it is the output of parallel to serial block. The second input is output of parallel to serial block with one delay while the third is the output of parallel to serial block with two delays. The output of the first X-OR is given out as data_out 1.

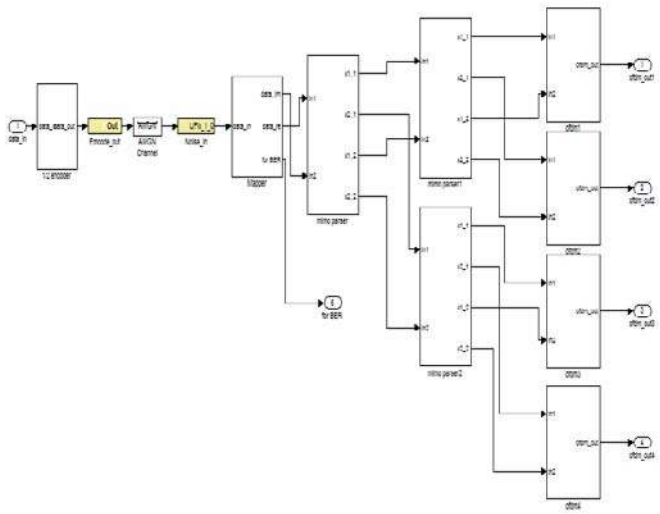

Figure 3.2 : Transmitter Module

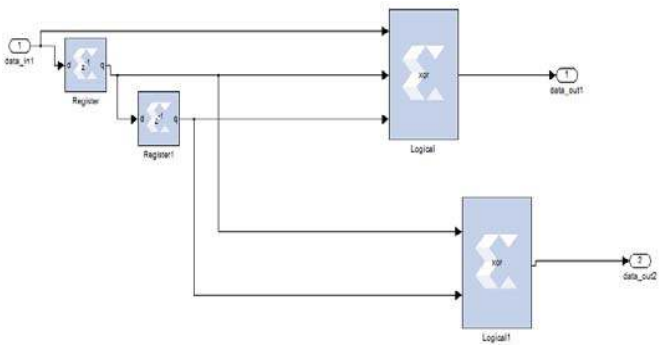

Figure 3.3 : Encoder Model

The outputs of parallel to serial blocks with one and two delays respectively are given to the second X-OR gate . The output of the second X-OR is given out as data_out 2.

- *Mapper*

The output of encoder/interleaver module is applied as input to the Mapper. The combination of ROM_Imag, ROM_Real altogether forms QAM mapper. The ROM_Imag provides the value on imaginary axis while ROM_Real provides the value on real axis. This is giving up the points on different quadrants.

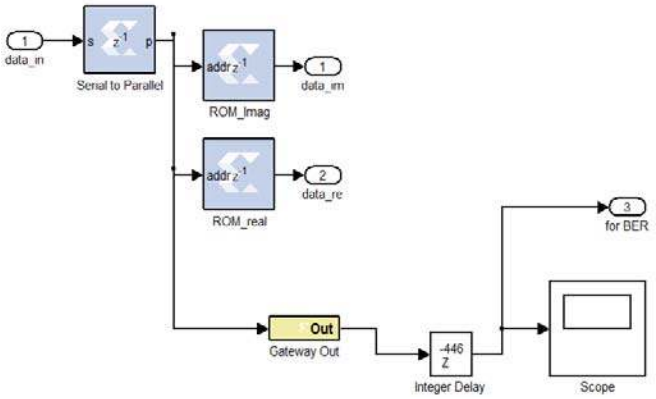

Figure 3.4 : Mapper

d) Receiver Subsystem

- *Demodulator*

The Figure 3.5 represents the demodulator i.e. demapper block. The ROM_REAL and ROM_IMAG signals are fed as input as xr and xi to the demodulator respectively. A Matlab code is used for QAM demodulator and is given out at dout.

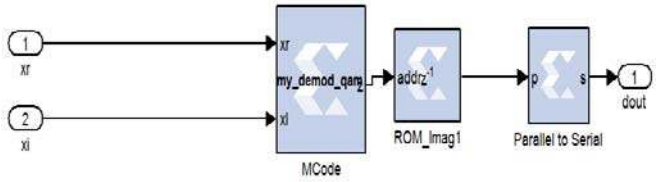

Figure 3.5 : Demodulator module

- *Decoder*

The Figure 3.6 represents the decoder which consists of serial to parallel block and a decoder block. A Matlab code is written for the purpose of decoding the actual data.

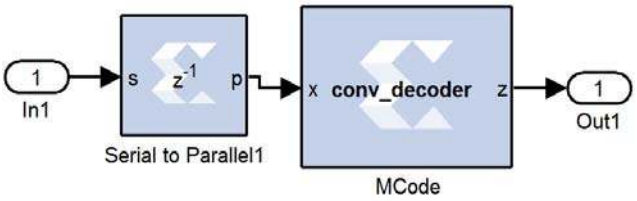

Figure 3.6 : Decoder module

IV. Implemented SLM Block

The SLM algorithm applied in this model uses 4 OFDM se-quences of 8 point each and applies 4 different mask on each sequence [6]. Blocks B1-4 are OFDM blocks which each multiply the input sequence with a predetermined mask. IFFT is then calculated on the masked stream. The PAPR calculator evaluates the PAPR for the stream independently. The stream with the lowest PAPR is then selected for transmission. Along with the stream, the stream number is also transmitted

for the receiver to know which mask to apply to decode the sequence.

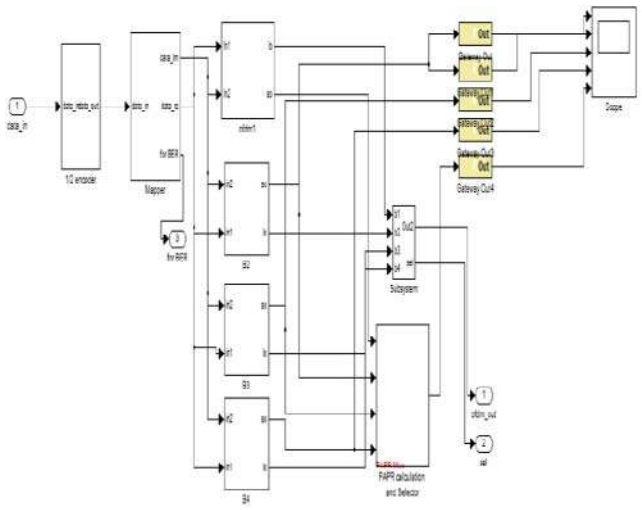

Figure 3.7 : Showing PAPR calculation block

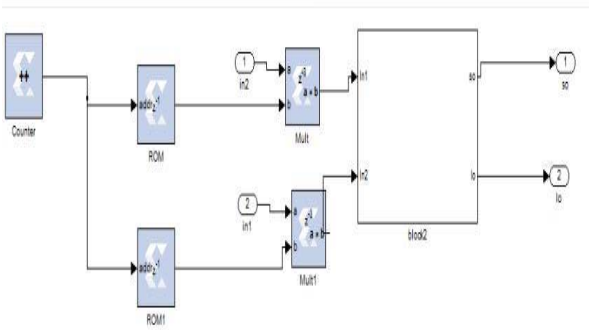

Figure 3.8 : Inner details of one of the 4 OFDM blocks

V. Hardware Implementation

Using XILINX and modelsim the developed simulink model is converted into its JTAG equivalent.[2] Internal simulator of XILINX, i-sim can also be used in place of modelsim.[20]

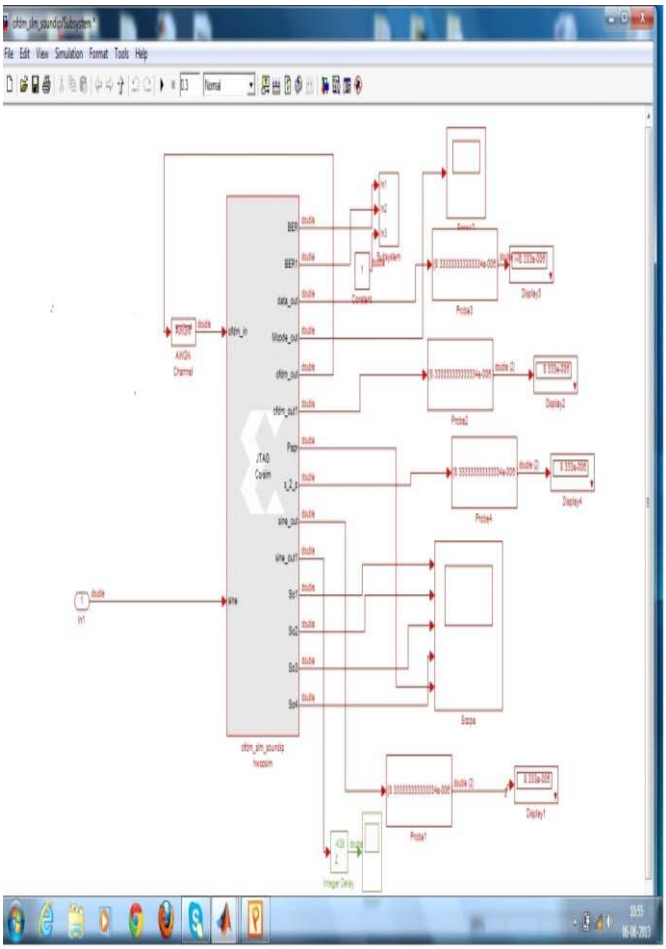

Figure 3.9 : JTAG-Hardware Co-sim block

The hardware implementation of the simulink model is done using JTAG. The process of developing such a hardware is called Hardware-In-Loop.

VI. Methodology

The algorithm of each block using Matlab Simulink is imple-mented by use of constructing block diagrams in Simulink. VHDL code is imported into Simulink using the Xilinx Sys-tem Generator block set, which gives flexibility to design flow. Simulink and Xilinx System Generator create bit-true. The Xilinx Integrated Software environment (ISE) is used as the synthesizer in the design flow diagram. ModelSim is used to verify the hardware simulation of the blocks by using test vectors generated by System Generator or HDL test benches. Finally synthesis and performance results of the blocks are reported using ISE, and bit streams are generated to program the FPGA board. [24][25].

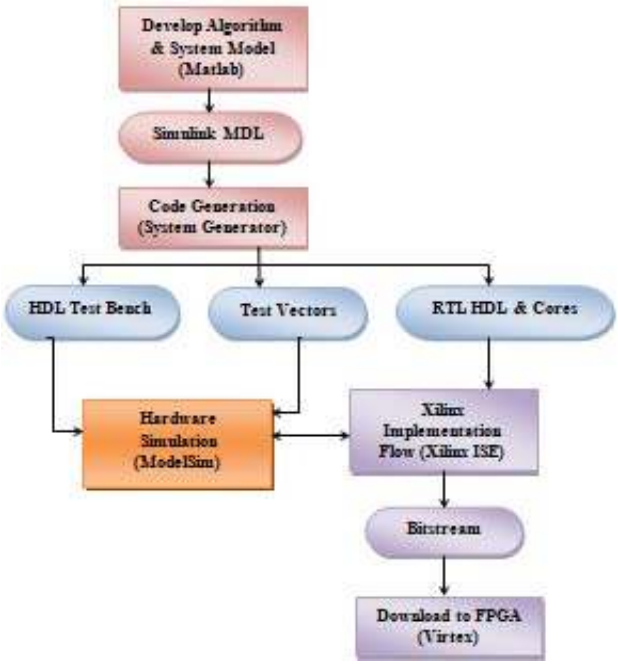

Figure 4.1 : Methodology and flow diagram [24][25]

VII. Result and Discussion

a) FPGA kit analysis

The DONE LED glows indicating that the FPGA is now ready to be programmed.

The output of the scope can be seen in the Figure 5.2 where the first waveform is the signal which has been achieved at the output of model which is the received signal and the second waveform is the actual signal which was been fed as input to the model.

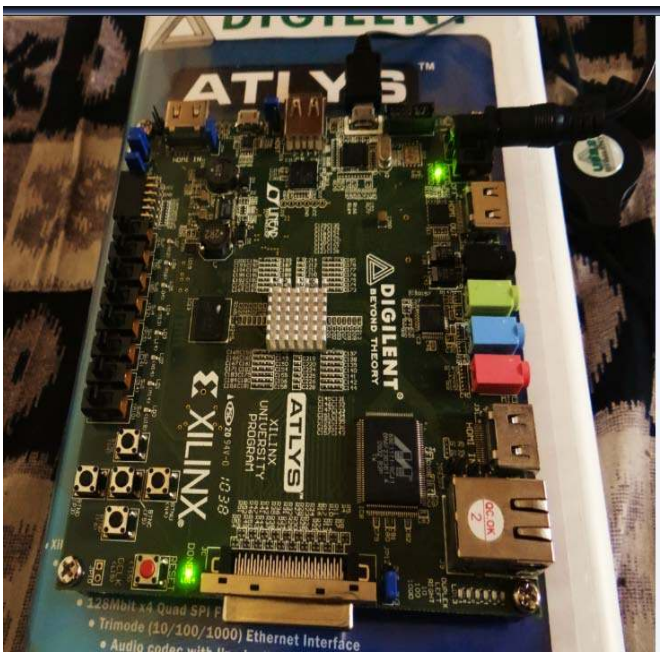

Figure 5.1 : FPGA ready for programming[25]

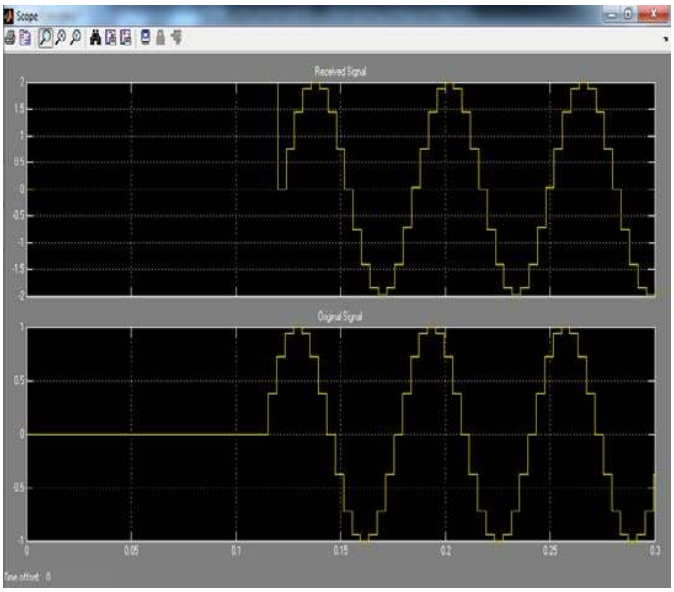

Figure 5.2 : Received and Original Signal (Test sinewave)

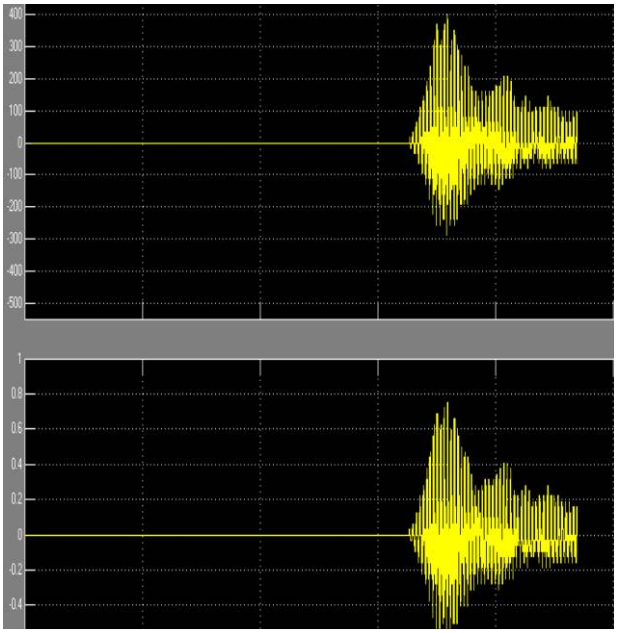

Figure 5.3 : Received and Original Signal (Realtime audio sinewave)

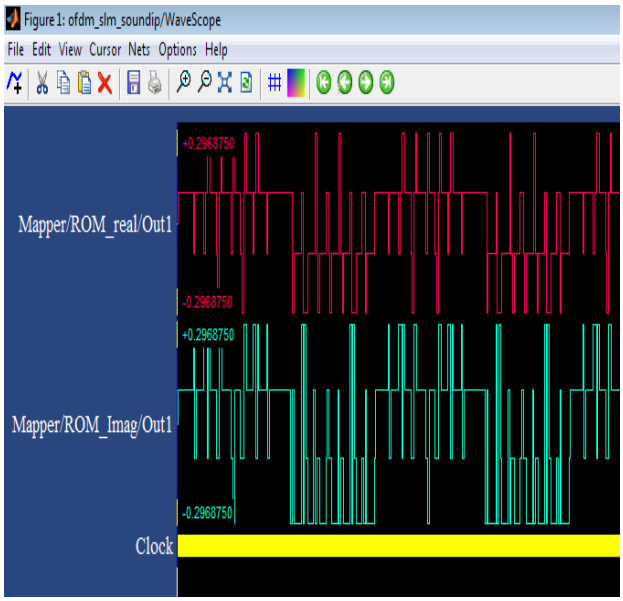

Figure 5.4 : Output of Wavescope (after running it for 30 secs)

b) Output of the wavescope- QAM Explaination

Wavescope block shows following two signals. First one is Rom_real and Rom_imaginary as shown below. These two signals represent the real and imaginary part of the input signal resulting in 16 – QAM.

After running the model for almost 30 seconds and the wavescope block is opened. The following output is observed.

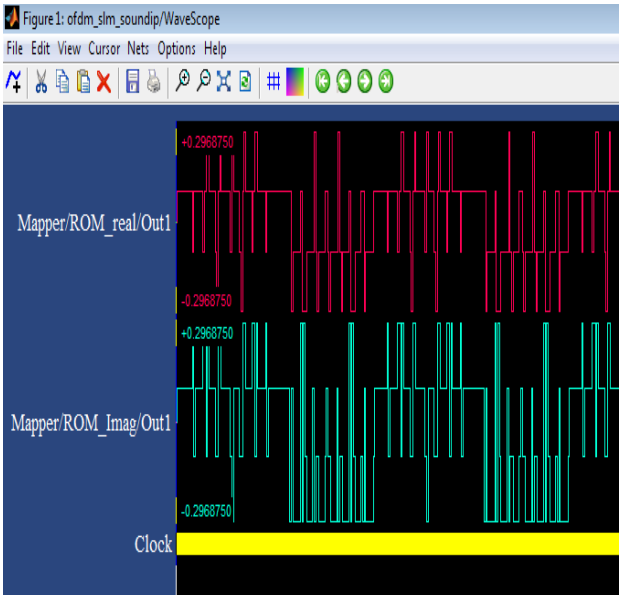

Figure 5.5 : QAM Output

Observing the output carefully, it is seen that the signal is repeating after certain intervals (16 Frames) as shown by square.

From the waveform it is clearly observed that the maximum and minimum value for the real and imaginary signal is same and it is (+0.29) as shown below.

Table 5.1 : Showing 16-Qam Constellation Points

QAM Input Symbol	QAM constellation	Array Index	Array Value (Real + j*Imaginary Part)
0	-3-3j	0000	-0.29 – 0.29 j
1	-3-1j	0001	-0.29 – 0.10j
2	-3+3j	0010	-0.29 + 0.29j
3	-3+j	0011	-0.29 + 0.10 j
4	-1-3j	0100	-0.10 – 0.29 j
5	-1-1j	0101	-0.10 – 0.10 j
6	-1+3j	0110	-0.10 + 0.29j
7	-1+j	0111	-0.10 + 0.10 j
8	+3-3j	1000	+0.29 – 0.29j
9	+3-1j	1001	+0.29 -0.10j
10	+3+3j	1010	+0.29 + 0.29j
11	+3+j	1011	+0.29 + 0.10j
12	+1-3j	1100	+0.10 – 0.29j
13	+1-1j	1101	+0.10 – 0.10j
14	+1+3j	1110	+0.10 + 0.29j
15	+1+j	1111	+0.10 + 0.10j

Thus the signal lies between +0.29 to -0.29 on both real and imaginary axis.

From the repeated sequence of 16-QAM in the model from Rom_real and Rom_imaginary signals, it is concluded that the signal represents the non uniform 16– QAM.

From the above symbols , the 16 – QAM Constellation Map-ping is obtained.

VIII. Hardware Co-Simulation

ofdm_slm_soundip_cw Project Status			
Project File:	ofdm_slm_soundip_cw.xise	Parser Errors:	No Errors
Module Name:	synth_reg_w_init	Implementation State:	Synthesized
Target Device:	xc6slx45-3csg324	•Errors:	
Product Version:	ISE 12.3	•Warnings:	
Design Goal:	Balanced	•Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	•Timing Constraints:	
Environment:	System Settings	•Final Timing Score:	

Figure 5.6 : project status report

a) Project Status Report

The following diagram shows the project status report which includes details like:

Project file name, target device, product version etc.[20]

b) RTL Schematic

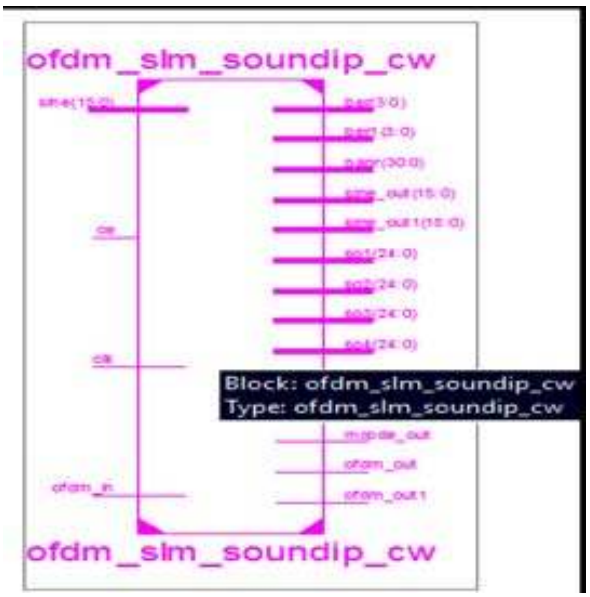

Figure 5.7 : RTL Schematic

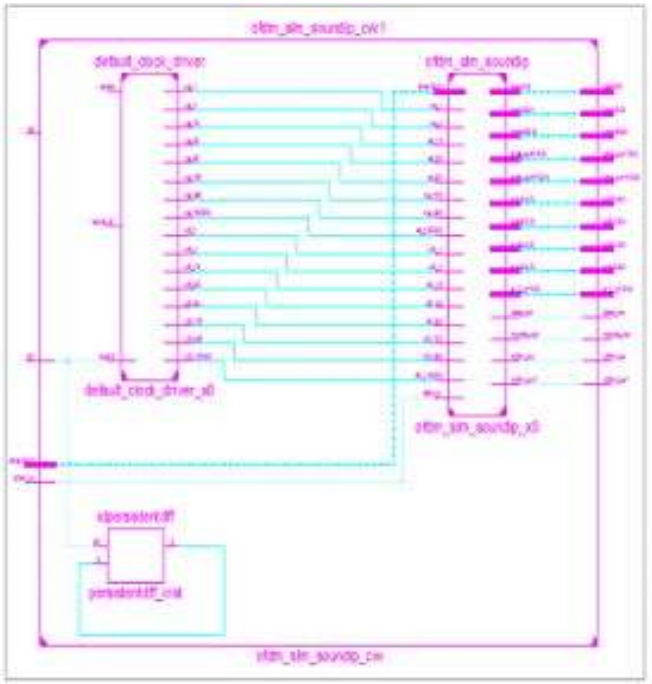

Figure 5.8 : RTL Schematic inside ofdm_soundip_cw

c) Test Benches

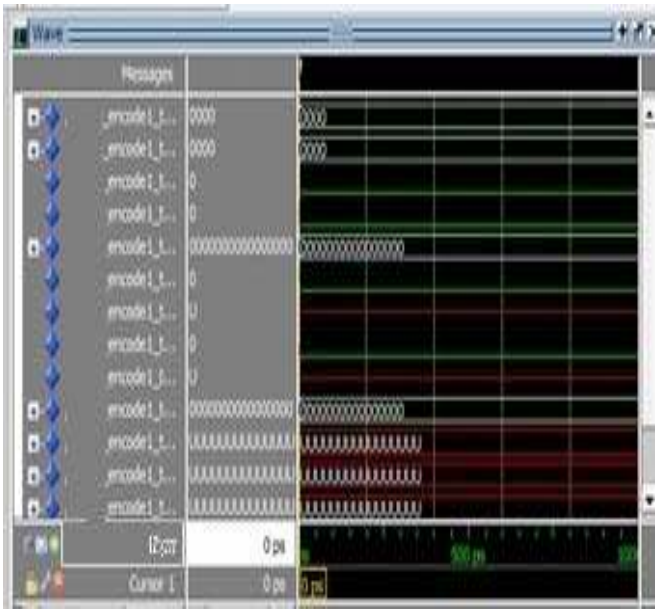

*Figure 5.9 .*Generating Test Bench

d) Graphs Plotted

Table 5.2 indicates PAPR values with SLM and without SLM. Last coloum shows Crest Factor(√ K).

It is evident from the table that PAPR reduction of about 2 dB is obtained using 64 carriers.

Varying difference in PAPR is obtained using 2,4,8 and 64 number of carrier.

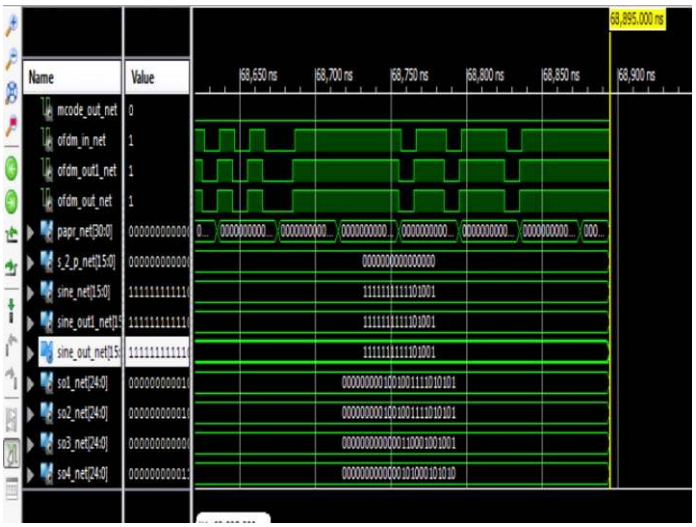

Figure 5.10 : Test Bench [20]

PAPR reduction of nearly 1.6dB is obtained using 2 carriers. Higher reduction of PAPR is obtained using 8 carriers.

Table 5.2 : Papr Values With and Without Slm, Crest Factor

Number of carriers	PAPR without SLM in dB	PAPR with SLM in dB	Difference in PAPR	Crest Factor =□√K
2	12.61	11.01	1.6	1.264
4	25.22	24.01	1.21	1.1
8	37.83	35.03	2.77	1.67
16	50.45	48.89	1.56	1.24
32	63.06	62.01	1.59	1.024
64	75.76	73.76	2	1.414

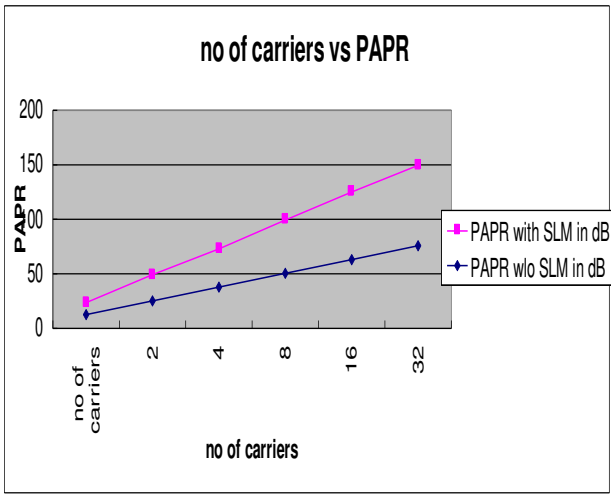

Figure 5.11 : Number of carriers v/s PAPR

As number of carriers increase the PAPR increases. Implementing the proposed technique PAPR can obtain reduction in PAPR.

Table 5.3 : Probability of Papr and Papr (Db)

PAPR in dB	Without SLM	With SLM
0	0.985	0.945
1	0.984	0.944
2	0.9832	0.944
3	0.983	0.9
4	0.982	0.85
5	0.981	0.8
6	0.98	0.712
7	0.885	0.612
8	0.8	0.511
9	0.7	0.21
10	0.6	0
11	0.512	0
12	0.001	0

The above table shows that nearly 2 dB reduction is achieved by using LCM technique.

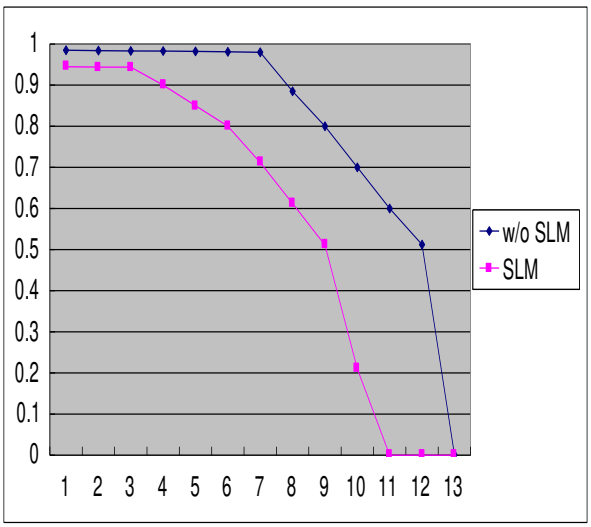

Figure 5.12 : CCDF of PAPR v/s PAPR(in dB)

The PAPR without SLM for OFDM system is 12dB and with SLM is 10dB resulting in overall reduction of 2dB.

It is observed from figure.5.17 that in case of OFDM systems without employing SLM technique the PAPR that is evaluated is constant upto 10dB and it results in a steep slope after 10dB terminating at 12dB. The OFDM system with SLM block for which the PAPR is calculated initially remains constant between 0 to 2dB and 3 to 5dB but varies between 5 to 10dB. Thereby the final PAPR with SLM is 10dB and without SLM is 12dB resulting in overall PAPR reduction of 2dB.

Difference of PAPR in **dB** calculated for OFDM system with & without SLM	PAPR calculated as factor not in **dB**	Crest Factor as **Sqrt(PAPR)** as factor not in **dB** - C^2
2dB	**1.58483**	**1.2589**

Crest Factor=√ PAPR

IX. Conclusion

OFDM is a very attractive technique for wireless communications. One of the serious drawbacks of OFDM is very high PAPR when the input sequences are highly correlated. The PAPR obtained without SLM for OFDM system is 12dB and with SLM is 10dB resulting in overall reduction of 2dB. Thus SLM technique has the potential to reduce PAPR for OFDM systems and improve its performance in terms of low PAPR high SNR and improved BER.

Xilinx System Generator combined with Matlab Simulink provides an easier and efficient way of developing the FPGA system design and simulating it. Also the hardware co-simulation feature of the software enables easier way to test and debug the design effectively on the actual hardware.

The hardware co-simulation, RTL Schematics, Test Bench and VHDL codes, are also obtained for the implemented OFDM system. First the model is created in the Matlab/Simulink environment. The Matlab Simulations were carried out and necessary modifications were done. The hardware co-simulation was done to run the model on the hardware platform. The VHDL code, RTL Schematics and Test Bench were generated for the model. Test Vectors are passed through the test bench to verify functionality of the each block of the model. At the end complete functionality of the model is verified using Matlab Simulations, Test Bench/Modelsim Simulations and Hardware co-simulations.

e) Future Scope

The paper deals with reduction of PAPR in a SISO OFDM. The concept of reduction of PAPR can be implemented in MIMO technology. If such a model is implemented it shall give the advantages of low PAPR as well as high data rate, which is an advantage of MIMO.

Different modulation techniques such as QPSK or QAM ac-commodating number of subcarriers as 1024 or up to 4096 can be experimentally tried to achieve data rates in multiple of 100 Mbps or more.

The new system model can emphasis on performance of Signal to Noise Ratio, Bit Error Rate, CDF and CCDF with respect to channel capacity.

X. Acknowledgement

Our thanks to the experts who have contributed towards development of this paper.

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