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Design Space for Low Sensitivity to Size Variations in (110] PMOS Nanowire Devices: The Implications of Anisotropy in the Quantization Mass

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Letter

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Design Space for Low Sensitivity to Size Variations in [110] PMOS Nanowire Devices: The Implications of Anisotropy in the Quantization Mass

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ABSTRACT

A 20-band $sp^3d^5s^*$ spin−orbit-coupled, semiempirical, atomistic tight-binding model is used with a semiclassical, ballistic, field effect transistor (FET) model, to examine the ON-current variations to size variations of [110]-oriented PMOS nanowire devices. Infinitely long, uniform, rectangular nanowires of side dimensions from 3 to 12 nm are examined and significantly different behavior in width versus height variations are identified and explained. Design regions are identified, which show minor ON-current variations to significant width variations that might occur due to lack of line width control. Regions which show large ON-current variations to small height variations are also identified. The considerations of the full band model here show that ON-current doubling can be observed in the ON-state at the onset of volume inversion to surface inversion transport caused by structural side size variations. Strain engineering can smooth out or tune such sensitivities to size variations. The cause of variations described is the structural quantization behavior of the nanowires, which provide an additional variation mechanism to any other ON-current variations such as surface roughness, phonon scattering, etc.

Motivation. As transistor sizes shrink down to the nanoscale, a possible device approach that has attracted a great deal of attention recently because of its possibility of enhanced electrostatic control, is the multigated nanowire (NW) transistor.[1] Nanowire transistors of diameters even down to 3 nm have already been demonstrated by various experimental groups.[2−6] At such small scales, however, the issue of device sensitivity to parameter fluctuations will be critical. Atomistic variations of the side lengths, surface roughness, line edge roughness, cross section shape variations, defects, surface states will exist in these devices and need to be tolerated (if at all possible). Device orientation as well as the quantization surfaces will also be an important design parameter. In the case of nanowires (and thin body devices), the high symmetry orientations [100], [110], and [111] as shown in Figure 1, have been extensively studied. Both experiments and simulations have identified that for NMOS nanowires the beneficial transport orientations are [110] and [100][7−9] to deliver the highest currents. In the case of ballistic PMOS devices, however, simulation has shown that the [100] transport orientation lacks behind the [110] orientation[10,11] in its current currying capabilities. For this reason, and because of the fact that the optimized conventional CMOS architecture orientations are (001)/[110], it would be ben-
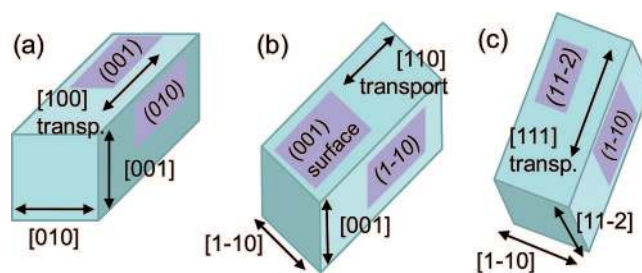

Figure 1. Nanowires in the high symmetry transport orientations: (a) [100], (b) [110], and (c) [111] transport orientation. The [110] nanowire in (b) is the one analyzed in this work. The width direction is [1$\bar{1}$0] and the height direction is [001]. Equivalently, the top/bottom quantization surfaces are (001) (perpendicular to the [001] direction). The left/right quantization surfaces are (1$\bar{1}$0) (perpendicular to the [1$\bar{1}$0] direction).

eficial to build devices on the (001) surface and utilize the [110] transport direction. The sensitivity of that geometry (Figure 1b) to size fluctuations is the subject to detailed discussions. Although several reasons might add to the device performance variations such as interface roughness and phonon scattering, this work considers infinitely uniform rectangular nanowires, and investigates the sensitivity of ON-current to side size variations, resulting alone from the internal structural and electrostatic quantization behavior of the nanowire. These fluctuations are attributed to the aniso-

tropic hole effective mass, and cannot be captured appropriately in effective mass models. This additional mechanism can result in current fluctuations of 100% while typical treatments of surface roughness scattering at ON-state have resulted in rather modest current variations of 10−20%.[12−14] The electronic structure effect discussed and explained here is an additional variation mechanism on top of the already existing mechanisms, and we believe it is significantly stronger than the perturbative effects typically considered in surface roughness models.

Summary of the Paper. In this work, an atomistic nearest-neighbor tight binding (TB) model (sp^{3}d^{5}s*-SO)[15−18] is used for the nanowires' electronic structure calculation, coupled to a two-dimensional (2D) Poisson solver for electrostatics. To evaluate transport characteristics, a simple semiclassical ballistic model[19,20] is used. The variations in the ON-current with size variation of [110] PMOS rectangular nanowire devices with (1$\bar{1}$0) and (001) quantization surfaces, as shown in Figure 1b, are investigated. Cross sectional widths and heights with lengths from 3 to 12 nm (all combinations of side lengths) are considered. The nanowires are considered infinitely long in the transport orientation, with uniform surfaces. Design regions in which the current is at large extent tolerant to the nanowires' side variations are identified. Fluctuations in the [1$\bar{1}$0] direction (width size, or equivalently fluctuations in the (001) surface area) have a small and almost linearly varying impact on ON-current variations. [001] (height) length variation (equivalently variations in the (1$\bar{1}$0) surface area) has a more complicated impact on the trend of the ON-current variation, with large ON-current sensitivity for nanowires with [001] heights of lengths 6−8 nm. This behavior appears at the onset of volume inversion to two surface inversion channels. Its specific side length appearance (6−8 nm) originates in the internal structural quantization and electrostatic confinement behavior of the nanowires. The reason it is only observed in the [001] direction is a result of the anisotropy of the Si heavy-hole (HH) valence band, which strongly affects the preference of charge placement in the wires' cross section and along its quantization surfaces. It is also observed for different gate biases at very similar side lengths. It is shown that strain engineering can change the anisotropy of the heavy-hole subband and make the sensitivity of the ON-current to side variations more uniform, or tune the sensitivity to different design regions.

Necessity of Atomistic Modeling. The problem of identifying the correct band structure for the valence band of Si in the inversion layers is complicated (especially for nanowires), because of the strong nonparabolicity and anisotropy of the heavy hole and its coupling to the light hole (LH). Several authors have investigated various techniques for description of the valence band,[21−23] for both unstrained and strained MOSFET channels. In addition, under extreme scaling of device dimensions, the atoms in the cross section will be countable, and crystal symmetry, bond orientation, distortions, surface truncation, and quantum mechanical confinement will dominate transport characteristics.[7,10] The nearest neighbor TB sp^{3}d^{5}s*-SO model used in this work, with a basis set composed of localized orthogonal orbitals,

is most appropriate for this purpose since it inherently includes all of the above features. The model itself and the parametrization presented in ref 15 have been extensively calibrated to various experimental data of various nature with excellent agreement (details and references in ref 7).

The Simulation Approach. The devices simulated are rectangular nanowires in the [110] transport orientations with 1.1 nm SiO$_2$ oxide thickness. [001] and [1$\bar{1}$0] are the two equivalent quantization directions (Figure 1b). The simulation procedure consists of three steps as described in detail in ref 7 and summarized here:

1. The band structure of the wire is calculated using the sp^{3}d^{5}s*-SO model. The atoms that reside on the surface of the nanowire are passivated in the sp^3 hybridization scheme.[24]

2. A semiclassical top-of-the-barrier ballistic model is used to fill the dispersion states and compute the transport characteristics.[19,20]

3. A 2D Poisson equation is solved in the cross section of the wire to obtain the electrostatic potential. The electrostatic potential is added to the diagonal on-site elements of the atomistic Hamiltonian as an effective potential for recalculating the band structure until self-consistency is achieved.

Although the transport model used is a simple ballistic model, it allows for examining how the band structure of the nanowire alone will affect its ballistic transport characteristics. The same conclusion to parts of this work can be obtained from full 3D quantum (NEGF) simulations,[11,25−27] and still simulations might be restricted to smaller nanowire cross sections (rather than up to the 12 nm × 12 nm cross sections we are considering). The simple model used here, however, provides critical physical insight. It is the simplicity of the transport model, which allows light to be shed on the importance of the dispersion details and the charge distributions, which might get lost in a full-fledged quantum transport simulation. The results presented in this work focus on the ON-current variation behavior of PMOS [110] nanowires. More detailed transport properties of PMOS nanowires, also in different transport orientations, are presented in ref 10.

Valence Band Anisotropy Affects Quantization. It is well-known that the valence bands of the standard semiconductors are very anisotropic with a general rule of thumb of $m_{[100]} < m_{[110]} < m_{[111]}$ for the heavy hole. For Si we find $m_{[110]} = -0.579$ and $m_{[100]} = -0.275$; therefore $m_{[110]}/m_{[100]} \sim 2.1$, which is a very significant distortion. The light-hole bands show typically significantly less anisotropy with $m_{[110]} = -0.147$ and $m_{[100]} = -0.204$, therefore $m_{[110]}/m_{[100]} \sim 0.72$. With these mass values a simple particle in a box model predicts an energy separation of dE = 0.26 eV for the heavy-hole and light-hole ground states in a 3 nm 2D box. The ground state, therefore, in a PMOS nanowire is dominated by the strongly anisotropic heavy-hole states. This argument will be used in the semianalytical explanation of the dispersion and quantization behavior. However, the nanowire dispersions we compute include all bands including heavy hole, light hole, and split off.

Figure 2a shows the (001) surface energy contour of the bulk heavy-hole Si valence band. The anisotropy is clearly evident in the band structure between the [100] and [110]
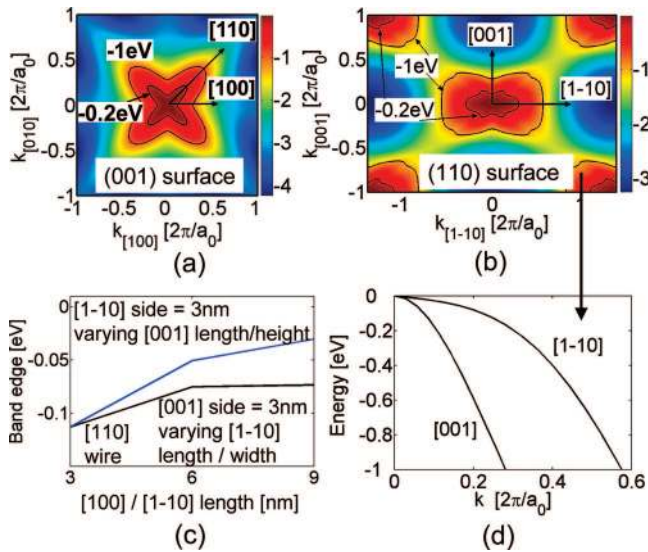
Figure 2. (a, b) Energy surface contours of the heavy hole calculated using the full 3D k-space information of the Si Brillouin zone. The energy contours for $E = -0.2$ eV and $E = -1$ eV are plotted. (a) The (001) surface. The anisotropy is evident between the [100] and [110] directions. (b) The (110) surface. (Or equivalently, −45° "cut" through the center of (a)). (c) The band edge of a [110] transport oriented nanowire for the cases: (1) The size of the [001] directed side increases from 3 to 9 nm while keeping the size of the [1$\bar{1}$0] side at 3 nm (blue). (2) The size of the [1$\bar{1}$0] directed side increases from 3 to 9 nm while keeping the size of the [001] at 3 nm (black). (d) The dispersions of the heavy hole in the [1$\bar{1}$0] and [001] directions.

directions. Figure 2b shows the (110) surface contour (the plane perpendicular at −45° in Figure 1a). The [1$\bar{1}$0] and [001] directions indicated in this figure are the relevant quantization directions of the [110] oriented structure examined in this work. The elongation along the [1$\bar{1}$0] direction (Figure 2, panels b and d) indicates a heavier quantization mass than that seen in the [001] direction, which makes the valence band edge more sensitive to variations in the [001] side (smaller mass) than in the [1$\bar{1}$0] side (larger mass). Figure 2c shows the band edge of [110] nanowire devices (as in Figure 1b) starting from a 3 nm × 3 nm wire, and increasing the width, [1$\bar{1}$0], or the height, [001], directions to 9 nm. Changes in the width, [1$\bar{1}$0] (black), cause smaller variations to the band edge compared to changes in the height, [001] (blue). Most of the total band edge shift because of 2D quantization is a result of the lighter quantization mass (001) surface, in agreement with the particle in a box quantization picture.

Anisotropy Implications on Device Performance. In that scope, Kobayashi et al. in ref 5, showed experimentally that different quantizations impact the performance of nanowire devices through V_T fluctuations and ON-current variations directly originating from the anisotropic band variation. In that work, it was shown that V_T and I_{ON} of PMOS nanowire devices are very sensitive to [100] side variations, but much less sensitive to [110] side variations. This is evidence of the heavier [110] mass quantization that does not allow large subband variations with size fluctuations.

Different Charge Distribution in Different Orientations. The anisotropy in the band structure also affects the charge distribution in the cross section in the wire. As we have shown earlier,[10] in the case of the [110] wires quantized in the [001] and [1$\bar{1}$0] directions, the charge tends to accumulate closer to the heavy quantization mass (1$\bar{1}$0) surfaces rather than the lighter (001) ones. This is also shown in the smaller subfigures surrounding Figure 3a, which show device cross sections and the charge distribution under high bias conditions. The top/bottom surfaces in these figures are (001), whereas the left/right ones are (1$\bar{1}$0) surfaces. Figure 3a (central) shows the ON-current of the nanowires as a function of their height (in the [001] direction) and their width (in the [1$\bar{1}$0] direction) as they change from 3 to 12 nm. More on the details of the centered figure will be discussed further on.

The charge distribution in Figure 3a(iii−v) in the bottom row, for widths [1$\bar{1}$0] 3, 6, and 12 nm, respectively, shows that the charge is preferably accumulated on the (1$\bar{1}$0) left/right surfaces in agreement with ref 28 and splits into two lobes as the width increases. In the body of the wire, as well as along the (001) top/bottom surfaces, smaller charge accumulation is observed. The situation is different in the case were the height [001] increases from 3 to 12 nm in Figure 3a(iii, ii, i) shown in the left column. The charge is accumulated closer to the left/right (1$\bar{1}$0) surfaces, and finally two parallel "3 nm × 3 nm wire" like channels are formed at the top/bottom regions of the nanowire. As the dimensions of the device increase to 6 nm × 12 nm and 12 nm × 12 nm (Figure 3a(vi, vii) in the right column), clearly, a stronger inversion layer is formed along the (1$\bar{1}$0) surfaces (right/left), rather than the (001) surfaces (top/bottom). The inversion layer on the (1$\bar{1}$0) surface extents ~1.5 nm. This distance almost doubles in the case of the (100) surface. We would like to mention here that the charge placement in the devices' corners is a pure electrostatic effect coming from the stronger inversion near the corners of the device due to stronger electric fields. The electrostatic potential in the width and height directions, however, is virtually identical as shown in ref 10. The charge along the surface is the quantity that depends on the quantization mass and the detailed crystal symmetry.

Implications on the ON-Current Variations with Size Variations. The centered plot of Figure 3a shows the ballistic ON-current of [110] oriented nanowire devices as a function of the x axis width [1$\bar{1}$0] and y axis height [001] dimensions of the device. All width/height combinations from 3 nm × 3 nm of nanowires (left/bottom corner), all the way to 12 nm × 12 nm wires (right/upper corner) are presented in steps of 1 nm. (Around the 6−8 nm height size, the steps used are 0.5 nm). All parameters in the simulation are fixed in all cases, with only the dimensions changing. The gate bias is set to $V_G = 1$ V, drain bias $V_D = 0.5$ V in all cases, and the insulator thickness $t_{ins} = 1.1$ nm. The current plotted is in microamperes, while contour lines are drawn every 5 μA.

Clear Boundary Identified between Two Insensitive Regions. Starting from the 3 nm × 3 nm wire (left/bottom corner) where the current is the lowest, the current levels
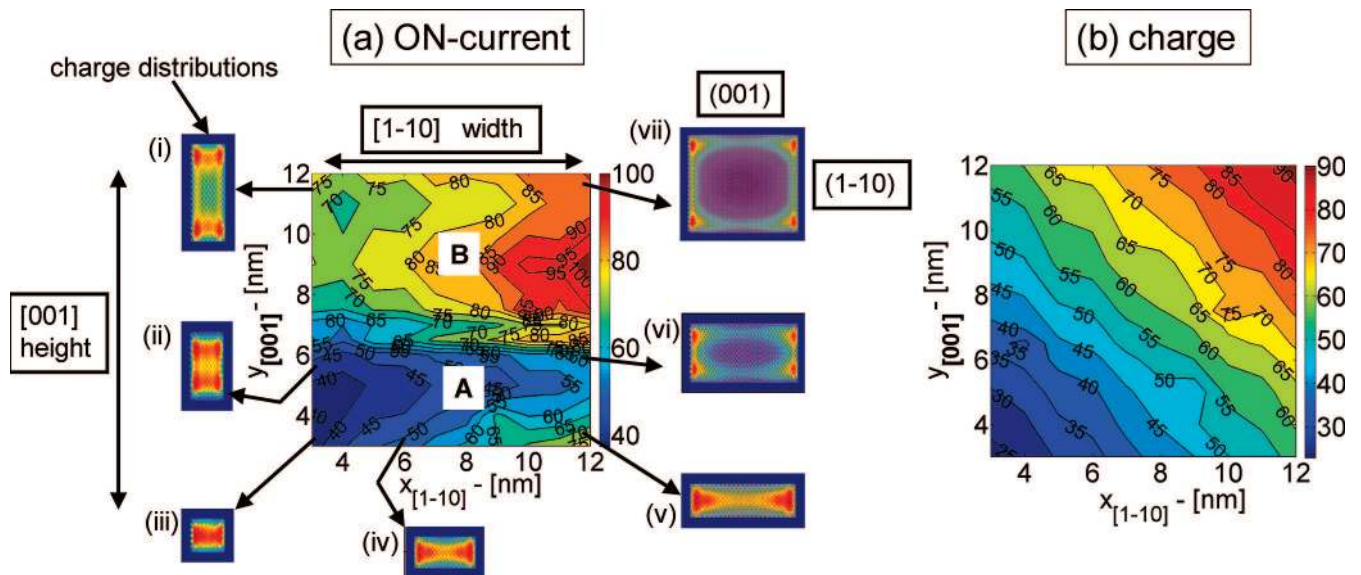
Figure 3. (a) The ON-current contour plot in microamperes as a function of the [110] nanowire's side size variations. The *x* axis is the width in the [1$\bar{1}$0] direction, and the *y* axis is the height in the [001] direction. The side figures show the nanowire's cross section and the charge distribution at high bias for the devices indicated by the arrows in the centered figure. Wires shown (width [1$\bar{1}$0] × height [001]): (i) 3 nm × 12 nm; (ii) 3 nm × 6 nm; (iii) 3 nm × 3 nm; (iv) 6 nm × 3 nm; (v) 12 nm × 3 nm; (vi) 12 nm × 6 nm; (vii) 12 nm × 12 nm. The top/bottom surfaces are (001). The left/right surfaces are (1$\bar{1}$0). (b) The total charge contour plot in the devices of (a). All parameters in the simulations are the same for all devices with only the sizes changing. The gate bias is $V_G = 1$ V and the drain bias $V_D = 0.5$ V.

increase as the dimensions of the device increase to 12 nm × 12 nm (right/upper corner). Regions where the ON-current does not significantly vary with size variations and others that suffer from enhanced variations with size variations can be identified. A region very lightly affected by size variations is the one between 3 and 6 nm of height, and for any width (region A). Within this region, the current does not vary significantly with changing width. Increasing the width from 3 to 12 nm (300%), and equivalently the perimeter by 150%, only increases the ON-current by 50%. The region from 8 to 12 nm of height and any width (region B) can also be considered to be relatively tolerant to height variations, although somewhat higher ON-current variation is observed at widths of 10−12 nm. This variation behavior is almost linear with size variations. In contrast, the region between 6 and 8nm of height and for any width shows very sharp ON-current variations with relatively small height variations and needs to be avoided for a design to be tolerant to variations. A clear boundary between two regions that can be considered relatively insensitive to variations is therefore identified. This current variation originates from the structural and electrostatic quantization behavior of nanowires' band structure in the transverse direction. It is also observed in lower gate biases ($V_G = 0.5$ V), although somewhat smoothed out, i.e., the fast current varying region is expanded to heights [001] of 6−9 nm. The same qualitative results as above were also obtained by using a different set of TB parameters obtained from ref 29, with the same fast varying current region between 6 and 8 nm.

The ON-Current Variation with Width, [1$\bar{1}$0] Variation. The shape of the charge distribution in the cross section of the device as the width increases sheds light on the reason that large variations in the width [1$\bar{1}$0] direction do not result in large variations in the ON-current. As shown in Figure

3a(iii, iv, v), at the bottom of Figure 3a, the charge has formed two channels, on the left/right of the channel. Increasing the width (at a constant 3 nm height), is equivalent to increasing the upper−lower (001) surface areas. Hence, the (001) surface current, as well as the current in the middle of the wire, both increase. This causes a controllable and almost linear change in the ON-current as the width changes (at a constant height). In region labeled "B", for devices with heights from 8 to 12 nm, as the width changes, the changes in the ON-current come from changes in the upper//lower surface areas at the top/ bottom of the nanowire (Figure 3a(vii)). Similar ON-current variations are therefore observed.

The ON-Current Variation with Height, [001] Side Variation. Variations in the [001] equivalent quantization direction also do not cause significant variations in the ON-current performance, except in the region between 6 and 8 nm of width, in which the variations are very large (the ON-current almost doubles with only 2 nm increase in the width). The explanation is also understood from the charge distribution figures along the left/right of Figure 3a. As the [001] quantization height increases, at some point around 6 nm, the charge distribution splits into two "3-nm-like" wires on the top/bottom (001) equivalent surfaces. Two channels are formed now. The ON-current undergoes a sharp increase during this formation. (The reason this sudden change is not observed in the case of width increase is that the two channels have already been formed at the 3 nm width due to the heavier [1$\bar{1}$0] direction quantization mass). Further increase in the height up to 12 nm (at any constant width [1$\bar{1}$0]), increases the length of the inversion layer charge along the left/right (001) equivalent surfaces. The ON-current however does not follow a smooth and linear increase, but it is rather not-sensitive to variations with small oscillations observed. This has to do with the interplay between the carrier velocity
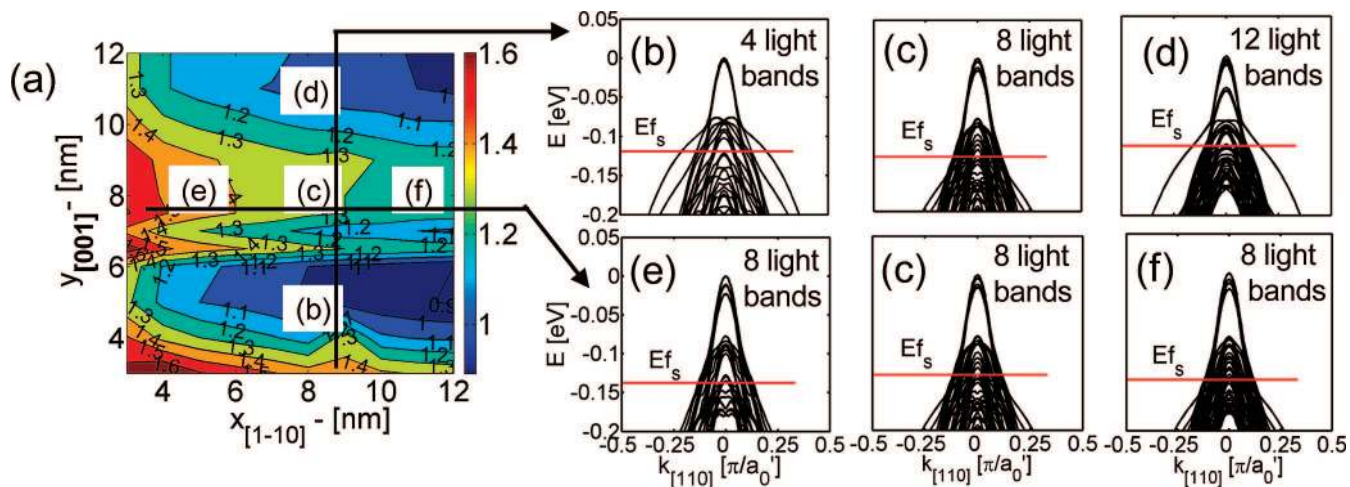
Figure 4. (a) The average velocity contour plot in the devices of Figure 3a. (b) The dispersion relation for the 8 nm × 5 nm wire (point b). (c) The dispersion relation for the 8 nm × 8 nm wire (point c). (d) The dispersion relation for the 8 nm × 12 nm wire (point d). (e) The dispersion relation for the 5 nm × 8 nm wire (point e). (f) The dispersion relation for the 12 nm × 8 nm wire (point f). a_0' is the wires' unit cell length.

and charge as the height [001] increases as it will be explained further down.

Charge Variations. Figure 3b shows the charge variations corresponding to the ON-currents presented in Figure 3a. The charge variation is very symmetric, with respect to the width and height of the device. (A purely symmetric case would be a mirror image about the 45° line across the figure.) It seems that the charge of devices with same perimeter length is very similar, independently if the largest surface is $(1\bar{1}0)$ or (100). This is an observation also noted in refs 7 and 30 when comparing channels of materials with different quantum capacitance (C_Q). In these works, it was shown that in channels with bias-dependent quantum wells, differences in C_Q are smeared out and create much less differences in the total gate capacitance and the inversion layer charge of the device.

Velocity Variations. In the ballistic limit, the ON-current can be calculated by the product of charge times the average carrier velocity. Since the charge is very similar for devices with the same perimeter, the significant differences in the ON-current must originate from the velocity differences. In Figure 4a the average velocity of the carriers is plotted. (This is defined as the total current divided by the total charge in each of the nanowires). The velocity contour plot in Figure 4a has indeed a very different pattern than the charge pattern, and it is the major reason behind the ON-current variation pattern. Noticeable in this figure is the three almost similar velocity regions that can be identified for heights [001] from 3 to 6 nm, ~6 to 9 nm, and ~9 to 12 nm and for any width $[1\bar{1}0]$. In Figure 4b−f the dispersions of the nanowires for the devices labeled (b−f) in Figure 4a are shown. There are two main features that can be identified in the dispersions. The first one is the light mass subbands at higher energies, and the second is the heavier subbands at lower energies, near or below the Fermi level. (Ef_s denotes the position of the Fermi level at the particular bias point.) We would like to stress that these light/heavy subbands should *not* be identified as being heavy- or light-hole-like subbands. They

are rather a mixture of the two. As explained in ref 10, the light subbands originate from the quantization of the heavy hole in the $[1\bar{1}0]$ quantization direction, from states that are physically or electrostatically quantized (and not from the light hole). The heavy subbands originate mostly from the heavy hole states that are lower in energy (outside of the quantized potential well) and do not feel large quantization.

Light Subbands along $(1\bar{1}0)$ Surfaces, Increase in the Height [001]. For a constant width $[1\bar{1}0]$ and varying height [001] as labeled (b), (c), and (d) in Figure 4a, the number of occupied *light* subbands increases from 4 to 8 and then to 12. The charge distribution from these light subbands (with energies near the ground state) accumulates in the potential wells formed along the inverted left/right $(1\bar{1}0)$ surfaces. Increasing the area of these surfaces increases the number of lighter, near-ground-state subbands. An increase in the number of the lighter subbands indicates an increase in the average carrier velocities. Indeed, the average carrier velocity increases as the height [001] increases from 3 to 9 nm. As the height of the nanowire increases more, however, the number of the heavier subbands (with energies farther from the ground-state and wave functions more spread in the body of the wire) also increases, and the average velocity reduces (Figure 4a, region d). An interplay between the light and heavy subbands is what determines the carrier velocity.

Heavier Subbands along (001) Surfaces, Increase in the Width $[1\bar{1}0]$. In the horizontal direction, on the other hand, as the width $[1\bar{1}0]$ increases, the (001) surface increases (labels e, c, and f in Figure 4a). The inversion charge on the (001) surfaces resides further in the nanowires' body than the $(1\bar{1}0)$ surface charge and is primarily composed of the heavier transport mass subbands. The number of light subbands in the dispersions in Figure 4, regions e, c, and f, remains constant at eight subbands in all cases, but the number of heavy subbands increases as the width increases, and the average velocity drops as the wire widths change from region

e to c and finally to f. The interplay between the charge and velocity surfaces results in the current surface shown in Figure 3a.

On the Additional Role of Surface Roughness Scattering (SRS) on Device Variations. Having examined this internal to the nanowire properties quantization behavior and its implication on ON-current variations, we would like to stress that the mechanism described in Figure 3, at which the current undergoes a large increase as the internal charge placement undergoes a transition from two to four surface channels is a fundamental one, solely determined by the crystal direction and the anisotropic masses. Surface roughness will surely modulate the internal mode spectrum and cause performance reduction due to mode-to-mode scattering. However (SRS) will not eliminate the formation of two to four mode transitions which is rather evident here. The effective doubling of the channels that is sensitive to the height variation but not the width variation roughly causes a doubling of the current (∼100% increase), which is much larger than any simulated SRS variation effects in similar cross section size nanowires (∼10%−20% at high inversion conditions).[12−14]

For small side length wires (<4 nm), SR causes performance variations through deforming the subbands by creating local barriers and wells.[14,31] A theoretical quantum transport (NEGF) study in ref 14 showed that SR for wires of side lengths of 3 nm suffers from mobility degradation and large variations at low gate biases; however, the performance is partly recovered and variations in the performance are reduced at high inversion conditions. The reduced effect of SRS in narrow nanowires at high gate biases was also concluded from a semiclassical study in ref 13. In another quantum transport study, Wang et al.[12] showed that the ballisticity of a 3 nm × 3 nm rough nanowire was close to 85%, which does not leave much space for significant variations due to SRS. The reason for the reduced effect of SR variations at high bias is that as the gate bias increases and more carriers are in the channel, further propagating states appear, localization effects become less important, and the potential wells/barriers are smoothen/widen out.

In the case of wires with larger sides (>5 nm), where more modes are now occupied, SRS affects the device mostly through mode coupling/mixing as shown in full 3D transport in an effective mass model.[14] Poli et al.[14] showed that for 20 nm long nanowires of 5 nm × 5 nm, and 7 nm × 7 nm cross sections, SRS itself can only degrade the mobility of the nanowire by ∼10% for both low and high gate biases. In that work, statistics on 20 different roughened nanowire samples showed that the variation in the characteristics of the samples was less than ∼10%. (Larger devices feel the effect of averaging more, and variations are reduced, and since the mobility of the roughened devices is very close to the mobility of the ideal devices (∼90%), there is no room for large variations.) We plan to examine these conclusions with our full 3D atomistic transport model in more detail, especially to examine the effects of atomistic disorder. We believe, however, that the
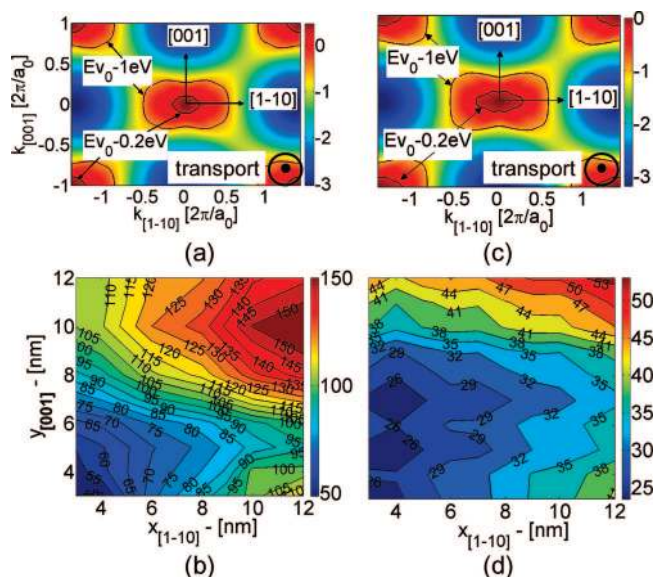

Figure 5. (a) (110) quantization energy surface contour of the heavy hole using 3% compressive strain in the transport [110] direction, 3% tensile strain in the [1$\bar{1}$0] quantization direction, and 0.05% compressive strain in the [001] quantization direction. The energy contours for $E = -0.2$ eV and $E = -1$ eV below the valence band maxima are plotted. Compared to Figure 3a the quantization mass is more isotropic. (b) Same as Figure 3a for the case of the strain tensor described above in (a). (c) (110) quantization energy surface contour of the heavy hole using 1% compressive strain in the transport [110] direction, 3% compressive strain in the [1$\bar{1}$0] quantization direction, and 3% compressive strain in the [001] quantization direction. The energy contours for $E = -0.2$ eV and $E = -1$ eV below the valence band maximum are plotted. Compared to Figure 3a the quantization mass is more anisotropic. (d) Same as Figure 3a for the case of the strain tensor described above in (c).

fundamental conclusion of channel formation and different height and width sensitivities govern the ON-current transport. Fluctuations along the channel will no doubt affect the performance and introduce some variations that will modulate the current further, but the different sensitivity in height and width will remain.

Strain Engineering to Tune the Sharp Current Variation Regions. In the case of PMOS devices, uniaxial compressive strain engineering has been utilized to enhance performance.[32] Here, the effect of two different strain tensor cases on the current variations is examined: One that reduces and one that enhances the heavy-hole anisotropy.

Reduced Anisotropy. Introducing 3% compressive strain in the transport orientation, 3% tensile in the [1$\bar{1}$0] quantization orientation, and moderate compressive strain (0.05%) in the [001] quantization orientation can make the quantization surface look almost isotropic at least for higher energies (Figure 5a), while still having a light transport mass. In this case, as shown in Figure 5b, at the expense of losing some of the tolerance to variations in the previously more insensitive regions, the fast varying boundary can be almost completely removed for widths [1$\bar{1}$0] below 8 nm. It still appears slightly in the 8−12 nm width [001] region. The price of this, however, is the loss of the large variation tolerance in the rest of the design space.

Enhanced Anisotropy Case. On the other hand, introducing a different strain tensor (in this case 3% compressive strain in the two quantization directions and 1% compressive strain in the transport direction), enhances the anisotropy of the heavy hole as shown in Figure 5c. This causes the sharp varying region to shift to larger [001] heights, around 9 nm as shown in Figure 5d. A reduction in the [100] quantization mass allows a larger spread for the wave function in the [001] direction of the wire's cross section, which shifts the transition between a single to double channel at larger [001] heights. (We mention here that this strain combination decreases the transport effective mass, so the current levels are lower; however, it is just a demonstration on how the insensitivity to side size variations can be tuned with strain engineering.)

In summary, the effect of side length sensitivity in the ballistic transport properties of infinitely long and uniform PMOS [110] oriented nanowires with width [1$\bar{1}$0]/height [001] dimensions from 3 nm up to 12 nm was examined. The [110] wires examined, with (1$\bar{1}$0)/(001) quantization surfaces, have asymmetric charge distribution in their cross section, with preferable accumulation along the (1$\bar{1}$0) surface which has a higher quantization mass. Variations in the [1$\bar{1}$0] wire width cause only small and linear variations the ON-current. Variation in the [001] wire height appears to have large impact on the ON-current variation around the 6−8 nm length region, where the transport shifts from volume inversion to two surface inversion layer transport on the two (001) surfaces (equivalently, from two to four lobes, one in each corner). This effect will appear in any situation at which the device shifts from bulk/volume-like transport to two surface-like transport channels. The placement of the boundary in that respect will depend on the quantization masses. Strain engineering can smooth out the large variation of the ON-current or can tune the sensitivity to different design regions. These observations can give guidance toward the design of multisurface devices such as nanowires and FinFETs.

The authors would like to mention that the simulator used in this study will be released as an enhanced version of the Bandstructure Laboratory on nanoHUB.org.[33] This simulation engine will allow any user to duplicate the simulation results presented here. Over 1800 users have run over 12000 simulations in the existing Bandstructure Laboratory, which has not yet included the charge self-consistent transport model we demonstrate here. This new charge self-consistent capability has been added very recently (August 2008).

References

(1) ITRS Public Home Page.http://www.itrs.net/reports.html.

(2) Singh, N.; Lim, F. Y.; Fang, W. W.; Rustagi, S. C.; Bera, L. K.; Agarwal, A.; Tung, C. H.; Hoe, K. M.; Omampuliyur, S. R.; Tripathi, D.; Adeyeye, A. O.; Lo, G. Q.; Balasubramanian, N.; Kwong, D. L. Ultra-narrow silicon nanowire gate-all-around CMOS devices: Impact of diameter, channel-orientation and low temperature on device performance, *International Electron Devices Meeting*, 2006.

(3) Cho, K. H.; Jung, Y. C.; Hong, B. H.; Hwang, S. W.; Oh, J. H.; Ahn, D.; Suk, S. D.; Yeo, K. H.; Kim, D.-W.; Park, D.; Lee, W.-S. Observation of single electron tunneling and ballistic transport in twin silicon nanowire MOSFETs (TSNWFETs) fabricated by top-down CMOS process, *International Electron Devices Meeting*, 2006.

(4) Cho, K. H.; Yeo, K. H.; Yeoh, Y. Y.; Suk, S. D.; Li, M.; Lee, J. M.; Kim, M.-S.; Kim, D.-W.; Park, D.; Hong, B. H.; Jung, Y. C.; Hwang, S. W. Experimental evidence of ballistic transport in cylindrical gate-all-around twin silicon nanowire metal-oxide-semiconductor field-effect transistors. *Appl. Phys. Lett.* **2008**, *92*, 052102.

(5) Kobayashi, M.; Hiramoto, T. Experimental study on quantum confinement effects in silicon nanowire metal-oxide-semiconductor field-effect transistors and single-electron transistors. *J. Appl. Phys.* **2008**, *103*, 053709.

(6) Xiang, J.; Lu, W.; Hu, Y.; Wu, Y.; Yan, H.; Lieber, C. M. Ge/Si nanowire heterostructures as high-performance field-effect transistors. *Nature* **2006**, *441*, 25.

(7) Neophytou, N.; Paul, A.; Lundstrom, M.; Klimeck, G. Bandstructure effects in silicon nanowire electron transport. *IEEE Trans. Electron Devices* **2008**, *55* (6), 1286–1297.

(8) Luisier, M.; Schenk, A.; Fichtner, W. Full-Band Atomistic Study of Source-To-Drain Tunneling in Si Nanowire Transistors. *Proc. SISPAD* **2007**, *97*, 221–224, 978.3-211.72860.4.

(9) Yang, M.; et al. Hybrid-orientation technology (HOT): opportunities and challenges. *IEEE Trans. Electron Devices* **2006**, *53* (5), 965–978.

(10) Neophytou, N.; Paul, A.; Klimeck, G. Bandstructure effects in silicon nanowire hole transport. *IEEE Trans. Nanotechnol.* **2008**, *7* (6), 710–719.

(11) Luisier, M.; Schenk, A. Atomistic simulation of nanowire transistors. *J. Comput. Theor. Nanosci.* **2008**, *5* (June), 1–15.

(12) Wang, J.; Polizzi, E.; Ghosh, A.; Datta, S.; Lundstrom, M. Theoretical investigation of surface roughness scattering in silicon nanowire transistors. *Appl. Phys. Lett.* **2005**, *87*, 043101.

(13) Lenzi, M.; Gnudi, A.; Reggiani, S.; Gnani, E.; Rudan, M.; Baccarani, G. Semiclassical transport in silicon nanowire FETs including surface roughness. *J. Comput. Electron.* **2008**, *7*, 355–358.

(14) Poli, S.; Pala, M. G.; Poiroux, T.; Deleonibus, S.; Baccarani, G. Size dependence of surface-roughness-limited mobility in silicon-nanowire FETs. *IEEE Trans. Electron Devices* **2008**, *55*, 11.

(15) Boykin, T. B.; Klimeck, G.; Oyafuso, F. Valence band effective-mass expressions in the sp^{3}d^{5}s* empirical tight-binding model applied to a Si and Ge parametrization. *Phys. Rev. B* **2004**, *69*, 115201–115210.

(16) Klimeck, G.; Oyafuso, F.; Boykin, T. B.; Bowen, R. C.; von Allmen, P. *Comput. Model. Eng. Sci.* **2002**, *3* (5), 601–642.

(17) Klimeck, G.; Ahmed, S.; Bae, H.; Kharche, N.; Clark, S.; Haley, B.; Lee, S.; Naumov, M.; Ryu, H.; Saied, F.; Prada, M.; Korkusinski, M.; Boykin, T. B. Atomistic simulation of realistically sized nanodevices using NEMO 3-D−Part I: Models and benchmarks. *IEEE Trans. Elecron Devices* **2007**, *54* (9), 2079–2089.

(18) Slater, J. C.; Koster, G. F. Simplified LCAO method for the periodic potential problem. *Phys. Rev.* **1954**, *94*, 6.

(19) Lundstrom, M. S.; Guo, J. *Nanoscale transistors: Device physics, modeling and simulation*; Springer: Berlin, 2006.

(20) Rahman, A.; Guo, J.; Datta, S.; Lundstrom, M. Theory of ballistic nanotransistors. *IEEE Trans. Electron Devices* 2003 *50* (9), 1853 1864.

(21) Fischetti, M. V.; Ren, Z.; Solomon, P. M.; Yang, M.; Rim, K. Six-band k.p calculation of the hole mobility in silicon inversion layers: Dependence on the surface orientation, strain, and silicon thickness. *J. Appl. Phys.* **2003**, *94*, 2.

(22) Wang, E. X.; Matagne, P.; Shifren, L.; Obradovic, B.; Kotlyar, R.; Cea, S.; Stettler, M.; Giles, M. Physics of hole transport in strained silicon MOSFET inversion layers. *IEEE Trans. Electron Devices* **2006**, *53*, 8.

(23) De Michelis, M.; Esseni, D.; Tsang, Y. L.; Palestri, P.; Selmi, L.; O'Neil, A. G.; Chattopadhyay, S. *IEEE Trans. Electron Devices* **2007**, *54*, 9.

(24) Lee, S.; Oyafuso, F.; Von Allmen, P.; Klimeck, G. Boundary conditions for the electronic structure of finite-extent embetted semiconductor nanostructures. *Phys. Rev. B* **2004**, *69*, 045316–045323.

(25) Luisier, M.; Klimeck, G. Full-band and atomistic simulation of n- and p-doped double-gate MOSFETs for the 22nm technology node, *Simulation of Semiconductor Processes and Devices*; SISPAD 2008. International Conference on 9−11 Sept 2008;pp 17−20, IEEE Proceedings, Digital Object Identifier 10.1109/SISPAD.2008.4648226, 2008.

(26) Luisier, M.; Klimeck, G. OMEN an Atomistic and Full-Band Quantum Transport Simulator for post-CMOS Nanodevices, *8th IEEE Conference on Nanotechnology*; NANO '08., 18−21 Aug. 2008, pp 354−357, IEEE proceedings, Digital Object Identifier 10.1109/NANO.2008.110, 2008.

(27) Luisier, M.; Neophytou, N.; Kharche, N.; Klimeck, G. Full-Band and Atomistic Simulation of Realistic 40 nm InAs HEMT *IEEE Proceedings of International Electron Devices Meeting*, 2008.

(28) Saitoh, M.; Kobayashi, S.; Uchida, K. Physical Understanding of Fundamental Properties of Si (110) pMOSFETs Inversion-Layer Capacitance, Mobility Universality, and Uniaxial Stress Effects. *IEEE Proceedings of International Electron Devices Meeting* **2007**, 711–714.

(29) Jancu, J. M.; Scholz, R.; Beltram, F.; Bassani, F. Empirical spds* tight-binding calculation for cubic semiconductors: general method and material parameters. *Phys. Rev. B* **1998**, *57* (11), 15.

(30) Pal, H. S.; Cantley, K. D.; Ahmed, S. S.; Lundstrom, M. S. Influence of bandstructure and channel structure on the inversion layer capacitance of silicon and GaAs MOSFETs. *IEEE Trans. Electron Devices* **2008**, *55*, 904–908.

(31) Uchida, K.; Takagi, S. Carrier scattering induced by thickness fluctuation of silicon-on-insulator film in ultrathin-body metal-oxide-semiconductor field-effect transistors. *Appl. Phys. Lett.* **2003**, *82*, 17.

(32) Thompson, S. E.; Armstrong, M.; Auth, C.; Alavi, M.; Buehler, M.; Chau, R.; Cea, S.; Ghani, T.; Glass, G.; Hoffman, T.; Jan, C.-H.; Kenyon, C.; Klaus, J.; Kuhn, K.; Ma, Z.; Mcintyre, B.; Mistry, K.; Murthy, A.; Obradovic, B.; Nagisetty, R.; Nguyen, P.; Sivakumar, S.; Shaheed, R.; Shifren, L.; Tufts, B.; Tyagi, S.; Bohr, M.; El-Mansy, Y. A 90-nm logic technology featuring strained-silicon. *IEEE Trans. Electron Devices* **2004**, *51* (11), 1790–1797.

(33) Bandstructure lab on nanoHUB.org (https://www.nanohub.org/tools/bandstrlab/).

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