Open access • Journal Article • DOI:10.1088/1748-0221/5/12/C12021

Design studies of the ATLAS muon Level-1 trigger based on the MDT detector for the LHC upgrade — Source link

Osamu Sasaki, Y. Suzuki, Kunihiro Nagano, Masaya Ishino ...+11 more authors

Institutions: KEK, University of Tokyo, Tokyo Metropolitan University, Nagoya University ...+2 more institutions

Published on: 01 Dec 2010 - Journal of Instrumentation (IOP Publishing)

Design studies of the ATLAS muon Level-1 trigger based on the MDT detector for the LHC upgrade

2010 JINST 5 C12021

(http://iopscience.iop.org/1748-0221/5/12/C12021)

PUBLISHED BY IOP PUBLISHING FOR SISSA

RECEIVED: *October 29, 2010*
ACCEPTED: *November 16, 2010*
PUBLISHED: *December 10, 2010*

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2010,
20–24 SEPTEMBER 2010,
AACHEN, GERMANY

Design studies of the ATLAS muon Level-1 trigger based on the MDT detector for the LHC upgrade

O. Sasaki,[a,1] **Y. Suzuki,**[a] **K. Nagano,**[a] **M. Ishino,**[a] **M. Ikeno,**[a] **K. Bendtz,**[b] **T. Domae,**[b] **H. Sakamoto,**[b] **T. Kawamoto,**[b] **C. Fukunaga,**[c] **H. Shichi,**[d] **M. Tomoto,**[d] **Y. Sugaya,**[e] **K. Tokunaga**[f] **and H. Kurashige**[f]

[a] *High Energy Accelerator Research Organization (KEK), Institute of Particle and Nuclear Studies, 1–1 Oho, Tsukuba-shi, Ibaraki-ken 305-0801, Japan*
[b] *The University of Tokyo, International Center for Elementary Particle Physics and Department of Physics, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-0033, Japan*
[c] *Tokyo Metropolitan University, Graduate School of Science and Technology, 1-1 Minami-Osawa, Hachioji, Tokyo 113-0033, Japan*
[d] *Nagoya University, Graduate School of Science, Furo-Cho, Chikusa-ku 464-8602, Japan*
[e] *Osaka University, Graduate School of Science, 1-1 Machikaneyama-machi, Toyonaka, Osaka 560-0043, Japan*
[f] *Kobe University, Graduate School of Science, 1-1 Rokkodai-cho, Nada-ku, Kobe 621-8522, Japan*

E-mail: osamu.sasaki@kek.jp

ABSTRACT: The present muon Level-1 trigger of the ATLAS detector is given by dedicated detectors; RPC and TGC chambers in barrel and end-cap regions, respectively. The Monitored Drift Tube (MDT) chambers and the Cathode-Strip Chambers (CSC) are used for precision measurements of muon tracks. The performance of the muon Level-1 trigger is limited by the momentum resolution of the trigger chambers. In order to improve the trigger performance, a muon track finding scheme based on MDT signals is envisaged. Studies of the scheme and the algorithm are presented. The trigger latency is estimated to be approximately 3 μs.

KEYWORDS: Muon spectrometers; Trigger algorithms; Trigger detectors; Digital electronic circuits

[1] Corresponding author.

doi:10.1088/1748-0221/5/12/C12021

2010 JINST 5 C12021

Contents

2010 JINST 5 C12021

1 Present system and improvement scenario

The ATLAS muon spectrometer system consists of two types of chambers, which are for the purpose of either the precision momentum measurements of tracks or fast track finding for the Level-1 trigger, as shown in figure 1 [1]. The Monitored Drift Tube chambers (MDT, tube of 30 mmϕ) and the Cathode-Strip Chambers (CSC) in the innermost end-cap region are used as precision-tracking chambers. The Resistive Plate Chambers (RPC) in the barrel and the Thin Gap Chambers (TGC) in the end-cap region are dedicated to triggering. The RPC has three stations at the middle (BML) and the outer (BOL) areas. The TGC consists of three stations at the middle area (EML). There is no trigger chamber at the inner stations (BIL, EIL and EEL). There is a toroidal magnetic field in

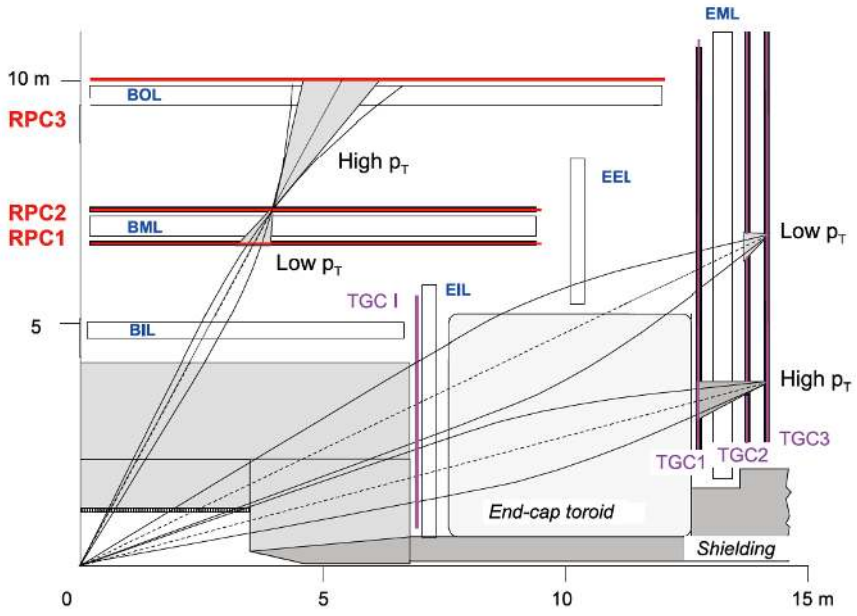

Figure 1. Cross-section of the present Muon Level-1 Trigger system. BIL/BML/BOL: Barrel Inner/Middle/Outer Large MDT. EIL/EEL/EML: End-cap Inner/Extra/Middle Large MDT.

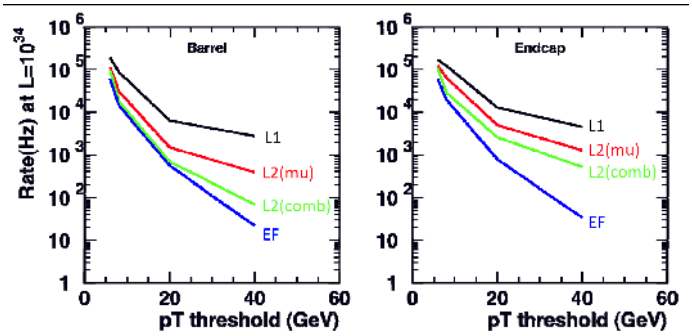

Figure 2. The simulated trigger rates of Level-1, Level-2 and Event Filter at L=1034 cm-2s-1. Black: Level-1, Red: Level-2 (mu) using MDT data, Green: Level-2 (comb) combination with MDT and inner tracker, Blue: full tracking using all the data. The left is the barrel part and the right is the endcap part.

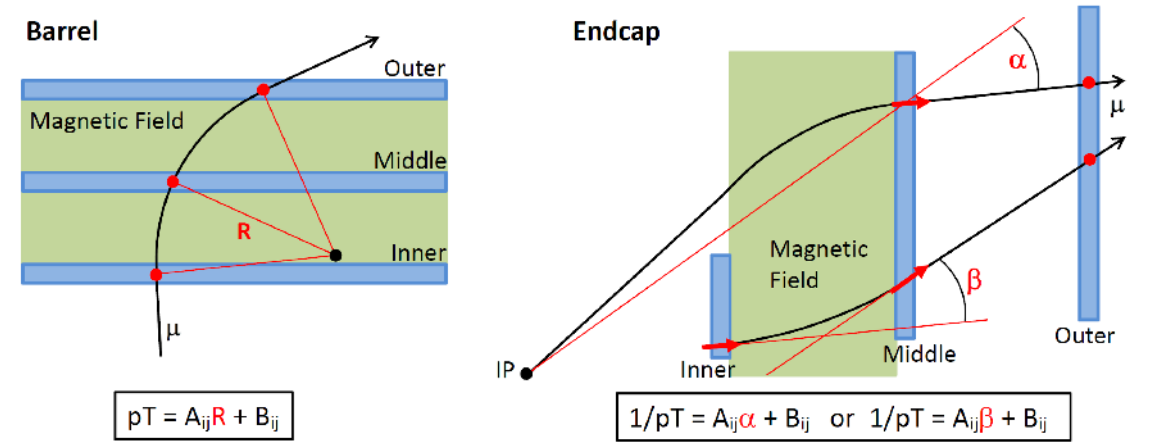

Figure 3. Level-2 Trigger Algorithm using MDT stations in Barrel and Endcap.

the barrel region, located between the inner and the outer station, as well as in the end-cap region between the inner and the middle station. The muon trigger system flags a muon track with the p_T thresholds in the range of 6–35 GeV. The latency of the Level-1 trigger has been decided to be 2.5 μs, which will be kept in the Phase-I upgrade.

Figure 2 shows the simulated trigger rates at Level-1, Level-2 and Event Filter (EF, Level-3) at L=10^{34} cm^{-2}s^{-1} [2]. The trigger chambers and their trigger circuits satisfy the requirements of the L=10^{34} cm^{-2}s^{-1} operation. In the luminosity upgrade of the LHC, improvements of the trigger performance are required in order to increase the robustness against background. According to simulation studies of the Level-1 muon trigger, the dominant contribution to the trigger rate is sharpness of the p_T threshold curve, which is determined by the momentum resolution of the detector system. The long tail of the threshold curve towards the lower momentum region increases the background rate. The estimated momentum resolution of the present trigger system is 15–20% at p_T =20 GeV and 30% at p_T =40 GeV. Detectors having higher momentum resolution for the trigger will make the p_T threshold curves sharper. Additional trigger detectors at the innermost regions of the barrel and the end-cap will also improve the Level-1 trigger rate.

2010 JINST 5 C12021

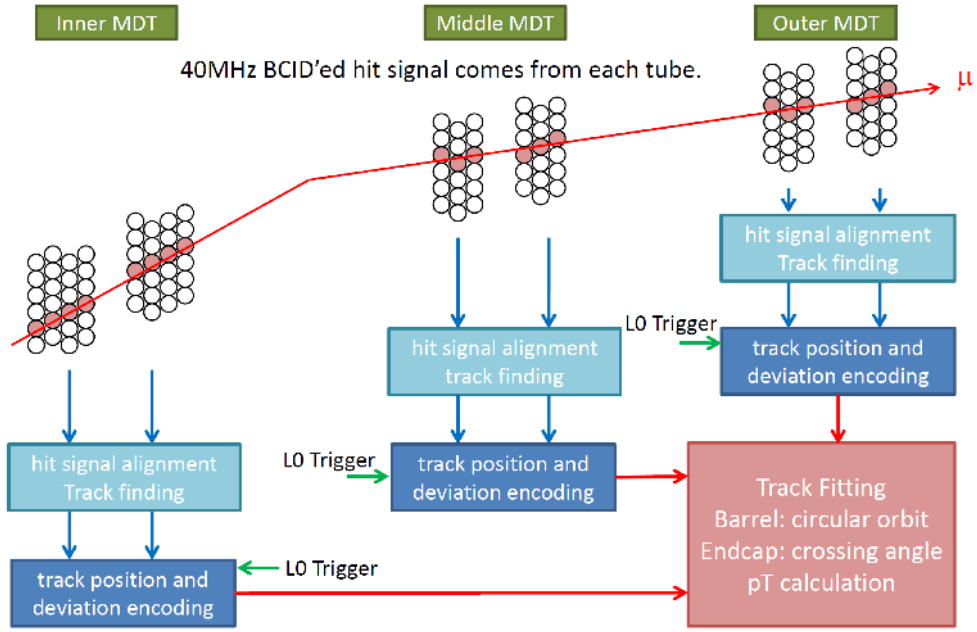

Figure 4. Block diagram of MDT based Level-1 Trigger.

A replacement of the existing trigger electronics would not be a solution to the problem, since it would not further reduce the muon trigger rate at low p_T and accordingly the total rate. This is because the trigger performance is determined only by the spatial resolution of the trigger chambers and their geometrical layout. However, if we can implement the Level-2 (mu) algorithm using MDT data in the Level-1 hardware logic, a factor of ~ 5 reduction for the trigger rate can be expected. Figure 3 shows the algorithm of the Level-2 muon tracking (software code "muFast") [2]. Track fitting with a straight-line is made in each MDT station (Inner, Middle and Outer). In the barrel, the hit position at the center of each station is calculated. Fitting with a circular arc is made from three hit positions and then its radius R gives the p_T value. In the end-cap, the crossing angle α between the track slope measured in Middle and the infinite momentum track from the interaction point (IP), or the angle difference β between track slopes in Inner and Middle are measured. The angle α or β is then converted to a p_T value using Look-up-Tables (LUT).

2 MDT based Level-1 Trigger

A block diagram of the MDT based Level-1 Trigger is shown in figure 4. The signals from all the MDT tubes are bunch-identified (BCID) with the 40 MHz LHC clock and sent to the counting room. Track fitting/finding with a straight line in each MDT station is made in parallel. The output from the finding logic is information about the track position and its deviation from an infinite p_T track. The TGC and the RPC can provide unique bunch identification of a muon track. The bunch timing when a muon passes through MDT stations is obtained from the TGC or the RPC as a Level-0 signal. The Level-0 signal enables a bunch identification of the MDT system and will also assist in finally determining a track from the MDT signals. The track information from each station is combined and the p_T value is calculated.

2010 JINST 5 C12021

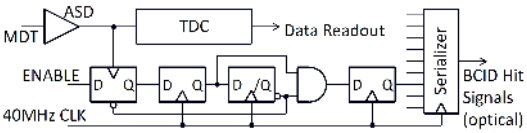

Figure 5. Bunch-Identification circuit.

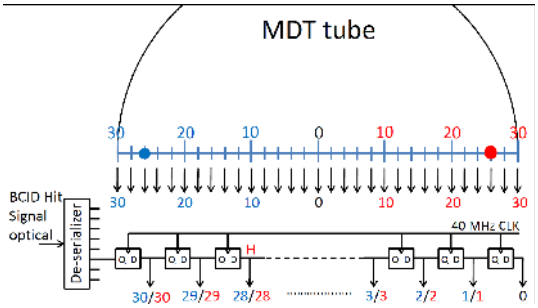

Figure 6. Hit signal decoding with 25 ns time slice using a 31-stage shift register.

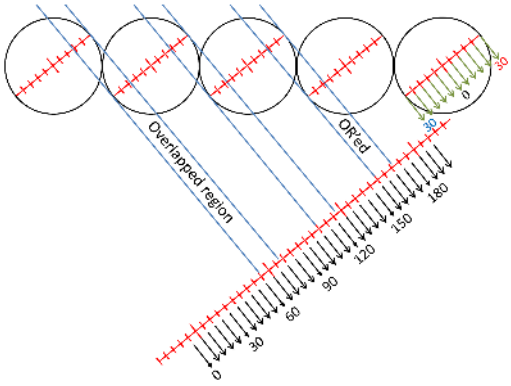

Figure 7. Spatial-aligned hit signals.

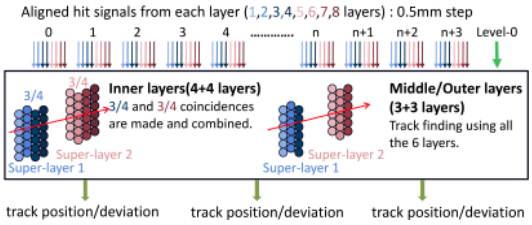

Figure 8. Station coincidence logic.

Figure 5 shows the BCID circuit, where leading edges of the hit signals from the ASD's are detected in each bunch (25 ns), which corresponds to 0.5 mm spatial resolution. The BCID hit signals are serialized and transmitted to the counting room via high speed optical links. The signals from the MDT front-end boards are deserialized and fed to decoding circuits as shown in figure 6. Each MDT tube has a 31-stage shift-register, which decodes the BCID hit signal to time/spatial-aligned hit signals (25 ns timing and 0.5mm spatial-aligned). One BCID hit signal is converted to 61 hit signals [30,29,28,,1,0,1,,28,29,30]. A "hit signal" is then transmitted from register to the next from 30/30 to 0 at the 40MHz clock. The colours (blue or red) correspond to the two possible drift directions of the drift electrons. Decoded hit signals from each layer are projectively aligned in accordance with the expected incidence angle of an infinite p_T muon, as shown in figure 7. Hit signals from the overlapped region of neighboring tubes are logical-OR'ed. Aligned hit signals from each layer are fed to the track fitting/finding block in figure 8. The required p_T threshold for the experiment at the LHC upgrade is larger than 20 GeV.

At the inner stations, the expected deviations of the tracks from infinite p_T muons are less than $\pm 1^\circ$, so that one can restrict the track finding window to a very narrow range. 3-out-of-4 coincidence is imposed in each super-layer individually. The information of positions and track deviations from both super-layers are combined and the track candidates are extracted.

At the middle and outer stations, the track finding window is expanding into a larger area since the expected deviations of the tracks are up to $\pm 2.5^\circ$. We have to perform the track finding using

2010 JINST 5 C12021

Table 1. Latency estimation of MDT Track Trigger.

	ns	CLK	Total CLK
TOF from interaction point to MDT	65	2.5	2.5
Propagation delay along wire	30	1.5	4
MDT drift time (0–700 ns)	700	28	32
ASD	10	1	33
Bunch ID		2	35
Serializer + Optical Tx		2	37
Optical fiber cable (90m)		18	55
Optical Rx + De-serializer		3	58
Shift Register (28-steps, 0–700 ns)		0	58
Local coincidence		2	60
Track finding		2	62
Encoding		1	63
Track information from 3 MDT stations combined			
Crossing angle calculation		3	66
pT calculation (LUT)		3	69
pT encoding		1	70
Cable to MUCTPI (10m)		2	72
MUCTPI		11	83
Cable to CTP (2.4m)		0.5	83.5
CTP		6	89.5
Cable to LTPI (10m)		2	91.5
LTPI + LTP + TTCvi + TTCex		2	93.5
Variable delay		2	95.5
Optical cable (110m max.)		22	117.5
TTCrq + fanout		3	120.5
Cable to frontend electronics		1.5	122
Total latency			3.05 μ s

aligned hit signals from all the 6 layers of the station in order to distill track candidates efficiently, shown in figure 8. The algorithm for the track finding is being studied. The Level-0 trigger signal from TGC/RPC will be used to distill track candidates as well as the bunch identification. The information (position and deviation) of distilled tracks is sent to the next block, where the final track fitting is made using all the information from the three MDT stations. The fitting of a circular arc is made in the present Level-2 algorithm using the barrel data (figure 3: Barrel). It may be too ambitious to implement a similar algorithm in hardware within the limited latency budget and studies for the algorithm of hardware are to be continued. The implementation of the algorithm for the end-cap part is feasible for hardware. Using the fitting results, p_T values are obtained. An algorithm based on LUT's is envisaged.

3 Latency estimation

Table 1 shows the estimated latency of the MDT muon track trigger. The latency budget from "Cable to MUCTPI" to "Cable to front-end electronics" in the table is the measured values of

2010 JINST 5 C12021

the present TGC Level-1 system. The total latency is 3.05 μs, which is 500 ns longer than that of the present TGC system. A considerable contribution comes from the MDT drift time. The contingency of the present ATLAS system is estimated to be less than 20 clocks. Further effort to reduce the latency of the Level-1 trigger and improvement of each sub-detector to cope with longer latency are desired for the upgrade of the LHC.

4 Conclusion

The ATLAS muon Level-1 trigger based on the MDT signals is being studied for the LHC upgrade. The conceptual design has been proposed and we have started R&D towards a concrete design for implementation. The latency of the trigger is estimated to be approximately 3 μs. The software code for the trigger simulation is being developed to study the algorithm of the track fitting/finding and the p_T calculation. The algorithm should be hardware-oriented to be able to implement in FPGA's and is better to be fully synchronized logic with fixed latency ($<$3.2 μs in total). We also have to evaluate the tracking efficiency, any efficiency holes and the probability of incorrect tacking using real data as well as Monte Carlo data.

References

[1] G. Aad et al., *The ATLAS Experiment at the CERN Large Hadron Collider*, 2008 *JINST* **3** S08003.

[2] G. Asd et al., *Expected Performance of the ATLAS Experiment: Detector, Trigger and Physics*, *Rev. Sci. Instrum* **76** (2005) 054503 [arXiv:0901.0512v4].

2010 JINST 5 C12021