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Design techniques for a stable operation of cryogenic field-programmable gate arrays

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In this paper, we show how a deep-submicron field-programmable gate array (FPGA) can be operated more stably at extremely low temperatures through special firmware design techniques. Stability at low temperatures is limited through long power supply wires and reduced performance of various printed circuit board components commonly employed at room temperature. Extensive characterization of these components shows that the majority of decoupling capacitor types and voltage regulators are not well behaved at cryogenic temperatures, asking for an *ad hoc* solution to stabilize the FPGA supply voltage, especially for sensitive applications. Therefore, we have designed a firmware that enforces a constant power consumption, so as to stabilize the supply voltage in the interior of the FPGA. The FPGA is powered with a supply at several meters distance, causing significant resistive voltage drop and thus fluctuations on the local supply voltage. To achieve the stabilization, the variation in digital logic speed, which directly corresponds to changes in supply voltage, is constantly measured and corrected for through a tunable oscillator farm, implemented on the FPGA. The impact of the stabilization technique is demonstrated together with a reconfigurable analog-to-digital converter (ADC), completely implemented in the FPGA fabric and operating at 15 K. The ADC performance can be improved by at most 1.5 bits (effective number of bits) thanks to the more stable supply voltage. The method is versatile and robust, enabling seamless porting to other FPGA families and configurations. https://doi.org/10.1063/1.5004484

I. INTRODUCTION

The cryogenic operation of electronic circuits in general and field-programmable gate arrays (FPGAs) in particular has been extensively studied over the past years.[1–7] The majority of the FPGA building blocks, in Xilinx Artix 7 series, for instance, has been shown to operate rather stably over the temperature range from 4 K to 300 K.[5–7] For example, the delay change in both look-up tables (LUTs) and carry elements has been shown to change by less than 10%.

Although the performance of FPGAs operating at deep-cryogenic temperatures is shown to be stable, this is only demonstrated in specific cases, e.g., when building blocks were tested individually. These tests ignored the influence of voltage drop over the long power supply wires into the cryogenic environment and also ignored the influence the blocks might have on one another. Furthermore, the behaviour of other components, ancillary to the FPGA, is not well known. This is of particular importance when, as it is the case in this work, a platform is to be implemented to control a quantum processor.

The most important components for such a platform are a power decoupling network and DC power supplies or voltage regulators. Capacitors in general tend to drop significantly in capacitance and they increase the effective series resistance (ESR) by up to 1000×.[8–12] Previous studies[13,14] have shown some voltage regulators to operate at cryogenic temperatures, as low as 90 K, but no regulators were found to be working stably below that temperature due to either protection circuitries, bipolar transistors,[15,16] or biasing.

Power networks, that do not behave properly, can pose a burden on optimal FPGA performance, especially when the power is supplied over long wires. While FPGAs switch significant amounts of current at high frequencies, fluctuating voltage drop over these wires can be significant. While a static voltage drop would not cause significant problems, the dynamic voltage drop continuously alters the internal delays of the FPGA, causing potential glitches and irregularities. Usually, these problems are mitigated using decoupling capacitors, but the performance of capacitors at cryogenic temperatures is not sufficient to compensate for these fluctuations.

In this paper, we propose a novel methodology to implement hardware modifications in FPGAs via firmware design, so as to compensate for any potential fluctuations of power dissipation due to sub-optimal structures or biasing in the interior of the FPGA. The technique is based on real-time measurements of the variation of cell delay in the carry chain. This fluctuation is mainly caused by voltage drop of the logic supply voltage and also by temperature fluctuations. A small farm of oscillators is used to flatten out the power consumption in real-time, so as to automatically stabilize the power supply as well.

Similar techniques have been shown before, but mainly for the purpose of avoiding security attacks. In those systems,

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TABLE I. Summary of the performance change of several capacitors as used on the FPGA platform PCB and some potential better candidates. All values are measured at a test frequency of 100 Hz.

			300 K		4 K			
Specified capacitance (μF)	Type	Part number	Capacitance (μF)	ESR (Ω)	Capacitance (μF)	ESR (Ω)	ΔC (%)	ΔESR (%)
0.47	NP0	C2220C474J5GACTU	0.475	0	0.475	0.54	0	∞
1	PPS	SMDIC04100TB00KQ00	1.01	0	1.02	0	1	0
4.7	X8L	C1206C475J8NACTU	4.75	6	0.32	189	−93	3050
47	Tantalum	16TQC47MW	44.5	0.8	38.2	0	−14	−100
100	Tantalum	T495D107K010ATE050	102.8	0.2	91.9	1.8	−11	800
330	Tantalum	T495X337K010ATE035	328.2	0.1	265.4	0	−19	−100
0.47	PPS	SMDIC03470TB00JQ00	0.475	0	0.478	0	1	0
1	Silicon	935133427710-T3N	1.03	1.4	1.01	0	−2	−100

the power consumption or heat has to be flattened in order to prevent one from reading data through power or heat changes. For instance, Ref. 17 proposes the use of a distributed oscillator farm to equalize the heat map from the FPGA seen from outside. Its control is based on the difference in frequency shift of two differently sized ring oscillators, which is proportional to temperature.

In this paper, we first study the behaviour of (passive) decoupling capacitors and (active) voltage regulators in Sec. II. In Sec. III, we propose an architecture, implemented inside the FPGA to stabilize power consumption. Results showing the effectiveness of the stabilization technique are presented in Sec. IV.

II. PASSIVES AND ACTIVES

A. Capacitors

Passive components form an important part of any printed circuit board (PCB) design, whether the PCB houses a field-programmable gate array (FPGA) or an application specific integrated circuit (ASIC) as the main embodiment. Especially capacitors, which are not only used for the decoupling networks of power supplies but also used for analog filters, are important. At cryogenic conditions, the material properties can differ significantly, altering the dielectric values and thus the resulting junction capacitance and/or resistance. As this is such an important part of any system, a study was conducted to find the optimal capacitor materials that are commercially available, while for some applications, it might be worth investigating the performance of cryogenic specialized materials.

Several studies[8–12] revealed that significant changes are to be expected, with a large dependency on material dielectric properties. For example, high k-dielectric constant materials, such as X5R or X7R, drop almost to zero capacitance, while low k materials, such as NP0, are very stable.

FPGA systems in particular require a large decoupling network, with capacitance values ranging from 1 to 330 μF. With this large diversity, it is impossible to use only one dielectric (due to size and availability), and a solution for the higher values has to be found. Tantalum capacitors seem to be a good trade-off between performance and available values.[9,11] There are also special tantalum capacitors available for cryogenic applications, but their performance is only optimal down to 77 K (see the supplementary material).

In Table I, an overview of the tested capacitors is given together with their type and values. Listed are the capacitors currently used on the FPGA PCB and some potential better candidates, with the measured capacitance and effective series resistance at 4 K and 300 K. Tests were executed using a Keysight impedance analyzer and a test frequency of 100 Hz. The variance of both capacitance and effective series resistance (ESR) is mainly dictated by the material type. Clearly NP0/COG and PPS capacitor materials are ideal with both limited change in capacitance and no significant increase in ESR as a function of temperature. The worst capacitors are based on ceramic materials with high dielectric constants. In these devices, the capacitance drops over 90% and ESR increases over 3000%.

The relative capacitance and ESR over temperature are plotted in Fig. 1(a) for the majority of capacitors from Table I. For the ceramic capacitor, the capacitance drops almost linearly with temperature. The ESR on the other hand increases quasi-exponentially while lowering temperature as is shown in

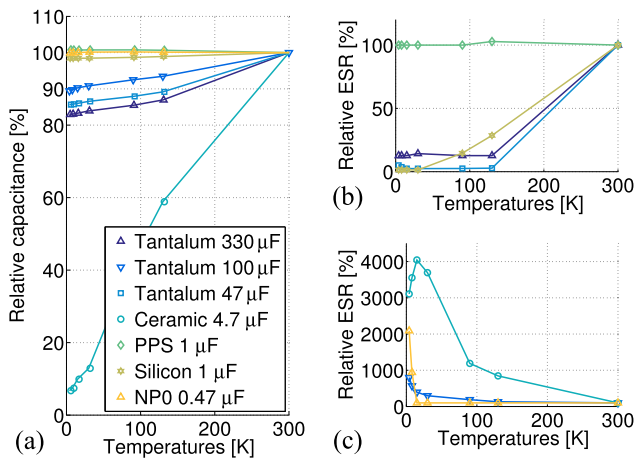

FIG. 1. (a) Relative capacitance, (b) relative effective series resistance (ESR) decreasing towards 4 K, and (c) relative ESR increasing towards 4 K, for the majority of capacitors from Table I over temperature. Results extended from Ref. 6.

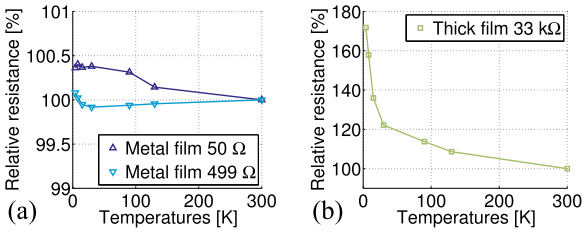

FIG. 2. Relative resistance for different materials, (a) metal and (b) thick film, over temperature. More detailed plots are shown in the supplementary material.

Fig. 1(b). More extensive characterization results are reported in the supplementary material.

For optimal cryogenic performance of the decoupling network, selecting the appropriate capacitor type is important. Special cryogenic capacitors, based on tantalum EPPL2,[18] were tested and found to be generally better down to 77 K. At 4 K, however, those capacitors significantly loose capacitance and increase ESR. Another type of capacitor is based on silicon, which is only available for small values under 1 μF. Those capacitors exhibit a very similar performance to NP0/COG types, with, as main advantage, a significantly smaller footprint. As space is limited in dilution fridges, significantly smaller components are preferable.

B. Resistors

Although not as important as capacitors, resistors are commonly used for filters, protection circuits, termination, etc. Therefore, the behaviour of resistances at cryogenic temperatures has to be well understood. As for capacitors, several resistive materials have been studied in the past.[11] Metal film resistors are found to be most stable over temperature, with fairly limited change in resistance (<1%). Figure 2(a) shows the resistance of a Vishay 50 Ω (FC0603E50R0BST1) and a Panasonic 499 Ω SMD resistor (ERA-3AEB4990V) over temperature. As comparison, a thick film equivalent is shown in Fig. 2(b).

C. Voltage regulators

Voltage regulators or DC-DC converters form the core of any power distribution network. Especially for FPGA systems with significant switching currents, the voltage regulation has to be done as close as possible to the FPGA in order to reduce latency and thus increase stability and reduce voltage drop. As the wire length into any cryogenic system is generally several meters long, voltage regulation at cryogenic temperatures can significantly improve system stability and performance.

Previous studies have shown operating voltage regulators; however, the temperature range was generally limited to 77 K. Simple shunt regulators based on Zener diodes have been shown to operate down to 100 K with relatively stable performance.[14] Also low drop-out (LDO) voltage regulators have been shown to operate down to 77 K.[13]

Several voltage regulators have been tested in the temperature range from 4 K to 300 K and the output voltage is plotted versus temperature in Fig. 3(a). Measurements were done at the specified V_{in} and the regulators were loaded with 100 Ω. As can be seen, none of the regulators are stable in voltage over the complete temperature range. Most regulators simply switch off or clip (proportionally) to their input voltage. The switching-off behaviour can be explained by the internal protection circuitry, which shuts down the regulator when a certain temperature or internal voltage limit has been reached. To concretize functionality, a 2.5% margin was allowed on the output voltage with respect to room temperature. The corresponding output voltage plots for all regulators are presented in the supplementary material. The best performing regulator was found to be an LDO from Texas Instruments (TPS7A7002), at least in terms of output voltage. The device is extremely stable down to 90 K, at which temperature it completely turns off.

Besides a stable output, the power consumption is extremely important at cryogenic temperatures, due to limited power budgets in any cryogenic system. The power consumed

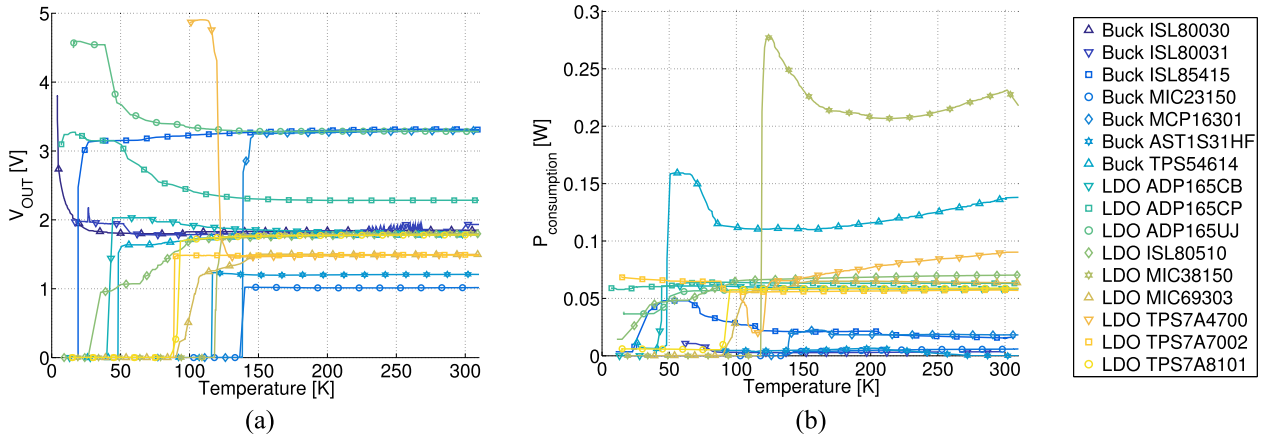

FIG. 3. (a) Output voltage and (b) consumed power of several DC-DC converters/voltage regulators over temperature. All tested regulators fail operation at temperatures roughly below 90 K when assuming a 2.5% margin on the voltage at 300 K. More complete characterization can be found in the supplementary material.

in the same set of regulators is shown in Fig. 3(b). It is well known that switching voltage supplies outperform other regulator types in terms of power consumption, as is also shown here. The most stable converter (TPS7A7002) has a power consumption of roughly 60 mW, roughly an order of magnitude higher than most switching converters.

Of course the main trade-off is regulator stability versus noise (output ripple, etc.) and power consumption. In general, switching supplies introduce more noise, while consuming less power. LDOs introduce very limited amounts of noise, while, due to the drop-out behaviour, the power consumption is higher.

The best performing switching converter is the ISL80031 from Intersil, which is stable in voltage until roughly 60 K (although with a larger variation compared to TPS7A7002), consuming less than 4 mW. While these regulators introduce more noise, this is in general not a severe complication for FPGA based systems that are digital in nature.

Extensive characterization results of the various voltage regulators are reported in the supplementary material.

In this study, no regulators were found to operate reliably below 60 K; however, when operating the FPGA system, it is preferable to operate the regulators at 4 K to be able to integrate them as close as possible to the FPGA. This can be achieved either in the form of a discrete regulator, built from components operating at cryogenic temperatures, or by an FPGA-based solution.

In Sec. III, we propose a technique for stabilizing the FPGA supply voltage from within the FPGA, (partially) eliminating the need for an external regulator.

III. INTERNAL REGULATOR ARCHITECTURE

A. Measurement setup

The problematic voltage drop is mainly caused by powering an FPGA over extremely long wires (compared to regulating the voltage on the PCB itself). The wire length is needed because the power has to be supplied from outside the cryogenic environment, as the power supplies do not work at these temperatures (shown in Sec. II). The measurement setup is schematically drawn in Fig. 4. As can be seen, there are roughly 2 m of wires from supply towards the cryogenic setup and roughly 1.5 m within the cryogenic setup. While different cable types have to be used, low ohmic wires do not represent a problem at room temperature but cause significant heat injection into the cryogenic environment. The main resistive path is therefore the cryogenic cable, which is estimated to be roughly 0.2 Ω for R_+ and 0.1 Ω for R_-. Besides the problems arising from these resistances, as will be discussed in Sec. III B, wire inductance and latency are also important. The latency over several meters of coaxial cable accounts for 10–15 ns of delay; combined with the finite power supply reaction time (limited supply bandwidth) and the long wires with a few hundred micro-Henri of inductance, the effect of the fluctuating voltage drop is significant for several milliseconds after each large current burst due to switching. Placing decoupling capacitors reduces this effect; however, the reduced performance of capacitors at cryogenic temperatures limits the inductance compensation.

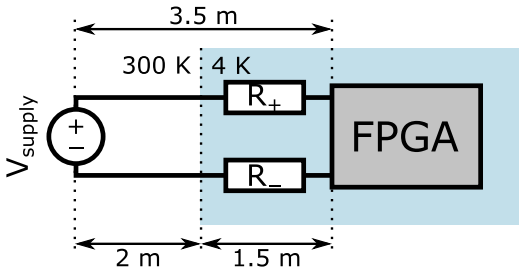

FIG. 4. Schematic drawing of the FPGA operating at cryogenic temperatures while supplying its power through long wires coming from room temperature.

B. Operating principle

To regulate the voltage from within the FPGA, the power consumed by the FPGA has to be made constant, so as to keep internal delays also constant. To achieve constant power consumption, an architecture was developed to monitor the FPGA's internal delays and act upon detected variations.

The operation and its results are simulated in Fig. 5; the room temperature power supply was set to 1.1 V, to arrive at the nominal FPGA supply voltage of 1 V in the cryogenic environment. In Fig. 5(a), the operation without regulation is shown. In this example, the system is triggered at a certain time to start with an operation. At that time, the power consumption is suddenly increased, in this example from 0.25 to 0.4 W. The resulting voltage on the FPGA drops by 5%, when assuming a resistive drop in the cable of 0.3 Ω from 1.02 to 0.97 V. As a result, the propagation delay of the carry chain is increased by approximately 12% or 3.3 ps when operating at 300 K. At 4 K, this effect is severely worsened; the delay increases by roughly 20% or 4 ps. This change is significantly more than the 4% drop in voltage due to their semi-exponential relationship as shown

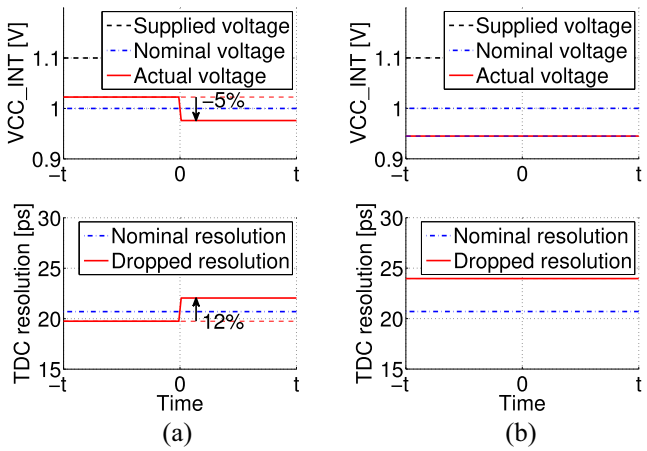

FIG. 5. Simulated impact of the power stabilizer on the FPGA voltage and the resulting delay of the carry elements, i.e., the resolution of the TDC derived from Fig. 6. The resistive loss in the cables is approximately 0.3 Ω, while the power dissipated by the system is 0.25, 0.4, and 0.5 W (Fig. 8), respectively, in steady-state, after the trigger and with the stabilizer active. The voltage at the room temperature supply is set to 1.1 V, while the voltage on the FPGA is nominal 1 V.

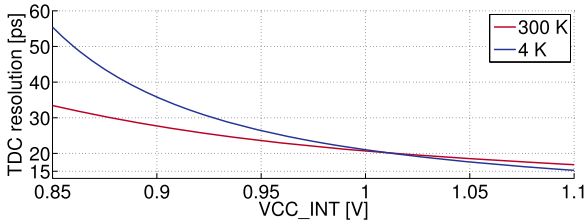

FIG. 6. TDC resolution or carry delay versus the internal FPGA supply voltage (VCC_INT) at both 300 K and 4 K.

in Fig. 6. The resolution of a time-to-digital converter (TDC), implemented in the carry chain of the FPGA, is shown as a function of the supply voltage. The TDC resolution equates to the delay of a single carry element and approximates to 21 ps at the nominal supply voltage of 1 V. At cryogenic temperatures, the delay is increased at lower supply voltages due to the increase in the transistor threshold voltage, thus resulting in a stronger influence of the supply voltage on the carry delay.

With the regulation turned on, this effect is effectively smoothed, as shown in Fig. 5(b). The power consumption before the system is triggered is slightly higher than that in the non-regulated system, around 0.5 W; after the trigger, the power consumption remains stable. While this technique can achieve a more stable system, the main drawback is the increased power consumption. This is especially important for designs operating at cryogenic temperatures, for which the power budgets are limited.

These problems can be partially addressed with a supply capable of forcing and sensing the voltage through different terminals. In this way, the voltage is measured closer to the FPGA through high-ohmic contacts and the supply can therefore adjust its internal voltage to compensate for the voltage drop in the cables. In practice, this technique is limited to the bandwidth of the feedback and the supplies' capability of acting quickly and accurately enough, especially with a system switching current frequently and at a high rate.

C. Implementation

To achieve the stabilization of the supply voltage, a small oscillator farm is employed together with a regulator consisting of a time-to-digital converter, an input-output (IO) delay block, and some control logic. The complete circuit is shown in Fig. 7(a).

The internal clock signal, provided by a mixed-mode clock manager (MMCM), is used as a stable reference. It is routed through an IO delay block and a carry chain towards a small TDC. This TDC constantly measures the timing of the clock edge. At system start-up, the IO delay is used to shift the clock edge to the middle of the TDC range. As a result, the output of the TDC should be constantly indicating half of its range, as the position of the clock edge.

However, as a result of voltage drop and consequent shifts in logic delay, this is not the case. As the resistive voltage drop increases, the delay of the elements increases and the propagation of the clock will slow down; hence a higher TDC output is expected. On the other hand, with lower power consumption, and thus lower voltage drop, the internal logic will be faster and the edge will shift to lower TDC values. As the TDC is one of the most precise elements in the FPGA, the changes can be significant even with slight variations in the power consumption, as discussed in Sec. III B.

To correct for the changes in power consumption, oscillators in the farm are turned on or off depending on the direction of the shift. With a lower measured TDC output, some oscillators are turned on. A higher TDC output will lead to a decrease in the amount of enabled oscillators.

The TDC is operated with a 400 MHz clock, while decisions are made at a rate of 6.25 MHz, i.e., every 160 ns. The decision maker and the oscillator farms are detailed in Fig. 7(b). First, the decision maker filters out noise and jitter from the TDC by averaging multiple measurements, 64 in total for a decision rate of 6.25 MHz. Four results are summed to cross from the 400 MHz to the 100 MHz clock domain. The remaining 16 results are processed using an infinite impulse response (IIR) filter. The result of the averaged measurements is then taken as a measure for the required

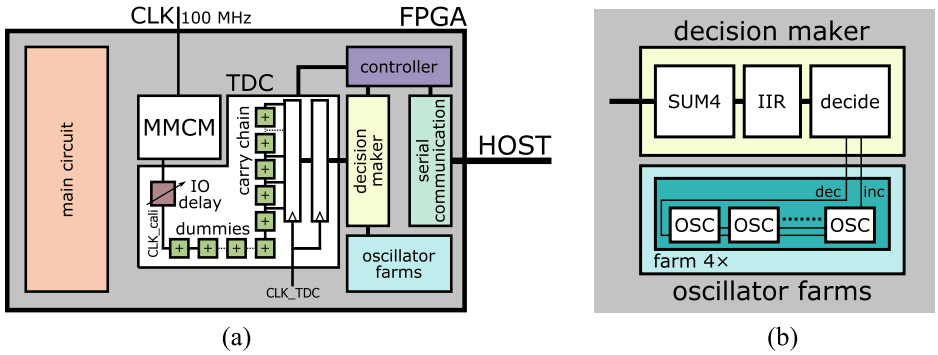

FIG. 7. FPGA internal stabilizer architecture. (a) The oscillator stabilizer control system is divided into the following parts: a TDC with IO delay and a dummy carry chain in order to calibrate the clock delay into the delay line and to generate extra impact of voltage change on the TDC outcome. The outcome is routed towards a decision maker which detects if the voltage is increased or decreased. Control signals are finally sent to the oscillator farms. (b) Details of decision maker and farm. The decision maker first integrates and filters the TDC data, leading to increment (inc) or decrement (dec) signals that are sent to four oscillator farms, each consisting of 128 oscillators.

increase or decrease in the number of enabled oscillators. An averaged value higher than half of the TDC range will flag the decrement signal, and a value lower than half of the TDC range will force an increment. A value of exactly half the TDC range is ideal and no change to the number of running oscillators is performed.

The oscillators are implemented as rings of logic elements in which at least one inverting element is present to enable oscillation. A NAND is used in the ring as an enable element to turn the oscillators on and off as decided by the decision maker. Each oscillator consists of 6 logic elements, implemented in the look-up tables of the FPGA, 5 configured as buffers and one as a NAND gate for the first stage to implement both the inversion and the enable element.

The number of required oscillators greatly depends on the power consumed in the core circuitry. First, the minimum and maximum power consumption of the core circuitry has to be roughly known. Afterwards, the number of implemented oscillators should be capable of bridging the gap between minimum and maximum power consumption with some margin.

In our design, the core circuit is our analog-to-digital converter (ADC),[19] which dissipates 250 mW in the idle mode and about 400 mW at a maximum conversion rate. To bridge this gap, four farms were implemented, each containing 128 oscillators. Therefore, the total number of active oscillators out of the 512 oscillators can be incremented or decremented with four at a time, i.e., the same increment and decrement signals are routed to each oscillator farm.

IV. RESULTS

A. Voltage regulation

The implemented system consists of our 1.2 GSa/s analog-to-digital converter (ADC)[19] combined with the voltage regulation circuit as discussed in Sec. III. The system was tested at 300 K and 15 K as the performance at 4 K was deteriorated compared to 15 K by increased jitter in some components and the reduced decoupling capability. The ADC is triggered at time $t = 0$ to start converting the analog input and store these

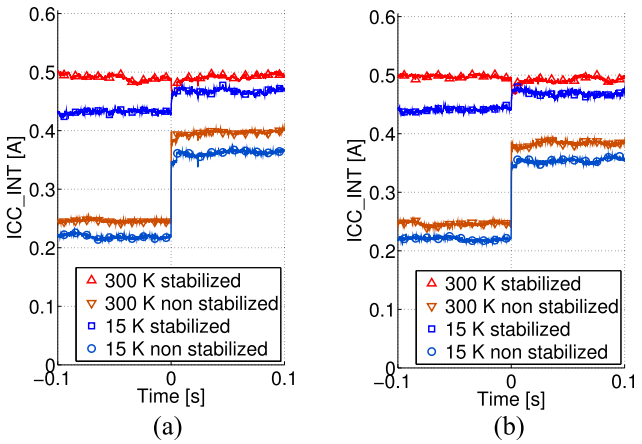

FIG. 8. Measured FPGA current with stabilizer turned on and off at 300 K and 15 K. At time $t = 0$, the ADC starts a measurement with an input sinusoid of (a) 2 MHz and (b) 40 MHz.

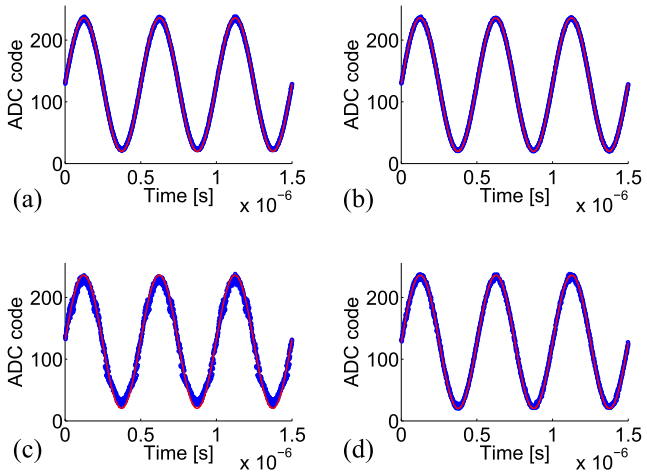

FIG. 9. Three periods of a 2 MHz sinusoid digitized at 1.2 GSa/s at 300 K and 15 K with the stabilized and non-stabilized systems. The input sine wave spans 90% of the ADC input range to prevent the system from clipping, etc. The solid line is a best fitted sinusoid for reference. (a) Non-stabilized at 300 K, (b) stabilized at 300 K, (c) non-stabilized at 15 K, and (d) stabilized at 15 K.

data in the internal FPGA memory. At time zero, the power consumption is significantly increased for the non-stabilized system, as shown in Fig. 8. In Fig. 8(a), the ADC starts converting a sinusoidal signal with a 2 MHz frequency, while in 8(b), the conversion is done with a 40 MHz input signal. Although the difference in power consumption between these two cases is small, about 2.5%, it will still affect the signal-to-noise ratio (SNR). The main problem for our ADC though is the difference between calibration and final conversion. While the calibration is done with signals in the low kHz frequency range, the difference in the power consumption is more significant. In principle, the final conversion system stability is not the same as the system stability at the time of the calibration,

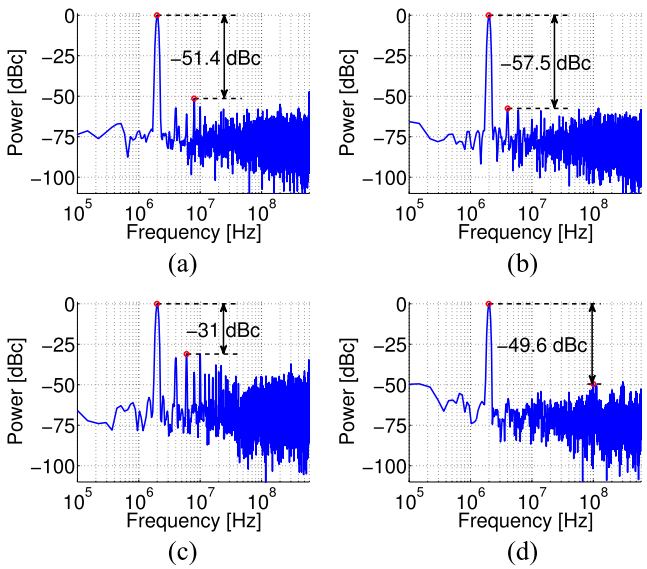

FIG. 10. Frequency domain representation of the sinusoids depicted in Fig. 9. Frequency spectra were obtained from 48 000 samples while using a Blackman-Harris window of length 2^{14} shifted over the samples. Furthermore, the spurious-free dynamic range (SFDR) is indicated. (a) Non-stabilized at 300 K, (b) stabilized at 300 K, (c) non-stabilized at 15 K, and (d) stabilized at 15 K.

TABLE II. Summary of the obtained ADC specifications while converting a 2 and 40 MHz sine at 1.2 GSa/s with the stabilizer turned on or off. The stabilizer improves the performance, especially at cryogenic temperatures, with up to 1.5 bit in terms of ENOB or roughly 9 dB SNDR.

Frequency (MHz)	2				40			
Temperature (K)	300		15		300		15	
Stabilizer	Off	On	Off	On	Off	On	Off	On
SNR (dB)	38.5	41.1	24.7	32.2	30.8	31.6	22.9	28.8
SNDR (dB)	36.8	38.9	21.3	30.3	28.6	29.3	19.4	26.5
SFDR (dBc)	−51.4	−57.5	−31.0	−49.6	−36.7	−37.5	−27.1	−35.7
ENOB (bits)	5.8	6.2	3.2	4.7	4.5	4.6	2.9	4.1

leading to significant differences in signal shapes that cannot be easily accounted for.

Therefore stabilizing the power consumption in all these cases can improve the final ADC conversion results. Our stabilization technique indeed stabilizes the current as shown in both figures; however, the current is not as flat at 15 K as it is at 300 K and a clear transient at $t = 0$ is still visible. This transient is mainly caused by inaccurate tuning of the initial settings for the oscillator farms at 15 K, which is somewhat harder due to the more significant impact on both carry delay (Fig. 6) and temperature compared to tuning at 300 K. Combined with increased jitter of especially the IO delay component, the decision logic is no longer capable of fully correcting the power difference.

B. Calibration and conversion

Although we can indeed see a significantly more stable current over time, the question remains whether that improves the performance of our ADC. To study the performance of the ADC, tests were done in the four operating conditions, with and without stabilization at 300 K and 15 K.

First, the ADC is calibrated at both temperatures. As the ADC is built-up from 12 individual sources, i.e., 6 TDC channels and all measuring rising and falling edges, the calibration is essential. The calibration is discussed in detail in Ref. 19 and can be summarized with the following four steps: tuning of the length of the 6 TDCs to match the clock period of 2.5 ns, aligning of the 6 TDCs with the clock edge, calibrating of the timestamp to the analog value, and finally synchronising of the phases of the 6 channels for proper sorting of the analog values.

Using those calibration sets, measurements were performed with an input sinusoidal signal of 2 and 40 MHz. The results for the 2 MHz conversion are shown in Fig. 9 after merging 12 sources and applying the calibration. The digitized sine waves can be seen to be quasi-spur-free when the stabilizer is used. However, especially at 15 K, the result is not as clean as at 300 K. This can be partially explained by the non-equalization of the current at 15 K, as shown before in Fig. 8, but is also caused by the decreased decoupling capabilities of our capacitor network and increased jitter in some of the FPGA components.[19]

To quantify the improvement in performance, the sine waves are converted to the frequency domain, as shown in Fig. 10. Clearly, the stabilizer brings significant reduction in signal distortion, especially at cryogenic temperatures. The harmonics of the 2 MHz input tone are reduced, increasing the spurious-free dynamic range (SFDR) by more than 18 dB at 15 K. Furthermore, the signal-to-noise ratio (SNR) and signal-to-noise and distortion ratio (SNDR) are enhanced by up to 9 dB at 15 K thanks to a reduction in especially high frequency noise when enabling the stabilizer. Stabilizing the supply voltage enables a better calibration effectively visible in a lower noise floor.

The main specifications of the ADC are listed in Table II for the use-cases described before. At 300 K, the stabilizer does not bring significant improvements. The effective number of bits (ENOB) is improved by 0.4 bit at low frequencies, but at higher frequencies, there is only a minor improvement of 0.1 bit (which is in the error-margin). At cryogenic temperatures, however, the improvement is more significant. For low frequencies, there is a 1.5 bit better ENOB and at high frequencies, the ENOB still improves with 1.2 bit. These results clearly show that the ADC operation at cryogenic temperatures is challenging, especially when not considering power fluctuations and the significant effect of voltage drop on the FPGA behaviour. Though, there are still many unknown effects of electronics, materials, and the corresponding behaviours while operating at temperatures so far out of the normal industrial temperature range, thus prompting more research in many aspects of cryogenic FPGA design.

V. CONCLUSION

We have demonstrated an approach to circumvent the ineffectiveness of voltage regulators at deep-cryogenic temperatures by regulating the FPGA power consumption internally. This has been done by constantly measuring the carry cell delay and acting upon change by decreasing or increasing the amount of running oscillators in a small oscillator farm.

The stabilization of power consumption has been demonstrated and has been quantified by showing significant improvement of the performance of our FPGA ADC system. The ENOB of the ADC was at most 1.5 bits higher while using the stabilizer.

Besides the implementation of the FPGA power regulation, a study was conducted on the behaviour of various components needed in the power distribution network at cryogenic temperatures. The best behaving capacitors are those based on low dielectric constant materials, such as NP0/COG,

while those with high dielectric constants tend to drop over 90% in capacitance and increase the ESR with over 3000%. Commercial voltage regulators were not found to be working at 4 K but cease operation around 90 K.

This study shows the complexity of operating at cryogenic temperatures, especially in terms of power supply over long wires, the unavailability of cryogenic regulators, and the degraded performance of the decoupling network. Despite these complications, performance of the FPGA system can be significantly improved while regulating its supply voltage from within itself.

SUPPLEMENTARY MATERIAL

See supplementary material for the complete characterization results of the passive components, both capacitors and resistors, and the voltage regulators.

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