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Design techniques for low-voltage analog integrated circuits

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In this paper, a review and analysis of different design techniques for (ultra) low-voltage integrated circuits (IC) are performed. This analysis shows that the most suitable design methods for low-voltage analog IC design in a standard CMOS process include techniques using bulk-driven MOS transistors, dynamic threshold MOS transistors and MOS transistors operating in weak or moderate inversion regions. The main advantage of such techniques is that there is no need for any modification of standard CMOS structure or process. Basic circuit building blocks like differential amplifiers or current mirrors designed using these approaches are able to operate with the power supply voltage of 600 mV (or even lower), which is the key feature towards integrated systems for modern portable applications.

K e y w o r d s: bulk-driven, dynamic-threshold, inversion region, low-voltage, analog integrated circuits

1 Introduction

In the last decades, an increased demand for wireless devices led towards a growing need for the development of new design techniques for low-voltage (LV) analog integrated circuits (IC) in standard CMOS technology. These techniques meet today's requirements related to a decreasing voltage supply and higher IC performance. LV design is a rather difficult challenge for the designer taking into account today's customer requirements and parameter fluctuation of submicron and nanometer CMOS technologies.

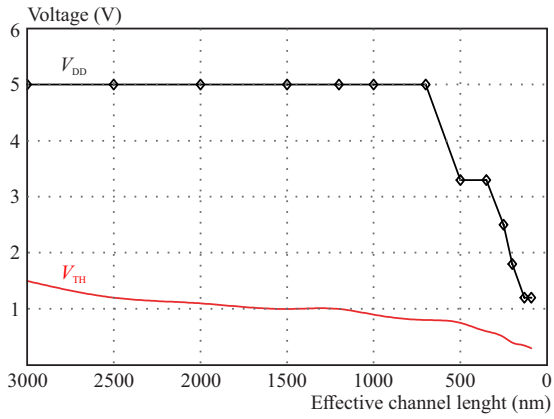

Fig. 1. V_{DD} and V_{TH} versus the transistor channel length downscaling [1]

Reducing the transistor channel length into sub-micron size and continuous shrinking of the gate-oxide thickness down to a few nanometers causes low breakdown voltages of MOS transistors. The decrease of the transistor threshold voltage (V_{TH}) over the years is less significant in comparison to the decrease of the power supply voltage V_{DD} (Fig. 1), which leads to a lower voltage swing and worse on/off characteristics. Better performance can be achieved using BiCMOS technology but at higher manufacturing expenses. However, sophisticated design techniques for CMOS technology were developed over the time to compete with BiCMOS circuits in performance.

The minimum power supply voltage of CMOS analog ICs designed without dedicated low-voltage (LV) techniques is limited by a value given by the sum of the turning-on voltage V_{GS} of MOS transistor and required voltage swing. The V_{GS} voltage of 300 mV is quite typical for a standard V_{TH} of NMOS device (in 130 nm CMOS process) to open and achieve the strong inversion region or saturation region. Subsequently, there is a problem while using low supply voltages ($V_{DD} \approx 600$ mV) and structures stacked into a cascode, because of insufficient or no voltage headroom left [2].

2 Overview of low-voltage design techniques

There are several techniques suitable for low-voltage (and low-power) analog IC design. The most used ones include: (i) Floating-gate MOS, transistors, (ii) Self-cascode topologies, (iii) Level shifters, (iv) MOS transistor operating in sub-threshold region, (v) Bulk-driven MOS transistor, (vi) Dynamic-threshold MOS transistor.

2.1 Floating-gate MOS transistor

The floating-gate MOS (FGMOS) transistor [3] is shown in Fig. 2. Its floating gate is an equivalent to the gate of a standard MOS transistor. The difference is in the way of channel driving. The floating-gate voltage V_{FG} is not driven directly but by the control gates through capacitance coupling. The floating-gate voltage can be expressed by (1), where Q_{FG} is the floating-gate static charge, C_{Σ} is the total capacitance with respect to

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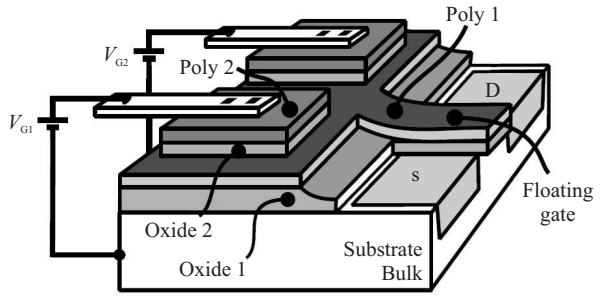

Fig. 2. Structure of FGMOS transistor

the floating-gate, $C_{FG,D}$, $C_{FG,S}$ and $C_{FG,B}$ are capacitances between the floating-gate and individual terminals of the FGMOS transistor, and C_{Gi} is the capacitance between the i-th control gate and the floating-gate.

$$V_{FG} = \frac{Q_{FG} + C_{FG,D}V_D + C_{FG,S}V_S + C_{FG,B}V_B + \sum_{i=i}^{n} C_{Gi}V_{Gi}}{C_\Sigma}. \quad (1)$$

The dependence of the drain current I_D on the input voltage V_{FGS} of a FGMOS transistor is similar to the transfer characteristic of a conventional MOS transistor. FGMOS symbol with parasitic capacities is depicted in Fig. 3.

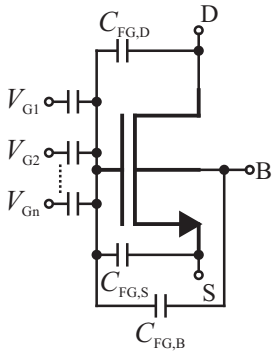

Fig. 3. Parasitic capacities of FGMOS transistor

An interesting property of FGMOS transistor is its electrical insulation between the floating gate and other nodes, which is nearly ideal. Therefore, at room temperature, the floating gate static charge can for several years remain with variation lower than 2 % from the original value. The equivalent threshold voltage of the FGMOS transistor can be reduced by controlling the floating gate static charge Q_{FG} that can be changed by several ways:

- Ultraviolet radiation
- Injection of hot electrons
- Fowler-Nordheim tunneling

2.2 Self-cascode topologies

The self-cascode configuration with MOS transistors (Fig. 4) offers a higher output impedance along with an increased voltage swing in comparison with a standard cascode topology. The lower (upper) transistor M1 (M2) operates out of saturation (in saturation). For $(W/L)_2 \gg (W/L)_1$, such a circuit behaves like a single MOS transistor operating in the saturation region, but with a significantly lower influence of the channel length modulation λ. The output resistance r_{out} of this topology is approximately proportional to $(W/L)_2/(W/L)_1$ ratio, and the saturation voltage $V_{DS(sat)} = V_{GS} - V_{TH}$ is roughly comparable with the conventional MOS transistor. The basic principle of this technique is in different threshold voltages $(V_{TH2} \neq V_{TH1})$, which is not feasible in the standard low-cost CMOS process [4].

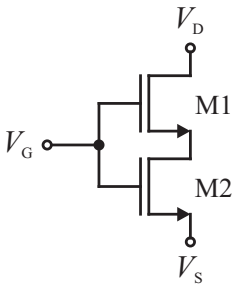

Fig. 4. The self-cascode topology

2.3 Voltage level shifters

Dynamic voltage level shifters represent a potential solution for low-voltage input transistors of a differential pair. This technique uses resistors for shifting the input common-mode voltage to the operation region of the input MOS transistors. Thus, the input transistor pair, modified in such a way, keeps sufficient transconductance g_m in comparison with other low-voltage design techniques. However, the main drawback of lever shifters is their high input impedance and high area consumption, which is unacceptable in modern CMOS ICs and their applications [5].

2.4 MOS transistor operating in subthreshold region

MOS transistor operating region is one of the most important aspects for IC design. The optimum IC design is characteristic by the minimal power consumption, minimal area and sufficient frequency response with fulfilled circuit specifications. MOS transistor operating in strong inversion has a good frequency response and a small area but at the cost of a high power consumption with high saturation voltage $V_{DS(sat)}$, which are not acceptable in many applications. Therefore, it is often necessary to use less-conventional MOS transistor operating regions. A widely used design technique which employs MOS transistors operating in the sub-threshold region is described in details in Section 3 [6].

Table 1. Comparison of main parameters

	GBW	Supply voltage	Power consumption	Technology
FGMOS	Medium	$< V_{TN} + \lvert V_{TP}\rvert$	High	2x polysilicon
Self-cascode	Medium	$< V_{TN} + \lvert V_{TP}\rvert$	Medium	Multiple threshold
Level-shifter	High	$< V_{TN} + \lvert V_{TP}\rvert$	Medium	Standard
Sub-threshold reg.	Low	$< V_{TN} + \lvert V_{TP}\rvert$	Low	Standard
Bulk-driven	Low	$< V_{TN} + \lvert V_{TP}\rvert$	Low	Std. (triple-well)
Dynamic-threshold	Medium	$< V_{TN} + \lvert V_{TP}\rvert$	Low	Std. (triple-well)

2.5 Bulk-driven MOS transistor

Bulk-driven (BD) concept appears as a promising technique to achieve a better performance in low-voltage conditions along with low-power ICs. The main advantages of this technique is the compatibility with the standard CMOS process, hence there is no need to change the structure of the conventional MOS transistor. At the same time, the need to overcome the input voltage $V_{GS} > V_{TH}$ of MOS transistor is suppressed and the voltage headroom is increased. BD MOS transistor uses the bulk electrode as a signal input while the gate is biased with V_{BIAS} voltage. BD technique is described deeply in Section 4 [7].

2.6 Dynamic-threshold MOS transistor

The dynamic-threshold (DT) design technique is derived from BD technique. This technique uses the bulk tight together with the gate as a signal input, so that the voltage between the gate and substrate is changed simultaneously with the input signal swing and hence, the threshold voltage is changed dynamically. The advantage of this technique is a higher overall transconductance, which consists of the gate transconductance g_m and body transconductance g_{mb}. DT technique is described in more detail in Section 5 [8].

2.7 Summary of low-voltage design

Each of the low-voltage design techniques described below has certain performance limitations such as gain bandwidth (GBW) degradation, increased input noise, increased input impedance or decreased overall transconductance. Main characteristics of the analyzed design techniques are summarized and compared in Table 1 [9].

Based on the feasibility of these IC design techniques in different technologies, it is advantageous to use techniques employing MOS transistors operating in the sub-threshold region, BD MOS transistors and DT MOS transistors because there is no need for modification of a standard CMOS process and, additionally, low power consumption of the designed circuits can be achieved.

3 MOS transistors operating in sub-threshold region

A conventional MOS transistor model using different equations for the weak and strong inversion regions is often used for computer circuit simulations. Sometimes, more complex equations for bridging (using a transitive region) between these two regions are used, but still very often it is impossible to avoid significant inaccuracies and discontinuities. Moreover, it is very difficult for IC designers to assume the circuit power consumption by simple handmade calculations. Therefore, most of them choose the strong inversion region at the cost of unnecessarily high speed and power consumption. In the past, low power consumption was not considered crucial in IC specifications. This has been drastically changed in mobile applications of ICs [10].

The inversion region of the MOS transistor operation is defined by the so-called inversion coefficient i_c expressed by

$$i_c = \frac{I_D}{I_0(W/L)} = \frac{I_D}{2\mu C_{ox} U_T^2 (W/L)}\,, \tag{2}$$

where I_0 is the technological current that is technology-related, μ is the charge-carrier mobility, C_{ox} is the capacitance of the gate oxide, W is the channel width, L is the channel length and U_T is the thermal voltage.

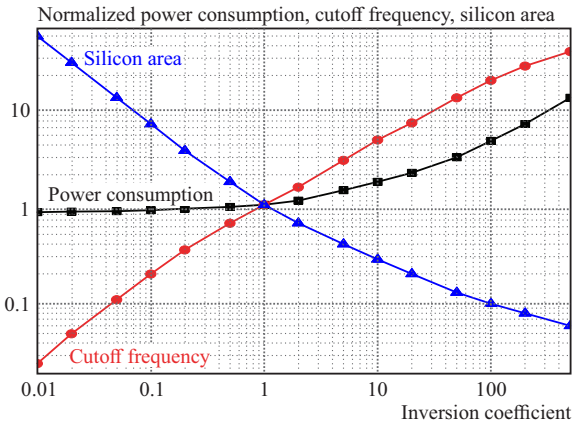

Fig. 5. Normalized power consumption, cut-off frequency and area *vs* the inversion coefficient [2]

If the technological current equals to the transistor drain current, MOS transistor operates exactly in the middle of the moderate inversion (MI) region. MOS transistor operates in weak inversion (WI) for $i_c < 0.1$. Strong inversion (SI) is for $i_c > 10$. Everything in between belongs to MI with center in $i_c = 1$ (in logarithmic scale) as seen in Fig. 5 showing the relationship between the normalized speed, power consumption and silicon area occupation.

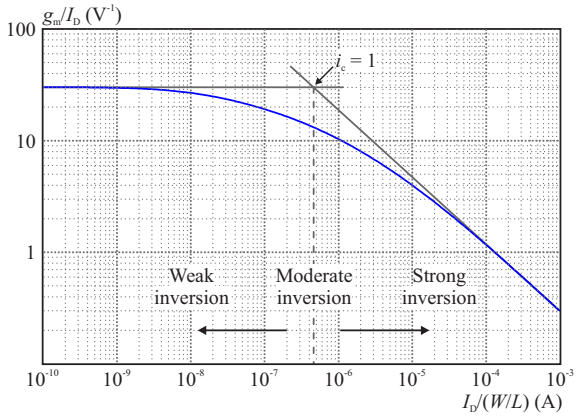

Fig. 6. Parameter g_m/I_D versus the normalized drain current

Strong inversion region is typical for the input voltage greater by about 100 mV than the threshold voltage V_{TH}. MOS transistor operating in this inversion region creates a significant depletion layer beneath the gate electrode with the drift current as a dominant component of the overall current. The total drain current can be described by quadratic dependence on the input voltage V_{GS} by

$$I_D(SI) = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}), \qquad (3)$$

where λ is the channel-length modulation coefficient and V_{DS} is the drain-source voltage [11].

Weak inversion region is typical for input voltages lower than the threshold voltage. The number of charge carriers is small and, therefore, a very weak inversion layer beneath the gate is created. In weak inversion, the diffusion current is a dominant component of the overall current floating through MOS transistor with exponential dependence on voltage V_{GS}. This dependence is

$$I_D(WI) = 2\mu C_{ox}\frac{W}{L}U_T^2 \exp\frac{V_{GS} - V_{T0}}{U_T}, \qquad (4)$$

where V_{T0} is the threshold voltage when bulk-source voltage $V_{BS} = 0$ V.

Moderate inversion region is a good trade-off between the speed, power consumption and silicon area for most of the analog circuits. This issue was for the first-time introduced by Koomen [12] 40 years ago and later Vittoz and Fellrah [13] continued in Koomen's work. This field of research was explored in detail in many publications over the years [14–16]. If the input voltage is approximately comparable with the threshold voltage, none of the mentioned current components is dominant and the overall current is a sum of both components. In this case, the dependence between the drain current and the input voltage is not cleanly exponential or quadratic and it is difficult to describe this relationship analytically (equation 5). As already mentioned, most of the designers therefore chose SI option at the cost of unnecessarily high power consumption and speed. Moreover, it is very difficult to expect the power consumption of a circuit by simple manual calculations

$$I_D(MI) = 1\mu C_{ox}\frac{W}{L}U_T^2\left[\ln\left(1 + \exp\frac{V_{GS} - V_{TH}}{2U_T}\right)\right]^2. \qquad (5)$$

Extreme cases of strong or weak inversion regions do not provide a good compromise between the frequency response, power and area consumption. Therefore, it is necessary to consider a one-equation MOS transistor model for all regions which would be helpful for an optimized IC design considering the speed, power and area consumption.

Parameter g_m/I_D expresses the transconductance efficiency of MOS transistor and describes how effectively the current (power) is transformed to the MOS transistor transconductance. It means that for higher values of g_m/I_D it is possible to achieve higher g_m at a constant drain current I_D. In analog ICs designed in standard CMOS technology the MOS transistor reaches the highest value of g_m/I_D when operating in the weak inversion region. The advantage of this approach is that it defines easy MOS transistor sizing rules for IC design that can be used for any inversion region thanks to the one-equation transistor model. The dependence between g_m/I_D parameter and the normalized drain current is depicted in Fig. 6 [17].

The g_m/I_D design methodology presents a good compromise between transconductance g_m and the value of MOS transistor saturation voltage $V_{DS(sat)}$. Moreover, it significantly simplifies calculations of MOS transistor dimensions, which is the common routine during IC design phase. Moreover, it is possible to achieve the minimum power consumption thanks to the low operating currents but at a cost of a lower speed and larger silicon area. The g_m/I_D methodology describes the moderate inversion region with high accuracy, which is the best compromise for most of the analog ICs from the point of view of power consumption, speed and area. As is shown in Fig. 7, g_m/I_D parameter also represents the inversion coefficient ic for different slope factors n.

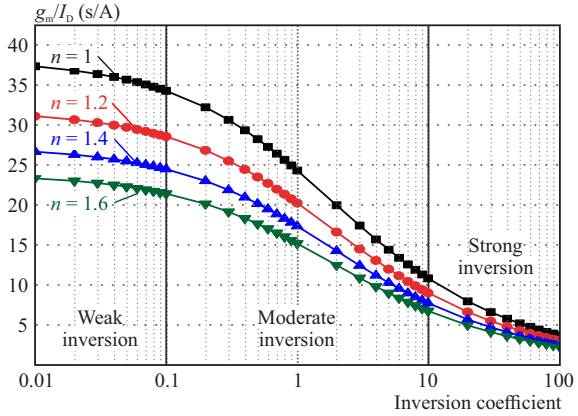

Fig. 7. Dependence of g_m/I_D parameter on the inversion coefficient

This characteristic became fundamental for analog IC design in submicron and nanometer technologies. Parameter g_m/I_D suggests the operation region of a MOS transistor and, more importantly, g_m/I_D does not change across different technologies. There are several equations describing the relationship between g_m/I_D and i_c. These equations differ in interpolation accuracy of the transition region between individual inversion regions. The simplest expression of g_m/I_D is given by [18]

$$\frac{g_m}{I_D} = \frac{1}{nU_T} \frac{1}{0.5 + \sqrt{0.25 + i_c}}. \tag{6}$$

The g_m/I_D design approach requires new MOS transistor models which have to be accurate in both weak and moderate inversion regions. Accurate transistor modeling does not mean only correct I–V characteristics but also correct current derivatives (transconductances), which are one of the most important parameters for analog IC design. Such models have to be continuous within all inversion regions. Therefore, MOS transistor models developed decades ago (*eg* BSIM) are nowadays replaced by their fourth generation. Fortunately, evolving EKV models use the described g_m/I_D method for calculations. Moreover, EKV models have the smallest number of root parameters in comparison with other models from the same generation, which significantly increases the speed of simulations.

4 Bulk-driven MOS transistors

Bulk-driven (BD) MOS transistors were first mentioned by A. Guzinsky in 1978 as active components in OTA in the form of input differential pairs [19]. The original purpose of BD transistor was in delivering small transconductance g_m to improve linearity of the amplifier.

Drain current I_D of a conventionally connected MOS transistor is usually controlled by the gate-source voltage V_{GS}. This current can be also modulated by the bulk-source voltage V_{BS}, which is usually considered as a parasitic effect and may introduce unwanted body transconductance g_{mb}. If a constant voltage V_{GS} is kept as a bias voltage and an input signal is applied to the bulk electrode, then a JFET-like transistor can be obtained. Schematic of BD transistor is shown in Fig. 8 [20].

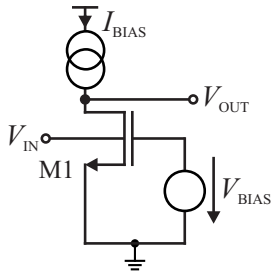

Fig. 8. Schematic of bulk-driven MOS transistor

The principle of this technique is in the MOS transistor structure itself which consists of four electrodes – gate, drain, source and bulk. As mentioned above, the BD technique uses the bulk as a signal input, which results in a significantly reduced need to overcome the threshold voltage at the MOS transistor input. Advantages of the BD design technique include:

- BD transistor depletion characteristics significantly reduce the need to overcome the threshold voltage V_{TH} at the transistor input and increase the voltage headroom for low-voltage applications,
- possibility to operate with low-voltage power supply,
- use in a standard CMOS technology.

Unfortunately, BD technique has also the following disadvantages:

- body transconductance g_{mb} of BD transistor is 3–4 times lower than the gate transconductance g_m, which can lead to a lower gain band-width (GBW) and worse frequency response,
- the input capacitance of BD transistor is increased to the value of $C_{B,sub}$+C_{BS} in comparison with the input capacitance of a conventional MOS transistor that is given by $C_{GS} + C_{BG}$,
- the input noise of BD transistor is increased,
- BD transistors are prone to turn-on parasitic bipolar transistors in the substrate, which can lead to an unwanted latch-up effect.

4.1 Body transconductance

The body transconductance g_{mb} is a small-signal parameter of MOS transistor which describes the dependence of the drain current I_D on the body-source voltage V_{BS}. Body transconductance is the secondary effect of MOS transistor, and is given by a partial derivative of the drain current with respect to V_{BS} with constant values of V_{GS} and V_{DS}, where ϕ_F is the Fermi potential and γ is a substrate coefficient

$$g_{mb} = \frac{\partial i_d}{\partial v_{BS}} = \frac{\partial i_D}{\partial V_{TH}} \frac{\partial V_{TH}}{\partial V_{BS}} = -g_m \frac{\partial V_{TH}}{\partial v_{BS}} = \frac{\gamma g_m}{2\sqrt{-2\phi_F - V_{BS}}}. \tag{7}$$

Body transconductance is the gain factor of the voltage-controlled current source $g_m v_{bs}$ in the MOS transistor equivalent circuit (Fig. 9.), which is situated between the drain and source electrodes.

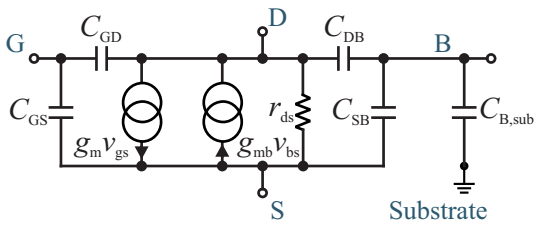

Fig. 9. MOS transistor equivalent circuit

An increase of the voltage V_{BS} leads to a decrease of the threshold voltage V_{TH}, which is caused by the body effect. As a result, the voltage swing $V_{OV(\max)} = V_{GS} - V_{TH}$ along with the drain current I_D are increased. The body transconductance is often indicated by the ratio η (equation 8) which typically ranges from 0.2 to 0.4. It means that the body transconductance is approximately from 2.5 to 5 times lower than the gate transconductance. Below, C_{dep} stands for the capacitance of the depletion layer beneath the gate

$$\eta = \frac{g_{mb}}{g_m} = \frac{\gamma}{2\sqrt{-2\phi_F - V_{BS}}} = n - 1 = \frac{C_{dep}}{C_{ox}}. \qquad (8)$$

Considering the fact that the body transconductance of BD MOS transistor is lower than the gate transconductance of a conventional MOS transistor, the maximum transit frequency $f_{t(BD)}$ of the BD transistor is significantly lower than the maximum transit frequency $f_{t(GD)}$ of a gate-driven equivalent

$$f_{t(BD)} = \frac{g_{mb}}{2\pi(C_{SB} + C_{DB} + C_{B,sub})}, \qquad (9)$$

$$f_{t(GD)} = \frac{g_m}{2\pi C_{GS}}. \qquad (10)$$

4.2 Latch-up

The first MOSFET generation provided only n-channel transistors and ICs designed in this technology had rather high power consumption. Further development of CMOS technology was motivated mainly by low power consumption in a static state at the cost of more layout masks, technology steps and total costs. Another drawback which came to existence along with CMOS technology is a parasitic effect called latch-up [11, 21].

The parasitic bipolar *pnp* (*npn*) transistor is created in n-well (p-well) of PMOS (NMOS) transistor with its collector connected to the bulk of NMOS (PMOS) transistor. Their mutual interconnection is shown in Fig. 10 and together they create a positive feed-back loop. If a parasitic current is injected into node X, voltage V_X at this node is increased and *npn* transistor starts opening. This results into an increase of the collector current $IC_{(npn)}$ and decrease of the voltage V_Y at node Y. Lowering the voltage V_Y causes opening of *pnp* transistor, which leads to a further increase of the collector current $I_{C(pnp)}$. If the gain of this loop is greater than one, this action continues until both parasitic transistors are fully open, which finally results into a current leakage from the supply voltage source to the ground.

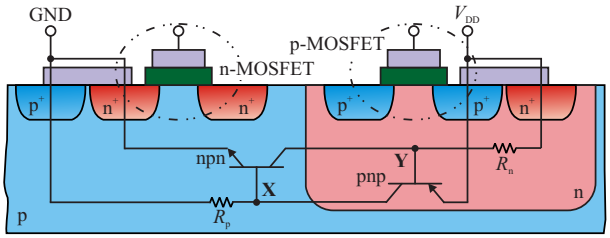

Fig. 10. Cross-section of a CMOS structure with parasitic devices

The initial parasitic current that might startup this effect can be caused by different sources in ICs. It can be, for example, coupling between the bases of the parasitic bipolar transistors and drains of CMOS structure. A high voltage swing can also excite a parasitic current into n-well or substrate, which can be the beginning of the latch-up effect. This problem can be avoided by several techniques. One of these techniques uses suitable doping profiles of individual layers and very strict follows the layout rules to minimize the substrate resistance R_p and well-resistance R_n. Another technique to minimize the latch-up risk uses a triple-well technology. In the triple-well process, p-well is insulated from p-substrate with a buried n-well, which ensures significantly reduced signal coupling. Cross-section of a CMOS structure in triple-well technology is depicted in Fig. 11.

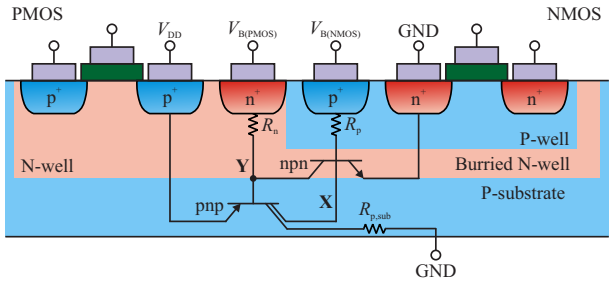

Fig. 11. Cross-section of CMOS structure in triple-well technology with parasitic lateral transistors

Another effective technique to reduce the risk of triggering the latch-up effect uses guard rings created from n-well and p-well structures between individual transistors along with triple-well technology (Fig. 12). Connecting n-wells to the highest potential and p-wells to the lowest potential of the circuit creates reverse-polarized diodes

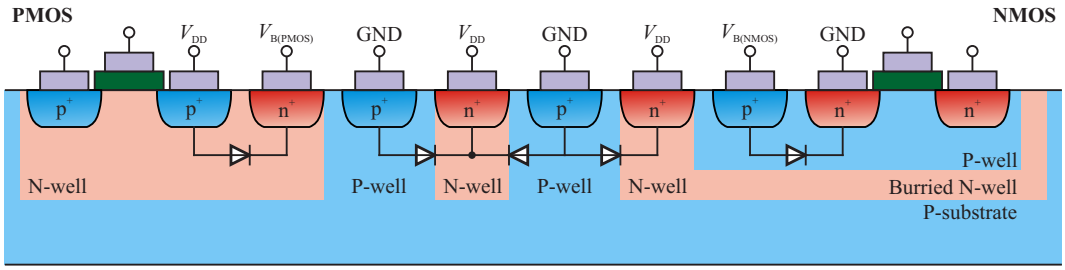

Fig. 12. Cross-section of CMOS structure with guard rings

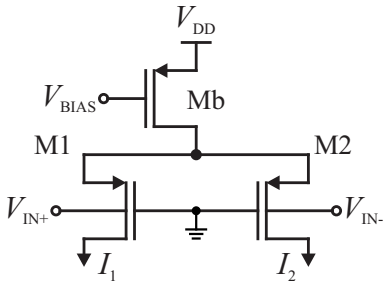

Fig. 13. BD differential pair

between NMOS and PMOS transistor, which effectively prevents latch-up.

BD transistors are prone to other type of unwanted effect. MOSFET driven through the well (bulk) increases the risk of turning on a parasitic diode between the source and bulk as seen in Fig. 12. In NMOS transistor, if the voltage difference between the bulk and source grows to a value greater than the built-in barrier potential of the PN junction, a leakage current starts flowing from the well to the ground. The same principle works for PMOS transistor. A prevention action for this kind of problem is the voltage supply limitation to the value lower than the barrier potential of the PN junction between these terminals. Unfortunately, still a subthreshold current will flow through this barrier.

4.3 Application of a bd technique on basic IC building blocks

The BD technique has been applied to design selected basic building blocks for analog ICs in order to analyze and evaluate the technique in low-voltage applications. The following circuits were designed and analyzed:

BD differential pair amplifier – Fig. 13 shows one of the most frequently used topologies based on BD transistors – an input differential pair. The gates of transistors M1 and M2 are connected to a negative supply potential to ensure their right operation in saturation. The input voltage range V_{CM} of a conventional transistor pair is limited by high threshold voltages. This voltage range can be described by

$$V_{CM} = V_{DD} - V_{DS(sat),M_b} - V_{TH}\,. \qquad (11)$$

Input BD transistors are used to obtain the rail-to-rail input voltage range, which is important for achieving a sufficient voltage swing when 0.6 V supply voltage is used. In addition, BT technique appreciably improves the input common mode range (ICMR). Another advantage of using a bulk-driven differential pair over gate-driven differential pair is the linear transconductance with respect to the differential input. The drawback of the BD differential pair is that grounded gates of the input transistors do not catch any noise generated by the negative supply potential, which leads to a lower power supply rejection ratio (PSRR) values [22]. An example of using the BD differential pair was published in [23] as an input pair of variable gain amplifier (VGA).

BD current mirrors – Current Mirrors (CM) are one of the most frequently used IC building blocks. The current mirror is a two-port device that accepts current I_{REF} at the input branch and produces current I_{OUT} at the output branch according to equation $I_{\mathrm{OUT}} = kI_{\mathrm{REF}}$, where k is an amplifying coefficient. If we apply the BD technique to a simple current mirror, the circuit shown is Fig. 14 is obtained. Using the same principle, more difficult CM topologies can be designed [24].

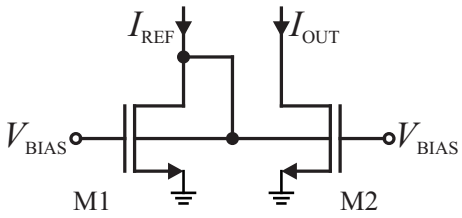

Fig. 14. Simple BD current mirror

The bulks of transistors M1 and M2 in both branches are tight together and the gates are connected to the bias voltage V_{BIAS}. The input current brought into the input branch creates voltage V_{BS} between the bulks and sources of both transistors. By this voltage, the threshold voltage V_{TH} can be modulated and decreased according to

$$V_{TH} = V_{T0} + \gamma\left(\sqrt{2|\phi_F| - V_{BS}} - \sqrt{2|\phi_F|}\right), \qquad (12)$$

where V_{T0} is the threshold voltage when $V_{BS} = 0$ V.

5 Dynamic-threshold MOS transistors

MOS transistors with the dynamic threshold voltage are derived from the BD technique with a simple difference in gate biasing conditions. DT transistor has the gate and bulk electrodes tight together and biasing is realized dynamically with the input signal swing, which leads to a dynamically reduced value of the threshold voltage V_{TH}. Thanks to the dynamic biasing conditions, a potential in the field of the conductive channel is controlled by both the gate and bulk at the same time, which results in a high overall transconductance $g_m + g_{mb}$ and faster current transfer. Schematic and small-signal equivalent circuit of DT MOS transistor is depicted in Figs. 15(a) and (b), respectively.

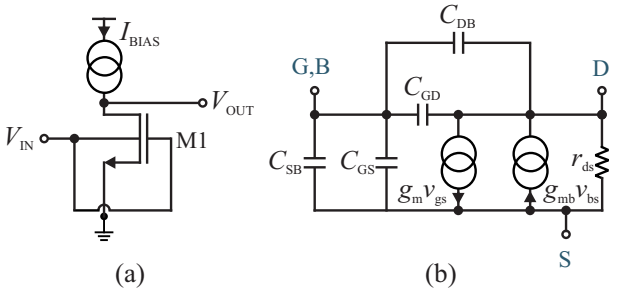

Fig. 15. DTMOS transistor : (a) – schematic, (b) – small-signal equivalent circuit

The threshold voltage V_{TH} and transconductances g_{mb} and g_m of DTMOS transistor are given by equations (12, 7 and 8), respectively. The main difference between DT and BD techniques is in the input capacitance and maximum transit frequency, which can be expressed by

$$f_{t(DT)} = \frac{g_m + g_{mb}}{2\pi(C_{GD} + C_{BD} + C_{GS} + C_{BS})}. \qquad (13)$$

By applying the DT technique to a simple current mirror, a DT simple current mirror can be obtained which is depicted in Fig. 16. As mentioned before, DT transistors in both branches have bulks and gates tight together and the voltage between the bulk/gate and source controls both of the transistors dynamically in the same way.

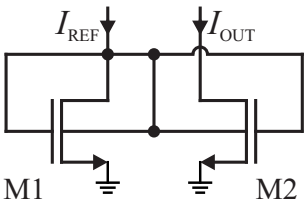

Fig. 16. DT simple current mirror

6 Experimental results

The most important characteristic for the design of low-voltage and low-power ICs using g_m/I_D approach is the dependence between the transconductance efficiency g_m/I_D and inversion coefficient i_c (Fig. 7). This characteristic is not technology-related, which predicts a wide usability over different CMOS technologies. Nevertheless, simulation analysis of this characteristic using the widely used BSIM transistor models shows an inaccuracy in weak inversion ($i_c < 0.1$) and moderate inversion ($0.1 < i_c < 10$) regions. Comparison of the characteristics acquired by analytical method (equation 6) and simulation shows almost a 20 % error in the weak inversion region for 90 nm CMOS process and more than 10 % error for 130 nm standard CMOS technology (Fig. 17). It is important to note that this inaccuracy of the simulation models is the most critical problem in the design and simulation of low-voltage ICs in nanometer technologies. This is the reason why new transistor models such as EKV models have been developed.

Selected analog building blocks were designed employing the respective low-voltage design technique. Then, the

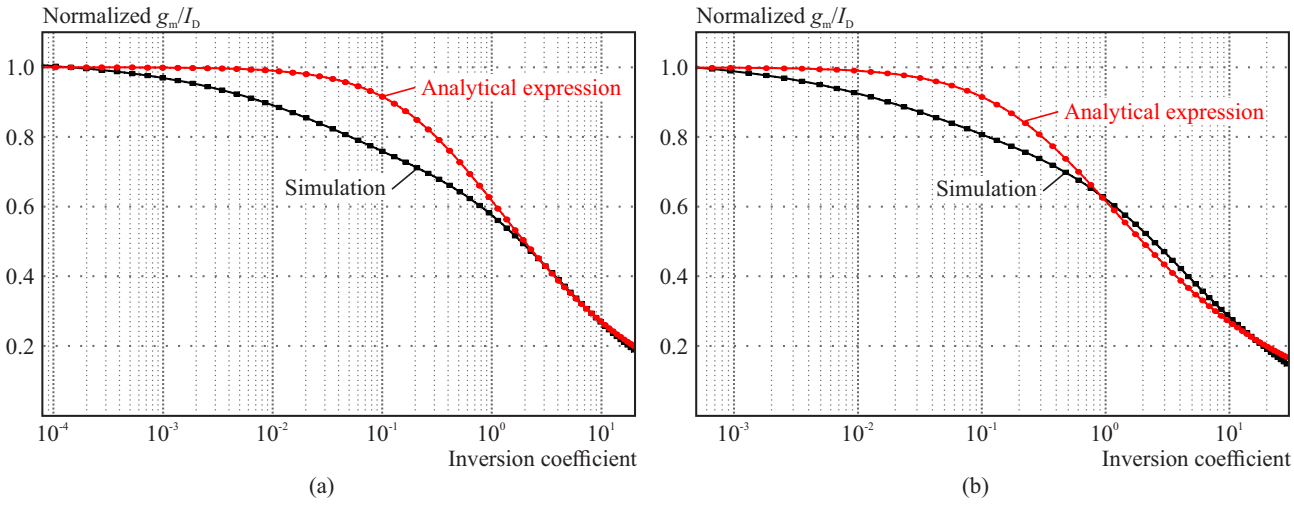

Fig. 17. Normalized g_m/I_D *vs* inversion coefficient for: (a) – 90 nm; (b) – 130 nm standard CMOS technology

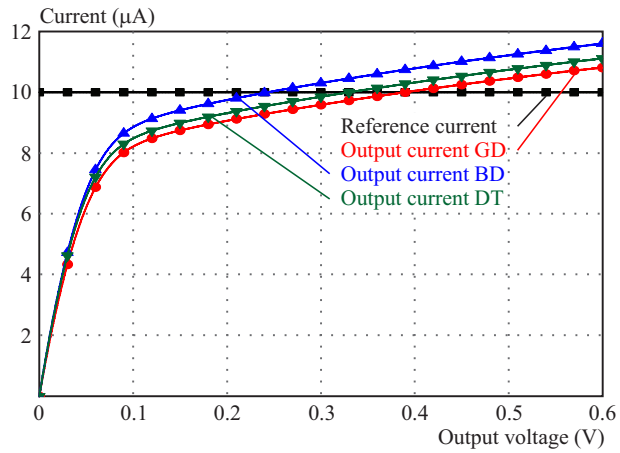

Fig. 18. Output characteristics of simple CMs

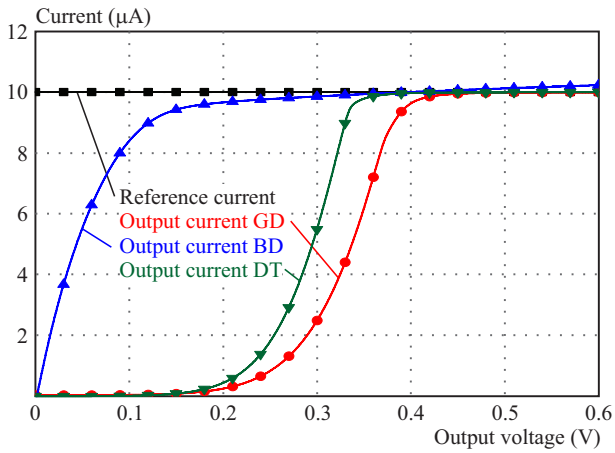

Fig. 19. Output characteristics of improved Wilson CMs

analysis of the main parameters was performed by simulation for 90 nm standard CMOS technology. Dimensions (channel width W and channel length L) of simulated transistors were following: $W = 5\,\mu$m and $L = 1\,\mu$m. The selected channel length represents a compromise between the low area consumption and sufficiently large output resistance.

The obtained results proved that the minimum output voltage $V_{\mathrm{MIN}} = V_{DS(sat)}$ of a simple current mirror does not depend on the threshold voltage V_{TH} or transconductance and thus the output characteristics and output resistance $r_{\mathrm{out}} = r_{ds}$ of both mirror topologies should be similar. It means that a simple CM designed by the conventional gate-driven (GD) approach is still suitable for the design of low-voltage ICs but its drawback is that it exhibits a rather low output resistance (hundreds of kΩ). Simulated output characteristics are shown in Fig. 18. Low output resistance can be observed in the slope of the output characteristics which has an increasing tendency.

An improved Wilson CM can enhance the output impedance by a negative serial feedback added to the circuit. Since the minimum output voltage of these CMs depends on the threshold voltage ($V_{\mathrm{MIN}} = V_{TH} + 2V_{DS(sat)}$), there will be differences in the output characteristics. The output resistance of the improved Wilson CM can be expressed as $r_{\mathrm{out}} = g_m r_{ds}^2$. From Fig. 19 one can observe that the DT technique reduces the V_{MIN} voltage from 400 mV to approximately 300 mV and, moreover, the BD design technique moves the V_{MIN} to 110 mV, which behavior is similar to a simple current mirror but with a much higher output resistance (in the order of MΩ).

The same analysis has been performed for the cascode current mirror (Fig. 20). We would like to underline that the low-voltage design approaches presented above can substantially improve the current mirror performance under low-voltage conditions, which has been also proven by the performed analysis. In Fig. 20, one can see that the minimum output voltage is significantly reduced using the BD technique to a value of about 140 mV.

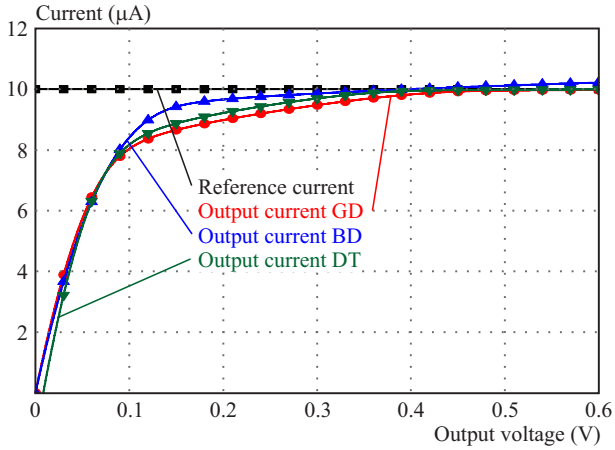

Fig. 20. Output characteristics of cascode CMs

More complex topologies of CMs were simulated too [25]. All results are summarized in Table 2 in section 7. Current mirrors designed in 130 nm technology have had a similar behavior [26] and the obtained results are summarized in Tab. 3.

7 Summary and discussion

Integrated circuits for resent portable applications and their different building blocks must meet specifications related to low supply voltage conditions. Conventional design methods are usually not able to fulfill these specifications and therefore it is necessary to developed new IC design techniques intended for the low-voltage issue. Analysis of circuit conditions while using standard CMOS technologies with voltage supply conditions below 1 V shows that the crucial limitation is insufficient or no voltage headroom is left for signal processing. A sufficient voltage swing can be achieved by reducing the need to overcome the MOS transistor threshold voltage or by operating in the subthreshold region. Selection of appropriate techniques took into account the following conditions:

- Possibility of using standard CMOS technology
- Capability of application into IC design

Table 2. Comparison of output parameters in 90 nm technology

CM Topology	GD		*multispan2BD*		DT	
	$r_{\text{out}}(\text{M}\Omega)$	$V_{\text{MIN}}(\text{mV})$	$r_{\text{out}}(\text{M}\Omega)$	$V_{\text{MIN}}(\text{mV})$	$r_{\text{out}}(\text{M}\Omega)$	$V_{\text{MIN}}(\text{mV})$
simple	0.29	78.6	0.21	76.8	0.21	73.2
Wilson	9.33	388.4	0.63	106.2	1.22	342.4
improved Wilson	1.65	375.8	0.79	141.6	2.87	337.8
cascode	4.36	477	0.81	139.8	0.81	361.2
regulated cascode	4.23	388.2	0.46	123	0.9	138.6
high compliance	0.44	120.6	0.35	107.4	0.44	115.2
Mulder	0.67	139.2	0.86	142.8	0.89	142.8

Table 3. Comparison of output parameters in 130 nm technology

CM Topology	GD		BD		DT	
	$r_{\text{out}}(\text{M}\Omega)$	$V_{\text{MIN}}(\text{mV})$	$r_{\text{out}}(\text{M}\Omega)$	$V_{\text{MIN}}(\text{mV})$	$r_{\text{out}}(\text{M}\Omega)$	$V_{\text{MIN}}(\text{mV})$
simple	0.96	118	0.97	114	0.97	114
improved Wilson	14.2	286	1.74	131	7.67	261
cascode	35.6	372	1.75	131	9.25	132

- Capability of increase voltage swing or operating in subthreshold region

Simulations of the designed current mirrors prove that the BD and DT design approaches can increase the signal swing by reducing the MOS transistor dependence on the threshold voltage. This can be the key towards modern low-voltage IC design, especially when cascode current mirror topologies are used (due to their simplicity and good characteristics). Output parameters of different CM topologies that were obtained from simulations are summarized in Table 2 (90 nm technology) and Table 3 (130 nm technology).

8 Conclusion

Considering low-voltage and low-power operation conditions for todays' integrated circuits, three promising low-voltage design techniques were selected for a more detailed analysis and evaluation. The technique using MOS transistors operating in the subthreshold region is a modern approach to IC design. This technique provides the power consumption minimization and, moreover, it is a basis for widely used EKV transistor models that is useful for simulations of MOS transistors operating in the weak and moderate inversion regions. Other two techniques use the advantages of bulk-driven MOS transistors and derived dynamic-threshold MOS transistors that often operate in the subthreshold operating regions, too.

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