

Designing Power Efficient Fibonacci Generator Using Different FPGA Families

Abhay Saxena^{#1}, Puneet Chandra Verma^{*2}, Chandrashekhar^{#3}, Pragya Agarwal^{*4}, Apurva Omer^{#5}

^{1, 2, 3, 4, 5} Department of Computer Science DSVV Haridwar, India

¹abhaysaxena2009@gmail.com, ²cvermapuneet@gmail.com

³shekharrockin1988@gmail.com, ⁴pragyaagarwal30@gmail.com, ⁵apurva.omer@dsvv.ac.in

Abstract—In consideration to wireless communication Fibonacci number is used to generate WPA and WPA2 (Wi-Fi Protected Access) key. Here, in our work we have designed green Fibonacci Generator under different FPGA families. Families we taken into consideration is Automotive Artix7, Artix7 and Kintex7.

First we have calculated power consumption of our designed at 2Volt & 1GHz frequency and change the capacitance from 5 to 30pf and found there is tiny changes in Artix7 and kintex7 Family but got significant changes in Automotive Artix7 around 16.79%. Secondly we have calculated power consumption of our designed at 2Volt & 10 GHz frequency and change the capacitance from 5 to 30pf, and found 41.09%, 13.95% and 38.06% change respectively for Automotive Artix7, Artix7 and Kintex7 FPGA families. Third we have worked with 3V and 1 GHz and got tiny changes with Artix7 and Kintex7 and found error value with Automotive Artix7. Lastly we have worked with 3V and 10 GHz and changed the capacitance from 5 to 30pf, we got 4.7% and 30.10% significant reduction in power consumption for Artix7 and Kintex7 FPGA families but for Automotive Artix7 we again got error value.

Keyword - Artix7, kintex7, FPGA, Energy Efficient Design

I. Introduction

The Fibonacci numbers are the numbers in which every number is the sum of the preceding two numbers. This sequence is known as Fibonacci sequence. The first two numbers in the Fibonacci series are either 0 and 1, or 1 and 1, depending on the selected starting point of the series, and each succeeding number is the sum of the previous two numbers. Here we have designed our Fibonacci generator and test the power consumption in different FPGA families.

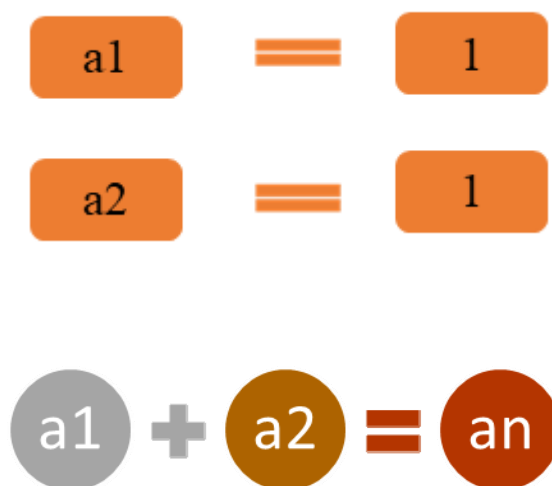


Fig:1 Idea of Fibonacci generator

In figure 1 we have shown that a_n is the next element of the series. That is, the current value is the sum of the previous two values. In figure 2 and figure 3 we have shown Top Level of Schematic of Fibonacci Generator and RTL Schematic of Fibonacci Generator respectively.

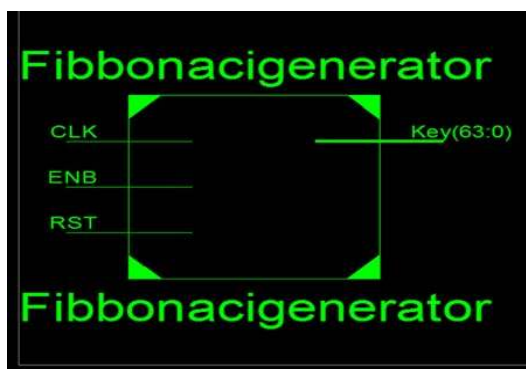


Figure 2: Top Level of Schematic of Fibonacci Generator

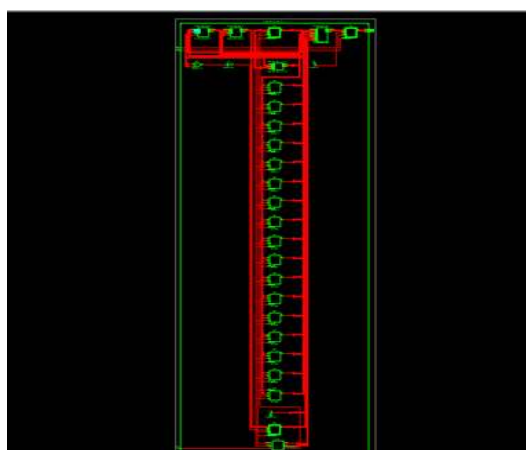


Figure 3: RTL Schematic of Fibonacci Generator

II. Literature Work

CRC is an error detection technique [1]. High Performance FIFO Design for Processor through Voltage Scaling Technique [2]. HSTL IO Standards Based Processor Specific Green Counter[3]. Capacitance Scaling Based Low Power Comparator Design on 28nm FPGA[4]. SSTL Based Energy Efficient FIFO Design for High Performance Processor of Portable Devices [5]. Energy Efficient CRC Design for Processor of Workstation, and Server using LVC MOS [6]. Cyclic redundancy check is a basic requirement for speed-optimized computation [6]. Memory controller logic includes a CRC component configured to enable the CRC processes on the individual ranks [6]. Speed-optimized computation of cyclic redundancy check codes[7]. Cyclic Redundancy Check (CRC) False Detection Reduction in Communication Systems[8]. In reference [9], researcher developed an instruction set architecture for programmable cyclic redundancy check (CRC) computation. Energy Efficient ALU Design Based On Voltage Scaling[10]

III. RESULT

TABLE I. Power consumption at 2V & 1 GHz

capacitance(pf)	Automotive Artix7	Artix7	kentix7
5	0.54	0.455	0.633
10	0.584	0.457	0.635
15	0.649	0.459	0.638

In table 1, power consumption of Fibonacci Generator is shown at 1 GHz frequency and 2V. In our table total power consumption is sum of I/O Power & Leakage Power. There is drop by 15.74% as we move from Automotive Artix7 to Artix7 and there is increment by 39.12% as we have moved from Artix7 to Kentix7 at 5pF. There is drop by 21.74% as we move from Automotive Artix7 to Artix7 and there is increment by 38.94% as we move from Artix7 to Kentix7 at 15pF. There is drop by 29.27% as we move from Automotive Artix7 to Artix7 and there is increment by 38.99% as we have moved from Artix7 to Kentix7 at 30pF. The above table data is shown by fig.4.

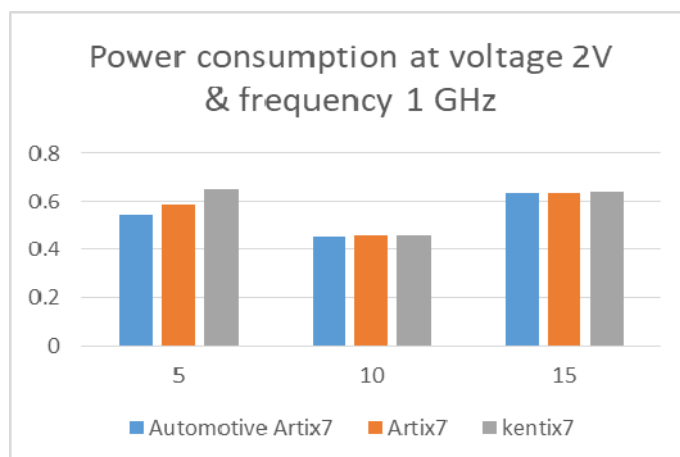


Fig.4 Power consumption at 2Volt & 1GHz

TABLE II. Total load at 2Volt & 10 GHz

capacitance(pf)	Automotive Artix7	Artix7	kentix7
5	1.587	0.937	1.783
10	2.028	0.998	2.221
15	2.694	1.089	2.879

In table 2, power consumption of Fibonacci Generator is shown at 10 GHz frequency and Voltage 2V. In our work we have found that there is drop by 40.95% as we have moved from Automotive Artix7 to Artix7 and there in increment by 90.28% as we switch from Artix7 to Kentix7 at 5pF. There is drop by 50.78% as we go from Automotive Artix7 to Artix7 and there in increment by 122.54% as we shift from Artix7 to Kentix7 at 10pF. There is drop by 59.57% as we move from Automotive Artix7 to Artix7 and there in increment by 164.3% as we changed from Artix7 to Kentix7 at 15pF. The above table data is also shown by Figure 5.

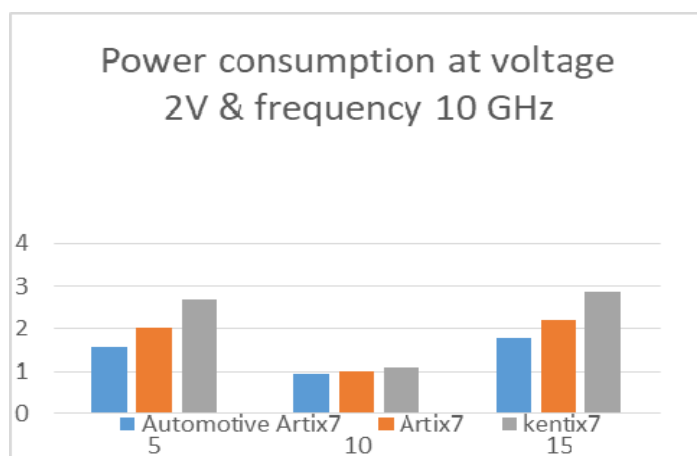


Fig.5 Power consumption at 2Volt & 10 GHz

TABLE III. Total load at voltage 3V & frequency 1 GHz

capacitance(pf)	Automotive Artix7	Artix7	kentix7
5	241.12	9.876	16.667
10	-	9.881	16.674
15	-	9.889	16.686

In table 3, power consumption of Fibonacci Generator is shown at 1 GHz frequency and Voltage 3V. In our work we have found that there is lot of power consumption in Automotive Artix7 so we got error value for higher Capacitance. There is increment by 68.76% as we have moved from Artix7 to Kentix7 at 5pF. There is increment by 68.74% as we shift from Artix7 to Kentix7 at 10pF. There is increment by 68.73% as we change from Artix7 to Kentix7 at 15pF. The above table data is also shown by Figure 6.

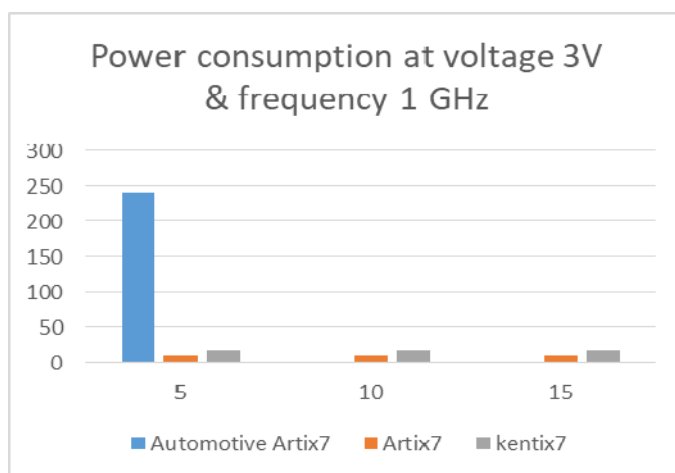


Fig.6 Power consumption at 3Volt & 1GHz

TABLE IV. Total load at voltage 3V & frequency 10 GHz

capacitance(pf)	Automotive Artix7	Artix7	kentix7
5	241.117	12.804	23.36
10	-	13.053	26.119
15	-	13.44	33.423
		4.7	30.10

In table 4, power consumption of Fibonacci Generator is shown at 10 GHz and 3Volt. In our work we have found that there is lot of power consumption in Automotive Artix7 so we got error value recorded for higher Capacitance. There is increment by 82.44% as we go from Artix7 to Kentix7 at 5pF. There is increment by 100.09% as we shift from Artix7 to Kentix7 at 10pF. There is increment by 148.68% as we move from Artix7 to Kentix7 at 15pF. The above table data is also shown by Figure 7.

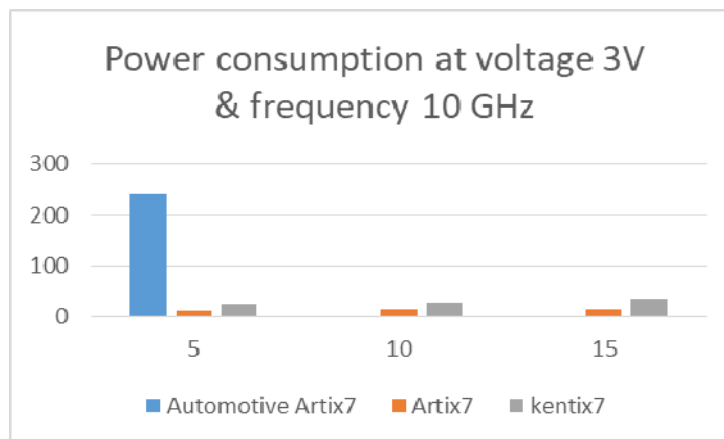


Fig.7 Power consumption at 2Volt & 10 GHz

IV. CONCLUSION

In our paper we have designed Power Efficient Fibonacci Generator using different FPGA families using VHDL language. Here we have applied capacitance scaling techniques for calculating total power consumption. As we know that Clock Power & Signal Power are independent of capacitance scaling and I/O Power & Leakage Power is varying with changing capacitance, so in our work, total power consumption is sum of I/O Power & Leakage Power. First we have calculated power consumption of our designed at 2Volt & 1GHz frequency and found the significant power consumption in Automotive Artix7 FPGA family. Secondly we have calculated power consumption of our designed at 2Volt & 10 GHz frequency and found 41.09% power reduction in Automotive Artix7 which is highest among the other FPGA families. In third, we have worked with 3Volt and frequency 1 GHz and got error value for Automotive Artix7 FPGA. In last, we have worked with 3Volt & 10 GHz and found 30.10% reduction in power consumption in kentix7 family which is highest among the other FPGA family .

V. FUTURE SCOPE

In this work, CRC Design is implemented on 28nm Kintex-7 FPGA family, but we have scope to redesign our CRC with different FPGA family like Virtex 7, Virtex 6, Virtex 5 or we can also apply different- different techniques for calculating total power consumption.

REFERENCES

- [1] CRC polynomial, <http://ghsi.de/CRC/index.php>, Last Visited on: 04 April 2016
- [2] A Saxena, A Bhatt, P Gautam, P Verma, C Patel, "High Performance FIFO Design for Processor through Voltage Scaling Technique" In Indian Journal of Science and Technology Vol 9(45), DOI: 10.17485/ijst/2016/v9i45/106916, December 2016.
- [3] A.Saxena, A.Bhatt B.Pandey, P.Tripathi "HSTL IO Standards Based Processor Specific Green Counter." In International Journal of Control and Automation, Vol. 9, No. 7, (2016), pp. 331-342.
- [4] A Saxena, S Gaidhani, A Pant, C Patel "Capacitance Scaling Based Low Power Comparator Design on 28nm FPGA" in International Journal of Computer Trends and Technology (IJCTT) – Volume X Issue Y- Month 2015
- [5] A Saxena, S Sharma, P Agarwal, C Patel "SSTL Based Energy Efficient FIFO Design for High Performance Processor of Portable Devices" in International Journal of Engineering and Technology (IJET) Vol 9 No 2 Apr-May 2017 DOI: 10.21817/ijet/2017/v9i2/170902113.
- [6] A Saxena, C Patel, M. Khan "Energy Efficient CRC Design for Processor of Workstation, and Server using LVCMOS" in Indian Journal of Science and Technology, Vol 10(4), DOI: 10.17485/ijst/2017/v10i4/110890, January 2017.
- [7] C. D. Kirkpatrick, "Speed-optimized computation of cyclic redundancy check codes." U.S. Patent No. 8,800,000, 18 Jun. 2013.
- [8] Subashchandra Bose, et al. "Rank-specific cyclic redundancy check." U.S. Patent No. 8,745,464. 3 Jun. 2014. 468,439. 18 Jun. 2013.
- [9] R. Cohen, and A. Kleinerman. "Cyclic Redundancy Check (CRC) False Detection Reduction in Communication Systems" U.S. Patent No. 20,160,026, 523. 28 Jan. 2016.
- [10] V. Gopal, et al. "Instruction-set architecture for programmable cyclic redundancy check (CRC) computations." U.S. Patent No. 8,732,548. 20 May 2014.
- [11] A Saxena, C Patel, M. Khan "Energy Efficient ALU Design Based On Voltage Scaling" in Gyancity Journal of Electronics and Computer Science, Vol.1, No.1, pp.29-33, September 2016 ISSN: 2446-2918 DOI: 10.21058/gjecs.2016.11006.