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Desynchronizing Paralleled GaN HEMTs to Reduce Light-Load Switching Loss

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***Abstract*—Parallel connection of GaN high-electron-mobility transistors (HEMTs) is a more cost-effective or even an unavoidable solution to achieve higher current ratings. As the load decreases, however, the switching loss of paralleled HEMTs becomes dominant over the conduction loss, and the overall power conversion efficiency drops sharply. To reduce the light-load switching loss, this paper proposes a desynchronizable paralleling scheme. The midpoint (AC terminal) of each paralleled HEMT half bridge is connected with a commutation inductor, which thus, enables two operation modes: synchronous and asynchronous modes. The synchronous mode is activated at heavy loads to share the high current; the added commutation inductors lead to better current sharing than the direct parallel. When operating at light loads, however, the paralleled devices are desynchronized to generate a circulating current flowing through the commutation inductors. The circulating current enables the lagging HEMTs to achieve the zero-voltage switching (ZVS) and allows the leading ones to turn on at a current lower than the load, thereby significantly reducing the total switching loss. In addition, a thermal balancing scheme is proposed to alleviate the thermal stress imbalance between the desynchronized GaN HEMTs. The operating principle and design guidelines of the desynchronizable paralleling scheme are detailed. Finally, experimental results from multi-pulse and continuous tests of GaN HEMTs are provided to verify the advantages of the proposed paralleling scheme in reducing light-load switching loss and improving light-load efficiency.**

***Index Terms*—Parallel of GaN HEMTs, desynchronized parallel, commutation inductors, switching loss, ZVS, light-load efficiency**

I. Introduction

COMPARED with Si counterparts, GaN enhancement-mode high-electron-mobility transistors (HEMTs) feature a higher switching speed and lower switching loss. Thus, it is easier for GaN-based power electronics converters to achieve high efficiency and high power density. Hence, GaN HEMTs have been applied to various industrial and consumer products such as photovoltaic (PV) converters [1], on-board electric vehicle (EV) chargers [2], motor drives [3], and portable chargers [4].

The on-state resistance $R_{ds,on}$ of GaN HEMTs has a strong dependency on the junction temperature T_j, e.g., the $R_{ds,on}$ of GS66508T is tripled when T_j increases from 0 °C to 137 °C [5]. To reduce the conduction loss and maintain high efficiencies in high-current and high-temperature conditions, it is desired to adopt high-current-rating GaN HEMTs. To date, the maximum current rating of commercial 650-V GaN HEMTs is 60 A, i.e., GS66516T [6]. However, it is challenging to use unparalleled GS66516T devices (size: 9.0 mm × 7.6 mm × 0.54 mm) in high power applications (e.g., >10-kW motor drives) due to the caused high power loss and high thermal stress [7]. Furthermore, in many cases, the price of GaN HEMTs varies nonlinearly with the current rating; one high-current device can be much more expensive than multiple low-current counterparts, e.g., GS66516T×1 for $46.96, versus GS66508T×2 for $27.84 [8]. Therefore, parallel connection of power devices can be a cost-effective or even an unavoidable solution for power electronic converters [9]–[17].

When operating at light loads, however, the switching loss of the paralleled HEMTs dominates over the conduction loss, which deteriorates the light-load efficiency performance. Meanwhile, the light-load operation represents the dominant use in many operating environments, e.g., microprocessors [18], PV [19] and EVs [20]; reducing the light-load switching loss may contribute to a remarkable energy efficiency improvement [21], [22]. Accordingly, it is desired to develop a paralleling technique that is able to lower both the light-load switching loss and the heavy-load conduction loss.

The dynamic turn-on/-off speed/timing mismatches among paralleled power semiconductor devices occur frequently due to the inevitable differences from the gate delay, threshold voltage $V_{gs,th}$, transconductance g_{fs}, junction temperature T_j, gate resistance R_g, parasitic capacitance, and parasitic inductance [10]–[12], [15], [23]–[31]. Therefore, many paralleling techniques have been proposed to improve the current sharing performance among paralleled semiconductor power devices. Specifically, refs. [26]–[28] actively control the gate resistance or delay times of paralleled devices to balance the transient currents. However, these approaches need multiple high-bandwidth current sensors and analog feedback control which are difficult to fabricate and complicated to implement [14], [17], [30], [31]. Recently, the passive current balancing approaches [14], [17], [29]–[31] become popular due to their simplicity and robustness. In these works, inversely-coupled inductors are added to the paralleled SiC and GaN transistors; a high differential-mode impedance can be formed and it is able to alleviate the current imbalance among paralleled devices. However, these techniques cannot reduce the low-current switching loss that is dominant in the total light-load power losses of high-frequency power converters.

The multiphase interleaving of half-bridge (HB) legs (e.g., the synchronous buck converter and the intercell transformer for inverters) is able to reduce the output filter size and to enhance the dynamic response performance of converters [32]–[35]. To improve the light-load efficiency, multiple techniques, e.g., the pulse skipping, pulse frequency modulation, half-full-bridge switching, constant ON time, and phase shedding, have been proposed in the literature [21], [22], [34], [36]–[40].

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Among them, the most popular scheme for the multiphase interleaved systems is to adjust the operational phase number based on the load current condition [21], [32], [34], [40]. However, the multiphase interleaving requires relatively large ($>$ several hundreds of μH) inductors, which are normally not desired in some inductive-load applications, e.g., motor drives, due to the added power loss, cost and volume [41], [42]. Recently, the triangular-current-mode (TCM) multiphase interleaving has attracted increasing research attention owing to its soft-switching characteristics for all switches [43]–[45]. This approach requires high-speed zero current detection (ZCD) and accurate timing for the zero-voltage switching (ZVS) realization, and therefore its implementation complexity is high [30], [46], [47].

To reduce the light-load switching loss of parallel-connected GaN HEMTs, this paper proposes a desynchronized control scheme for the first time. In the scenario of low load currents, the paralleled HB legs are desynchronized at their turn-on instants; thus, a small circulating current can be generated, which allows the lagging HEMTs to achieve the ZVS and the leading HEMTs to turn on at a current lower than the load. Consequently, the light-load switching loss can be significantly reduced. In order to alleviate the asynchronous-mode thermal stress deviation between the leading and lagging GaN HEMTs, a thermal balancing scheme is proposed as well. In addition, when operating at heavy loads, all the paralleled HEMTs are driven synchronously to share the high current and to reduce the total power loss; the small commutation inductors added to the midpoints of paralleled HB legs lead to better transient current sharing performance than the direct parallel.

The remainder of this paper is organized as follows: the switching loss characteristics of paralleled GaN HEMTs and the derivation of the proposed desynchronizable paralleling structure are presented in Section II. Section III details the operating principles of the proposed paralleling technique in both the synchronous and asynchronous modes before Section IV presents design guidelines and a thermal balancing scheme. After that, the experimental results of multi-pulse and continuous tests are provided in Section V for proposal verification. Finally, conclusions are drawn in Section VI.

II. Derivation of Proposed Desynchronizable Paralleling Structure

A. Swtiching Loss Breakdown of GaN HEMTs

Typical hard-switching (HS) waveforms of a GaN HEMT are shown in Fig. 1(a) and (b), and the measured switching losses of paralleled GaN HEMTs (GS66508T×1, GS66508T×2, and GS66516T×1) are shown in Fig. 1(c). As can be seen, both the turn-on and turn-off energy losses E_{on} and E_{off} are composed of two portions, i.e., the current-independent capacitive losses E_{qoss} and E_{oss}, and the current-dependent losses $E_{on,VI}$ and $E_{off,VI}$ [48].

The energy loss E_{oss} of N paralleled GaN HEMTs is introduced by the self-discharging current of their output capacitance, whereas E_{qoss} is caused by the capacitive charging current from the opposite switching devices [48]–[50]. The two types of losses E_{oss} and E_{qoss} can be obtained as

$$E_{oss(V_{dc},N)} = \int_0^{V_{dc}} v_{ds} N C_{oss(v_{ds})} \mathrm{d}v_{ds} \tag{1}$$

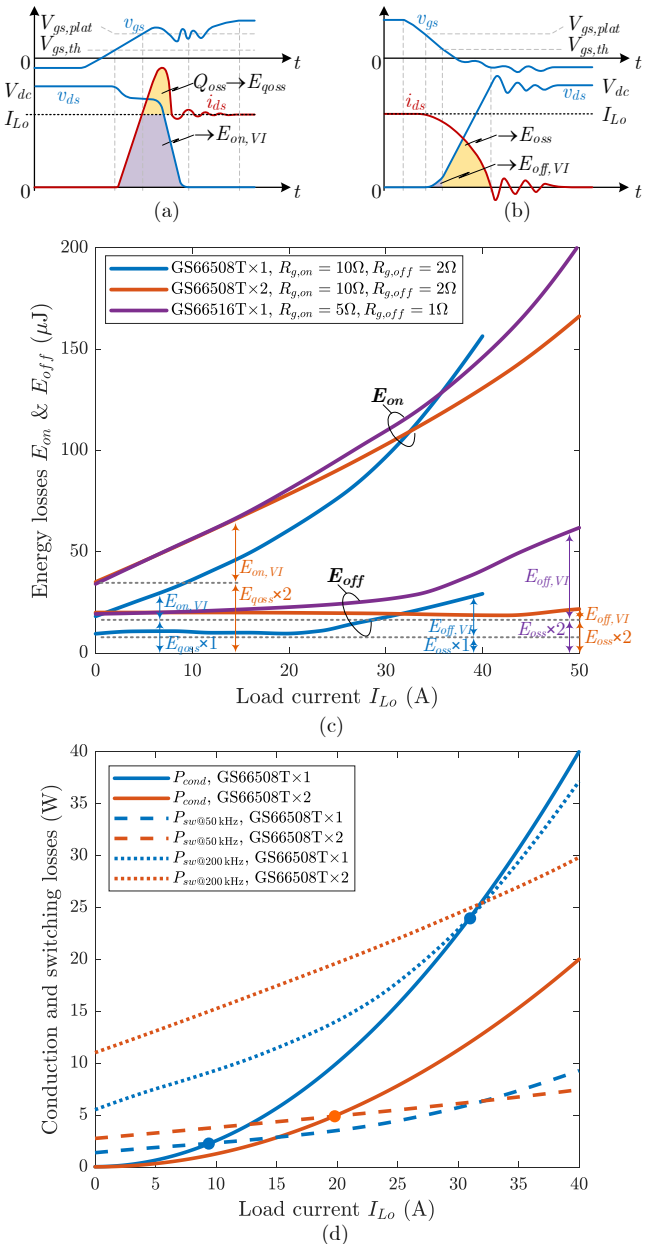

Fig. 1. Typical voltage and current waveforms of a GaN HEMT at (a) turn-on and (b) turn-off transitions. The energy loss E_{oss} of a GaN HEMT is introduced by the self-discharging current of its output capacitance, whereas E_{qoss} is caused by the capacitive charging current from the opposite switching device [48]–[50]. These two type of losses are independent of the switching current and junction temperature [48]. (c) Measured switching energy losses of multiple ($N = 1, 2$) paralleled 30-A GaN HEMTs (GS66508T) and one 60-A device (GS66516T). The schematic of N paralleled GaN HEMT half bridges is shown in Fig. 2(a), and the low-side switches are the devices under test (DUTs). The junction temperature $T_j = 25$ °C. The turn-on and -off gate resistances of each GS66508T device are $R_{g,on} = 10\ \Omega$ and $R_{g,off} = 2\ \Omega$, respectively. For the 60-A device, GS66516T, its input capacitance is twice as large as that of the 30-A device GS66508T, and therefore, its turn-on and -off gate resistances are halved in order to achieve the same gate drive speed with GS66508T. The evaluation boards GS66508T-EVBDB2 and GS66516T-EVBDB2 [51] are tested to extract the above switching loss data. The loop inductance of one GS66516T half-bridge board is higher than that of two paralleled GS66508T half-bridge boards, and therefore, the measured switching loss of one GS66516T device is higher than that of two paralleled GS66508T devices when the load current I_{Lo} is high ($>$ 15 A). (d) Conduction and switching power losses of paralleled GS66508T GaN HEMTs operating at 50 kHz and 200 kHz. The three dots represent the cases where the switching loss equals the conduction loss.

$$\begin{aligned} E_{qoss(V_{dc},N)} &= \int_0^{V_{dc}} (V_{dc} - v_{ds}) N C_{oss(v_{ds})} \mathrm{d}v_{ds} \\ &= V_{dc} N Q_{oss(V_{dc})} - \int_0^{V_{dc}} v_{ds} N C_{oss(v_{ds})} \mathrm{d}v_{ds} \\ &= V_{dc} N Q_{oss(V_{dc})} - E_{oss(V_{dc},N)} \end{aligned} \tag{2}$$

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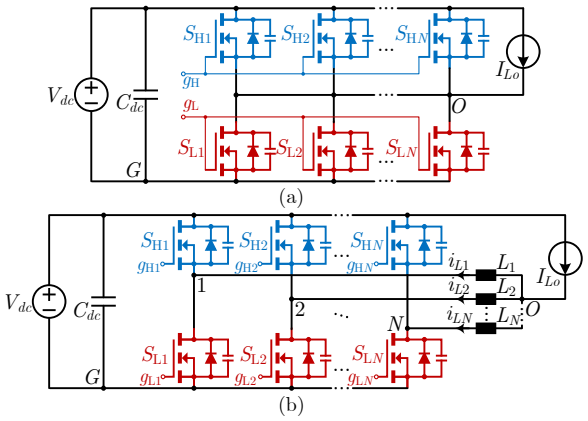

Fig. 2. (a) Conventional paralleling structure and (b) proposed commutation-inductor-based desynchronizable paralleling structure for GaN HEMT half bridges. L_1, L_2, ..., L_N are the added commutation inductors. I_{Lo} represents the load current. GaN enhancement mode HEMTs do not have an intrinsic body diode, and therefore, there is no reverse recovery; the zero-recovery diodes here are used to facilitate the commutation analysis.

where V_{dc} is the dc bus voltage, $C_{oss(v_{ds})}$ denotes the v_{ds}-dependent output capacitance of a GaN HEMT, and $Q_{oss(V_{dc})}$ is the charge stored in one output capacitor at $v_{ds} = V_{dc}$. The output capacitance C_{oss} of a GaN HEMT nonlinearly decreases with respect to the increase of v_{ds}; as a result, E_{qoss} is larger than E_{oss} at the same V_{dc}. It is seen from (1) and (2) that both E_{qoss} and E_{oss} are independent of the switching current and junction temperature; instead, these two capacitive losses are directly proportional to the number of GaN HEMTs in parallel, N, and the dc bus voltage V_{dc}, as indicated in Fig. 1(c). However, for the losses $E_{on,VI}$ and $E_{off,VI}$, they are determined by the switching current, junction temperature, and gate resistance [49].

From Fig. 1(c), it is also seen that the losses $E_{on,VI}$ and $E_{off,VI}$ are dominant at high load currents. As the load current decreases, the fixed capacitive losses E_{oss} and E_{qoss} then make up a higher proportion in the total switching loss. In particular, at medium and low load currents, E_{off} is mainly determined by E_{oss} due to the small $E_{off,VI}$. This is because the two-dimensional electron gas (2DEG) conducting channel of a GaN HEMT can be fast cut off before the voltage of the nonlinear output capacitance, i.e., v_{ds}, rises significantly [52].

B. Derivation of Desynchronizable Paralleling Structure

As seen from Fig. 1(c) and (d), at high currents, more GaN HEMTs in parallel (i.e., a larger N) leads to lower switching and conduction losses; at low currents, however, it results in a higher switching loss that dominates the total light-load power loss. In order to reduce the power loss in the whole load range, it is desired to flexibly adjust the effective number of HEMTs in parallel based on the load current. It seems sensible to separately drive the paralleled HEMTs in Fig. 2(a) and to keep some legs off at light loads. However, this method actually causes much higher switching losses than a single device or more in parallel because the effective output capacitance of the paralleled HEMTs remains but the active HEMTs have to turn on and turn off at the full load current.

By adding small commutation inductors, i.e., L_1, L_2, ..., L_N, to the midpoints of the parallelled GaN HEMT half bridges, we can obtain a desynchronizable paralleling structure, as shown in Fig. 2(b). It enables both the synchronous and asynchronous operations for the paralleled HBs. Typically, the output filter inductance L_o is significantly larger than the commutation inductance, i.e., $L_o \gg L_c = L_1 = L_2 = ... = L_N$, but still, the commutation inductors can act as part of L_o.

It should be noted that GaN enhancement mode HEMTs do not have an intrinsic body diode, but the added body diodes in Fig. 2 are used to facilitate the commutation analysis below.

III. Operating Principles of Proposed Desynchronizable Paralleling Structure

A. Synchronous Mode

When the load current is high, it is desired to synchronously switch the paralleled HEMTs such that the conduction and switching losses can be reduced, as indicated in Fig. 1(c).

The operating waveforms of the desynchronizable paralleling structure in the synchronous mode are shown in Fig. 3. The N low-side switches $S_{Ln}, n = 1, 2, ..., N$, (the DUTs), are turned on at $1/N$ of the load current I_{Lo}, which is similar to the conventional paralleling structure without commutation inductors. However, the addition of commutation inductors leads to better transient current sharing characteristics than the conventional structure, as illustrated below.

The equivalent circuit of the proposed paralleling structure (cf. Fig. 2(b)) is shown in Fig. 5(a). Considering an ideal switching process, i.e., both the turn-on and turn-off times are equal to 0, we can obtain that the midpoint voltages $v_n (n = 1, 2, ..., N)$ is equal to eithor 0 or V_{dc}.

The commutation inductor currents, $i_{L1}, i_{L2}, ..., i_{LN}$, can be decoupled into the common-mode current i_{CM} and the differential-mode currents $i_{DM1}, i_{DM2}, ..., i_{DMN}$. By definition, the common-mode and differential-mode currents can be obtained as

$$i_{CM} = \frac{1}{N}\sum_{n=1}^{N} i_{Ln} = \frac{I_{Lo}}{N} \tag{3}$$

$$\begin{cases} i_{DM1} = i_{L1} - i_{CM} \\ i_{DM2} = i_{L2} - i_{CM} \\ \quad\vdots \\ i_{DMN} = i_{LN} - i_{CM} \end{cases} \tag{4}$$

It is seen from (4) that the real current difference among the commutation inductors is equal to the difference of their differential-mode currents. If all the paralleled GaN HEMT HBs are exactly the same and also they are synchronized, then $i_{DM1} = i_{DM2} = ... = i_{DMN} = 0$, and $i_{L1} = i_{L2} = ... = i_{LN} = \frac{I_{Lo}}{N}$, which implies that current sharing can be achieved for the commutation inductors and the paralleled GaN HEMT HBs.

In practice, however, the dynamic turn-on/-off speed/timing mismatch of paralleled GaN HEMTs is inevitable due to the differences from the gate delay, threshold voltage $V_{gs,th}$, transconductance g_{fs}, junction temperature T_j, gate resistance R_g, parasitic capacitance, and parasitic inductance [10]. As a result, the voltages of HB midpoints $(v_1, v_2, ..., v_N)$ and those across the commutation inductors $(v_{1O}, v_{2O}, ..., v_{NO})$ are misaligned with each other.

In the first step, it is assumed that n_{ld} $(1 \leqslant n_{ld} \leqslant N-1)$ of the N paralleled HBs are leading the remaining $N - n_{ld}$ ones by a time delay of $\Delta\tau$. In this case, the midpoint voltages and the unbalanced inductor currents are shown in Fig. 5(b).

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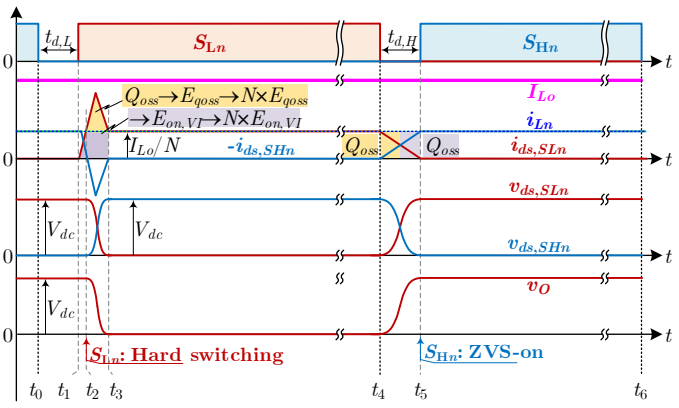

Fig. 3. Typical waveforms of the desynchronizable paralleling structure of GaN HEMT half bridges (see Fig. 2(b)) when operating in the synchronous mode.

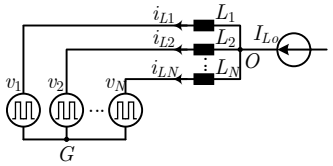

Fig. 4. Equivalent circuit of the proposed paralleling structure with commutation inductors (cf. Fig. 2(b)).

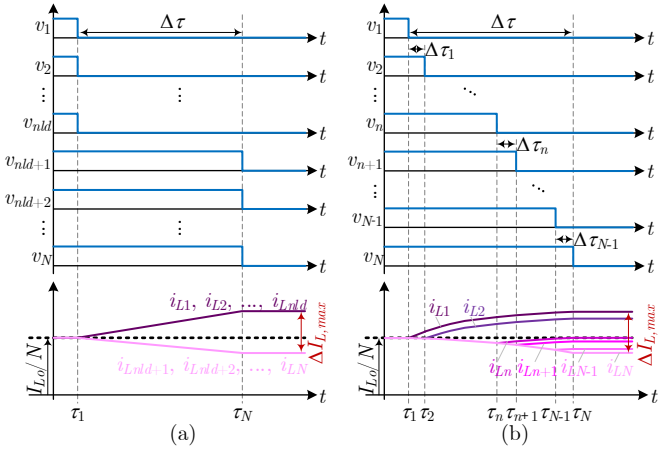

Fig. 5. (a) Unbalanced commutation inductor currents when n_{ld} of the N midpoint voltages are leading the remaining $N - n_{ld}$ ones. (b) Unbalanced commutation inductor currents when all the N midpoint voltages are out of phase with each other; $\Delta\tau_n$ $(n = 1, 2, ..., N-1)$ represents the time delay between v_n and v_{n+1}. The maximum time delay among the midpoint voltages and the maximum current imbalance among the commutation inductor currents are denoted as $\Delta\tau$ and $\Delta I_{L,max}$, respectively.

The generated differential-mode currents flowing through each leading leg and each lagging leg can be obtained as

$$\begin{cases} I_{DM,ld} = \frac{V_{dc}\Delta\tau}{NL_c}(N - n_{ld}) \\ I_{DM,lg} = -\frac{V_{dc}\Delta\tau}{NL_c} n_{ld} \end{cases} \tag{5}$$

Thus, the maximum current difference between the leading and lagging legs is obtained as

$$\Delta I_{L,max} = |I_{DM,ld} - I_{DM,lg}| = \frac{V_{dc}\Delta\tau}{L_c} \tag{6}$$

In a general case, the time delays of the N paralleled GaN HBs may differ with each other, as shown in Fig. 5(c). The maximum current difference is between the earliest leg and the latest leg, i.e., between i_{L1} and i_{LN} in Fig. 5(c).

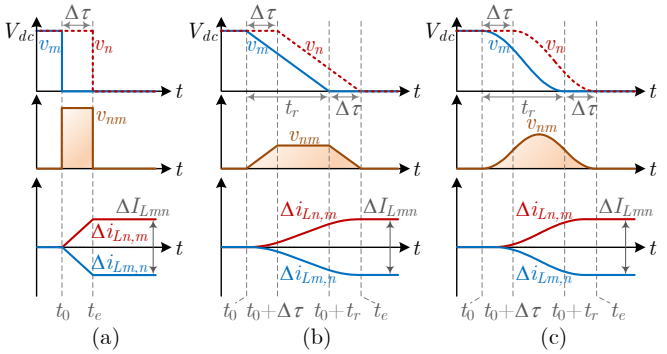

Fig. 6. Unbalanced current waveforms between two commutation inductors L_m and L_n $(m = 1, 2, ..., N, n = 1, 2, ..., N,$ and $m \neq n)$ when neglecting or considering the rise and fall time of the midpoint voltages (see Fig. 4): (a) the midpoint voltages are ideal, i.e., the rise and fall time $t_r = 0$; (b) the midpoint voltages linearly rise and fall with a transition time of t_r $(t_r > 0)$; (c) the midpoint voltages non-linearly rise and fall with a transition time of t_r $(t_r > 0)$.

According to (6), the generated current difference between i_{Ln} and i_{Ln+1} $(n = 1, 2, ..., N-1)$ within the interval $[\tau_n, \tau_{n+1}]$, i.e., $\Delta I_{L,\Delta\tau_n}$, can be obtained as

$$\Delta I_{L,\Delta\tau_n} = \frac{V_{dc}\Delta\tau_n}{L_c} \tag{7}$$

The maximum inductor current imbalance $\Delta I_{L,max}$ can be obtained by

$$\Delta I_{L,\max} = \sum_{n=1}^{N-1} \Delta I_{L,\Delta\tau_n} = \frac{V_{dc}\Delta\tau}{L_c} \tag{8}$$

As can be seen, the maximum inductor current imbalance is independent of N and N_{ld}, but is determined by the maximum time delay among the N paralleled GaN HEMT legs and the commutation inductance L_c.

The analysis above is based on the assumption that the rise and fall time of the midpoint voltages, t_r, equals 0. In practice, however, $t_r > 0$. Neglecting and considering the rise and fall time t_r, the voltage and current waveforms of two commutation inductors L_m and L_n $(m = 1, 2, ..., N,$ $n = 1, 2, ..., N,$ and $m \neq n)$ are shown in Fig. 6. The voltage v_{nm} represents the difference between two random midpoint voltages v_n and v_m, i.e., $v_{nm} = v_n - v_m$. $\Delta i_{Ln,m}$ and $\Delta i_{Lm,n}$ denote the current variations of i_{Ln} and i_{Lm} caused by v_{nm}, i.e.,

$$-\Delta i_{Lm,n} = \Delta i_{Ln,m} = \frac{1}{2L_c}\int_{t_0}^{t_e} v_{nm}(t)\mathrm{dt} = \frac{1}{2L_c}A_{vnm} \tag{9}$$

where A_{vnm} represents the volt-second product of v_{nm} during $[t_0, t_e]$, i.e., the shaded areas in Fig. 6. Regardless of the shape of the rise and fall edge of midpoint voltage, the shaded areas in Fig. 6(a), (b) and (c) can be always obtained as $A_{vnm} = V_{dc}\Delta\tau$. Thus, (9) can be expressed as $-\Delta i_{Lm,n} = \Delta i_{Ln,m} = \frac{V_{dc}\Delta\tau}{2L_c}$. That is, the resulting current difference between L_m and L_n, $\Delta I_{Lmn} = |\Delta i_{Lm,n} - \Delta i_{Ln,m}| = \frac{V_{dc}\Delta\tau}{L_c}$, is independent of the rise (fall) time and shape of midpoint voltages. Therefore, the analyses above $(t_r = 0)$ also hold true in practical scenarios where $t_r > 0$.

Compared with the direct parallel where $L_1, L_2, ..., L_N$ represent parasitic inductances and have small values (e.g., < a few tens of nH), the proposed paralleling structure with added commutation inductors is capable of alleviating the current imbalance among the paralleled GaN HEMT HB legs.

B. Asynchronous Mode

As the load decreases, fewer effective GaN HEMTs in parallel lead to lower switching losses, as shown in Fig. 1(c). Hence, it is preferable for the proposed desynchronizable paralleling structure to operate in an asynchronous mode. In this asynchronous mode, n_{ld} legs are leading the remaining n_{lg} ($n_{lg} = N - n_{ld}$) ones at their turn-on instants, as shown in Fig. 7(a). Meanwhile, the n_{ld} leading legs are synchronously gated, and so are the n_{lg} lagging legs. The theoretical midpoint voltages of these HBs are shown in Fig. 5(b). However, it should be noted that in this proposed asynchronous mode, the time delay is much longer than the inevitable small delay in the synchronous mode.

To simplify the analysis in the asynchronous mode, the n_{ld} leading legs and their corresponding commutation inductors are lumped into a single leading leg $S_{Ha}\&S_{La}$ with a single commutation inductor L_a. Likewise, the n_{lg} lagging legs and their corresponding commutation inductors can be lumped into $S_{Hb}\&S_{Lb}$ + L_b. The equivalent circuit of Fig. 7(a) is shown in Fig. 7(b). It is noted that the equivalent output capacitances of $S_{Ha}\&S_{La}$ and $S_{Hb}\&S_{Lb}$ are $n_{ld}C_{oss}$ and $n_{lg}C_{oss}$, respectively; the inductances of L_a and L_b are L_c/n_{ld} and L_c/n_{lg}, respectively. Thus, the equivalent differential-mode inductance between the two lumped legs is

$$L_{DM} = L_a + L_b = \frac{n_{ld} + n_{lg}}{n_{ld} n_{lg}} L_c \tag{10}$$

The typical operating waveforms of the proposed paralleling structure in the asynchronous mode are shown in Fig. 8. Depending on the polarity of the leading indutor current at t_0, i.e., $I_{La,t0}$ ($I_{La,t0} = I_{Lo} - i_{Lb}(t_0) = I_{Lo} - I_{cir,pk}$), two operating cases can be identified in the asynchronous mode: *Case I* ($I_{La,t0} = I_{Lo} - I_{cir,pk} \geqslant 0$, see Fig. 8(a)) and *Case II* ($I_{La,t0} = I_{Lo} - I_{cir,pk} < 0$, see Fig. 8(b)).

1) Case I: $I_{La,t0} = I_{Lo} - I_{cir,pk} \geqslant 0$

Considering the parasitic output capacitance of HEMTs, we can identify ten operation stages for one switching cycle $[t_0, t_{10}]$, as shown in Figs. 8(a) and 9.

Stage 1 $[t_0, t_1]$ (see Figs. 8(a) and 9(a)): The high-side switches S_{Ha} and S_{Hb} have been reversely conducting before t_0. At t_0, S_{Ha} and S_{Hb} are turned off, and thus, their body diodes begin conducting.

Stage 2 $[t_1, t_2]$ (see Figs. 8(a) and 9(c)): After the deadtime $t_{d,L}$, the low-side switch of the leading HB leg, i.e., S_{La}, is applied with a turn-on signal. When its gate-source voltage $v_{gs,SLa}$ rises to the threshold voltage $V_{gs,th}$, the channel of S_{La} begins to conduct, operating as a voltage-controlled current source. The drain current $i_{ds,SLa}$ rises as the gate voltage goes up, diverting part of the load current to S_{La}. However, the drain-source voltage of S_{Ha} is clamped by its conducting body diode, and thus, the drian-source voltage of S_{La} is clamped to the dc-bus voltage V_{dc} if the loop inductance is neglected.

Stage 3 $[t_2, t_3]$ (see Figs. 8(a) and 9(d)): Once the current $i_{ds,SLa}$ reaches i_{La}, ($i_{La} = I_{Lo} - i_{Lb}$), it means that the current flowing through the body diode of S_{Ha} falls to zero; then the output capacitor of S_{Ha}, i.e., $C_{oss,SHa}$($C_{oss,SHa} = n_{ld}C_{oss}$) begins to be charged. The current $i_{ds,SLa}$ is the sum of the inductor current i_{La} and the current charging $C_{oss,SHa}$, thereby generating a current bump. The current

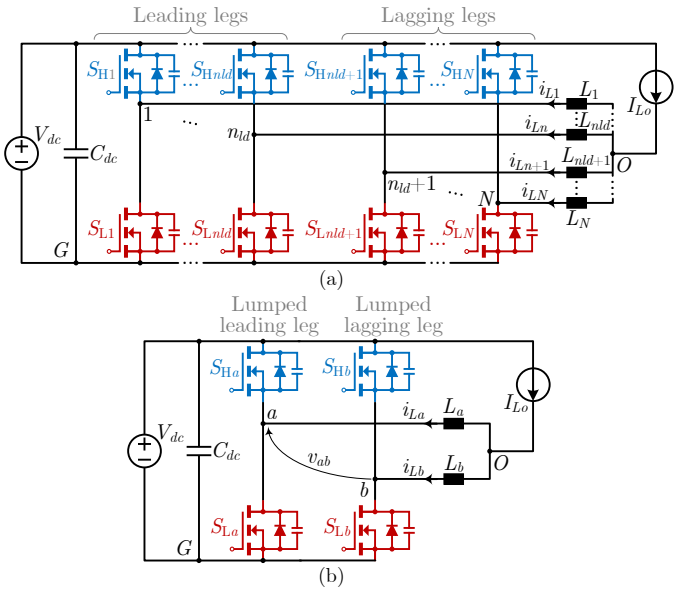

Fig. 7. (a) Diagram of the proposed desynchronizable paralleling structure of N GaN HEMT HBs when operating in the asynchronous mode, and n_{ld} legs are leading the remaining $n_{lg}(n_{lg} = N - n_{ld})$ ones at their turn-on instants. (b) Equivalent circuit of Fig. 7(a) where the n_{ld} leading legs and n_{lg} lagging legs are lumped into the leg $S_{Ha}\&S_{La}$, and the leg $S_{Hb}\&S_{Lb}$, respectively. The lumped inductors $L_a = L_c/n_{ld}$ and $L_b = L_c/n_{lg}$.

bump (as shaded in Fig. 8(a)) corresponds to the charge stored in $C_{oss,SHa}$, i.e., $n_{ld}Q_{oss} = \int_0^{V_{dc}} C_{oss,SHa}(v_{ds})\mathrm{d}v_{ds} = n_{ld}\int_0^{V_{dc}} C_{oss}(v_{ds})\mathrm{d}v_{ds}$. In this stage, the output capacitor of S_{La}, i.e., $C_{oss,SLa}(C_{oss,SLa} = n_{ld}C_{oss})$, is self discharging via its 2DEG, leading to a decreasing $V_{ds,SLa}$ and an energy loss $n_{ld}E_{oss}$, as indicated by the light blue dashed line in Fig. 9(d). It should be noted that the energy loss $n_{ld}E_{oss}$ is stored during last turn-off event and is included in the measured turn-off energy loss.

Stage 4 $[t_3, t_4]$ (see Figs. 8(a) and 9(e)): At t_3, $C_{oss,SHa}$ and $C_{oss,SLa}$ are fully charged to V_{dc} and discharged to 0, respectively, which means that S_{La} is fully turned on and S_{Ha} is fully turned off. Then, the negative midpoint voltage $v_{ab} = -V_{dc}$ drives the circulating current i_{Lb} to decrease. That is, during the interval of $[t_3, t_4]$, the energy stored in the commutation inductor L_b is delivered to the dc source V_{dc}. The decrease of i_{Lb} follows

$$\begin{aligned} i_{Lb}(t) &= i_{Lb}(t_3) - \tfrac{V_{dc}}{L_{DM}}(t - t_3) \\ &= i_{Lb}(t_3) - \tfrac{n_{ld}n_{lg}V_{dc}}{(n_{ld}+n_{lg})L_c}(t - t_3) \\ &\approx I_{cir,pk} - \tfrac{n_{ld}n_{lg}V_{dc}}{(n_{ld}+n_{lg})L_c}(t - t_3) \end{aligned} \tag{11}$$

where $I_{cir,pk}$ represents the peak value of the circulating current i_{Lb}. From (11), we can obtain the time between t_3 and t_4 as

$$\Delta t_{34} = t_4 - t_3 \approx \frac{I_{cir,pk}}{V_{dc}} \frac{(n_{ld} + n_{lg})L_c}{n_{ld}n_{lg}} \tag{12}$$

It is also noted that during the interval $[t_1, t_4]$, the circulating current i_{Lb} remains freewheeling through S_{Hb}, and thus, the states of the lagging-leg switches S_{Hb}-S_{Lb} keep unchanged.

Stage 5 $[t_4, t_5]$ (see Figs. 8(a) and 9(f)): The circulating current i_{Lb} falls to 0 at t_4, after which the output capacitors

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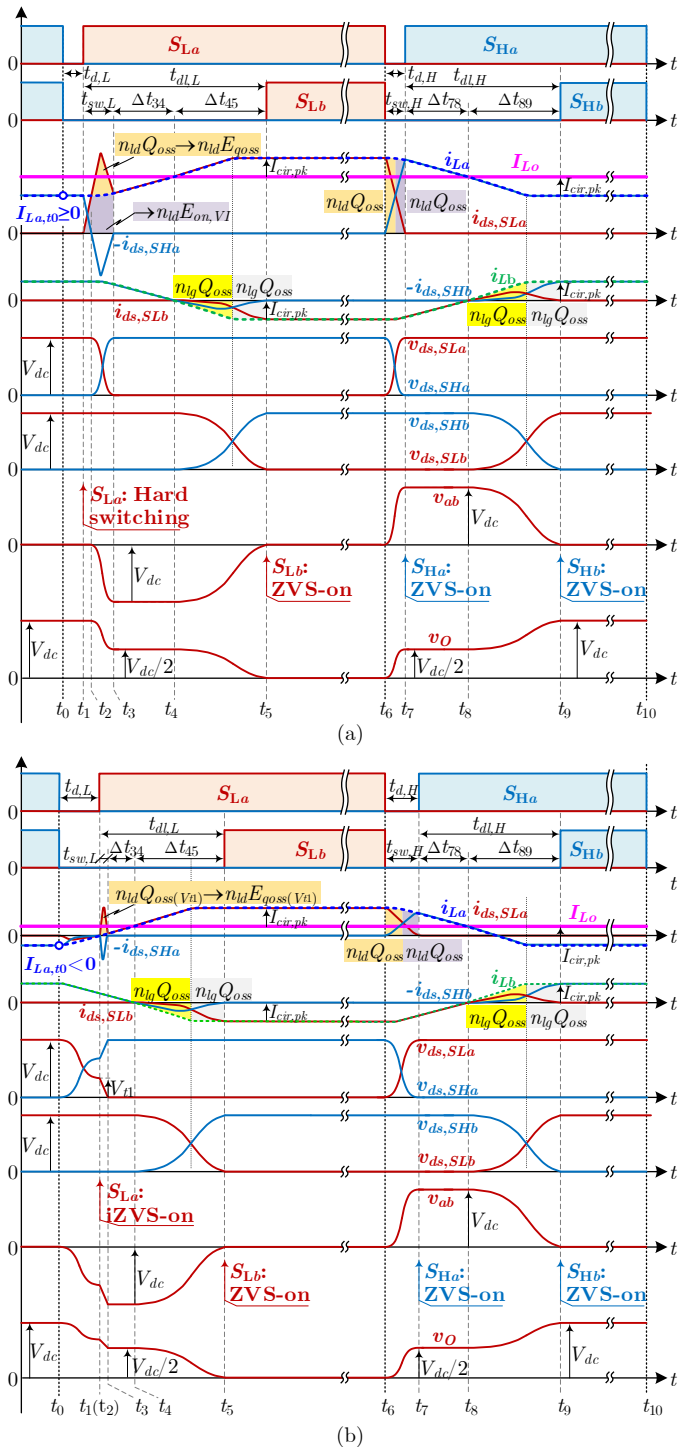

Fig. 8. Typical waveforms of the proposed desynchronizable paralleling structure of GaN HEMT half bridges (see Fig. 7(b)) when operating in the asynchronous mode. (a) *Case I*: $I_{La,t0} = I_{Lo} - I_{cir,pk} \geqslant 0$. (b) *Case II*: $I_{La,t0} = I_{Lo} - I_{cir,pk} < 0$. The load current I_{Lo} is regarded as constant over a switching cycle. It is the voltage difference between the midpoints of HB legs, i.e., v_{ab} in Fig. 7(b), that causes a circulating current flowing through the commutation inductors in this asynchronous mode.

$C_{oss,SHb}$&$C_{oss,SLb}$ begin to transfer charge through the commutation inductors L_a&L_b under the excitation of V_{dc}, setting at t_5 with $C_{oss,SHb}$ charged to V_{dc} and $C_{oss,SLb}$ discharged to 0. Assuming there is no resistive energy loss during $[t_4, t_5]$, then according to the law of conservation of energy, we have

$$\frac{L_{DM}[(i_{Lb}(t_5))]^2}{2} = \frac{(n_{ld}+n_{lg})L_c}{n_{ld}n_{lg}} \frac{I_{cir,pk}^2}{2} = n_{lg}V_{dc}Q_{oss} \tag{13}$$

where the peak value of the circulating current i_{Lb}, i.e., $I_{cir,pk}$, can be obtained as

$$I_{cir,pk} = -i_{Lb}(t_5) = \sqrt{\frac{2n_{ld}n_{lg}^2 V_{dc}Q_{oss}}{(n_{ld}+n_{lg})L_c}} \tag{14}$$

The output capacitance of a GaN HEMT is strongly dependent on its drain-source voltage. Due to this dependency, the shape of i_{Lb} is almost trapezoidal during $[t_4, t_5]$. In [43], [53], the highly nonlinear output capacitance C_{oss} is further idealized, i.e., C_{oss} is assumed as extremely large at low voltages and extremely small at high voltages; thus, a Q_{oss}-based time model is proposed for power MOSFETs and HEMTs [43], [53]. According to this model, the total accumulated charge of i_{Lb} over $[t_4, t_5]$ is $2n_{lg}Q_{oss}$, and the trapezoidal current i_{Lb} reaches it vertex when the accumulated charge equals $n_{lg}Q_{oss}$. Thus, we can obtain the time between t_4 and t_5, i.e.,

$$\Delta t_{45} = t_5 - t_4 = \frac{2n_{lg}Q_{oss}}{I_{cir,pk}} + \frac{n_{lg}Q_{oss}}{I_{cir,pk}} = \frac{3n_{lg}Q_{oss}}{I_{cir,pk}} \tag{15}$$

Stage 6 $[t_5, t_6]$ (see Figs. 8(a) and 9(g)): After t_5, the body diode of S_{Lb} begins conducting the circulating current i_{Lb}. Subsequently, applying a turn-on gate signal to S_{Lb} enable it to achieve the ZVS-on, thereby minimizing its switching loss. During the interval $[t_5, t_6]$, both the load current I_{Lo} and the small circulating current i_{Lb} are flowing through S_{La}.

Stage 7 $[t_6, t_7]$ (see Figs. 8(a) and 9(h)): At t_6, the turn-off gate signals of the low-side switches S_{La}&S_{Lb} are applied. S_{La} is then switched off at t_7. During this interval, $C_{oss,SLa}$ is charged to V_{dc} and thus stores energy of E_{oss}. However, it should be noted that this energy of E_{oss} is not dissipated until next turn-on interval $[t_2, t_3]$ (see the light blue dashed line in Fig. 9(d)). During the whole interval $[t_6, t_7]$, the body diode of S_{Lb} conducts the negative circulating current i_{Lb}, and therefore, S_{Lb} has not truly turned off.

Stage 8 $[t_7, t_8]$ (see Figs. 8(a) and 9(i)): The output capacitors $C_{oss,SLa}$ and $C_{oss,SHa}$ are respectively fully charged and discharged at t_7, after which the body diode of S_{Ha} begins to conduct. Therefore, S_{Ha} is able to achieve the ZVS-on if the turn-on signal is applied subsequently. Meanwhile, the differential voltage v_{ab} is equal to V_{dc}, causing the circulating current i_{Lb} to linearly increase as

$$\begin{aligned} i_{Lb}(t) &= i_{Lb}(t_7) + \frac{V_{dc}}{L_a+L_b}(t-t_7) \\ &= i_{Lb}(t_7) + \frac{n_{ld}n_{lg}V_{dc}}{(n_{ld}+n_{lg})L_c}(t-t_7) \end{aligned} \tag{16}$$

From (16), we can obtain the time between t_7 and t_8 as

$$\begin{aligned} \Delta t_{78} = t_8 - t_7 &= \frac{i_{Lb}(t_7)}{V_{dc}} \frac{(n_{ld}+n_{lg})L_c}{n_{ld}n_{lg}} \\ &\approx -\frac{t_{sw,H}}{2} + \frac{I_{cir,pk}}{V_{dc}} \frac{(n_{ld}+n_{lg})L_c}{n_{ld}n_{lg}} \end{aligned} \tag{17}$$

Stage 9 $[t_8, t_9]$ (see Figs. 8(a) and 9(j)): At t_8, the circulating current i_{Lb} reaches 0, and thus, the output capacitors $C_{oss,Hb}$ and $C_{oss,Lb}$ begin transfer charge through the commutation inductors L_a and L_b under the excitation of V_{dc}, setting at t_9 with $C_{oss,Hb}$ discharged to 0 and $C_{oss,Lb}$ charged to V_{dc}. As

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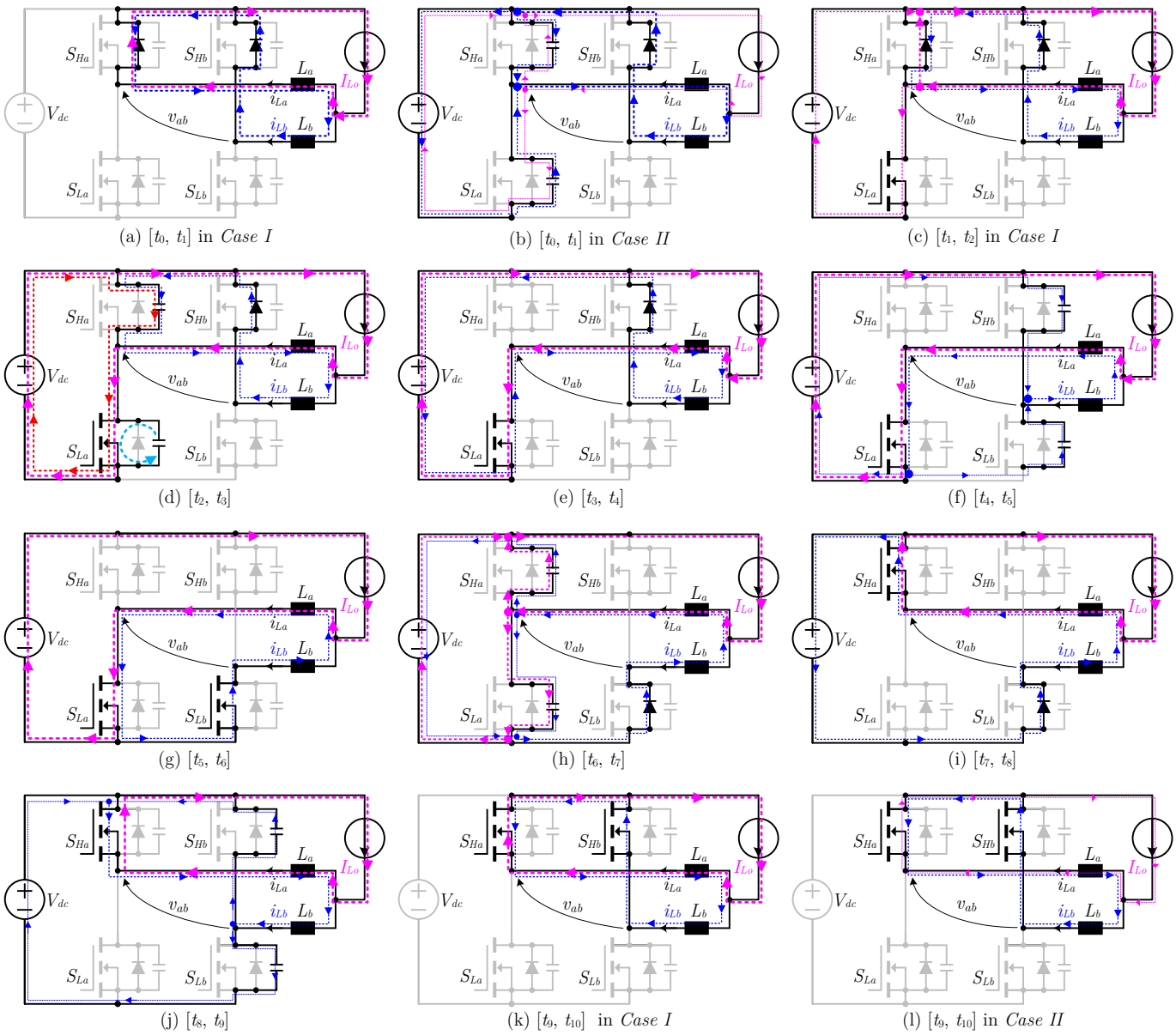

Fig. 9. Equivalent circuits of paralleled GaN HEMT half bridges operating (see Fig. 7(b)) in the asynchronous mode. The purple and blue loops represent the load current I_{Lo} and the circulating current i_{Lb}, respectively. The lumped inductors $L_a = L_c/n_{ld}$ and $L_b = L_c/n_{lg}$; the lumped output capacitors $C_{oss,SHa} = n_{ld}C_{oss}$, $C_{oss,SLa} = n_{ld}C_{oss}$, $C_{oss,SHb} = n_{lg}C_{oss}$, and $C_{oss,SLb} = n_{lg}C_{oss}$.

with the interval [t_4, t_5], neglecting the resistive energy loss during [t_8, t_9] yields

$$\frac{L_{DM}[(i_{Lb}(t_9))]^2}{2} = \frac{(n_{ld}+n_{lg})L_c}{n_{ld}n_{lg}}\frac{I_{cir,pk}^2}{2} = n_{lg}V_{dc}Q_{oss} \tag{18}$$

From (18), we have

$$i_{Lb}(t_9) = -i_{Lb}(t_5) = I_{cir,pk} = \sqrt{\frac{2n_{ld}n_{lg}^2V_{dc}Q_{oss}}{(n_{ld}+n_{lg})L_c}} \tag{19}$$

As with the interval [t_4, t_5], the time between t_8 and t_9 can be derived as

$$\Delta t_{89} = t_9 - t_8 = \frac{2n_{lg}Q_{oss}}{I_{cir,pk}} + \frac{n_{lg}Q_{oss}}{I_{cir,pk}} = \frac{3n_{lg}Q_{oss}}{I_{cir,pk}} \tag{20}$$

From (12),(15),(17) and (20), we have $\Delta t_{78} = \Delta t_{34}$ and $\Delta t_{89} = \Delta t_{45}$.

Stage 10 $[t_9, t_{10}]$ (see Figs. 8(a) and 9(k)): After t_9, the body diode of S_{Hb} conducts, and thus, S_{Hb} is able to achieve ZVS-on by being applied with a turn-on gate signal. During the interval $[t_9, t_{10}]$, the drain-source current of S_{Ha} is lower than the load current, i.e., $-i_{ds,SHa} = i_{La} = I_{Lo} - i_{Lb}$.

A brief summary of the asynchronous operation in *Case I* can be drawn, as follows:

- The leading lower switch S_{La} is hard switched-on at a current lower than the load current, i.e., at $I_{La,t0} = I_{Lo} - I_{cir,pk} > 0$;
- The lagging lower switch S_{Lb} is able to achieve the ZVS-on, and thus its switching loss can be eliminated compared with the synchronous operation.

2) Case II: $I_{La,t0} = I_{Lo} - I_{cir,pk} < 0$

As the load current I_{Lo} further decreases, the leading inductor current at t_0, $I_{La,t0}$, will become negative, i.e., $I_{La,t0} = I_{Lo} - I_{cir,pk} < 0$. This case is termed as *Case II* in which the operating process of the proposed paralleling structure is the same as that in *Case I* except for intervals [t_9, t_{10}] and [t_0, t_1], as shown in Figs. 8(b), 9(b) and 9(l).

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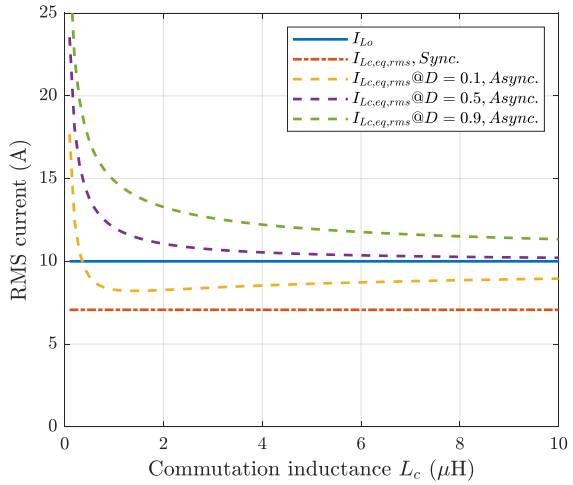

Fig. 10. Calculated RMS current of each commutation inductor with different inductances and duty cycles. The GS66508T GaN HEMT is selected, and its output charge Q_{oss} at $v_{ds} = 400$ V is 57 nC [5]. The number of HBs in parallel $N = 2$, the dc bus voltage $V_{dc} = 400$ V, the switching frequency $f_s = 200$ kHz, and the load current $I_{Lo} = 10$ A.

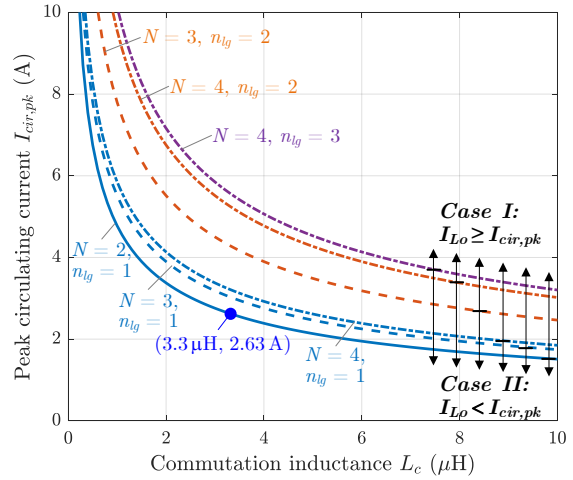

Fig. 11. Calculated peak circulating current $I_{cir,pk}$ (eq.(14)) with respect to the commutation inductance L_c at different numbers of devices in parallel N, and different numbers of lagging devices n_{lg}. The dc bus voltage $V_{dc} = 400$ V. The GS66508T GaN HEMT is selected, and its output charge Q_{oss} at $v_{ds} = 400$ V is 57 nC. The paralleled HB legs operate in *Case I* and *Case II* when the load current $I_{Lo} \geqslant I_{cir,pk}$ and $I_{Lo} < I_{cir,pk}$, respectively.

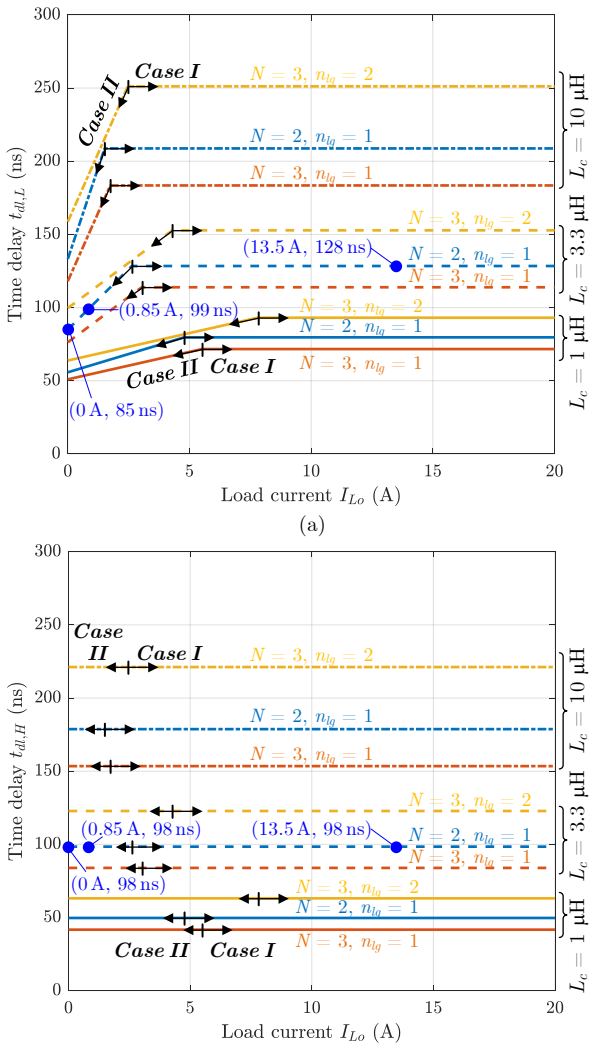

Fig. 12. Calculated time delays (a) $t_{dl,L}$ (eq.(28)) and (b) $t_{dl,H}$ (eq.(29)) with respect to the load current I_{Lo} at different commutation inductances L_c, numbers of devices in parallel N, and numbers of lagging devices n_{lg}. The dc bus voltage $V_{dc} = 400$ V, and the output charge $Q_{oss} = 57$ nC.

As with *Case I*, due to the delay between the leading and lagging legs and the commutation inductors L_a&L_b, a circulating current i_{Lb} with a peak value of $I_{cir,pk}$ (14) can be also generated in *Case II*. Thus, the lagging switches are able to achieve the ZVS-on, leading to minimized switching losses. For the turn-on of the leading switch S_{La}, the operating principle in *Case II* is different from that in *Case I*, as illustrated below.

Before t_0, the lagging upper switch S_{Hb} is reversely conducting due to the positive circulating current i_{Lb}. For the leading inductor current i_{La}, however, it is negative, i.e., $i_{La} = I_{Lo} - i_{Lb} < 0$, which means that a positive current $-i_{La}$ is flowing through the leading upper switch S_{Ha} during $[t_9, t_{10}]$, as shown in Fig. 9(l). At t_0, turn-off gate signals are applied to cut off the channels of S_{Ha} and S_{Hb}. Thus, the body diode of S_{Hb} is conducting during $[t_0, t_1]$. For the leading upper switch S_{Ha}, however, its channel current is diverted to the output capacitors $C_{oss,Ha}$ and $C_{oss,La}$, as shown in Fig. 9(b). That is, the two output capacitors $C_{oss,Ha}$ and $C_{oss,La}$ begin transferring charge through the commutation inductors L_a&L_b under the excitation of V_{dc}. During this interval $[t_0, t_1]$ in *Case II*, the inductor currents i_{La} and i_{Lb} decrease in magnitude; the drain-source voltages of the leading leg switches $v_{ds,SHa}$ and $v_{ds,SLa}$ rises and decreases, respectively. This interval terminates at t_1 when i_{La} reaches 0, i.e., $i_{La}(t_1) = I_{Lo} - i_{Lb}(t_1) = 0$.

If $v_{ds,SHa}$ increases to V_{dc} and $v_{ds,SLa}$ decreases to 0 at t_1, then the leading lower switch S_{La} is able to achieve the ZVS-on. If $v_{ds,SLa}$ decreases but not to 0 when i_{La} reaches 0, then S_{La} is only able to achieve the incomplete zero-voltage switching (iZVS) ON [54].

Assuming $v_{ds,SLa}$ decreases to 0 at t_1 when i_{La} reaches 0, then according to the law of conservation of energy, we have

$$V_{dc} n_{ld} Q_{oss} = \frac{1}{2} L_{DM} (I_{Lo} - I_{cir,pk})^2 \tag{21}$$

Substituting (14) into (21) yields the critical load current below which the leading lower switch S_{La} can achieve the

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ZVS-on, i.e.,

$$\begin{aligned} I_{Lo,cri} &= I_{cir,pk} - \sqrt{\frac{2V_{dc}n_{ld}Q_{oss}}{L_{DM}}} \\ &= \sqrt{\frac{2n_{ld}n_{lg}^2V_{dc}Q_{oss}}{(n_{ld}+n_{lg})L_c}} - \sqrt{\frac{2V_{dc}n_{ld}^2n_{lg}Q_{oss}}{(n_{ld}+n_{lg})L_c}} \\ &= \left(\sqrt{n_{lg}} - \sqrt{n_{ld}}\right)\sqrt{\frac{2n_{ld}n_{lg}V_{dc}Q_{oss}}{(n_{ld}+n_{lg})L_c}} \end{aligned} \tag{22}$$

Based on (22), we can conclude:

- In the scenario of $n_{lg} \geqslant n_{ld}$, the critical load current $I_{Lo,cri} \geqslant 0$. It implies that switch S_{La} is able to achieve the ZVS-on when the load current satisfies $0 \leqslant I_{Lo} \leqslant I_{Lo,cri}$, and achieve the iZVS-on [54] when $I_{Lo,cri} < I_{Lo} < I_{cir,pk}$.
- If $n_{lg} < n_{ld}$, then $I_{Lo,cri} < 0$. It means that switch S_{La} is not able to achieve the ZVS-on under the condition of $I_{Lo} \geqslant 0$; however, it still can achieve the iZVS-on when $0 \leqslant I_{Lo} < I_{cir,pk}$.

In *Case II*, the time durations Δt_{45}, Δt_{78}, and Δt_{89} still follow (15), (17), and (20), respectively. For Δt_{34}, however, it has different expressions in both cases. In *Case II*, Δt_{34} becomes load-current-dependent and it follows

$$\Delta t_{34} = \frac{I_{Lo}}{V_{dc}}\frac{(n_{ld}+n_{lg})L_c}{n_{ld}n_{lg}} \tag{23}$$

In both *Case I* and *Case II*, the peak circulating current $I_{cir,pk}$ can be expressed by (14). Fig. 11 shows the curves of the peak circulating current $I_{cir,pk}$ with respect to the commutation inductance L_c at different numbers of paralleled devices N and different numbers of lagging devices n_{lg}. As can be seen from (14) and Fig. 11, the peak circulating current $I_{cir,pk}$ is independent of the load current I_{Lo}. Instead, it is determined by the commutation inductance L_c, the number of devices in parallel N, and the number of lagging devices n_{lg}. The more devices in parallel and the more lagging devices, the higher the peak circulating current. Moreover, it is seen that $I_{cir,pk}$ decreases with the increase of L_c; thus, the region of operating in *Case II* ($I_{Lo} < I_{cir,pk}$) becomes smaller.

C. Comparison Between Synchronous and Asynchronous Modes

1) Soft-Switching

As analyzed in Section III, when the load current I_{Lo} is positive, all the high-side switches S_{Hn} can achieve the ZVS-on in both the synchronous and asynchronous modes. For the low-side switches, i.e., the DUTs, they can be turned on under soft or hard conditions depending on the operation modes and cases, as summarized in Table I. Specifically, in the synchronous mode, all the DUTs are hard switched; in the asynchronous mode, the leading DUT S_{La} is turned on under HS and iZVS in *Case I* and *Case II*, respectively. By contrast, the lagging DUT S_{Lb} always achieves the ZVS in the asynchronous mode. Compared with the synchronous operation, the asynchronous mode leads to a reduced number of hard-switched GaN HEMTs, and therefore, it enables to decrease the switching loss.

It is noted that when the direction of the load current is reversed, i.e., $I_{Lo} < 0$, the soft-switching conditions of S_{Ha}&S_{Hb} and S_{La}&S_{Lb} will be swapped.

TABLE I
SOFT-SWITCHING OF SWITCHES IN DIFFERENT OPERATION MODES

Modes and Cases		DUTs S_{La}	DUTs S_{Lb}	S_{Ha}	S_{Hb}
Synchronous mode		HS	HS	ZVS	ZVS
Asynchronous mode	*Case I*	HS	ZVS	ZVS	ZVS
	Case II	iZVS	ZVS	ZVS	ZVS

2) dv/dt of Common-Mode Voltage v_O

As mentioned in Section II-B, the commutation inductance L_c is negligible compared with the output filter inductance L_o, i.e., $L_c \ll L_o$, the output (common-mode) voltage of the N paralleled HBs (see Figs. 2(b), 4 and 7) is the average of the N midpoint voltages, i.e.,

$$v_O = \frac{1}{N}\sum_{n=1}^{N} v_n \tag{24}$$

The waveforms of v_O in the synchronous and asynchronous modes are shown in Figs. 3 and 8, respectively. In the synchronous mode, the common-mode voltage v_O is identical to the drain-source voltage of the low-side switches. The high-side switches achieve the ZVS-on, leading to a slow rise time ($[t_4, t_5]$) for $v_{ds,SLn}$. Therefore, the maximum dv/dt of v_O in the synchronous mode is determined by the hard-switching-on of the low-side switches, i.e., during $[t_2, t_3]$ in Fig. 3.

In the asynchronous mode, the common-mode voltage v_O is the average of $v_{ds,SLa}$ and $v_{ds,SLb}$ which, however, are not in phase with each other. As a result, the edges of v_O are expanded to three or four intervals, i.e., $[t_2, t_3]$ ($[t_0, t_2]$ and $[t_2, t_3]$ in *Case II*), $[t_3, t_4]$ and $[t_4, t_5]$ for the falling edge, and $[t_6, t_7]$, $[t_7, t_8]$ and $[t_8, t_9]$ for the rising edge, as shown in Fig. 8. The maximum dv/dt of v_O in this mode is determined by the hard-switching interval $[t_2, t_3]$ during which the leading low-side switch S_{La} is being hard turned on, but the lagging low-side switch S_{Lb} is kept off. Thus, the dv/dt of v_O during $[t_2, t_3]$ is halved compared with the synchronous mode. During other switching intervals, i.e., $[t_0, t_1]$ (*Case II*), $[t_4, t_5]$, $[t_6, t_7]$ and $[t_8, t_9]$, it still holds true that only one of the two lumped HBs (see Figs. 7(b) and 8) is being turn-on under ZVS. Hence, the dv/dt of v_O in these switching intervals can be significantly reduced, leading to alleviated electromagnetic interference (EMI).

3) RMS Current and Peak-to-Peak Magnetic Flux Density of Commutation Inductors

i) Root-Mean-Square (RMS) Current:

The RMS currents of commutation inductors in the synchronous and asynchronous modes are obtained and shown in (31)-(33) in the Appendix. Fig. 10 shows the calculated RMS currents of commutation inductors with respect to the duty cycle and commutation inductance in both the synchronous and asynchronous modes. It is seen that the RMS current in the asynchronous mode is always higher than that in the asynchronous mode. This means that the proposed asynchronous operation results in higher conduction loss than the synchronous mode.

ii) Peak-to-Peak Magnetic Flux Density ΔB:

When operating in the asynchronous mode, the current ripple of commutation inductors can be approximated as $2I_{cir,pk}$, as shown in Fig. 8. The resulting peak-to-peak magnetic flux density of commutation inductors can be obtained as

$$\Delta B = L_c \frac{2I_{cir,pk}}{n_t A_e} \tag{25}$$

where n_t and A_e represent the number of turns and the effective cross-sectional area of a commutation inductor, respectively.

Substituting (14) to (25) yields

$$\Delta B = 2\sqrt{\frac{\mu_r \mu_0}{V_e}} \sqrt{\frac{2n_{ld} n_{lg}^2 V_{dc} Q_{oss}}{n_{ld} + n_{lg}}} \tag{26}$$

where the constant μ_0 is the permeability of free space, μ_r represents the relative permeability of the used magnetic core material, and V_e denotes the effective magnetic core volume of a commutation inductor. It is seen that the flux density swing ΔB is proportional to the square root of the relative permeability μ_r. According to Steinmetz's equation, the magnetic core loss is positively related to ΔB [55]. Therefore, from the perspective of core loss reduction, low-permeability core materials should be used and/or air gaps should be inserted.

When operating in the synchronous mode, the current ripple of commutation inductors is determined by the load current, i.e., $\Delta I_{Lc} = \Delta I_{Lo}/N$, which is relatively small. Therefore, the magnetic flux density fluctuation ΔB ($\Delta B = \frac{L_c \Delta I_{Lo}}{N n_t A_e}$) is also low, leading to low core loss. Nevertheless, the synchronous mode is activated when the load current is high, and this means that the commutation inductors need to withstand a DC current of I_{Lo}/N. To avoid magnetic saturation in the synchronous mode, it is also desired to use low-permeability core material or insert an air gap.

It is noted that the commutation inductors can be inversely-coupled to increase the differential-mode inductance, decrease the common-mode inductance, and lower the core loss in the synchronous mode.

IV. Design Guidelines and Thermal Balancing Scheme of Proposed Paralleling Structure

A. Design Guidelines

1) Number of GaN HEMT HB Legs in Parallel N

As aforementioned, the synchronous and asynchronous modes are selected at heavy and light loads, respectively. The number of paralleled GaN HEMTs, N, should be determined based on the maximum power loss and highest junction temperature of devices at the rated full power in the synchronous mode.

2) Commutation Inductors

i) Commutation Inductance L_c:

In the synchronous mode, the commutation inductors $L_1, L_2, ..., L_N$ (see Fig. 2(b)) are able to help the paralleled devices achieve better dynamic current sharing under parameter mismatches of HEMTs. The maximum inductor or HEMT current imbalance $\Delta I_{L,max}$ is a function of the dc voltage V_{dc}, the maximum gating time delay $\Delta\tau$ and the commutation inductance (8). The higher the commutation inductance, the smaller the current imbalance. When operating in the asynchronous mode, a higher L_c results in a lower circulating current peak $I_{cir,pk}$ (see (14) and Fig. 11), which is beneficial to the conduction loss reduction.

On the other hand, a higher commutation inductance results in higher inductor volume. Therefore, a trade-off among dynamic current sharing, conduction loss and inductor size should be made when selecting L_c.

ii) Bandwidth Requirement:

Bandwidth 1 $BW_{Lc,1}$: Neglecting the short turn-on and turn-off times of GaN HEMTs, the maximum rise and fall times of the commutation inductor currents are equal to the time delays $t_{dl,L}$ and $t_{dl,H}$ which depend on multiple parameters, as shown in Fig. 12. When the commutation inductance $L_c \geq 1\mu$H, the rise and fall times of i_{La} and i_{Lb} are above 50 ns which correspond to a bandwidth of $BW_{Lc,1} = \frac{0.35}{t_r} = 7$ MHz [58]. This means that in order to implement the proposed asynchronous operation, the commutation inductors need to maintain the desired inductance L_c at 7 MHz or above.

Bandwidth 2 $BW_{Lc,2}$: As mentioned in Section III-A, the commutation inductors are used also to alleviate the current imbalance between the paralleled HBs in the synchronous mode. The current mismatch is caused by the differential-mode voltage $v_{ab} = v_a - v_b$ whose bandwidth is not higher than that of v_a (i.e., $v_{ds,SLa}$) or v_b (i.e., $v_{ds,SLb}$). Therefore, the rise or fall times of $v_{ds,SLa}$ and $v_{ds,SLb}$ can be used to calculate the maximum bandwidth of the commutation inductors required to alleviate current imbalance in (8). Assume that the rise time of drain-source voltage of a 650-V GaN HEMT with a 400-V dc bus voltage is 10 ns, then the corresponding bandwidth $BW_{Lc,2} = \frac{0.35}{10\text{ ns}} = 35$ MHz.

If the maximum delay between the midpoint voltages is 5 ns, and the allowed maximum current imbalance is 1 A, then based on (8), the required commutation inductance at 35 MHz is

$$L_{c@35\text{MHz}} = \frac{400\text{ V} \times 5\text{ ns}}{1\text{ A}} = 2\ \mu\text{H} \tag{27}$$

Therefore, the commutation inductors are required to maintain an inductance of L_c (e.g., 3.3 μH) at $BW_{Lc,1}$, and also have an inductance over $L_{c@35\text{MHz}} = 2\,\mu$H at $BW_{Lc,2}$.

iii) Core Material Selection:

As discussed above, the required maximum bandwidth of commutation inductors is determined by $BW_{Lc,2}$ which can be as high as 35 MHz for paralleling the GS66508T GaN HEMTs. To have a desired inductance at 35 MHz, the relative permeability of used magnetic cores should be high (e.g., $>$ 50 [31]) so that the inductor size can be reduced.

In the meanwhile, it is seen from Figs. 3 and 8 that the commutation inductors are excited at the switching frequency f_s; thea core loss is generated at f_s as well. Therefore, the selected core material should also feature low core loss at the switching frequency f_s. If the switching frequency $f_s \geq 50$ kHz, then high-frequency Mn-Zn Ferrite materials can be selected due to their low cost and low power loss density over other materials, e.g., iron powder, nanocrystalline, and amorphous [59].

3) Time Delays $t_{dl,L}$&$t_{dl,H}$ in Asynchronous Mode

As seen in Fig. 8, in the asynchronous mode, the turn-on instants of the lagging leg switches S_{Hb}&S_{Lb} are delayed by $t_{dl,L}$&$t_{dl,H}$ with respect to the leading leg S_{Ha}&S_{La}. Based on the analysis in Section III-B, we can obtain the time delays

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TABLE II
COMPARISON BETWEEN THE PROPOSED DESYNCHRONIZABLE PARALLELING SCHEME AND THE CCM/TCM MULTIPHASE INTERLEAVING TECHNIQUES

	CCM multiphase interleaving [35], [56], [57]	**TCM multiphase interleaving [43]–[45]**	**Proposed desynchronizable paralleling scheme**
Phase shift	Switching frequency dependent $\frac{1}{Nf_s}$	Switching frequency dependent $\frac{1}{Nf_s}$	Independent of switching frequency *Synchronous mode*: 0 *Asynchronous mode*: Eqs.(28) and (29) (cf. Fig. 12)
Switching frequency	Fixed or variable	Variable High switching frequency at light loads	Flexible: fixed or variable
Required inductance	Large Switching frequency dependent e.g., 1.6 mH × 2, f_s = 65 kHz, P_{max} = 600 W [56] 3.32 mH × 6, f_s = 10 kHz, P_{max} = 4 kW [57] 1.16 mH × 2, f_s = 3.6 kHz, P_{max} = 260 kW [35]	Medium Switching frequency dependent e.g., 150 μH × 3, f_s = 100-470 kHz, P_{max} = 400 W [43] 180 μH × 3, f_s = 30-130 kHz, P_{max} = 1 kW [44] 430 μH × 3, f_s = 6-25 kHz, P_{max}= 20 kW [45]	Small Independent of switching frequency e.g., 3.3 μH × 2 in this paper Note: the external filter inductance depends on application
Integration difficulty of inductors with switches	High due to large inductance	High due to large inductance	Low due to small inductance
Generality	Low The interleaved inductors interact with the output filter	Low The interleaved inductors interact with the output filter	High The commutation inductors have a low impact on the output filter
Steady-state current imbalance among inductors	High	Medium	Low (the synchronous mode is activated at heavy loads)
Inductor current sensor and current balancing scheme	Needed	Needed	Not needed
Implementation complexity	Low	High • High-speed zero current detection (ZCD) needed • Accurate timing for ZVS realization	Low A look-up table needed to select the asynchronous or synchronous mode
RMS current at full load	Low	High	Low (the synchronous mode is activated at heavy loads)
Soft-switching in Boost mode	• *High-side switches*: ZVS • *Low-side switches*: HS	• *High-side switches*: ZVS • *Low-side switches*: ZVS	• *High-side switches*: ZVS • *Low-side switches*: ○ Asynchronous mode Leading switches: HS or iZVS Lagging switches: ZVS ○ Synchronous mode: HS

as

$$t_{dl,L} = t_{sw,L} + \Delta t_{34} + \Delta t_{45} = t_{sw,L} + \begin{cases} 5\sqrt{\frac{NQ_{oss}L_c}{2(N-n_{lg})V_{dc}}}, & Case\ I \\ 3\sqrt{\frac{NQ_{oss}L_c}{2(N-n_{lg})V_{dc}}} + \frac{I_{Lo}NL_c}{n_{lg}(N-n_{lg})V_{dc}}, & Case\ II \end{cases} \quad (28)$$

$$t_{dl,H} = \Delta t_{78} + \Delta t_{89} = -\frac{t_{sw,H}}{2} + 5\sqrt{\frac{NQ_{oss}L_c}{2(N-n_{lg})V_{dc}}} \quad (29)$$

where the switching times of S_{La} and S_{Ha}, i.e., $t_{sw,L}$ and $t_{sw,H}$, depend on many factors, e.g., the gate resistance, turn-on current, number of HEMTs turned on n_{ld}. Nevertheless, the turn-on time of a 650-V GS66508/16 GaN HEMT is normally less than 10-20 ns [5], [50], [51], [60] which is short compared to the other times Δt_{34}, Δt_{45}, Δt_{78}, and Δt_{89}. Therefore, in practice, a conservative fixed value, e.g., 20 ns, can be assigned to $t_{sw,L}$ and $t_{sw,H}$.

Fig. 12 shows the calculated theoretical time delays $t_{dl,L}$ and $t_{dl,H}$ with respect to multiple parameters, i.e., the load current I_{Lo}, the commutation inductance L_c, the number of devices in parallel N, and the number of lagging devices n_{lg}. As one can see, both time delays $t_{dl,L}$ and $t_{dl,H}$ are affected by the three parameters L_c, N, and n_{lg}. For the load current I_{Lo}, however, it has different impacts on the time delays $t_{dl,L}$ and $t_{dl,H}$ in *Case I* and *Case II* of the asynchronous mode. Specifically, in *Case I*, the load current I_{Lo} has no impact on both time delays $t_{dl,L}$ and $t_{dl,H}$. In *Case II*, I_{Lo} still does not affect $t_{dl,H}$, but influences $t_{dl,L}$; the time delay $t_{dl,L}$ linearly falls with the decrease of I_{Lo}.

The proposed desynchronizable control scheme can be applied to any converter topologies consisting of multiple paralleled HBs. The implementation diagram is shown in Fig. 13(a). In addition to the main control and modulation blocks of a specific converter, this desynchronizable paralleling scheme also requires blocks to select the operation mode and to determine the time delays based on the dc-bus voltage V_{dc} and the load current I_{Lo}. Specifically, the efficiency performance of the converter should be evaluated or tested in the synchronous and asynchronous modes, leading to a lookup table (LUT) for selecting an efficiency optimal mode. Then, (28) and (29) can be used to calculate or look up the time delays for the lagging low-side and high-side switches, respectively. Furthermore, the leading and lagging legs are swapped with each other in order to achieve balanced thermal performance, as detailed below.

B. Thermal Balancing Scheme for Paralleled GaN HEMTs

As aforementioned in Section III-A, the added commutation inductors enable the paralleled HEMTs to have a better current sharing capability in the synchronous mode; thus, the power losses and thermal stresses of the paralleled devices can be balanced as well.

When operating in the asynchronous mode, however, the leading and lagging legs do not share the same thermal stress because they have different power losses. The lagging lower

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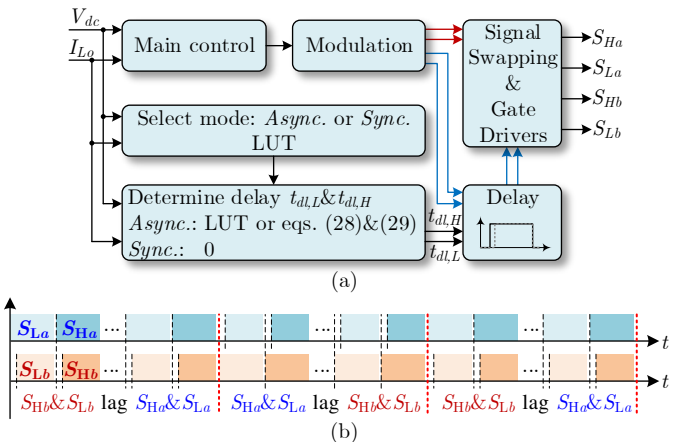

Fig. 13. (a) Block diagram of implementation of the proposed desynchronizable control scheme. (b) Gate signals of the paralleled GaN HEMT legs with an alternating delay scheme to balance the thermal stress between the paralleled legs.

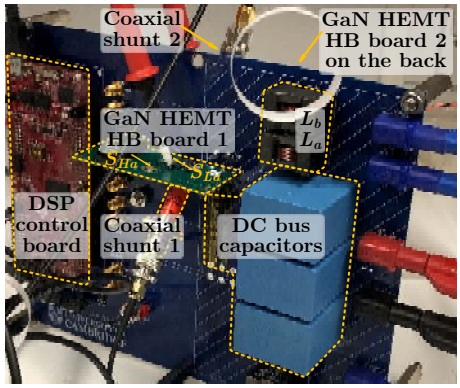

Fig. 14. Photo of the developed multi-pulse tester of two parallel-connected half bridges with GaN Systems™ GS66508T HEMTs. The test bench employs a high bandwidth oscilloscope (MSO64/Tektronix, 1 GHz) to process and display the measured data. High bandwidth current shunts (SDN-414-10/T&M Research, 2 GHz) are used to measure the drain-source currents by means of coaxial cables whereas the drain-source voltages are measured with high-voltage passive probes (PHV 1000/PMK, 400 MHz).

HEMT achieves the ZVS-on and conducts the small circulating current, whereas the leading counterpart is hard-switched and meanwhile, has a higher RMS current. Therefore, the leading device suffers from a severer thermal stress. In order to achieve a balanced thermal stress between the leading and lagging DUTs, an alternating delay scheme is proposed for the paralleling structure operating in the asynchronous mode, as shown in Fig. 13(a) and (b). One of the two legs S_{La}&S_{Ha} and S_{Lb}&S_{Hb} lags the other alternately. Thus, both legs generate the same power loss and are able to share the same junction temperature under the premise of having the identical thermal resistance.

C. Comparison With CCM/TCM Multiphase Interleaving

A comparison between the proposed desynchronizable paralleling scheme and the continuous-conduction-mode (CCM)/TCM multiphase interleaving techniques is shown in Table II. In the multiphase interleaving techniques, the phase shift is equal to $\frac{1}{Nf_s}$ which is switching frequency dependent, and is much larger than the small delay (e.g., 98 ns in Fig. 12) required by the proposed paralleling scheme. Therefore, both the CCM and TCM multiphase interleaving techniques need high inductance in order to limit the circulating current among phases. The large inductance significantly increases the difficulty for the inductors to be integrated with power switches in modules. By contrast, the small inductance in the proposed scheme has a low impact on the output filter, which implies that this scheme is of higher generality, and the commutation inductors can be potentially integrated in a power module.

Steady-state current imbalance among the multiphase inductors is inevitable due to small mismatches in the timing of switching signals, differing switching characteristics of semiconductor devices, and unequal inductor impedances [35], [47], [61]. Therefore, current balancing schemes are required in the CCM and TCM multiphase interleaved converters [35], [45], [62]. Although all the switches can achieve the ZVS in TCM converters, they have to suffer from high RMS currents, high conduction loss and high magnetic loss at high currents. Therefore, this technique is seldom used in applications over 50 kW. Another issue with the TCM multiphase interleaving is its high implementation complexity owing to the requirements of high-speed zero current detection (ZCD) circuit and accurate timing for ZVS [30], [46], [47]. By comparison, it is relatively easier for the CCM multiphase interleaving and the proposed desynchronizable paralleling scheme to be implemented.

When operating at light loads, phase-shedding can be applied to CCM multiphase interleaved converters [21]; some phases are shut down, and thus, only part of the switches are hard-switched at the load current, leading to reduced switching loss. By contrast, the proposed asynchronous control scheme enables the remaining switches to turn on at a current lower than the load or even to achieve the iZVS; therefore, the switching loss can be further reduced with the proposed asynchronous control, as shown in Fig. 17.

TABLE III
PARAMETERS OF OSCILLOSCOPE AND PROBES USED IN TESTS

Description	Type	Bandwidth
Oscilloscope	Tektronix MSO64	1 GHz
1-kV voltage probe for V_{ds}	PMK PHV 1000	400 MHz
300-V voltage probe for V_{gs}	Tektronix TPP1000	1 GHz
Coaxial shunt for I_{ds}	T&M SDN-414-10	2 GHz
Current probe for inductor currents	Agilent N2783B	100 MHz

V. EXPERIMENTAL VALIDATION

To verify the advantages of the proposed desynchronized paralleling scheme on the light-load switching loss reduction, multi-pulse tests and continuous Boost dc-dc operation of two parallel-connected GS66508T GaN HEMT HB legs (i.e., $N = 2$) are conducted.

A. Multi-Pulse Tests

A multi-pulse tester of two parallel-connected half bridges has been developed based on GaN Systems™ GS66508T HEMTs, as shown in Fig. 14. The commutation inductors L_1 and L_2 (see Figs. 7(b) and 14) are implemented with Coilcraft VER2923-332KL (3.3 μH) devices. Each HEMT has an independent gate driver, and thus, this tester allows for the operation of either a single HB or two parallel-connected HBs. Also, both the synchronous and asynchronous modes are achieved with the TMS320F28379D digital signal processor

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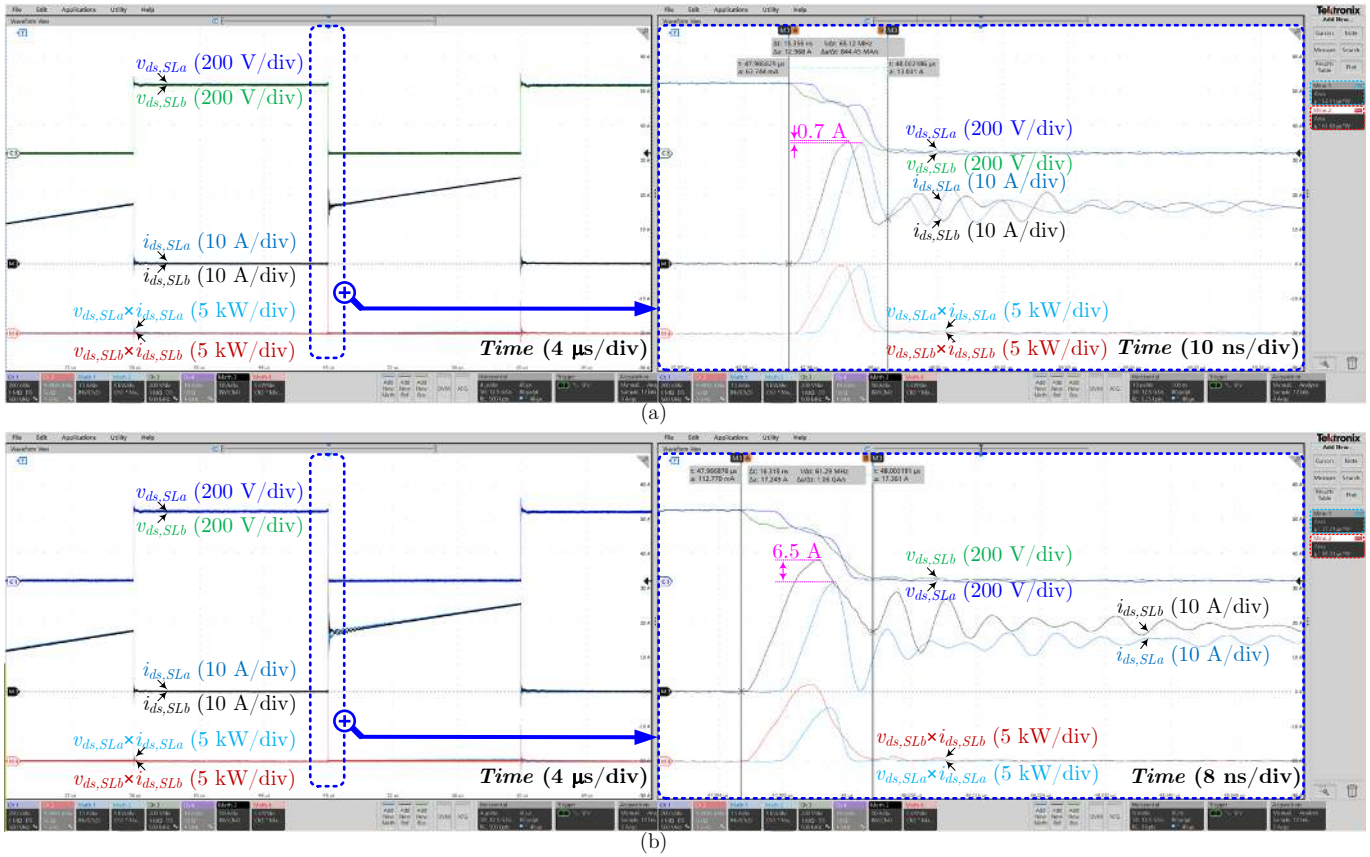

Fig. 15. Tested current balancing performance of two parallel-connected GS66508T GaN HEMT HB legs (a) with and (b) without commutation inductors. The dc bus voltage $V_{dc} = 400$ V, and the turn-on of S_{Lb} is leading that of S_{La} by 3.5 ns that is caused by the mismatches of gate driver propagation delay, threshold voltage, transconductance, loop inductance, and etc.

(DSP) control board. For high accuracy, a 1-GHz oscilloscope and 400-MHz deskewed voltage probes were used in tests along with 0.1-Ω coaxial current shunts, as shown in Table III.

The experimental waveforms of the two paralleled GaN HEMT HB legs with commutation inductors (see Fig. 7(b)) in the synchronous mode are shown in Fig. 15(a). Theoretically, the paralleled devices behave simultaneously. In practice, however, a 3.5-ns delay occurs at the turn-on instants of the HEMTs due to the aforementioned mismatches. With the help of the added commutation inductors, the turn-on current peaks and turn-on energy losses of the HEMTs are close with each other. From Fig. 15(a), it is seen that the peak current and turn-on energy loss differences are 0.7 A and $61.63\,\mu\text{J} - 52.11\,\mu\text{J} = 9.52\,\mu\text{J}$, respectively. These differences represent small percentages of the load current and the total turn-on energy loss, i.e., $\frac{0.7\,\text{A}}{34\,\text{A}} = 2\%$ and $\frac{9.52\,\mu\text{J}}{(52.11+61.63)\,\mu\text{J}} = 8.36\%$, respectively. By contrast, in the case of direct parallel of GaN HEMTs (i.e., without the commutation inductors added), significant current imbalance ($\frac{6.5\,\text{A}}{34\,\text{A}} = 19.1\%$) and turn-on energy loss difference ($\frac{(85.31-37.21)\,\mu\text{J}}{(85.31+37.21)\,\mu\text{J}} = 39.3\%$) will occur, as shown in Fig. Fig. 15(b).

The experimental waveforms of the paralleled GaN HEMTs in the asynchronous mode at $V_{dc} = 400$ V are shown in Fig. 16. It is seen that S_{Lb} is controlled to lag S_{La} at their turn-on instants. As a result, a circulating current i_{Lb} of 2.8-A peak value is generated in L_b. Given the number of paralleled GaN HEMTs N, the dc-link voltage V_{dc}, the commutation inductance L_c, and the C_{oss} characteristics of GS66508T [5], we can obtain the theoretical peak circulating current based on (14), i.e.,

$$\begin{aligned} I_{cir,pk} &= \sqrt{\frac{2n_{ld}n_{lg}^2 V_{dc} Q_{oss}}{(n_{ld}+n_{lg})L_c}} \\ &= \sqrt{\frac{2\times1\times1^2\times400\times57\times10^{-9}}{(1+1)\times3.3\times10^{-6}}} \\ &= 2.63\ \text{A} \end{aligned} \tag{30}$$

The error between the measured and the calculated peak circulating current values, i.e., 2.8 A −2.63 A = 0.17 A, is mainly caused by the parasitic capacitance of PCB and load inductor.

With the help of the circulating current i_{Lb}, the lagging switch S_{Lb} is able to achieve the ZVS-on and ZVS-off, leading to minimized switching losses. For the leading switch S_{La}, in *Case I* (see Fig. 16(a)), it still turns on under the hard switching, but the switching current is equal to $i_{La} = I_{Lo} - i_{Lb}$ which is lower than the load current I_{Lo}. Hence, the total turn-on energy loss of $S_{La}\&S_{Lb}$ in the asynchronous mode is smaller than a single HEMT at the same load current I_{Lo} (see Fig. 17).

When the load current I_{Lo} is lower than the peak circulating current $I_{cir,pk}$, the operation of the desynchronized paralleled GaN HEMT legs enters *Case II*, as shown in Fig. 16(b). In addition to that the lagging switch S_{Lb} achieves the ZVS-on and ZVS-off, the leading switch S_{La} is able to achieve the incomplete ZVS [54], resulting in decreased switching losses. It is obtained from (22) that the critical load current $I_{Lo,cri} = 0$, which implies that the leading switch can achieve the complete ZVS when the load current I_{Lo} decreases to 0.

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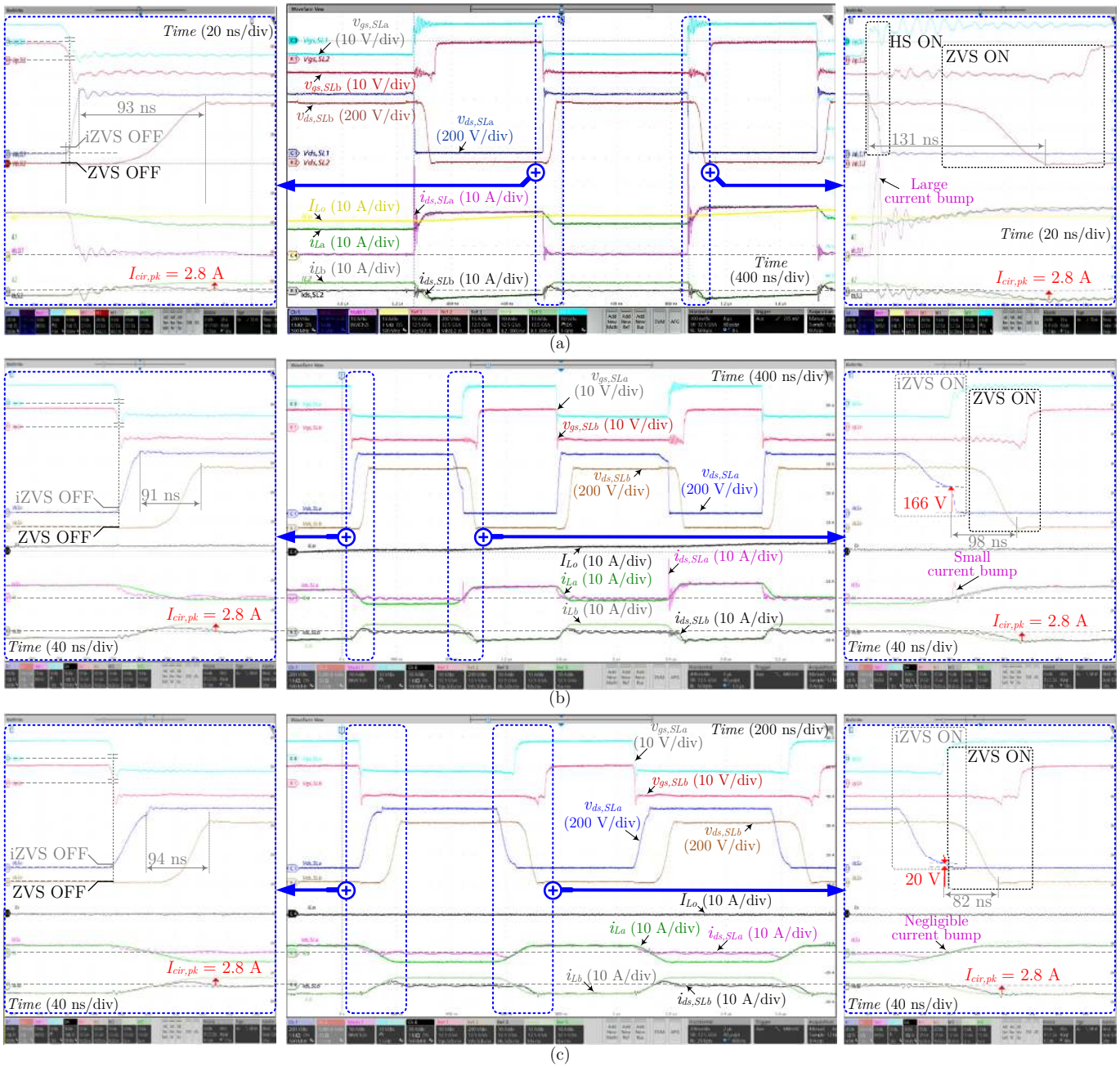

Fig. 16. Experimental waveforms of the two parallel-connected GS66508T GaN HEMT HB legs in different cases in the asynchronous mode. The dc bus voltage $V_{dc} = 400$ V. (a) *Case I*: $I_{Lo} = 11.5 \rightarrow 15.5$ A; (b) *Case II*: $I_{Lo} = 0 \rightarrow 2.5$ A; (c) *Case II* at zero load current: $I_{Lo} = 0$ A.

Fig. 16(c) shows the experimental results at $I_{Lo} = 0$ A. As one can see, the drain-source voltage of the leading switch, i.e., $v_{ds,SLa}$, has decreased from 400 V to 20 V (5% of 400 V) when its gate-source voltage $v_{gs,SLa}$ rises, leading to negligible turn-on current bump and energy loss (see Fig. 17).

The measured time delays $t_{dl,L}$ and $t_{dl,H}$ in the three operating scenarios in Fig. 16 are $t_{dl,L} = 131$ ns @$I_{Lo} = 13.5$ A, $t_{dl,L} = 98$ ns @$I_{Lo} = 0.85$ A, $t_{dl,L} = 82$ ns @$I_{Lo} = 0$ A, $t_{dl,H} = 93$ ns @$I_{Lo} = 13.5$ A, $t_{dl,H} = 91$ ns @$I_{Lo} = 0.85$ A, and $t_{dl,H} = 94$ ns @$I_{Lo} = 0$ A. The corresponding theoretical time delays in Fig. 12 are 128 ns, 99 ns, 85 ns, 98 ns, 98 ns, and 98 ns, respectively. The corresponding errors between the measured and calculated time delays are -3 ns (2.3%), 1 ns (1%), 3 ns (3.5%), 5 ns (5.1%), 7 ns (7.1%), 4 ns (4.1%), which are small. Therefore, the developed time delay models (28) and (29) are accurate.

The measured turn-on and turn-off energy losses of a single GaN HEMT and two paralleled HEMTs in the synchronous and asynchronous modes are shown Fig. 17(a). At high load currents, the synchronous operation of two parallel GaN HEMTs enables lower turn-on energy losses due to the reduced current stress on each HEMT. However, as the current decreases, the total turn-on energy loss in the asynchronous mode becomes smaller than that in the synchronous mode.

When the load current is smaller than the peak circulating current 2.8 A, the asynchronous operation enables a more significant switching loss reduction than the synchronous operation because S_{Lb} and S_{La} achieve the ZVS and the incomplete ZVS, respectively.

Fig. 17(b) shows the total switching energy losses E_{sw}. It can be seen that the switching loss reduction brought by

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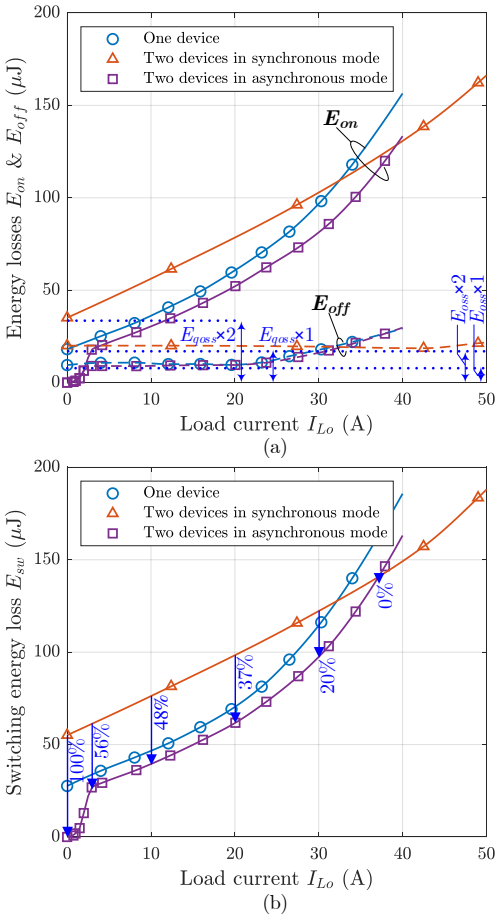

Fig. 17. Measured switching energy losses of GS66508T GaN HEMTs with different paralleling numbers and techniques. The dc bus voltage $V_{dc} = 400V$ and the ambient temperature is 25°C. The turn-on and -off gate resistances are $R_{g,on} = 10\ \Omega$ and $R_{g,off} = 2\ \Omega$, respectively. (a) Turn-on and turn-off energy losses; (b) Switching energy loss $E_{sw} = E_{on} + E_{off}$.

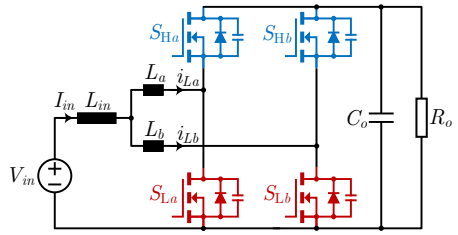

Fig. 18. Diagram of a Boost dc-dc converter where two GaN HEMT HB legs are connected with small (3.3-μH) commutation inductors L_a and L_b. The input Boost inductance $L_{in} = 235\,\mu$H.

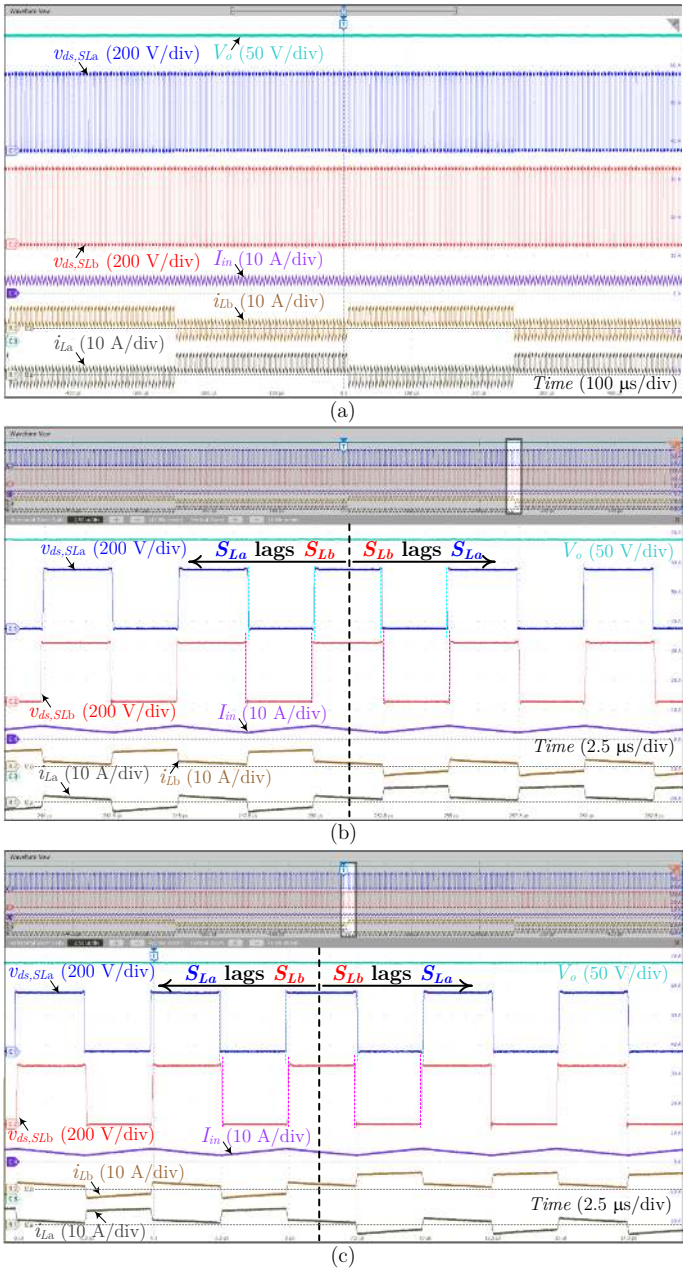

Fig. 19. Experimental waveforms of the Boost converter (see Fig. 18) operating in the alternating (thermal balancing, see Fig. 13) asynchronous mode. The input Boost inductor $L_{in} = 235\mu$H, the switches $S_{Ha}, S_{Hb}, S_{La}, S_{Lb}$ are implemented with GS66508T GaN HEMTs, the switching frequency $f_s = 200$ kHz, the input voltage $V_{in} = 200$ V, the output voltage $V_o = 400$ V, and the output power $P_o = 750$ W. (a) Voltage and current waveforms over 1 ms: the two HB legs $S_{Ha}\&S_{La}$ and $S_{Hb}\&S_{Lb}$ are altering their turn-on delays every 50 switching cycles (250 μs). (b) Transition from $S_{Ha}\&S_{La}$ lagging $S_{Hb}\&S_{Lb}$ to $S_{Hb}\&S_{Lb}$ lagging $S_{Ha}\&S_{La}$. (c) Transition from $S_{Hb}\&S_{Lb}$ lagging $S_{Ha}\&S_{La}$ to $S_{Ha}\&S_{La}$ lagging $S_{Hb}\&S_{Lb}$.

the asynchronous operation becomes more pronounced as the load current I_{Lo} decreases. The experimental results agree well with the theoretical analysis in Section III.

B. Continuous Boost DC-DC Operation

The multi-pulse tester (see Figs. 7(b) and 14) can be reconfigured as a Boost converter, as shown in Fig. 18. The input Boost inductance $L_{in} = 235\,\mu$H whereas the commutation inductance $L_c = 3.3\,\mu\text{H} = 1.4\% \times 235\,\mu\text{H}$ is much smaller. Fig. 19 shows the experimental waveforms of the Boost converter when applying the proposed thermal balancing scheme (see Fig. 13(b)) to the parallel-connected GaN HEMT HB legs. As can be seen, the two legs $S_{Ha}\&S_{La}$ and $S_{Hb}\&S_{Lb}$ are lagging with each other in an alternating manner. Seamless transitions can be achieved, and the transitions do not affect the output voltage V_o.

As analyzed in Sections III-B and IV-B, the asynchronous operation leads to unbalanced power loss and thermal stress to the leading and lagging devices. Without applying the proposed thermal balancing scheme, the two parallel-connected GaN HEMT HB legs suffer different case temperatures in the asynchronous mode, i.e., 72.9 °C for the leading HEMT and 35.8 °C for the lagging HEMT, as shown in Fig. 20(a) and (b). By contrast, the case temperatures of the GaN HEMTs with the proposed alternating-delay scheme can be balanced to 58.4 °C and 58.8 °C, as shown in Fig. 20(c) and (d).

The measured efficiencies of the Boost dc-dc converter in

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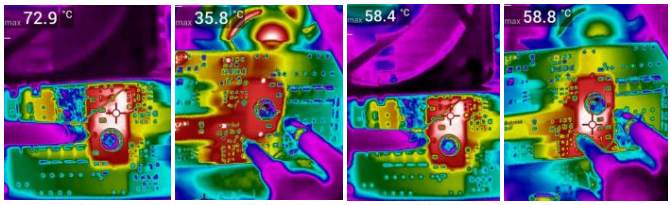

Fig. 20. Thermal images of the parallel-connected GS66508T GaN HEMT HBs operating in the asynchronous mode with and without the proposed thermal balancing scheme. The switching frequency $f_s = 200$ kHz, the input voltage $V_{in} = 200$ V, the output voltage $V_o = 400$ V, the output power $P_o = 750$ W, and the ambient temperature $T_a = 24°$C. (a) Leading and (b) lagging legs without the thermal balancing scheme. (c) Leading and (d) lagging legs with the thermal balancing scheme.

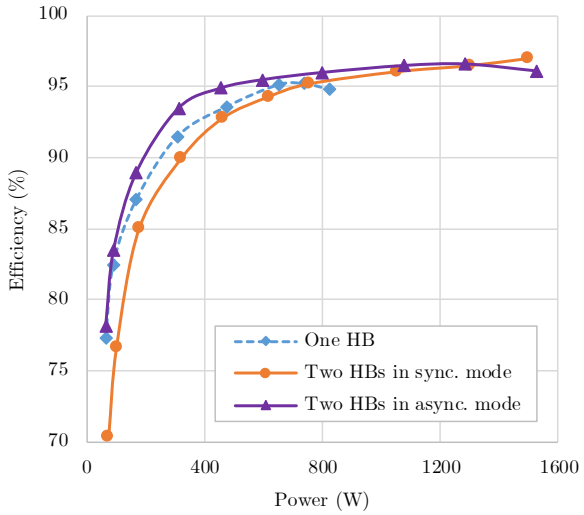

Fig. 21. Measured efficiencies of the Boost dc-dc converter operating in the synchronous and asynchronous modes. The switching frequency $f_s = 200$ kHz, the input voltage $V_{in} = 200$ V, and the output voltage $V_o = 400$ V.

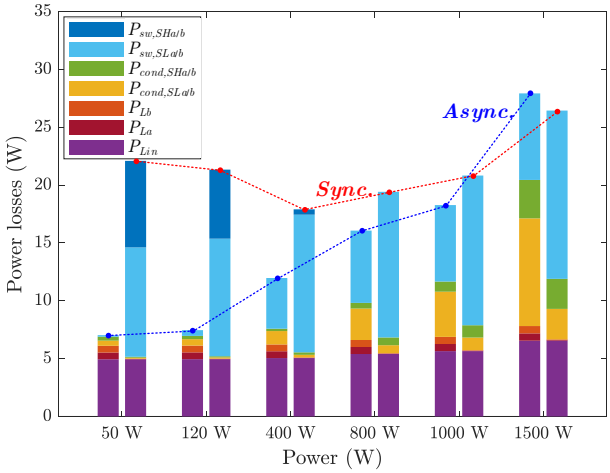

Fig. 22. Power loss breakdown of the Boost converter operating in the synchronous and asynchronous modes.

the synchronous and asynchronous modes are shown in Fig. 21. The synchronous operation enables higher efficiencies at high power levels ($>$ 1300 W) due to the reduced conduction loss at high load currents. When operating at medium and low loads, however, the asynchronous mode can remarkably increase the power conversion efficiency because of the decreased switching loss. The efficiency improvement becomes more significant as the decrease of load. Furthermore, the measured efficiency of one HB is also shown in Fig. 21. Its efficiency is superior than that of two synchronous HBs when the load is lower than 750 W because the switching loss can be reduced. However, it is still lower than the proposed asynchronous mode where the lagging devices achieve the ZVS and the leading ones turn on at a lower current or achieve the iZVS, as compared in Section IV-C.

To further illustrate the advantages of the proposed asynchronous mode in light-load efficiency over the synchronous mode, the distributions of power losses in both modes are calculated and shown in Fig. 22. For the Boost converter operating in the synchronous mode, the switching losses account for the largest share of the total power loss from light to heavy loads. By contrast, with the proposed asynchronous mode, the switching losses can be significantly reduced, particularly at light loads. Compared with the synchronous mode, the asynchronous operation increases the conduction loss of switches and the loss of commutation inductors. However, the loss increase is not as remarkable as the switching loss reduction when the load is not heavy. Therefore, the total power loss can be lowered, particularly at light loads.

VI. Conclusions

A commutation-inductor-based desynchronizable paralleling scheme is proposed for GaN HEMTs. The operating principle and design guidelines are detailed, and an alternating-delay thermal balancing scheme is proposed for the asynchronous operation. Multi-pulse and continuous Boost power conversion tests have been conducted to verify the feasibility and advantages of the proposal. The following conclusions can be drawn:

- Two operating modes, i.e., the synchronous and asynchronous modes, are enabled for the proposed paralleling structure;
- In the synchronous mode, the proposed paralleling structure is able to achieve better current sharing performance than the conventional solution without commutation inductors;
- In the asynchronous mode, the lagging ones of the paralleled GaN HEMT HB legs are capable of achieving the ZVS and the leading ones turn on at a current lower than the load current, thereby remarkably reducing the switching loss.
- The switching loss reduction and efficiency improvement brought by the asynchronous operation become more pronounced as the load current decreases;
- The proposed alternating delay scheme enables to balance the thermal stress between the paralleled GaN HEMTs operating in the asynchronous mode.

Appendix

In the synchronous mode, the load current I_{Lo} is shared by the N commutation inductors. Neglecting the ripple of I_{Lo}, the equivalent RMS current of the commutation inductors is

$$I_{Lc,rms,eq} = \frac{I_{Lo}}{\sqrt{N}} \tag{31}$$

In the asynchronous mode, the RMS currents of i_{La} and i_{Lb} can be expressed as

$$\begin{cases} I_{La,rms} = \sqrt{(I_{Lo} - I_{cir,pk})^2 + 4DI_{Lo}I_{cir,pk} - \frac{8f_s I_{cir,pk}^3 L_{dm}}{3V_{dc}}} \\ I_{Lb,rms} = I_{cir,pk}\sqrt{1 - \frac{8f_s I_{cir,pk} L_{dm}}{3V_{dc}}} \end{cases} \tag{32}$$

where D represents the duty cycle of the low-side switches, and f_s is the switching frequency. The equivalent RMS value of each commutation inductor can be derived as

$$I_{Lc,rms,eq} = \sqrt{\frac{I_{La,rms}^2}{n_{ld}} + \frac{I_{Lb,rms}^2}{n_{lg}}} \tag{33}$$

REFERENCES

[1] Q. Huang, A. Q. Huang, R. Yu, P. Liu, and W. Yu, "High-efficiency and high-density single-phase dual-mode cascaded buck–boost multilevel transformerless pv inverter with gan ac switches," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7474–7488, 2018.

[2] G.-J. Su, C. White, and Z. Liang, "Design and evaluation of a 6.6 kw gan converter for onboard charger applications," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*. IEEE, 2017, pp. 1–6.

[3] D. Han, W. Lee, S. Li, and B. Sarlioglu, "New method for common mode voltage cancellation in motor drives: Concept, realization, and asymmetry influence," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1188–1201, 2017.

[4] Floyd, "New and upcoming gan (gallium nitride) usb chargers (october 2019 updated)," Oct. 2019. [Online]. Available: https://www.chargerlab.com/new-and-upcoming-gan-gallium-nitride-usb-chargers/

[5] "GS66508T top-side cooled 650 V E-mode GaN transistor: Preliminary datasheet," GaN Systems, 2018. [Online]. Available: https://gansystems.com/wp-content/uploads/2018/04/GS66508T-DS-Rev-180424.pdf

[6] C.-T. Ma and Z.-H. Gu, "Review of GaN HEMT applications in power converters over 500 w," *Electronics*, vol. 8, no. 12, p. 1401, Nov. 2019.

[7] J. Lu, R. Hou, and D. Chen, "Loss distribution among paralleled gan hemts," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2018, pp. 1914–1919.

[8] Mouser Electronics, 2019. [Online]. Available: https://www.mouser.com/

[9] Y. Shen, S. Song, H. Wang, and F. Blaabjerg, "Cost-volume-reliability pareto optimization of a photovoltaic microinverter," in *Proc. IEEE Applied Power Electronics Conf. and Exposition (APEC)*, Mar. 2019, pp. 139–146.

[10] J. L. Lu and D. Chen, "Paralleling GaN E-HEMTs in 10kW-100kW systems," in *Proc. IEEE Applied Power Electronics Conf. and Exposition (APEC)*, Mar. 2017, pp. 3049–3056.

[11] J. Lu and R. Hou, "Parasitics optimization for GaN hemts in conventional housing-type power modules," in *Proc. Renewable Energy and Energy Management PCIM Europe 2019; Int. Exhibition and Conf. for Power Electronics, Intelligent Motion*, May 2019, pp. 1–7.

[12] W. Qian, J. Lu, H. Bai, and S. Averitt, "Hard-switching 650-V GaN hemts in an 800-V DC-grid system with no-diode-clamping active-balancing three-level topology," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1060–1070, Jun. 2019.

[13] M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, "Single-stage high-efficiency 48/1 V sigma converter with integrated magnetics," *IEEE Trans. Ind. Electron.*, vol. 67, no. 1, pp. 192–202, Jan. 2020.

[14] Z. Zeng, X. Zhang, and Z. Zhang, "Imbalance current analysis and its suppression methodology for parallel sic mosfets with aid of a differential mode choke," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1508 – 1519, Feb. 2020.

[15] H. Li, X. Zhang, L. Wen, J. A. Brothers, C. Yao, C. Han, L. Liu, J. Xu, J. Puukko, and J. Wang, "Paralleled operation of high-voltage cascode GaN hemts," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 815–823, Sep. 2016.

[16] A. Avila, A. Garcia-Bediaga, A. Rodriguez, L. Mir, and A. Rujas, "Analysis of optimal operation conditions for gan-based power converters," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2018, pp. 1932–1939.

[17] Q. Wu, M. Wang, W. Zhou, and X. Wang, "Current balancing of paralleled sic mosfets for a resonant pulsed power converter," *IEEE Trans. Power Electron.*, 2019, doi: 10.1109/TPEL.2019.2952326.

[18] J. Koomey and J. Taylor, "New data supports finding that 30 percent of servers are comatose, indicating that nearly a third of capital in enterprise data centers is wasted," Anthesis Group, Tech. Rep., Jun. 2015. [Online]. Available: https://info.anthesisgroup.com/hubfs/PDFs%20(guides,%20case%20studies%20etc)%20/Case-Study_DataSupports30PercentComatoseEstimate-FINAL_06032015.pdf

[19] Y. Shen, A. Chub, H. Wang, D. Vinnikov, E. Liivik, and F. Blaabjerg, "Wear-out failure analysis of an impedance-source PV microinverter based on system-level electro-thermal modeling," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3914 – 3927, May 2019.

[20] A. Babin, N. Rizoug, T. Mesbahi, D. Boscher, Z. Hamdoun, and C. Larouci, "Total cost of ownership improvement of commercial electric vehicles using battery sizing and intelligent charge method," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 1691–1700, Mar. 2018.

[21] J. Su and C. Liu, "A novel phase-shedding control scheme for improved light load efficiency of multiphase interleaved DCdc converters," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4742–4752, Oct. 2013.

[22] C. Fei, M. H. Ahmed, F. C. Lee, and Q. Li, "Two-stage 48 V-12 V/6 V-1.8 V voltage regulator module with dynamic bus voltage control for light-load efficiency improvement," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5628–5636, Jul. 2017.

[23] J. Hu, O. Alatise, J. A. Ortiz Gonzalez, R. Bonyadi, P. Alexakis, L. Ran, and P. Mawby, "Robustness and balancing of parallel-connected power devices: SiC versus coolmos," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 2092–2102, Apr. 2016.

[24] H. Li, S. Munk-Nielsen, S. Beczkowski, and X. Wang, "A novel dbc layout for current imbalance mitigation in SiC MOSFET multichip power modules," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8042–8045, Dec. 2016.

[25] H. Li, S. Munk-Nielsen, X. Wang, R. Maheshwari, S. Beczkowski, C. Uhrenfeldt, and W.-. Franke, "Influences of device and circuit mismatches on paralleling silicon carbide mosfets," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 621–634, Jan. 2016.

[26] D. Bortis, J. Biela, and J. W. Kolar, "Active gate control for current balancing of parallel-connected IGBT modules in solid-state modulators," *IEEE Trans. Plasma Sci.*, vol. 36, no. 5, pp. 2632–2637, Oct. 2008.

[27] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, and F. Wang, "Active current balancing for parallel-connected silicon carbide mosfets," in *Proc. IEEE Energy Conversion Congress and Exposition*, Sep. 2013, pp. 1563–1569.

[28] M. Sasaki, H. Nishio, and W. T. Ng, "Dynamic gate resistance control for current balancing in parallel connected igbts," in *Proc. Twenty-Eighth Annual IEEE Applied Power Electronics Conf. and Exposition (APEC)*, Mar. 2013, pp. 244–249.

[29] Z. Wang, Y. Wu, J. Honea, and L. Zhou, "Paralleling GaN hemts for diode-free bridge power converters," in *Proc. IEEE Applied Power Electronics Conf. and Exposition (APEC)*, Mar. 2015, pp. 752–758.

[30] Y. Mao, Z. Miao, C. Wang, and K. D. T. Ngo, "Passive balancing of peak currents between paralleled mosfets with unequal threshold voltages," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3273–3277, May 2017.

[31] Z. Miao, Y. Mao, G. Lu, and K. Ngo, "Magnetic integration into a silicon carbide (SiC) power module for current balancing," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11 026–11 035, Nov. 2019.

[32] C. Wang, M. Xu, F. C. Lee, and Z. Luo, "Light load efficiency improvement for multi-channel pfc," in *Proc. IEEE Power Electronics Specialists Conf*, Jun. 2008, pp. 4080–4085.

[33] O. Garcia, P. Zumel, A. de Castro, and A. Cobos, "Automotive DC-dc bidirectional converter made with many interleaved buck stages," *IEEE Trans. Power Electron.*, vol. 21, no. 3, pp. 578–586, May 2006.

[34] S. Waffler and J. W. Kolar, "Efficiency optimization of an automotive multi-phase bi-directional DC-dc converter," in *Proc. IEEE 6th Int. Power Electronics and Motion Control Conf*, May 2009, pp. 566–572.

[35] K. Park, R. Kieferndorf, U. Drofenik, S. Pettersson, and F. Canales, "Optimization of LCL filter with integrated intercell transformer for two-interleaved high power grid-tied converters," *IEEE Trans. Power Electron.*, p. 1, 2019, doi: 10.1109/TPEL.2019.2926312.

[36] B. Arbetter and D. Maksimovic, "Control method for low-voltage DC power supply in battery-powered systems with power management," in *Proc. PESC97. 28th Annual IEEE Power Electronics Specialists Conf.*, vol. 2, Jun. 1997, pp. 1198–1204 vol.2.

[37] B. Sahu and G. A. Rincon-Mora, "An accurate, low-voltage, CMOS switching power supply with adaptive on-time pulse-frequency modulation (pfm) control," *IEEE Trans. Circuits Syst. I*, vol. 54, no. 2, pp. 312–321, Feb. 2007.

[38] S. Kapat, B. C. Mandi, and A. Patra, "Voltage-mode digital pulse skipping control of a DCdc converter with stable periodic behavior and improved light-load efficiency," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3372–3379, Apr. 2016.

[39] Y. Shen, H. Wang, A. Al-Durra, Z. Qin, and F. Blaabjerg, "A structure-reconfigurable series resonant DCdc converter with wide-input and configurable-output voltages," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1752–1764, Mar. 2019.

[40] P. Zumel, C. Fernndez, A. de Castro, and O. Garca, "Efficiency improvement in multiphase converter by changing dynamically the number of phases," in *Proc. 37th IEEE Power Electronics Specialists Conf*, Jun. 2006, pp. 1–6.

[41] F. Luo, S. Wang, F. Wang, D. Boroyevich, N. Gazel, Y. Kang, and A. C. Baisden, "Analysis of cm volt-second influence on cm inductor saturation and design for input EMI filters in three-phase DC-fed motor drive systems," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1905–1914, Jul. 2010.

[42] T. Fuchslueger, H. Ertl, and M. A. Vogelsberger, "Reducing dv/dt of motor inverters by staggered-edge switching of multiple parallel SiC half-bridge cells," in *Proc. Renewable Energy and Energy Management PCIM Europe 2017; Int. Exhibition and Conf. for Power Electronics, Intelligent Motion*, May 2017, pp. 1–8.

[43] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (tcm) single-phase pfc rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 873–882, Feb. 2014.

[44] W. Konrad, G. Deboy, and A. Muetze, "A power supply achieving titanium level efficiency for a wide range of input voltages," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 117–127, Jan. 2017.

[45] Z. Yao and S. Lu, "A simple approach to enhance the effectiveness of passive currents balancing in an interleaved multiphase bidirectional DCdc converter," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7242–7255, Aug. 2019.

[46] Q. Huang, R. Yu, Q. Ma, and A. Q. Huang, "Predictive ZVS control with improved ZVS time margin and limited variable frequency range for a 99% efficient, 130-W/in3 MHz GaN totem-pole pfc rectifier," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 7079–7091, Jul. 2019.

[47] Y. Liu, Y. Syu, N. A. Dung, Chen-Chen, K. Chen, and K. A. Kim, "High switching frequency tcm digital control for bidirectional interleaved buck converters without phase error for battery charging," *IEEE J. Emerg. Sel. Topics Power Electron.*, p. 1, 2019, doi: 10.1109/JESTPE.2019.2954602.

[48] R. Hou, J. Lu, and D. Chen, "Parasitic capacitance eqoss loss mechanism, calculation, and measurement in hard-switching for GaN hemts," in *Proc. IEEE Applied Power Electronics Conf. and Exposition (APEC)*, Mar. 2018, pp. 919–924.

[49] R. Hou, J. Xu, and D. Chen, "A multivariable turn-on/turn-off switching loss scaling approach for high-voltage GaN hemts in a hard-switching half-bridge configuration," in *Proc. IEEE 5th Workshop Wide Bandgap Power Devices and Applications (WiPDA)*, Oct. 2017, pp. 171–176.

[50] E. A. Jones, F. Wang, D. Costinett, Z. Zhang, and B. Guo, "Temperature-dependent turn-on loss analysis for GaN HFETs," in *Proc. IEEE Applied Power Electronics Conf. and Exposition (APEC)*, Mar. 2016, pp. 1010–1017.

[51] "GS66508T-EVBDB2/GS66516T-EVBDB2 GaN E-HEMT Daughter Board and GS665MB-EVB Evaluation Platform: Users Guide," GaN Systems, Tech. Rep., Sep. 2018. [Online]. Available: https://gansystems.com/wp-content/uploads/2018/10/GS665xxT-EVBDB2-UserGuide-rev-20180905.pdf

[52] Y. Shen, H. Wang, Z. Shen, Y. Yang, and F. Blaabjerg, "A 1-MHz series resonant dc-dc converter with a dual-mode rectifier for PV microinverters," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6544–6564, Jul. 2019.

[53] F. Qi, Z. Wang, and Y. Wu, "Analysis of calculation models for device resonance in critical mode converters," in *Proc. IEEE 6th Workshop Wide Bandgap Power Devices and Applications (WiPDA)*, Oct. 2018, pp. 225–230.

[54] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016.

[55] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *Proc. IEEE Workshop Computers in Power Electronics*, Jun. 2002, pp. 36–41.

[56] H. Kim, G. Seo, B. Cho, and H. Choi, "A simple average current control with on-time doubler for multiphase ccm pfc converter," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1683–1693, Mar. 2015.

[57] D. Zhang, F. Wang, R. Burgos, R. Lai, and D. Boroyevich, "DC-link ripple current reduction for paralleled three-phase voltage-source converters with interleaving," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1741–1753, Jun. 2011.

[58] S. Sandler, "Faster-switching GaN : Presenting a number of interesting measurement challenges," *IEEE Power Electron. Mag.*, vol. 2, no. 2, pp. 24–31, Jun. 2015.

[59] M. Leibl, "Three-phase pfc rectifier and high-voltage generator for x-ray systems," Ph.D. dissertation, ETH Zurich, 2017.

[60] "GS66516T top-side cooled 650 V E-mode GaN transistor: Preliminary datasheet," GaN Systems, 2018. [Online]. Available: https://gansystems.com/wp-content/uploads/2018/04/GS66516T-DS-Rev-180422.pdf

[61] Y. Shi, Y. Zhang, L. Wang, and H. Li, "Reduction of EMI noise due to nonideal interleaving in a 100 kW SiC PV converter," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 13–19, Jan. 2019.

[62] Y. Roh, Y. Moon, J. Park, M. Jeong, and C. Yoo, "A multiphase synchronous buck converter with a fully integrated current balancing scheme," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5159–5169, Sep. 2015.

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