# Determination of electron effective mass and electron affinity in $HfO_2$ using MOS and MOSFET structures

S. Monaghan[a*], P. K. Hurley[a], K. Cherkaoui[a], M. A. Negara[a], and A. Schenk[b]

[a]Tyndall National Institute, University College Cork, Lee Maltings, Prospect Row, Cork, Ireland.
[b]Integrated Systems Laboratory, ETH Zürich, Gloriastrasse 35, CH-8092 Zürich, Switzerland.
*Corresponding author, tel. +353-21-420-5682; fax. +353-21-420-5703; email: scott.monaghan@tyndall.ie

## Abstract

We present a combined electrical and modeling study to determine the tunneling electron effective mass and electron affinity for $HfO_2$. Experimental capacitance-voltage (C-V) and current-voltage (I-V) characteristics are presented for $HfO_2$ films deposited on Si(100) substrates by atomic layer deposition (ALD) and by electron beam evaporation (e-beam), with equivalent oxide thicknesses in the range 10-12.5 Å. We extend on previous studies by applying a self-consistent 1D-Schrödinger-Poisson solver to the entire gate stack, including the inter-layer $SiO_x$ region - *and* to the adjacent substrate for non-local barrier tunnelling - self-consistently linked to the quantum-drift-diffusion transport model. Reverse modeling is applied to the correlated gate and drain currents in long channel MOSFET structures. Values of $(0.11 \pm 0.03)m_o$ and $(2.0 \pm 0.25)$ eV are determined for the $HfO_2$ electron effective mass and the $HfO_2$ electron affinity, respectively. We apply our extracted electron effective mass and electron affinity to predict leakage current densities in future 32 nm and 22 nm technology node MOSFETs with $SiO_x$ thicknesses of 7-8 Å and $HfO_2$ thicknesses of 23-24 Å.

*Keywords* – High-*k* gate stacks, $HfO_2$, reverse modeling, direct tunneling, electron effective mass, electron affinity, bulk properties, 32 nm and 22 nm technology nodes (*PACS Codes* – 72.20.-i, 77.55.+f).

## 1. Introduction

On the back of over ten years of research and development, the investigations of high dielectric constant materials (such as $HfO_2$) have reached the stage where they are now incorporated into the gate stack of silicon based MOSFET's. The $HfO_2$ insulator is used in conjunction with metal gate electrodes and a thin (~10 Å) interfacial silicon oxide layer ($SiO_x$).

Modeling the leakage currents in metal-gate/$HfO_2$/$SiO_x$/Si(100) structures requires knowledge of the dominant conduction mechanism and physical parameters of the $HfO_2$ thin film, such as the effective mass of electrons in the $HfO_2$ energy gap ($m_{HfO2}$) and the electron affinity in $HfO_2$ ($\chi_{HfO2}$). This is of technological importance to allow accurate simulations of the gate leakage current for existing and future technology nodes based on $HfO_2$ gate stacks over a typical bias range of 0 to 1 volts.

A range of publications have examined tunneling in heavily doped polysilicon and metal gate/$HfO_2$/$SiO_x$/Si structures, including determination of $m_{HfO2}$ and $\chi_{HfO2}$ [1-4]. A range of values for $m_{HfO2}$ are reported varying from $0.08m_o$ to $0.4m_o$. The reported values of $\chi_{HfO2}$ range from 1.75 eV to 2.82 eV. Based on the spread of results there is still scope for further analysis to establish if the reported ranges of $m_{HfO2}$ and $\chi_{HfO2}$ can be reduced and subsequently applied to future technology node modeling. In addition, it

would also be instructive to know if $m_{HfO2}$ and $\chi_{HfO2}$ vary with deposition method or gate material.

We extend on previous reports by examining metal-gate/$HfO_2$/$SiO_x$/Si(100) MOSCAP structures formed by electron beam evaporation (e-beam) and atomic layer deposition (ALD). The $HfO_2$ and silicon oxide interface layer thicknesses are determined by high resolution cross-sectional transmission electron microscopy. In the case of the ALD deposited $HfO_2$ gate stacks, full MOSFETs were available for the C-V and I-V analysis of the TiN/$HfO_2$/$SiO_x$/Si(100) structures.

The availability of the full MOSFET devices allows the simulations to be applied to the condition of tunneling of electrons from the channel inversion region. Moreover, the simultaneous modeling of the gate tunneling current and the drain current (which exhibits sign changes as a function of the gate voltage) provides additional experimental data for narrowing the uncertainty of $m_{HfO2}$ and $\chi_{HfO2}$, as there is a strong correlation between drain and gate currents in long-channel MOSFETs.

In contrast to previous modeling work, we apply a self-consistent 1D-Schrödinger-Poisson solver to the entire gate stack, including the inter-layer $SiO_x$ region, *and* to the adjacent substrate, which goes beyond the WKB approximation and automatically includes quantization effects in the channel. The direct tunneling current in the gate stack is self-consistently coupled to the drift-diffusion current which results from solving the continuity equations including all relevant physical effects, like mobility degradation, fixed oxide charges, and interface traps [5].

## 2. Sample and measurement details

### 2.1. *MOSCAP device*

In the case of the e-beam deposited film in the metal-oxide-semiconductor capacitor (MOSCAP), the $HfO_2$ layer is formed on *n* type silicon (100) with a resistivity of 2-4 Ωcm. The Si wafer undergoes a standard chemical clean and HF (10:1 DI water / HF for 10 seconds), to result in a H-terminated silicon surface. The $HfO_2$ film (~37 Å) is deposited at 150°C from 3-5 mm monoclinic $HfO_2$ pellets of 99.99% purity. MOSCAPs with an area 55 x 55 $\mu m^2$ are formed using photolithography and a resist lift-off process. The metal gate consists of 300 nm of Ni deposited ex-situ by e-beam, followed by a final forming gas anneal (5%$H_2$/95%$N_2$) at 400°C for 30 minutes. This will be referred to subsequently as the MOSCAP device. Figure 1 shows a HR-TEM micrograph of the dielectric layers for this device.

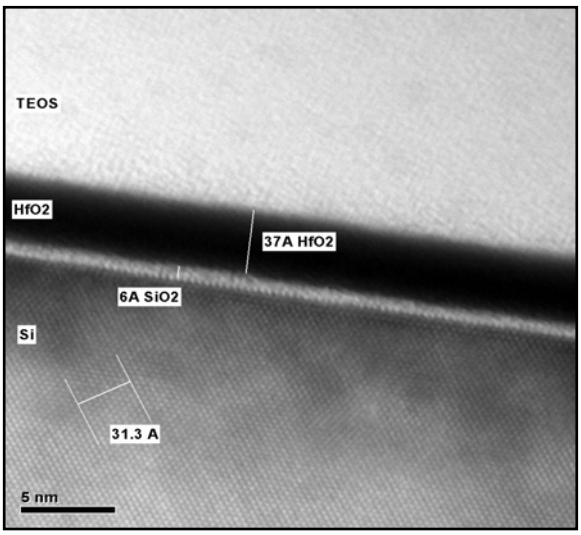



Figure 1: High Resolution cross-sectional Transmission Electron Microscopy (HR-TEM) micrograph of the MOSCAP device dielectric layers, showing an interfacial $SiO_x$ thickness of 6 Å and an $HfO_2$ thickness of 37 Å. The equivalent oxide thickness is estimated to be (10.9 ± 0.1) Å.

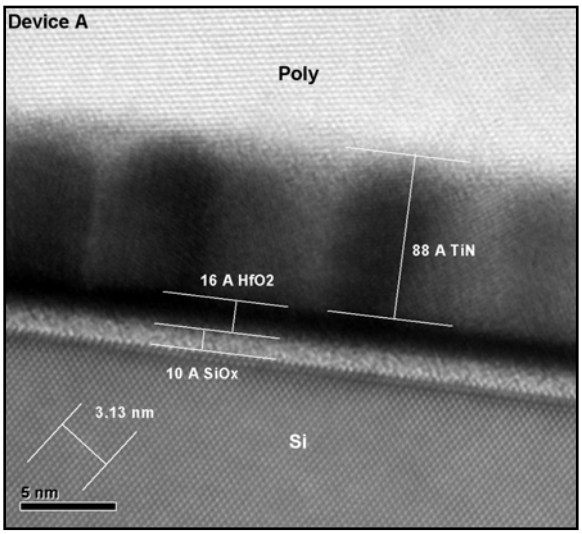
### 2.2. *MOSFET devices*

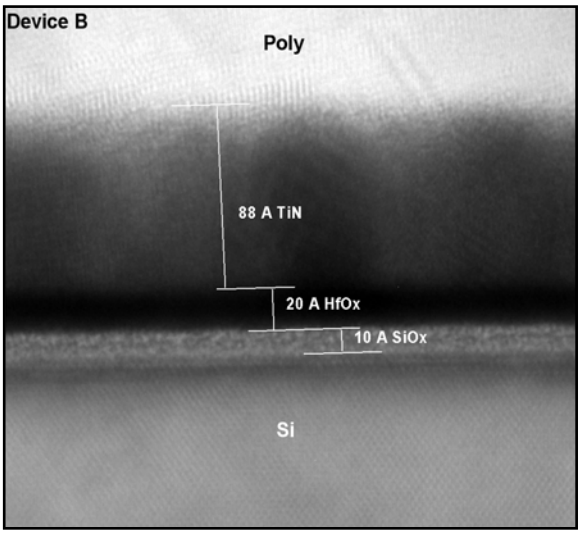
For the ALD deposited films in the metal-oxide-semiconductor field effect transistors (MOSFETs), the $HfO_2$ layers with nominal thicknesses of 16, 20, 24 and 30 Å are formed on *p* type silicon (100) with a ~10 Å interfacial $SiO_x$ layer. The gate electrode is 100 Å TiN. Isolated gate *n* channel MOSFETs with an area of 10 x 10 $\mu m^2$ are measured. Figure 2 shows HR-TEM

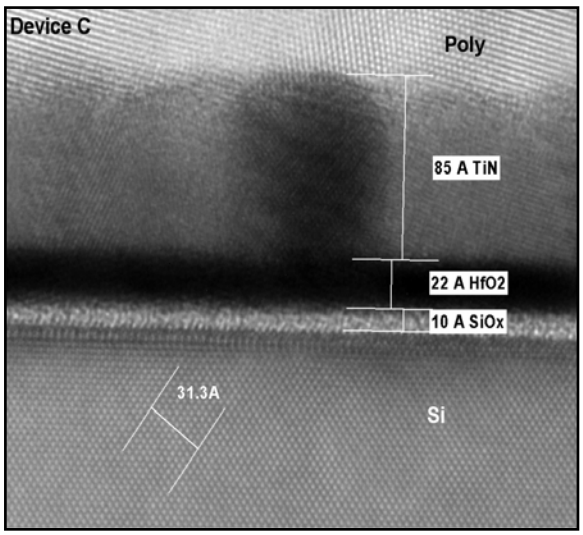
micrographs of the gate structures, with only device C showing a negligible 2 Å deviation in the nominal $HfO_2$ thickness (we use a $HfO_2$ thickness of 24 Å, as accurate HR-TEM proved problematic for device C). Physical and extracted parameters are presented in Table I. Further details of these devices can be found in [6], and they will be referred to subsequently in this paper as MOSFET devices A, B, C, and D.

2.3. *Measurement setup*

Current-voltage (I-V) measurements were performed with a HP4156A Precision semiconductor parameter analyzer. Capacitance-voltage (C-V) measurements were performed with a HP4284A precision LCR meter.



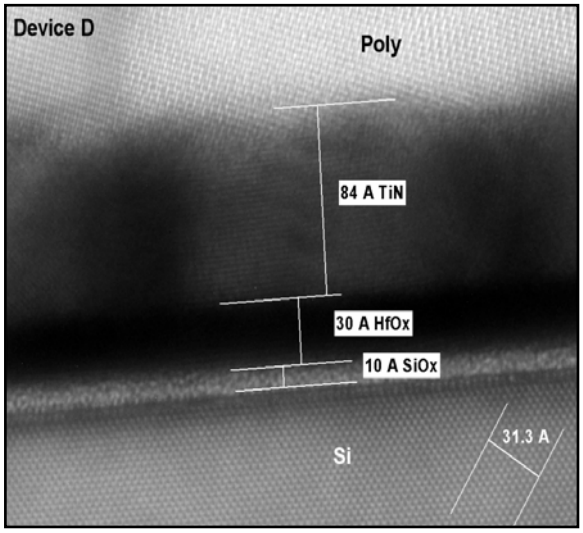




Figure 2: Gate stack High Resolution cross-sectional Transmission Electron Microscopy (HR-TEM) micrographs of MOSFET devices A, B, C, and D. Dielectric thicknesses are generally in very good agreement with those of Table I.

All measurements took place on-wafer in a microchamber probe station (Cascade Microtech, model Summit 12971B) in a dry air environment (dew point ~ -70$^o$C). Measurements were recorded at room temperature.

3. Models for C-V and I-V responses

The simulated quasi-static capacitance-voltage (QS C-V) responses of the e-beam device are obtained from charge-voltage curves that result from solving the

Schrödinger-Poisson system and finally differentiating them. Acceptor-like interface traps between the substrate and interfacial layer can be included.

Table I:

Summary of Physical and Extracted Parameters for the ALD $HfO_2$/TiN MOSFETs in this study.

| Wafer | A | B | C | D |
|---|---|---|---|---|
| t-$HfO_2$ [Å] | 16 | 20 | 24 | 30 |
| t-$SiO_x$ [Å] | 10 | 10 | 10 | 10 |
| $C_{ox\ eff}$ [F/cm$^2$] | 2.43x10$^{-6}$ | 2.35x10$^{-6}$ | 2.25x10$^{-6}$ | 2.16x10$^{-6}$ |
| $V_{FB}$ [V] | -0.49 | -0.51 | -0.58 | -0.6 |
| $E_{OT}$ [Å] | 10.6 | 11.4 | 12.1 | 12.5 |
| Na [x 10$^{17}$ /cm$^3$] | 3 | 3 | 3 | 3 |
| $\mu_{peak}$ [cm$^2$/V.s] | 225 | 212 | 195 | 178 |

In obtaining the I-V responses, 1D Schrödinger equations are solved along straight lines connecting the channel to the gate contact [7]. The results are self-consistently incorporated into a 2D drift-diffusion simulator [5]. We note that the influence of confinement from the quasi 2D states on the direct tunneling current is negligible in the inverted MOSCAP and MOSFET channels, mainly due to a cancellation effect between increased tunnel probability and decreased occupation probability for the lowest sub-band states, as described in [8]. Hence, parameter extraction from direct tunneling simulation fits is influenced solely by the underlying physical model which is well established.

A special-purpose grid has to be generated for the solution of the 1D Schrödinger-Poisson system. It consists of straight lines that are attached to a semiconductor vertex and connect this vertex to the closest grid point on the gate contact. In addition, points not directly situated under the gate can be connected to the gate corners by defining a maximum angle measured to the normal of the gate contact line. Two length parameters serve to include regions below and above the stack. Hence, the transmission probability can be computed not only for the stack barrier alone, but also for a possible potential barrier in the substrate.

Based on interpolation schemes, all data (as well as the refinement of the initial mesh) are transferred to the special-purpose grid. The 1D Schrödinger equation is solved in the (one-band) effective mass approximation (EMA) using the scattering matrix approach (SMA) [9]. Denoting coordinates on the lines of the special-purpose grid by $u$ (origin at the metal contact), the electron current density due to direct tunneling from the Si (by conduction band electrons only) can be written as [5,10]:

$$j_n = -\frac{g_n A_0 T}{k_B}\int_{0^-}^{\infty} du\, \mathcal{T}_n\left[u, 0^-, E_c(u)\right]\left|\frac{dE_c}{du}(u)\right| \times$$
$$\times\ \Theta\left[-\frac{dE_c}{du}(u)\right]\ln\left\{\frac{\exp\left[\frac{E_{F,n}(u)-E_c(u)}{k_B T}\right]+1}{\exp\left[\frac{E_{F,n}(0^-)-E_c(u)}{k_B T}\right]+1}\right\}.$$

Here, $A_0 = 4\pi m_0 k_B^2 q/h^3$ is the Richardson constant for free electrons, $T$ denotes the temperature (drift-diffusion model, no carrier heating), $k_B$ the Boltzmann constant, $E_c(u)$ the position-dependent conduction band edge (which is a function of electron affinity), $E_{F,n}(u)$ the quasi-Fermi energy, and $\mathcal{T}_n$ the tunneling probability resulting from the SMA solution of the 1D Schrödinger equation. The parameters $\mathcal{T}_n$ and $g_n$ are functions of electron effective masses. For tunneling across a (100)-oriented interface, reasonable choices are $g_n = 2m_t/m_0$ for the valley pair perpendicular to the interface, and $g_n = 4(m_t \cdot m_l)^{1/2}/m_0$ for the two valley pairs parallel to the interface, where $m_t$ is the transverse electron effective mass, $m_l$ is the longitudinal electron effective mass, and $m_0$ is the free electron mass. Separate simulations of the current are performed to account for changes in the effective mass of Si that enter the transmission probability $\mathcal{T}_n$.

## 4. Experimental results and simulations

Figure 3 shows the measured and simulated C-V responses for the MOSCAP device at a measurement frequency of 1 kHz. The device exhibits a low frequency response in inversion as a result of peripheral

inversion around the capacitors area defined by the Ni gate. This allows a fit of the simulated QS C-V to the measured data across the full range, from strong accumulation to strong inversion.

The simulated C-V is in very good agreement with the experimental data over the full bias range from strong accumulation (-1.25 V) to strong inversion (1.0 V), using the physical thicknesses available from the HR-TEM of Figure 1. The interface trap density ($D_{it}$) post forming gas anneal is in the range 2-3 x $10^{11}$ $cm^2eV^{-1}$ near the mid gap energy. $D_{it}$ does not have a significant influence on the C-V response and is not considered further. The fit of the simulation C-V yields dielectric constant estimates of 4.9 and 23 for the $SiO_x$ interlayer and the $HfO_2$ film, respectively. The effective Ni gate work function, which includes the effect of any fixed oxide charges, is 4.71 eV.

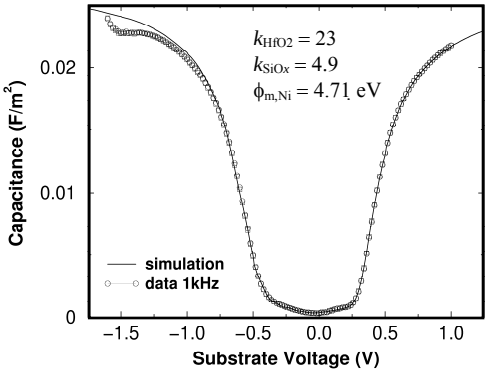



Figure 3: The measured (circles) and simulated (line) C-V response for the e-beam MOSCAP device. The measured data was recorded at an ac signal frequency of 1 kHz.

The experimental (circles) and simulated (solid and dashed lines) I-V responses are shown in Figure 4. The simulations are for direct tunneling by conduction band electrons only from the silicon substrate. Excellent fits to the magnitude and gradient of the measured data are obtained for a substrate voltage ($V_s$) < -0.7 volts. The parameters used for the solid (dashed) line fits are: $m_{HfO2}$ = 0.11$m_o$ (0.135$m_o$), $\chi_{HfO2}$ = 1.75 eV (2.0 eV), and $m_{SiOx}$ = 0.5$m_o$, $\chi_{SiOx}$ = 1.4 eV. The $SiO_x$ electron affinity $\chi_{SiOx}$ is different from the typical $SiO_2$ value of 0.9 eV because the $SiO_x$ is sub-stoichiometric. While direct conduction band tunneling is consistent with the measured data at $V_s$ < -0.7 volts, it is evident from Figure 4 that for lower absolute values of $V_s$ an additional defect-assisted tunneling mechanism is present. We concentrate only on the direct conduction band tunneling regions. The equivalent leakage current density from the leakage current of Figure 4 at $V_{fb}$ + 1 V into accumulation ($V_s$ ~ -1.3 V) is 1x$10^{-3}$ A/$cm^2$, with a MOSCAP device area of 55 x 55 $\mu m^2$. We note that corner effects are excluded experimentally in MOSCAP devices.

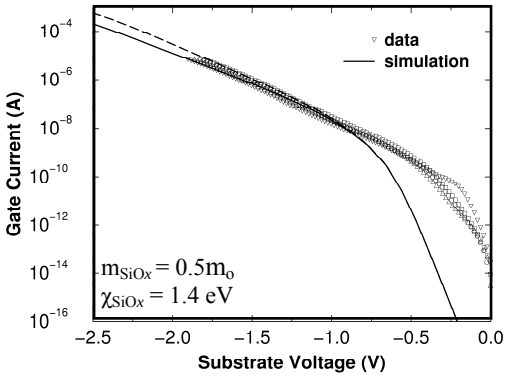


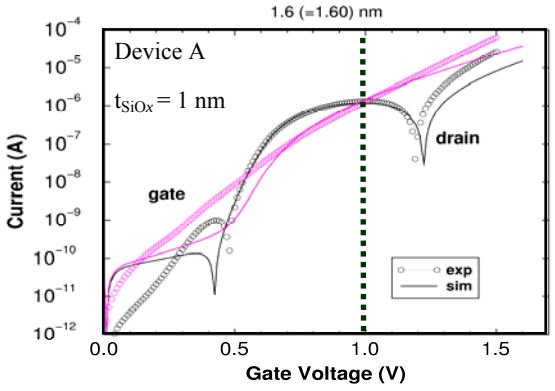

Figure 4: Measured and simulated I-V characteristics for the e-beam MOSCAP device. The measured current is for various sites across the wafer. The Ni gate area is 55 x 55 $\mu m^2$. Simulation parameters for $SiO_x$ are inset. Solid curve: $m_{HfO2}$ = 0.11$m_o$, $\chi_{HfO2}$ = 1.75 eV, dashed curve: $m_{HfO2}$ = 0.135 $m_o$, $\chi_{HfO2}$ = 2.0 eV.

In the case of MOSFET devices A, B, C and D (Table I), the availability of MOSFET structures allows the simultaneous fitting of the coupled gate ($I_g$) and drain ($I_d$) currents over a range of $HfO_2$ film thicknesses. Excellent agreement is found between the measured and simulated gate and drain currents presented in Figure 5 for MOSFET devices A-D. However, accurate simulation below a gate voltage of ~0.6 V is not possible because the $I_g$-$V_g$ curves in this region are dominated by tunneling in the vicinity of the drain-side gate corner, where no predictive modeling is possible since the

geometry and doping details are not known. Therefore, these regions ($V_g$ < 0.6 V) are not used in the parameter extraction method.

The drain current is the current measured at the drain terminal without gate current partition correction. As a consequence, the measured drain current is influenced by the gate leakage current density, which is evident from the changes in the sign of the drain current with increasing gate voltage. Relatively large device areas (10 x 10 μm$^2$) were selected so that $I_g$ exceeds $I_d$ at some gate bias within the range 0 to 1.5 V. The gate voltage corresponding to the drain current sign changes provides additional experimental data for the reverse modeling process.

Based on a series of systematic simulations, we determine the best fits to the experimental data, where: (i) the $SiO_x$ interlayer thickness, $m_{HfO2}$, and $\chi_{HfO2}$ are fixed and the $HfO_2$ thickness is varied; (ii) the $HfO_2$ thickness, $m_{HfO2}$, and $\chi_{HfO2}$ are fixed and the $SiO_x$ interlayer thickness is varied; and (iii) both the $HfO_2$ thickness and the $SiO_x$ thickness are fixed and $m_{HfO2}$ and $\chi_{HfO2}$ are varied. The best possible fits to the experimental data by this exhaustive process are achieved by using the following parameter sets: $m_{HfO2} = (0.08\text{-}0.14)m_o$, $\chi_{HfO2}$ = (1.75-2.25) eV, $m_{SiOx} = 0.5m_o$, and $\chi_{SiOx}$ = 1.4 eV.



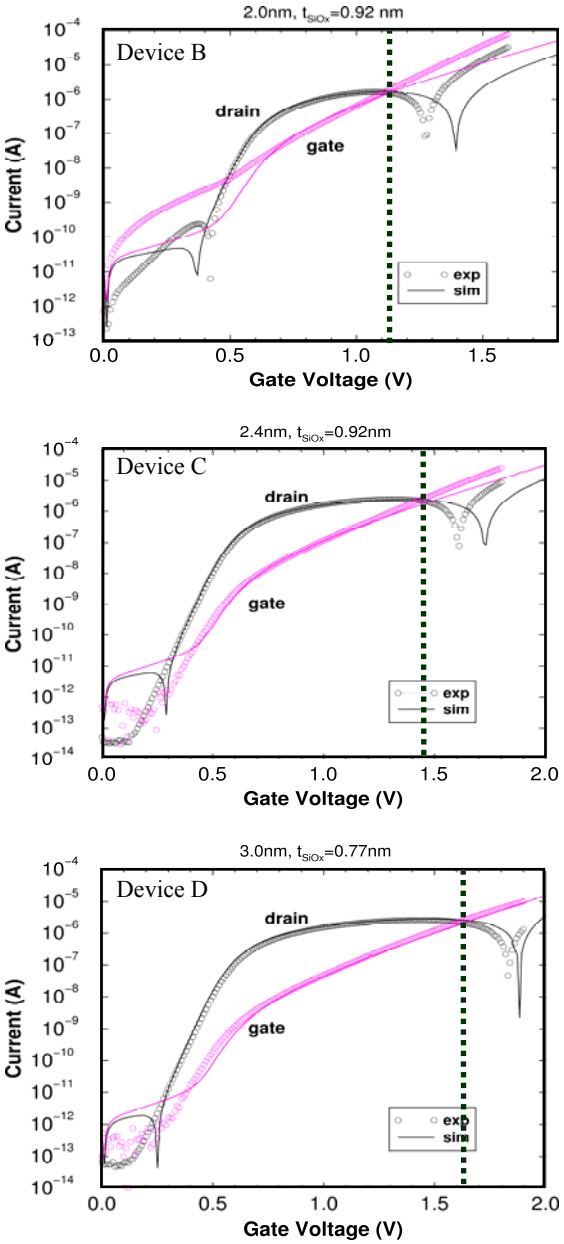




Figure 5: Measured (circles) and simulated (solid) gate and drain currents with $V_{DS}$ = 10 mV, for MOSFET device A: 16 Å $HfO_2$, device B: 20 Å $HfO_2$, device C: 24 Å $HfO_2$, and device D: 30 Å $HfO_2$. All fits to the measured data are obtained for the following parameters: $m_{HfO2}$ = (0.08-0.14)$m_o$, $\chi_{HfO2}$ = (1.75-2.25) eV, $m_{SiOx} = 0.5m_o$, and $\chi_{SiOx}$ = 1.4 eV. The TiN work function is in the range of 4.58-4.63 eV.

It was necessary to modify the $SiO_x$ interlayer thickness from 10 Å for MOSFET device A to 9.2 Å for MOSFET devices B and C, and to 7.7 Å for MOSFET device D. This is a possible indication that the $SiO_x$

interlayer stoichiometry is modified with increasing $HfO_2$ film thickness.

Considering both results from the e-beam deposited MOSCAP device and the ALD-deposited MOSFET devices A-D, the possible range of values for $m_{HfO2}$ and $\chi_{HfO2}$ are $(0.11 \pm 0.03)m_o$ and $(2.0 \pm 0.25)$ eV, respectively. The $\chi_{HfO2}$ range corresponds to a conduction band offset from the silicon conduction band to the $HfO_2$ conduction band of $\Delta E_c = (2.05 \pm 0.25)$ eV from the relation $\chi_{Si} = 4.05$ eV $= \chi_{HfO2} + \Delta E_c$.

## 5. Future technology nodes

We can use our estimates of electron effective mass and electron affinity to predict the leakage current densities in future $Si(100)/SiO_x/HfO_2$/metal-gate *n* channel template MOSFETs for the 32 nm and 22 nm technology nodes, as specified by the ITRS [11], and originally designed within the framework of the European Union project PULLNANO. The device structures are shown in Figure 6, with the 32 nm device on the left and the 22 nm device on the right.

The 32 nm (gate length) template device employed is a single-gate silicon-on-insulator *n* channel MOSFET with *p*-type substrate Si. The polysilicon and TiN gate electrode thicknesses are 50 nm and 10 nm, respectively. Source (S) and drain (D) are elevated by 10 nm. The channel is unstrained with <100> orientation and it has calibrated doping concentrations to meet the ITRS off-current requirements [11]. S/D contacts are 36 nm from the centre of the channel and are placed on top of the elevated S/D. Other device parameters are: $t_{SiOx} = 8$ Å, $t_{HfO2} = 23$ Å, $t_{Si} = 70$ Å, $t_{box} = 200$ Å, $N_A$ (bulk-Si) $= 1 \times 10^{18}$ cm$^{-3}$, and the metal gate work function = 4.6 eV. The 70 Å Si channel has a doping concentration of $N_A = 2.6 \times 10^{15}$ cm$^{-3}$ in the central region of the channel (between the dashed lines in Figure 6), and $N_D = 5.8 \times 10^{19}$ cm$^{-3}$ away from the central channel region (outside the solid lines of Figure 6). Between these two channel regions there is a doping concentration of $N_D = 1.5 \times 10^{17}$ cm$^{-3}$ to $N_D = 3.8 \times 10^{14}$ cm$^{-3}$ graded towards the acceptor-doped central channel region (from solid to dashed lines in Figure 6). The buried oxide (BOX) has a doping concentration of $N_A = 1.2 \times 10^{15}$ cm$^{-3}$.

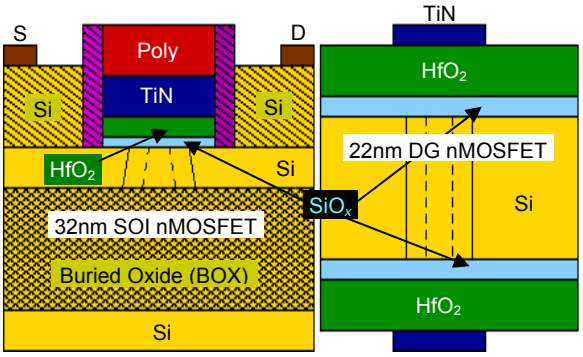



Figure 6: The single-gate SOI device (left, sectional view) is the 32 nm technology node simulated template, and the body region of the double-gate device (right, plan view, 60 nm S/D extensions not shown) is the 22 nm technology node simulated template. Both device gates have a width of 1 μm. The purple (b&w: dark grey) hatched regions either side of the 32 nm device gate are $Si_3N_4$ spacers ($k$ = 7.5). The source/drain contacts for the 22 nm device are placed vertically at the extension ends.

The 22 nm *n* channel MOSFET template device has a double-gate architecture with *p*-type substrate Si. The structure is symmetric with respect to the centre of the channel. The channel is unstrained with <100> orientation and, similar to the 32 nm template, it also has calibrated doping concentrations to meet ITRS requirements [11]. Other device parameters are: $t_{SiOx} = 7$ Å, $t_{HfO2} = 24$ Å, $t_{Si} = 100$ Å, and the metal gate work function = 4.8 eV. The doping concentration of the central Si channel region is $N_A = 1.2 \times 10^{15}$ cm$^{-3}$ (between the dashed lines in Figure 6). The rest of the Si channel has a doping profile similar in concentration and distribution to that already described for the Si channel of the 32 nm template device.

Figure 7 gives estimated leakage current densities (J or $J_g$) at $V_{DS} = 0$ V (top), and $V_{DS} = 1$ V (bottom). At zero drain bias ($V_{DS} = 0$

V), there is almost no difference in J at negative gate voltages and at zero gate voltage for the 22 nm and 32 nm technology node devices. In the positive voltage range of 0-0.7 V, the J of the 32 nm technology node device is slightly larger than that of the 22 nm technology node device, but then becomes less than that of the 22 nm technology node device at $V_g > 0.7$ V, with an eventual improvement over the 22 nm technology node device by a factor of ~2.7 at $V_g = 1$ V ($J \sim 1 \pm 1.5 \times 10^{-1}$ A/cm$^2$).

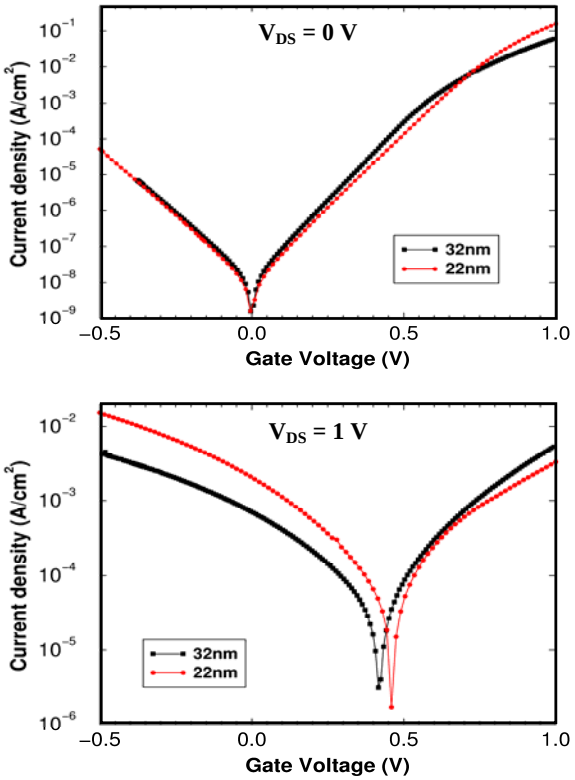



Figure 7: Simulated gate current densities for 32 nm (black) and 22 nm (red, b&w: light gray) technology node MOSFETs with $V_{DS}$ = 0 V (top), and $V_{DS}$ = 1 V (bottom). Note: the $J_g$-$V_g$ for the 22 nm template device includes the current density of *both* gates.

It can also be seen that, at a drain bias of 1 V ($V_{DS}$ = 1 V), the J of the 22 nm technology node device is ~3 times larger than that of the 32 nm technology node device at the off-state gate voltage ($V_g$ = 0 V, $J \sim 1 \pm 1.5 \times 10^{-3}$ A/cm$^2$), whereas the 22 nm device has a lower J than that of the 32 nm device by a factor of ~1.6 at the on-state gate voltage ($V_g$ = 1 V, $J \sim 6 \pm 1 \times 10^{-3}$ A/cm$^2$).

The simulated 32 nm and 22 nm technology node *n* channel MOSFETs predict off-state and on-state leakage current densities that can be compared to only limited data from the ITRS (citation [11], pp. 17, Table *PIDS3a*). In the low standby power (LSTP) logic case, there is only 22 nm extended planar bulk data available that targets $J_g = 8.11 \times 10^{-2}$ A/cm$^2$ at $V_g$ ($V_{dd}$) = 1.1 V. Figure 7 shows that predicted $J_g$ values at $V_g$ = 1 V and $V_{DS}$ = 1 V are $6 \pm 1 \times 10^{-3}$ A/cm$^2$, and if we do an approximate extrapolation to $V_g$ = 1.1 V then $J_g$ should be no greater than $1 \times 10^{-2}$ A/cm$^2$. Hence, these simulations show that scaling is possible for the Si(100)/$SiO_x$/$HfO_2$/metal-gate stacks, and the physical thicknesses of the $HfO_2$ high-*k* oxide layer, and of the $SiO_x$ interlayer, are predicted for these future technology nodes that maintains control of the gate leakage currents to within the limited data available from the ITRS.

## 6. Conclusions

Experimental and physically-based modeling results of the tunneling gate leakage currents have been presented for e-beam and ALD deposited metal-gate/$HfO_2$/$SiO_x$/Si(100) gate stack structures of MOSCAP and MOSFET devices, respectively. We have extended on previous studies by applying a self-consistent 1D-Schrödinger-Poisson solver to the entire gate stack, including the interlayer $SiO_x$ region, *and* to the adjacent substrate. The modeling also fits the gate current to the correlated drain current in the MOSFET devices. The electron effective mass $m_{HfO2}$ and electron affinity $\chi_{HfO2}$ of $HfO_2$ are determined to be within the ranges $(0.11 \pm 0.03)m_o$ and $(2.0 \pm 0.25)$ eV, respectively for the e-beam and ALD-deposited $HfO_2$ films, which reduces these parameter ranges found in the literature.

We use our estimates of electron effective mass and electron affinity to predict the leakage current densities in future Si(100)/$SiO_x$/$HfO_2$/metal-gate *n* channel MOSFETs for the 32 nm and 22 nm technology nodes. It is predicted that the Si(100)/$SiO_x$/$HfO_2$/metal-gate stacks can be scaled to the 32 nm and the 22 nm technology nodes. On and off state leakage current densities are predicted, alongside reduced physical thicknesses of the $HfO_2$ high-*k* oxide layer and of the $SiO_x$ interlayer.

## Acknowledgements

The authors would like to acknowledge the Sixth European Framework programme through the PULLNANO Project (IST–026828), Science Foundation Ireland (05/IN/1751), and the Swiss National Science Foundation (project NEQUATTRO SNF 200020-117613/1). We additionally acknowledge IUNET (Italy) and IMEC through the PULLNANO Project for the provision of the 32 nm and 22 nm template devices. One of the authors (A. Schenk) wishes to thank Dr. Andreas Wettstein (Synopsys LLC., Switzerland) for many valuable discussions. The authors also acknowledge Wilman Tsai (INTEL) and Prashant Majhi (INTEL/Sematech) for the provision of the Si(100)/$SiO_x$/$HfO_2$/TiN MOSFETs used in this study; and S. Cosgrove, R. Dunne, M. Brennan, A. Hooper, and J. Roche of INTEL for the provision of the MOSCAP and MOSFET HR-TEM micrographs.

## References

[1] W. J. Zhu, T. P. Ma, T. Tamagawa, J. Kim and Y. Di, "Current Transport in Metal/Hafnium Oxide/Silicon Structure", *IEEE Electron Device Letters*, vol. 23, no. 2, pp.97-99, 2002.

[2] Y. T. Hou, M. F. Li, H. Y. Yu and D. L. Kwong "Modeling of the Tunneling Currents Through $HfO_2$ and $(HfO_2)_x(Al_2O_3)_{1-x}$ Gate Stacks", *IEEE Electron Device Letters*, vol. 24, no. 2, pp.96-98, 2003.

[3] F. C. Chiu, "Interface Characterisation and carrier transport in metal/$HfO_2$/silicon structure, *Journal of Applied Physics*, 100, 114102 (2006).

[4] A. Campera, G. Iannaccone and F. Crupi, "Modelling of Tunneling Currents in Hf-Based Gate Stacks as a Function of Temperature and Extraction of Material Parameters", *IEEE Trans. on Electron Devices*, vol. 54, no. 1, pp.83-85, 2007.

[5] Synopsys Inc, *Sentaurus Device User Guide*, version Z-2007.03, Mountain View, California, (2007).

[6] M. A. Negara, K. Cherkaoui, P. Majhi, C. D. Young, W. Tsai, D. Bauza, G. Ghibaudo, P. K. Hurley, "The influence of $HfO_2$ film thickness on the interface state density and low field mobility of n channel $HfO_2$/TiN gate MOSFETs", *Microelectronic Engineering* 84, 1874–1877 (2007).

[7] A. Wettstein, A. Schenk, and W. Fichtner, "Simulation of Direct Tunneling through Stacked Gate Dielectrics by a Fully-Integrated 1D-Schrödinger-Poisson Solver", *IEICE Trans. Electron.* vol. E83-C, 1189 (2000).

[8] A. Wettstein, A. Schenk, A. Scholze, and W. Fichtner, "The Influence of Localized States on Gate Tunnel Currents - Modeling and Simulation", *IEEE Proceedings of SISPAD'97*, Boston, USA, September 8-10, 1997, pp. 101-104.

[9] A. C. Marsh and J. C. Inkson, "Scattering matrix theory of transport in heterostructures", *Semicond. Sci. Technol.* vol 1, 285 (1986).

[10] A. Schenk and G. Heiser, "Modeling and simulation of tunneling through ultra-thin gate dielectrics", J. Appl. Phys. 81, 7900 (1997).

[11] The International Technology Roadmap for Semiconductors, 2007: Process Integration, Devices, and Structures, pp. 17-35.