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DETERMINATION OF TRIGGERING ANGLE THROUGH A NOVEL GRAPHICAL METHOD ANALYSIS

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Abstract

This paper proposes a new graphical method analysis to determine the triggering angle of the Neutral-Point-Clamped Multilevel Inverter (NPCMI). The proposed graphical method analysis utilised the ideal sinusoidal waveform as the basis of the calculation. Based on the desired sinusoidal output waveform and switching state of Neutral-Point-Clamped Multilevel Inverter, triggering angle of each switching devices are calculated and determined. The triggering angles have been calculated for 3-level, 5-level and 7-level. Total Harmonics Distortion (THD) values of line voltage and phase voltage are calculated and compared and it has been concluded that this method is successfully applied where the low THDs values are obtained.

Keywords: Neutral-Point-Clamped, Multilevel inverter, Total harmonics distortion.

1. Introduction

Multilevel Inverters are a class of inverters that utilise the concept of connecting a series of power electronic switches in cascade. With this arrangement, the output voltage waveform of the multilevel inverter has an equal step, staircase profile where with the increased number of level, the more sinusoidal the output voltage becomes. Its operation is based on the concept of synthesizing an AC output voltage from several input DC supplies.

Nowadays, with the advancement of solid state technologies, power electronics devices have been fabricated with higher voltage, current and power rating. Further-

Nomenclatures

D	Switching duration, deg.
m	Number of level
n	Number of odd levels
S	Number of sections
V_{DC}	DC voltage, V
V_{LL}	Line-to-line voltage, V
V_{LN}	Line-to-neutral voltage, V
VSI	Voltage source inverter
$V1$	Lower limit voltage value, V
$V5$	Upper limit voltage value, V

Greek Symbols

αi_n	Sinusoidal waveform intersection angle, deg.

Abbreviations

GMA	Graphical method analysis
NPCMI	Neutral-point-clamped multilevel inverter
PWM	Pulse width modulation
SHE	Selective harmonic elimination
SVM	Space vector modulation
SVPWM	Space vector pulse width modulation
THD	Total harmonic distortion

more, multilevel inverter has the advantage over the conventional two-level voltage source inverter (VSI) by offering higher efficiency performance and reduction in production cost which are greatly sought by the industries, particularly when dealing in high voltage and high power application.

At low voltage, low power applications, the conventional two-level voltage source inverter are sufficient. However, the situation changes when subjected to medium voltage, medium power and high voltage, high power applications. By employing Multilevel Inverter, more than two levels of output voltage can be achieved with smoother, less distortion and low Total Harmonics Distortion (THD) contents. As the number of levels of the Multilevel Inverter increases, the harmonics contents of the output voltage waveform decreases significantly [1]. Another benefit of using Multilevel Inverter is the need of the phase shifting transformer can be avoided since the staircase steps of the output voltage is obtained through systematically connecting the DC supply one by one into the circuit. Also, with this Multilevel concept, each individual switches has smaller rating which help in reducing the cost and experience lower *dv/dt* stresses [2].

There are three main topologies for Multilevel Inverters; Neutral-Point-Clamped, Flying Capacitor and H-bridge Cascade. Each of these topologies has their own advantages and disadvantages. Low distortion, lower *dv/dt* stresses, lower harmonics contents, lower switching losses and reduced electromagnetic compatibility problems are some of the advantages of Multilevel Inverter [3]. While the disadvantages are as the number of level increases, the amount of switching

devices and other components such as capacitors and clamping diodes are also increased, and control becomes more complicated.

The motivation for this work comes from idea to find an easier approach to calculate the triggering angle that could produce an output voltage that has low THD value. From the previous work of others researchers, there four major modulation and control methods that can be applied to the Multilevel Inverter; Carrier-Based PWM Modulation (PWM) [4], Space Vector Modulation (SVM) [5], Selective Harmonics Elimination (SHE) [6] and Space Vector Pulse Width Modulation (SVPWM) [7].

Pulse Width Modulation was based on the comparison of a sinusoidal reference with two carriers. In [4], the researchers proposed a method on searching for optimal switching sequences using offset voltages.

Space Vector Modulation is a very attractive choice that is used by many researchers. In Leon et al. [5], the authors new proposed a method of three dimensional feed forward SVM where the actual values of the DC voltages are taken into account in the modulation process.

In three-level inverter applications, SHE is an alternative where the harmonics are selective selected to be eliminated based on the frequency spectrum of the output voltage. Franquelo et al., [6] proposed a new method called selective harmonic mitigation PWM that generates switching patterns by using a general-purpose random-search heuristic algorithm. In [7], a new space vector strategy that eliminates low frequency ripple from the dc link capacitors of a three-level converter has been proposed and verified.

The objective of this paper is to determine the triggering angle for three-phase Neutral-Point-Clamped Multilevel Inverter through the new proposed Graphical Method Analysis (GMA). For this purpose three levels of NPC which are 3-level, 5-level and 7-level, have been investigated and tested with the proposed analysis. The THDs values of the output voltages were then compared with others control methods.

2. Neutral-point-clamped Multilevel Inverter

The term Multilevel Inverter basically applies to conventional three-phase bridge configuration with an extension at the top and bottom rail of power supply. The lowest level of Multilevel Inverter starts from three level and can be extended to any level by adding a positive extension and negative extension for each level. The main feature of Multilevel Inverter is it utilises the conversion of power through a small increment of voltage step by synthesizing a staircase voltage from several DC capacitor voltages. Neutral-Point-Clamped Multilevel Inverter has several clamping diodes clamped to the DC capacitors rail and respective switching devices on the phase leg as shown in Fig. 1.

Neutral-Point-Clamped Multilevel Inverter (NPC), also known as Diode-Clamped was first introduced in the early 80's and has been extensively used in various applications. This structure was first proposed by Nabae et al. [8]. One of the advantages of this NPCMI is that when the number of levels is high, the harmonic content will be lower that the need for filters can be avoided. This NPC also has the easiest switching control and the protection circuit required is the least compared to the other multilevel inverter. While the major disadvantages of

this NPC are it is difficult to control the real power flow of the individual converter in multilevel converter and too much clamping diodes are required when the number of levels is high. The disadvantages also include relatively high switching losses which limit the switching frequency to a couple hundred hertz and unsymmetrical semiconductor loss distribution [9], the requirement of a sine filter for standard machines [10] and the difficult extension of the voltage converter range for use by semiconductors with higher blocking capability or a series connection of semiconductors [11]. A NPCMI with m number of levels characteristically comprises of (m-1) capacitors on the DC bus and voltage across each capacitor is V_{DC}/ (m-1).

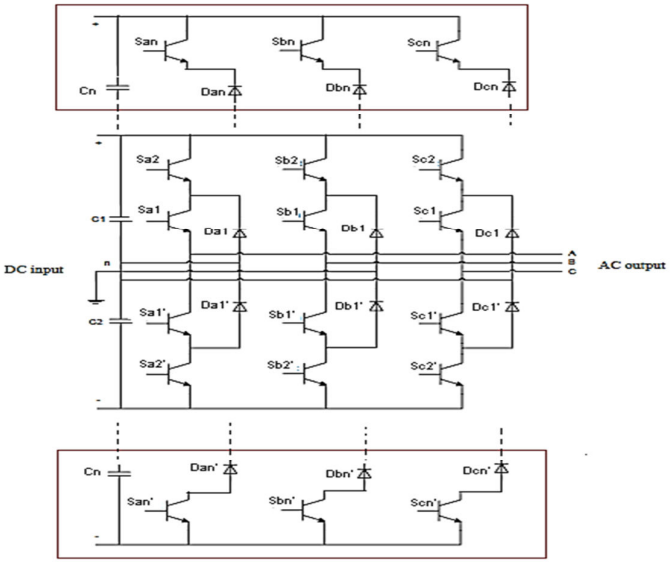

Fig. 1. General Structure for Three Phase NPCMI.

Figure 2 shows the basic structure of three-phase five-level NPCMI simulation model. In each phase leg, the forward voltage across each main power device is clamped by the connection of diodes between the main power devices and the DC capacitors rail. Table 1 below shows the switching state of five-level NPCMI inverter. $V1$ is considered as lower limit and $V5$ as the upper limit. At some stage in this NPC working, the switches near the neutral point are switch on for a longer time compared to the switches further away from the neutral point.

3. Graphical Method Analysis

Graphical method analysis has been carried out for 3-level [1], 5-level [2] and 7-level NPCMI with the aim of obtaining a low THDs output voltage waveform. This method utilised the ideal sinusoidal waveform as the basis of the calculation. For this GMA method, first the number of sections per phase leg is determined using the proposed Eqs. (1)-(3).

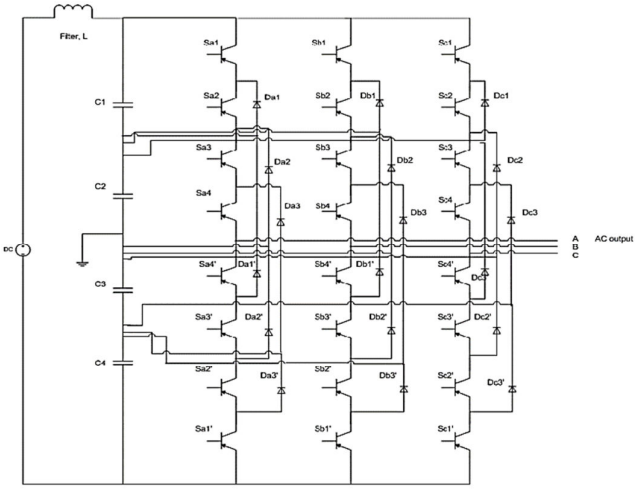

Fig. 2. Three-Phase Five-Level NPCMI Circuit.

Table 1. Switching State of Five-Level NPCMI.

	Sa1	Sa2	Sa3	Sa4	Sa1'	Sa2'	Sa3'	Sa4'
V1	0	0	0	0	1	1	1	1
V2	0	0	0	1	1	1	1	0
V3	0	0	1	1	1	1	0	0
V4	0	1	1	1	1	0	0	0
V5	1	1	1	1	0	0	0	0

Number of sections, S per phase leg, where m is number of levels.;

$$S = 2\,(m\text{-}1) \tag{1}$$

So, from Eq. (1), for a 5-level NPC, the number of section, S is 8 where the top section has 4 levels and bottom section also has 4 levels. Eq. (2) shows the Sinusoidal Waveform Intersection angle, where n is the number of odd levels; i.e., 1, 3, 5, … , n.

$$\alpha i_n = \sin^{-1}(n/S) \tag{2}$$

Based on this Sinusoidal Waveform Intersection angle, the switching duration for each IGBT at each level is calculated using Eq. (3).

Switching Duration, D;

$$D = 2\sin^{-1}(n/S) \pm 180° \tag{3}$$

Figures 3 and 4 show the Graphical Method Analysis for 5-level [2] and 7-level for NPC Multilevel Inverter where from Eqs. (1)-(3), the duration of each level are calculated and applied to each level. From the switching duration, D, the switching angle of each level are calculated and applied to the simulation model. Based on the equations and graphical figure, the angle of the switching have been determined to be 250°, 195°, 165° and 110° for Level 1, Level 2, Level 3 and Level 4

respectively for 5-Level NPC circuit. While for 7-level NPC circuit, the switching angles are 270°, 230°, 190°, 150°, 110° and 65° for Level 1 to Level 6 respectively.

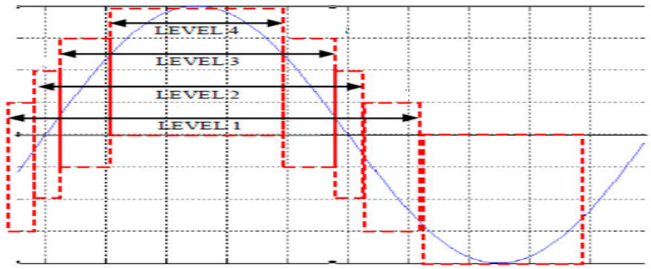

Fig. 3. Graphical Method Analysis for 5-Level NPCMI Circuit [2].

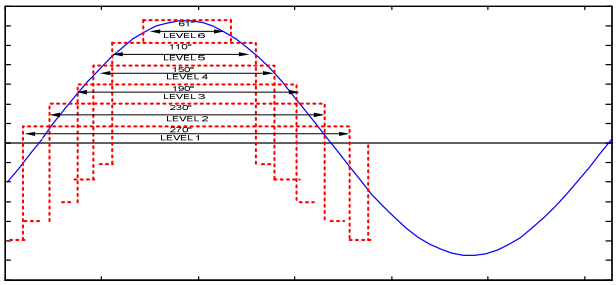

Fig. 4. Graphical Method Analysis for 7-Level NPCMI Circuit.

4. Results and Discussion

From the calculated triggering angles and switching states, their switching duration for each level of switches is determined. The values are then input to the simulation model that had been designed in the Matlab/Simulink software. Figures 5 and 6 shows the output voltage waveform for line-to-neutral voltage for 5-level NPC and line-to-line voltage NPC respectively. The THDs values of the output voltage are determined through the toolbox readily available in the software and tabulated in Table 2. Table 3 shows the THDs values of the output voltage for the others work of 5-level NPC.This shows that with the increment of number of NPC levels, the THDs values of the output voltage decrease and the proposed Graphical Method Analysis is able to obtain a low THDs value of the output voltage.

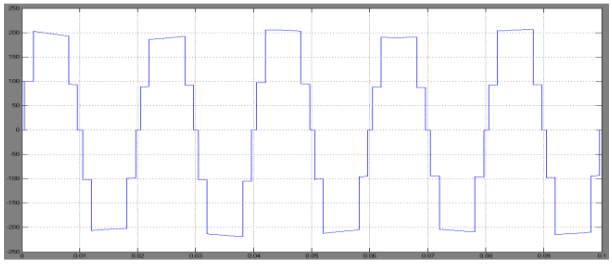

Fig. 5. Output Voltage Waveform for Line-to-Neutral Voltage, V_{LN} for 5-level NPCMI.

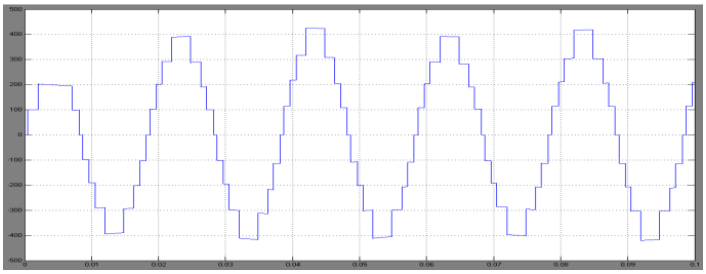

Fig. 6. Output Voltage Waveform for Line-to-Line Voltage, V_{LL} for 5-level NPCMI.

Table 2. THD for Different Level of NPCMI using Proposed Graphical Method Analysis (GMA).

THD (%)	No. of level NPCMI			No. of level (Cascade H-bridge)	
	3-level [1]	5-level [2]	7-level	7-level [3]	5-level [4]
V_{LL}	13.36	10.36	8.18	10.31	N/A
V_{LN}	29.44	18.45	16.00	17.06	37.80
I_L	29.44	18.45	16.00	N/A	N/A

Table 3. THDs Values of the Output Voltage for the Others Work of 5-level NPCMI.

	THD of Voltage line-to-line (V_{LL}), %	THD of Voltage line-to-neutral (V_{LN}), %	THD of Line current (I_L), %
GMA 5-level NPCMI [2]	10.58	18.62	18.62
PWM 5-level TCHB [12]	N/A	35.39	N/A
SPWM 5-level H-bridge [13]	N/A	18	N/A
PWM 5-level cascaded [14]	N/A	PDPWM 21.40 PODPWM 24.67 APODPWM 24.34	N/A
PWM 5-level cascaded [15]	N/A	45	N/A

5. Conclusions

A low THD values for a three phase 5-level and 7-level NPCMI using new proposed GMA has been successfully designed. The results obtained for this work have been compared to previous work using different switching angle determination method. From the comparison it showed that by using Graphical Method Analysis, lower THD value has been achieved for three phase 5-level NPC for both parameters, voltage line-to-neutral (V_{LN}) and voltage line-to-line (V_{LL}) as well as three phase 7-level NPCMI, the THD value for voltage line-to-neutral (V_{LN}) and line-to-line (V_{LL}) were lower than others.

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