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Deterministic assembly of releasable single crystal silicon-metal oxide field-effect devices formed from bulk wafers

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Deterministic assembly of ultrathin metal oxide-semiconductor field-effect transistors released from the surfaces of bulk wafers with (111) orientation provides a route to high quality electronics on nearly any type of substrate. Device parameters and bias stability characteristics from transistors on sheets of plastic confirm the effectiveness of the approach and the critical roles of thermally grown layers of silicon dioxide for the gate dielectrics and passivation layers. Systematic studies of the anisotropic etching processes used to release the devices illustrate capabilities into the sub-micron thickness regime, with beneficial effects on the bending stiffness and degree of bendability.
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Research in organic and inorganic materials for wearable/bio-integrated electronic devices has expanded rapidly in recent years.[1–5] Although the trend toward use of semiconductor nanomaterials has led to significant progress in various performance metrics, key limitations in cost, area coverage, and sophistication in function remain. Emerging strategies seek improved synergies between materials and manufacturing techniques used for these envisioned unconventional electronics systems and those associated with established silicon digital circuit technologies. For example, unusual device layouts and materials choices allow silicon metal oxide semiconductor field effect transistors (MOSFETs) fabricated on silicon-on-insulator (SOI) wafers to be released in ultrathin formats, suitable for integration on nearly any kind of substrate, including plastic and/or fabric.[6–8] Disadvantages arise from requirements for custom SOI wafers that use silicon with (111) orientation as the handle[6] and/or challenges in speed and accuracy of solution based assembly into desired arrays.[7–9] Recently, Zhai *et al.*[10] and Shahrjerdi *et al.*[11] reported alternative methods based on controlled exfoliation of MOSFETs from bulk silicon wafers and conventional SOI substrates, respectively. The main drawback is that the devices obtained in this manner[10] have rough bottom surface morphologies and relatively large thicknesses (20-30 μm), with corresponding limitations in bending stiffnesses and degrees of bendability. Moreover, the reported assembly/integration processes involve a one-to-one transfer of dense integrated circuits from the source wafer to the target substrate, with the potential to lead to prohibitively high costs for many applications due to inefficient utilization of the component devices. This situation is most significant in the many applications that require only sparse areal coverages of electronics, such as those in matrix arrays for displays, surgical monitoring systems, and others. Alternative approaches involve specialized wafers with embedded air gaps to enable removal of integrated circuits using pick-and-place techniques. The thicknesses are, however, large ($\sim$20 μm), and the throughput in assembly can be limiting, for certain cases.[12,13]

Other schemes could conceivably exploit anisotropic etching procedures and unconventional orientations of the silicon wafers. The (100) orientation, instead of (111), has traditionally been used for complimentary MOSFET (cMOS) fabrication due to improved electron mobility and reduced interface trap density.[14] Traps at the interface between the channel and the gate oxide degrade the mobility, subthreshold swing, threshold voltage, and operational stability.[15] Consequently, n-type MOSFETs built on (111) Si typically exhibit reduced mobility values (by approximately one third) compared to those on (100) Si.[16] The (111) orientation, however, has some appeal due to its ability to facilitate fabrication of vertical MOSFET structures, where 3D multi-gate structures improve performance by increasing the effective channel area per unit volume.[17] In addition, recent experimental studies indicate that MOSFET performance parameters, including reliability characteristics, are independent of silicon orientation when the gate oxide thickness is less than 2.0 nm, due to the dominant role of direct tunneling in this regime. (One parameter, n-type field-effect mobility is still lower than that of (100) Si)[18] As a result, there might

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be some value in revisiting the potential role of Si (111) substrates in certain cases. Here we introduce materials and device designs that allow highly flexible silicon MOSFETs to be formed directly from (111) wafers. Optimized configurations allow release from the wafer to enable high speed deterministic assembly of large collections of individual devices onto substrates of interest in programmable layouts and coverages by transfer printing.[19,20] Detailed electrical characterization of the devices and studies of process scaling with thickness illustrate some of the essential physics and materials science of this approach.

Figs. 1(a)–1(d) outline the steps for building releasable MOSFETs via a sequence of schematic illustrations and microscope images. Overall, various modified processes in semiconductor fabrication yield dense arrays of devices in rectangular shapes oriented parallel to the ⟨110⟩ direction of the underlying wafer. This configuration allows directional wet etching of the underlying (111) wafer in a manner that undercuts the devices but leaves each one tethered to the substrate by narrow bridges (i.e., "anchors") located at two of their four corners. In this layout, any subset of the MOSFETs can be removed from the wafer by van der Waals contact with a soft elastomer that has matching features of relief on its surface. A printing step then delivers these MOSFETs to a substrate of interest; sequential repetition of this process yields desired assemblies in layouts of choice. The processing begins with patterned solid state doping of phosphorous to form n+ regions for source and drain contacts on a (111) bulk wafer (Virginia Semiconductor, Inc. low miscut; orientation $\langle 111 \rangle \pm 0.1^\circ$, boron doped p-type wafer (resistivity: 8–15 Ω cm) with 700 nm SiO_2 for doping mask). Each device incorporates two anchors (3 μm wide, 15 μm long) defined by a reactive ion etching procedure (STS silicon RIE, Surface Technology Systems plc) that also sets the overall lateral dimensions. The gate dielectric consists of a thermal oxide (50 nm thick) grown at 1100 °C for 17 min. This step also forms oxide on the sidewalls of the etched trenches. Patterned deposition of metal (300 nm thick Cr deposited by sputtering (ATC 200, AJA international)) creates source, drain, and gate electrodes (Fig. 1(a)). Uniform passivation of the entire substrate with a thick layer (800 nm) of low stress SiN_x (by STS PECVD, Surface Technology Systems plc) protects the gate dielectric and the contacts. To prepare for undercut wet chemical release, a reactive ion etching (PlasmaTherm) step removes the top SiN_x layer (800 nm), the SiO_2 layer (50 nm), and the silicon to a depth of ~2 μm (Fig. 2(b)). Immersing the wafer in a boiling solution of TMAH (tetramethyl ammonium hydroxide, 25% H_2O) for 90 min etches the underlying silicon anisotropically along the ⟨110⟩ direction (Fig. 1(c)). After this undercut, the devices are ready for release and assembly onto foreign substrates by transfer printing.[19,20] Fig. 1(d) illustrates this process as applied to a single device. The anchors fracture immediately upon soft contact with the elastomeric stamp, where the devices remain adhered by van der Waals forces.

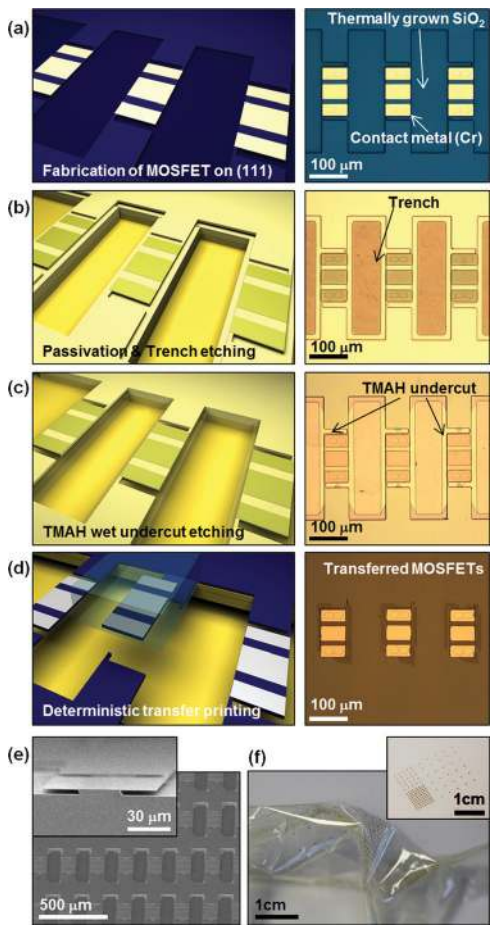

FIG. 1. Schematic illustrations and optical microscope images of steps for forming releasable single crystal silicon MOSFETs on bulk wafers and their deterministic assembly on foreign substrates by transfer printing, including (a) fabrication of single crystal silicon MOSFETs oriented along the ⟨100⟩ direction on the surface of a bulk (111) wafer, with thermal gate oxide and metallization for source/drain and gate electrodes, (b) uniform deposition of a layer of SiN_x followed by etching of trenches between the devices, (c) wet anisotropic undercut etching using TMAH, (d) manipulation of MOSFETs by transfer printing, and (e) SEM images of devices completely and partially undercut (inset). (f) 150 MOSFETs fabricated in this manner after transfer printing onto a substrate of ultrathin PET with thickness of 2.5 μm. The devices were printed in 9 by 10 arrays with 1 mm pitch (bottom left), 5 by 5 arrays with 2 mm pitch (top left), and 7 by 5 arrays with 4 mm pitch as shown in inset image.

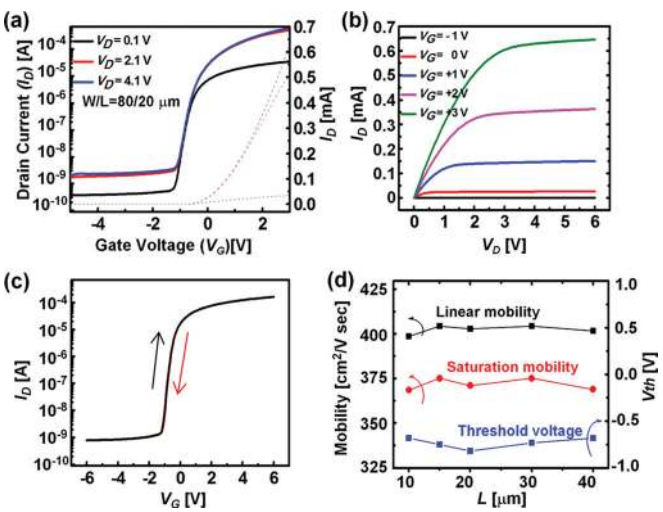

FIG. 2. (a) Transfer characteristics of a MOSFET with $W/L = 80/20\ \mu$m printed onto a sheet of polyimide. Colored solid and dashed lines correspond to drain currents at various drain voltages in logarithmic and linear scales, respectively. (b) Output characteristics at increasing gate voltages. (c) Transfer characteristics measured with gate voltage sweeps from negative to positive (black) and from positive to negative (red). (d) Linear and saturation mobility and threshold voltage as a function of channel length.

The right image in Fig. 1(d) shows three MOSFETs transferred onto a sheet of polyimide (PI; 1.2 μm thick). Fig. 1(e) presents a scanning electron microscope (SEM) image of the sample shown in Fig. 1(c). Here, the inset corresponds to a cross-sectional view of a partially undercut etched device. An image of 150 MOSFETs assembled on an ultrathin sheet of polyethylene terephthalate (PET) (2.5 μm thick, Mylar® film, Chemplex® industries) appears in Fig. 1(f) (after deformation) and its inset (before deformation). These devices are arranged in a 9×10 array with 1 mm pitch (bottom left), a 5×5 array with 2 mm pitch (top left), and a 7×5 array with 4 mm pitch.

Electrical measurements of n-type MOSFETs on PI are shown in Figs. 2(a)–2(d). The transfer characteristics (channel width, $W = 80\,\mu$m, and length, $L = 20\,\mu$m) are presented in Fig. 2(a) for three different drain voltages ($V_D = 0.1$, 2.1, and 4.1 V) in both logarithmic (solid) and linear (dashed) scales. The on/off ratio is $>10^5$, and the threshold voltage (V_{th}) is ~ -0.72 V. Using the measured thickness of the gate oxide (50 nm) and the dielectric constant of thermal SiO_2 (3.9), the gate capacitance, C_{ox}, is calculated to be 69.1 nF cm^{-2}. From Fig. 2(a), the maximum transconductance, g_m, is 11.5 μS for $V_D = 0.1$ V. The linear mobility is defined by

$$\mu_{lin} = \frac{L}{W} \cdot \frac{g_m}{C_{ox} V_D}\bigg|_{V_D \to 0}, \tag{1}$$

and the saturation mobility is

$$\mu_{sat} = \frac{2L}{WC_{ox}} \left[\left(\frac{\partial I_D^{1/2}}{\partial V_G} \right)\bigg|_{V_D} \right]^2, \tag{2}$$

where V_G is the gate voltage. The values of μ_{lin} and μ_{sat} are $\approx$405 cm^2 V^{-1} s^{-1} and $\approx$370 cm^2 V^{-1} s^{-1}, respectively. The output electrical characteristics shown in Fig. 2(b) illustrate expected saturation behavior at high drain voltages. Moreover, the device exhibits little gate induced hysteresis, as illustrated in forward and reverse gate voltage sweeps between -6 V and 6 V, as in Fig. 2(c). The key properties, μ_{lin}, μ_{sat}, and the threshold voltage, V_{th}, at different L (10, 15, 20, 30, and 40 μm) appear in Fig. 2(d); invariance with L is consistent with behavior that is dominated by the channel and not the contacts. For five representative MOSFETs, the on and off currents lie between 0.423 and 0.448 mA and 4.36 and 4.79 nA, respectively, at $V_D = 4.1$ V. Other parameters exhibit similarly low variations from device to device. The thermal gate dielectric is important to these good performance attributes, due to the high quality of the Si and SiO_2 interface and its ability to minimize carrier scattering and trapping. This interface is also key to optimizing for stable operation.[11,15] The unpassivated bottom surface can be a concern. To examine effects of bias stress, we applied V_{GS} of +2 V and -2 V while holding V_{DS} at 0.1 V, as shown in Figs. 3(a) and 3(b), respectively. The off-current increases and decreases significantly for the positive and negative cases, respectively. Interestingly, the off-current slightly increases with increasing V_{GS}. This behavior is different from that of conventional MOSFET's, where instability in gate induced drain leakage typically leads to increasing

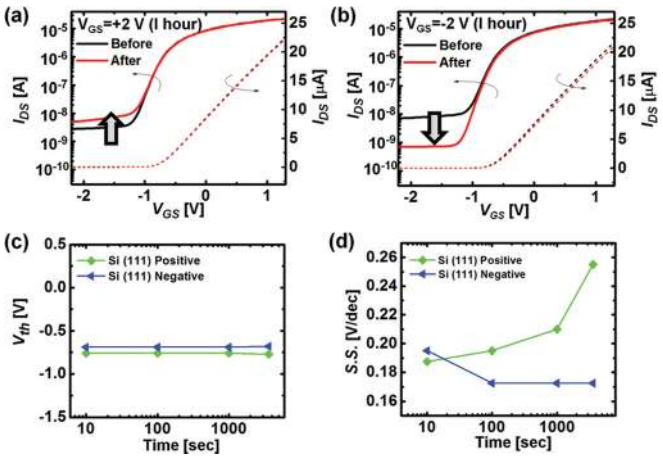

FIG. 3. Transfer characteristics of a MOSFET printed onto a polyimide substrate after (a) positive and (b) negative biases applied on the gate electrode for an hour. Variation in (c) threshold voltage (V_{th}) and (d) subthreshold slope ($S.S.$) as a function of duration of bias stress.

off-current with decreasing V_{GS}.[21] Instead, observations in our devices resemble those associated with materials selections and process conditions for passivation layers in a-Si:H thin film transistors.[22] Passivating the back surfaces of our devices with thermally grown SiO_2 results in exceptional off-current stability (i.e., no change) for both positive and the negative bias stresses.[6]

The evolution of V_{th} and $S.S.$ are shown in Figs. 3(c) and 3(d). The V_{th} values remain unaffected throughout the stress conditions. The increases in $S.S.$ induced by positive bias stress may reflect the creation of current induced defects in the channel.[23] The negative bias stress, on the other hand, causes a slight improvement in $S.S.$, and slight decrease in on-current (Fig. 3(b)), corresponding to a $\sim$2% reduction in mobility.

For flexible electronics, the degree of bendability is inversely proportional to the thickness, while the bending stiffness is directly proportional to the cube of thickness.[24] The ability to form devices with small thicknesses can, therefore, be important

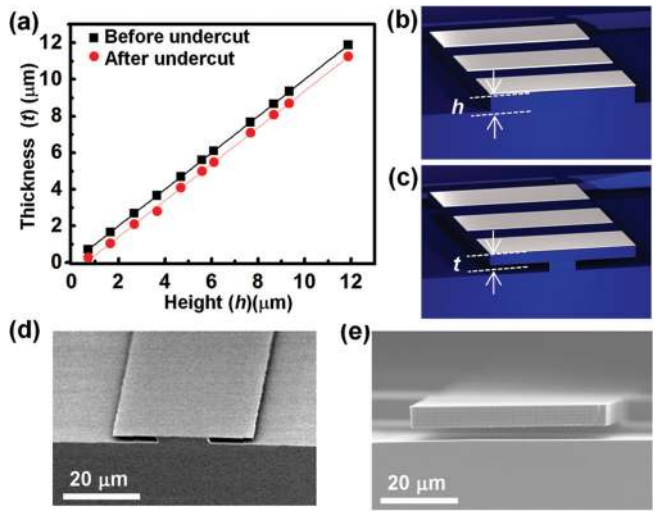

FIG. 4. Capabilities for achieving thicknesses of released device silicon, from several microns to several hundred nanometers. (a) Depth of initial trench (black dots; frame (b)) and undercut device thickness (red dots; frame (c)) after wet anisotropic undercut etching (TMAH, for 60 min at 100 °C). Cross sectional views of representative results, at thicknesses of 800 nm (d) and 11 μm (e).

in many cases. Systematic studies appear in Fig. 4(a), which show the relation between silicon thickness (t) (Fig. 4(c)) and trench height (h) (Fig. 4(b)). Here, the black squares represent the thicknesses and heights for slabs prior to undercut; the red dots represent them after undercut. The ratio of etching rates along (111) and (110) planes is ~0.02 for 25% TMAH etching solution.[25] As a result, the initial thickness ((h) black dots, before etching) is reduced to a smaller value by the etching ((t) red dots; after etching). Our data show a reduction of ~500 nm for 1 h of etching, corresponding to a lateral etch distance of up to ~25 μm, and released strips with widths as large as ~50 μm. Figs. 4(d) and 4(e) show representative cross-sectional SEM images for cases of 800 nm and 11 μm thick silicon slabs, respectively. These data suggest the ability to support device thicknesses in the sub-micron regime.

In summary, the concepts reported here might provide an attractive route to mechanically deformable electronics using assemblies of high performance single crystalline silicon MOSFETs fabricated on and then released from bulk wafers. Although the key performance parameters exceed previous results based on silicon derived from (111) oriented wafers,[26,27] MOSFETs[6] fabricated with (100) oriented silicon on plastic substrates reach mobilities $>700\,cm^2\,V^{-1}\,s^{-1}$ and on/off ratios $>10^7$. The difference is, at least partly, a consequence of higher trap density on the (111) surface compared to (100).[21] Nevertheless, the properties of the devices are better than those of most other alternatives for flexible electronics.

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[1]S.-W. Hwang, H. Tao, D.-H. Kim, H. Cheng, J.-K. Song, E. Rill, M. A. Brenckle, B. Panilaitis, S. M. Won, Y.-S. Kim, Y. M. Song, K. J. Yu, A. Ameen, R. Li, Y. Su, M. Yang, D. L. Kaplan, M. R. Zakin, M. J. Slepian, Y. Huang, F. G. Omenetto, and J. A. Rogers, Science **337**, 1640 (2012).
[2]T. Sekitani and T. Someya, MRS Bull. **37**, 236 (2012).
[3]S. C. B. Mannsfeld, B. C. K. Tee, R. Stoltenberg, C. V. H. H. Chen, S. Barmann, B. V. O. Muir, A. N. Sokolov, C. Reese, and Z. Bao, Nat. Mater. **9**, 859 (2010).
[4]C. Pang, G.-Y. Lee, T.-i. Kim, S. M. Kim, H. N. Kim, S.-H. Ahn, and K.-Y. Suh, Nat. Mater. **11**, 795 (2012).
[5]K. Takei, T. Takahashi, J. C. Ho, H. Ko, A. G. Gillies, P. W. Leu, R. S. Fearing, and A. Javey, Nat. Mater. **9**, 821 (2010).
[6]H.-J. Chung, T.-i. Kim, H.-S. Kim, S. A. Wells, S. Jo, N. Ahmed, Y. H. Jung, S. M. Won, C. A. Bower, and J. A. Rogers, Adv. Funct. Mater. **21**, 3029 (2011).
[7]S. W. Lee and R. Bashir, Adv. Mater. **17**, 2671 (2005).
[8]S. A. Stauth and B. A. Parviz, Proc. Natl. Acad. Sci. U.S.A. **103**, 13922 (2006).
[9]R. J. Knuesel and H. O. Jacobs, Proc. Natl. Acad. Sci. U.S.A. **107**, 993 (2010).
[10]Y. Zhai, L. Methew, R. Rao, D. Xu, and S. K. Banerjee, Nano Lett. **12**, 5609 (2012).
[11]D. Shahrjerdi and S. W. Bedell, Nano Lett. **13**, 315 (2013).
[12]J. N. Burghartz, W. Appel, H. D. Rempp, and M. Zimmermann, IEEE Trans. Electron Devices **56**, 321 (2009).
[13]E. A. Angelopoulos, M. S. Al-Shahed, W. Appel, S. Endler, S. Ferwana, C. Harendt, M. Hassan, H. Rempp, M. Zimmermann, and J. N. Burghartz, in *Solid-State Device Research Conference (ESSDERC) 2012: Proceedings of the European*, Bordeaux, France, 17–21 September 2012, edited by Y. Deval (IMS Lab, University of Bordeaux, France), pp. 141–144.
[14]R. F. Pierret, *Semiconductor Device Fundamentals* (Addison-Wesley, Natick, MA, 1996), Chap. 18.
[15]G. Barbottin and A. Vapaille, *Instabilities in Silicon Devices* (Elsevier, Amsterdam, 1989), Vol. 2, Chap. 15.
[16]S. Takahi, A. Toriumi, M. Iwase, and H. Tango, IEEE Trans. Electron Devices **41**, 2363 (1994).
[17]C. Fink, K. G. Anil, H. Geiger, W. Hansch, F. Kaesen, J. Schulze, T. Sulima, and I. Eisele, Solid State Electron. **46**, 387 (2002).
[18]H. S. Momose, T. Ohguro, S. Nakamura, and Y. Toyoshima, IEEE Trans. Electron Devices **49**, 1597 (2002).
[19]M. A. Meitl, Z.-T. Zhu, V. Kumar, K. J. Lee, X. Feng, Y. Y. Huang, I. Adesida, R. G. Nuzzo, and J. A. Rogers, Nat. Mater. **5**, 33 (2006).
[20]A. Carson, A. M. Bowen, Y. Huang, R. G. Nuzzo, and J. A. Rogers, Adv. Mater. **24**, 5284 (2012).
[21]J. H. Stathis and S. Zafar, Microelectron. Relab. **46**, 270 (2006).
[22]Y.-K. Choi, D. Ha, T.-J. King, and J. Bokor, Jpn. J. Appl. Phys. **42**, 2073 (2003).
[23]Y. Kuo, *Thin Film Transistors Materials and Processes* (Klewer Academic, Norwell, MA, 2004), Vol. 1, Chap. 6.
[24]J. A. Rogers, M. G. Lagally, and R. G. Nuzzo, Nature (London) **477**, 45 (2011).
[25]K. Sato, M. Shirkida, T. Yamashiro, K. Asaumi, Y. Iriye, and M. Yamamoto, Sens. Actuators, A **73**, 131 (1999).
[26]S. Mack, M. A. Meitl, A. J. Baca, Z.-T. Zhu, and J. A. Rogers, Appl. Phys. Lett. **88**, 213101 (2006).
[27]A. J. Baca, M. A. Meitl, H. C. Ko, S. Mack, H.-S. Kim, J. Dong, P. M. Ferreira, and J. A. Rogers, Adv. Funct. Mater. **17**, 3051 (2007).