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Developed cascaded multilevel inverter topology to minimise the number of circuit devices and voltage stresses of switches

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Abstract: In this study, a novel structure for cascade multilevel inverter is presented. The proposed inverter can generate all possible DC voltage levels with the value of positive and negative. The proposed structure results in reduction of switches number, relevant gate driver circuits and also the installation area and inverter cost. The suggested inverter can be used as symmetric and asymmetric structures. Comparing the peak inverse voltage and losses of the proposed inverter with conventional multilevel inverters show the superiority of the proposed converter. The operation and good performance of the proposed multilevel inverter have been verified by the simulation results of a single-phase nine-level symmetric and 17-level asymmetric multilevel inverter and experimental results of a nine-level and 17-level inverters. Simulation and experimental results confirmed the validity and effectiveness performance of the proposed inverter.

1 Introduction

A multilevel inverter is a power electronic device that has been given more attention since introduced early in 1980s [1]. The desired output voltage of multilevel inverters is synthesized by several discrete DC sources [2]. With increasing the number of DC sources, the number of levels in output waveform increases and the output voltage approaches nearly sinusoidal waveform while employing a fundamental frequency-switching method [3]. The multilevel inverters are used in various applications such as renewable energy interfaces circuit [4, 5], flexible alternating current transmission devices [6, 7] and high voltage direct current [8, 9]. For the purpose of comparison with the traditional two-level configuration, it is needed to mention to both merits and demerits together. Multilevel inverters have more advantages with respect to the traditional two-level configurations; nevertheless, just more important ones are mentioned here: high-power quality [10, 11]. However, the main disadvantages of multilevel structures against the traditional two-level configuration are more number of required elements and so the inverter circuit and control scheme will be complex. Therefore the cost of inverter is increased and its reliability is reduced [12]. Therefore reducing the number of circuit devices is the main concern from the point of design. The initial prototype of multilevel inverters is three-level neutral point clamped (NPC) inverter [13]. In NPC, the desired output voltage is attained by combinations of series capacitors voltage. The NPC inverters have some problems, such as clamping diodes and the balance of the DC-link capacitors while the number of output voltage level is increased [14]. An alternative for NPC was a new topology based on the interconnection of several modular structures, called cells, in different paths which were named multicell topology. Many subtopologies and hybrid topologies including their own control scheme based on multicell topologies have been derived. Cascaded multicell (CM) and flying capacitor (FC) are the main inspired from traditional multicell configuration [15–17]. The FC employs floating capacitors to clamp the voltage levels. In FC, more number of steps in output voltage can be produced by clamping several DC voltages of FCs. However, to maintain the FCs voltage at target values there is a need to more complex control scheme [18, 19]. The multicell topologies are simply scalable, and present some benefits while operating at internal fault states because of the existence of redundant states [20]. Also CMs are more attractive because of their modular nature, and uncomplicated control scheme and simpler implementation [21]. In this paper, a new modular configuration for cascaded multilevel inverters that generates a large number of steps with a low number of circuit devices is proposed. The proposed topology can be used as asymmetric and symmetric multilevel inverters. The proposed topologies control scheme is as simple as the cascaded multilevel inverter. In addition, to calculate the required magnitudes of DC voltage sources two different are proposed.

At the end of this paper, provided simulation and experimental results verify the advantages of proposed

multilevel inverter. The rest of this paper is organised as follows. The proposed topology is detailed in Section 2. In Section 3, the traditional cascaded multilevel inverter is briefly explained and the comparison results between the suggested inverter and traditional cascaded inverter is provided in Section 4. In Section 5, the power loss calculation for the proposed inverter is formulated. The simulation and experimental results are obtained in Sections 6 and 7. Finally, in Section 8 the conclusion is presented.

2 Proposed topology

Fig. 1 defines the proposed multilevel inverter topology. The proposed topology consists of n-isolated DC voltage sources, (n is even and more than 4), which makes it suitable to be used in photovoltaic systems because of viability of several isolated DC sources.

The proposed inverter with $2n+4$ switches is able to generate zero or positive and negative polarity voltages. As shown in Fig. 1, each switch in the proposed topology is composed of one IGBT and an anti-parallel diode and each switch requires one gate driver. Both switches, S_i and $\bar{S}_i$ are complementary in the whole operation cycle. Also switches H_i and $\bar{H}_i$ are turned on as complementary in each time. Output phase voltage is synthesized by summing the DC-source voltages. It can be seen from Fig. 1 that the proposed topology uses n-DC voltage sources with values of V_1 and V_2. The values of V_1 and V_2 can be equal or not.

The maximum output voltage ($V_{o\max}$) of the proposed structure is the sum of amplitude of n-individual voltage sources which is given in (1)

$$V_{o\max} = \frac{n}{2}(V_1 + V_2) \tag{1}$$

where n is the number of DC voltage sources.

The upper bound of number of output voltage levels for suggested topology can be obtained as follows

$$m = 2\frac{V_{o\max}}{V_1} + 1; \quad \text{in general case } V_2 > V_1 \tag{2}$$

Converter loss is one of the important parameters that must be noted in power electronic converter designing.

Power electronics converter losses is related to conduction losses and switching losses. For proposed topology, always $n+2$ switches must be turn on in various operation modes of inverter. Assuming that the forward voltage of switches is V_d; therefore the maximum output voltage is calculated as

$$V_{o\max} = \sum_{i=1}^{n} V_i - (n+2)V_d \tag{3}$$

Another parameter that is used for comparison of different topologies of inverters is peak inverse voltage (PIV). The total PIV of switches in the proposed topology in Fig. 1 is illustrated as

$$\text{PIV} = 2n^* \left(V_1 + V_2\right) \tag{4}$$

With note to the modular structure of the proposed topology, a solution for increasing the number of output voltage levels is to increase the number of switches and DC voltage sources. This method has a high cost. Therefore to reduce the costs and the number of elements, we can use the asymmetric multilevel inverter structure.

Relations given in (1)–(4) are true for both symmetric and asymmetric structures.

Asymmetric scheme is obtained when DC voltage sources can be defined with different values. To increase output voltage levels using asymmetrical DC sources instead of increasing the circuit devices is commodious. Although the closest prior inverter scheme [22] to the suggested topology is just a symmetric one and must use more circuit devices when increasing the voltage levels is needed.

In this paper, two different methods are suggested to determine the magnitudes of DC voltage sources for proposed multilevel inverter. All levels of output voltage can be generated in both methods.

2.1 First method

With assumption that the magnitude of all DC voltage sources in Fig. 1, V_1 and V_2, to be same and equal to V_{dc}, the symmetrical multilevel structure is achieved. The upper bound of number of output voltage levels of the inverter with n-DC voltage sources can be calculated as

$$m = 2n + 1 \tag{5}$$

The maximum output voltage can be evaluated by (6)

$$V_{o\max} = nV_{\text{dc}} \tag{6}$$

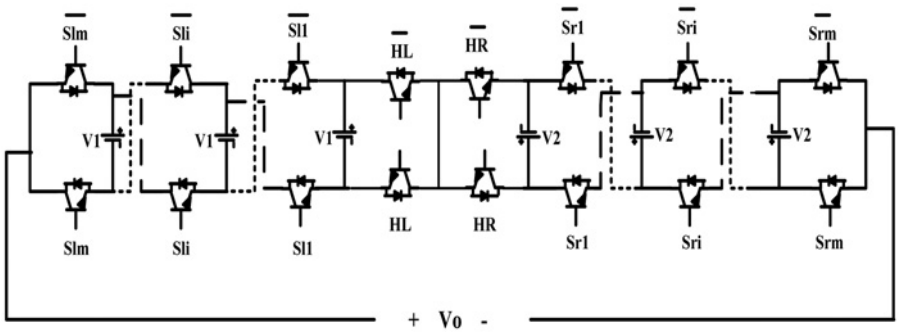

Fig. 1 *Overall scheme of the proposed multilevel inverter topology*

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Table 1 Comparison of requirements power component for the proposed multilevel inverter

	Symmetric	Asymmetric
no. of DC sources	N	N
no. of switches	$2n+4$	$2n+4$
no. of output levels	$2n+1$	$n*(p+1)+1$
maximum voltage	$n*V_1$	$n/2*(p+1)*V_1$
PIV	$4n*V_1$	$2n*(p+1)*V_1$
no. of on-state switches	$n+2$	$N+2$

2.2 Second method

In the proposed topology, V_2 can be set to be $p*V_1$, where $p = 2, 3, \ldots, n+1$; with this setting, the multilevel inverter known as asymmetric inverter, which gives a substantial increasing in the number of output levels. In previous schemes, with assumption $V_2 = p*V_1$, all steps in output voltage can be generated and value of each steps will be equal with V_1. For an asymmetric inverter with n-DC voltage sources and $V_2 = p*V_1$, the maximum output voltage and upper bound of number of output levels can be calculated as follows

$$V_{o\max} = \frac{n}{2}(1+P)V_1$$

$$m = n*(p+1)+1 \tag{7}$$

The number of requirement components for proposed symmetric and asymmetric multilevel inverters is given in Table 1.

3 Traditional cascade multilevel inverters configuration

Fig. 2 shows a single-phase topology of a cascade inverter with isolated DC voltage sources. Its output voltage is obtained by summing the output voltages of each bridge. Each bridge with four switches and a DC voltage source can generate three-level square-wave output voltage waveform. The maximum output voltage ($V_{o\max}$) of the cascaded multilevel inverter with n-DC voltage sources with values of V_1 and V_2, similar to the proposed inverter, also is illustrated in (1). The maximum number of output voltage levels (m) can be obtained from (2).

It is noted that always $2n$ switches must be turn on in various operation modes of cascaded inverter. Therefore the maximum output voltage can be defined as

$$V_{o\max} = \sum_{i=1}^{n} V_i - 2nV_d \tag{8}$$

where V_d is the forward voltage of each switch. Instead of increasing the number of H-bridges for obtaining more number of output voltage levels, the asymmetric cascaded multilevel structure can be used. For both symmetric and asymmetric cascaded multilevel inverter, the mentioned (1), (2) and (4) are true. In this structure, the total PIV of switches is illustrated as

$$\text{PIV} = \sum_{i=1}^{n} 4V_{i'} \tag{9}$$

where V_d is the value of the ith DC voltage source in the cascaded multilevel inverter with n-DC voltage sources. The substantial advantage of this topology is the modularity of control and protection requirements of each bridge and its drawback is the great number of switches. In the proposed inverter, the number of circuit devices is reduced.

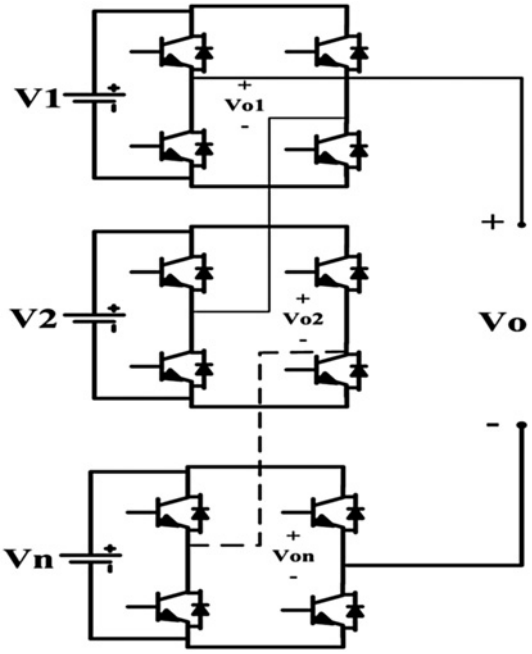

Fig. 2 *Single phase of the traditional cascade multilevel inverter*

Table 2 Comparison of power component requirements for the traditional cascade inverter

	Symmetric	Asymmetric
no. of DC sources	N	n
no. of switches	$4n$	$4n$
no. of output levels	$2n+1$	$n*(p+1)+1$
maximum voltage	$n*V_1$	$(n/2)*(p+1)+1$
PIV	$4n*V_1$	$2n*(p+1)*V_1$
no. of on-state switches	$2n$	$2n$

For comparison, the suggested methods for the proposed multilevel inverter that is illustrated in Section 2 are used for traditional cascaded inverter. To create the same conditions for comparison proposed topology, the half of DC voltage sources ($n/2$) are considered V_1 and other V_2 in the cascaded topology.

The number of requirement components for the traditional symmetric and asymmetric cascaded inverter is given in Table 2.

4 Comparison between proposed inverter and traditional cascaded multilevel inverter

This paper presents a novel topology for multilevel inverter with reduced number of components.

Considerable issues in multilevel inverters are the number and rating of switches.

It can be seen from Tables 1 and 2 that the number of switches in the proposed inverter is appreciably lower than the traditional cascaded inverter with same levels for symmetric and asymmetric structures.

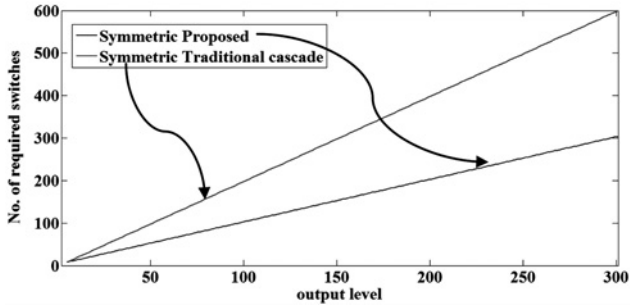

Fig. 3 *Number of required switches for proposed and traditional cascaded symmetric multilevel inverter against output voltage levels*

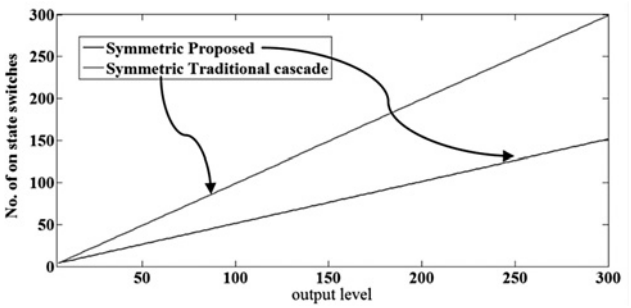

Fig. 4 *Number of on-state switches against output voltage levels for the proposed and traditional cascaded symmetric multilevel inverters*

Also, voltage and current rating of the semi-conductor switches play significant roles on the cost and realisation of the inverters.

In the proposed topology, the current of all switches are equal with load current. The PIV is one of the criteria for comparing different topologies of inverters. Tables 1 and 2 indicate the total PIV of the switches in the proposed multilevel inverter is lower than the traditional cascaded inverter. Number of on-state switches is important in conduction losses. Number of on-state switches in the proposed topology is lower than the traditional cascade inverter. Therefore the converter losses will be reduced.

Figs. 3 and 4 represent the comparison results of the proposed and traditional cascaded multilevel inverters from different points of view.

It can be seen from these figures that the proposed topology needs fewer switches for realising output voltage levels. This sufficiency reduces the installation area and the number of the gate driver circuits. Therefore the cost of the proposed topology will be lower than the traditional topology for realising the same output voltage levels. The total power loss of switches which causes undesired voltage drop depends on the number of on-state switches. So, the number of on-state switches is considered as an important term to compare the different topologies, as illustrated in (3) and (8).

As shown in Fig. 4, the number of on-state switches for the proposed inverter is lower than the traditional cascaded structure and therefore the conduction losses of the proposed topology will be less than the traditional cascade topology.

5 Power losses calculation

As illustrated before, commonly two types of losses are mentioned in inverters. The on-state resistance and voltage drop of the switches are the factors of conduction losses. The switching losses are the results of non-ideal operation of switches. The below paragraph is organised to calculate the losses of the proposed multilevel inverter. For calculating the conduction losses, at first, a typical power switch conduction losses are computed and then they are expanded to the proposed inverter. It is noted that each power switch includes a transistor and a diode, in which both have power losses. Equations (10) and (11) are the instantaneous conduction losses, in which $P_{c.\mathrm{T}}(t)$ and $P_{c.\mathrm{D}}(t)$ describe the transistor and diode losses, respectively [23]

$$P_{c.\mathrm{T}}(t) = \left[V_{\mathrm{T}} + R_{\mathrm{T}} i^{\beta}(t)\right] i(t) \tag{10}$$

$$P_{c.\mathrm{D}}(t) = \left[V_{\mathrm{D}} + R_{\mathrm{D}} i(t)\right] i(t) \tag{11}$$

where V_{T} and V_{D} are considered as the on-state voltage of the transistor and diode, respectively, and β is a constant dependent to the specification of the transistor and usually is close to 0.5.

Table 3 Switching states nine-level proposed inverter

Output voltage level	SI2–SI1–HL–HR–Sr1–Sr2
−4E	(1 1 0 0 1 1)
−3E	(1 1 0 0 1 0)
−2E	(1 1 0 0 0 1)
−E	(1 1 1 1 1 0)
0	(1 0 0 0 0 1)
E	(0 0 0 0 0 1)
2E	(0 0 1 1 1 0)
3E	(0 0 1 1 0 1)
4E	(0 0 1 1 0 0)

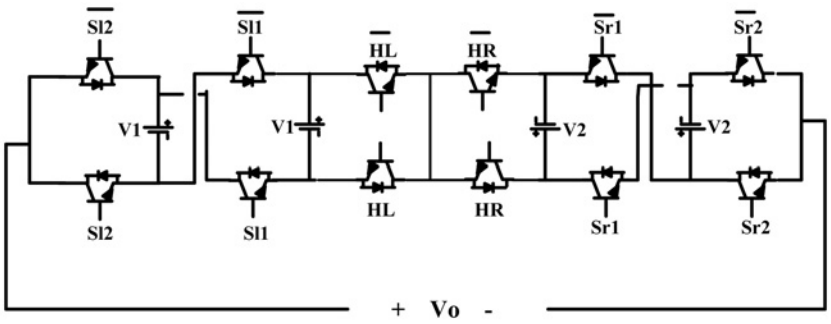

Fig. 5 *Symmetric nine-level proposed inverter ($V_1 = V_2$)*

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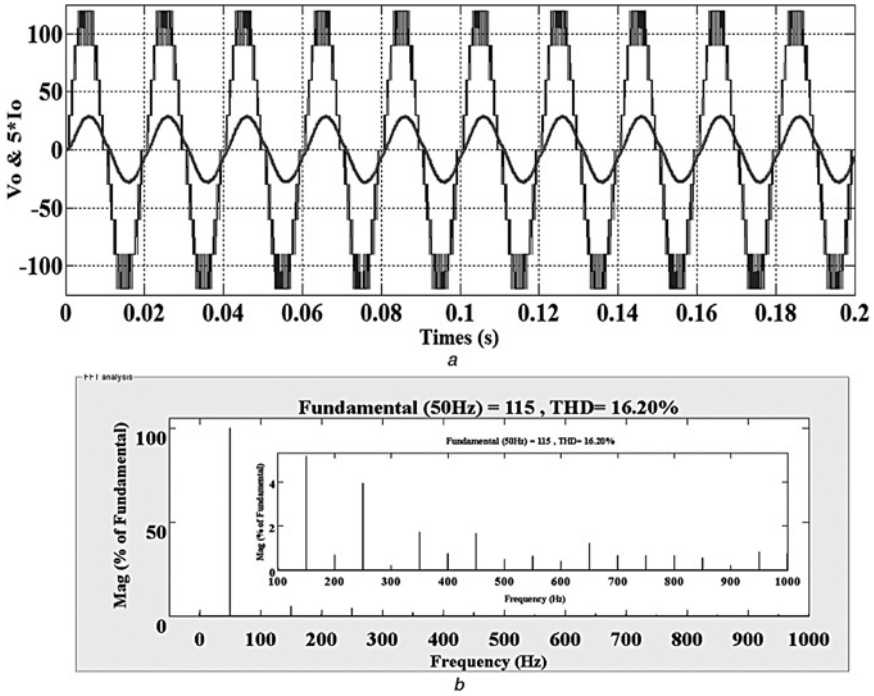

Fig. 6 *Output voltage and load current of the proposed symmetric nine-level inverter and harmonic spectra for output voltage*

a Voltage and current waveform
b Harmonic content of the proposed nine-level inverter

R_T and R_D are the equivalent on-state resistance of the transistor and diode, respectively.

The specifications of the used power switches in different multilevel inverters may be various. In the proposed inverter, at any time there are $N_T(t)$ transistors and $N_D(t)$ diodes in the current path. The value of $N_T(t)$ and $N_D(t)$ is related to the output voltage level and operating conditions (essentially direction of the current). Therefore using (10)

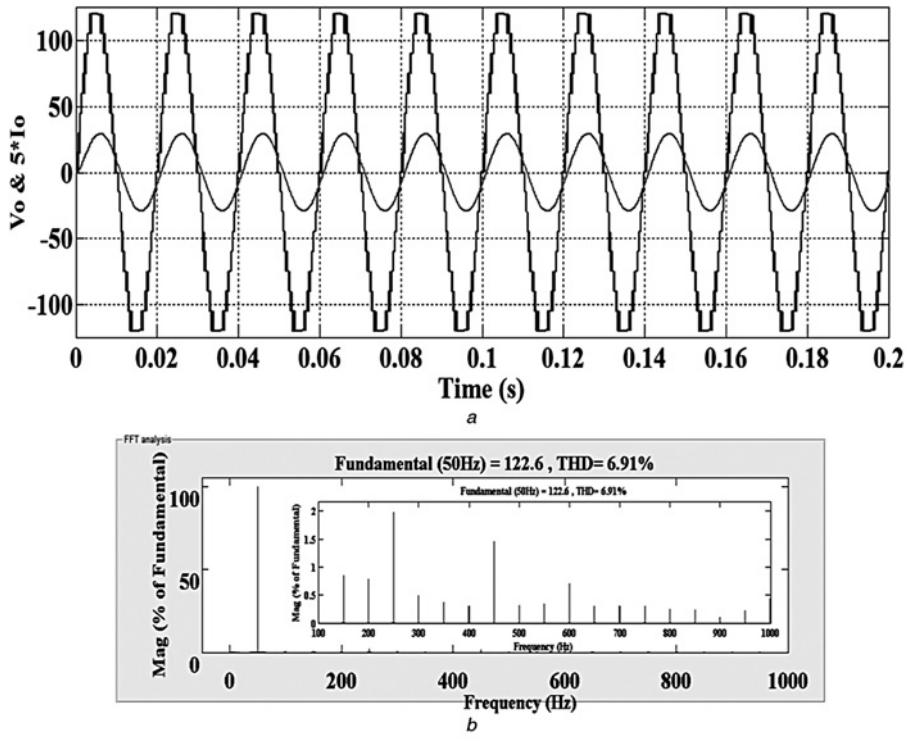

Fig. 7 *Output voltage, load current and harmonic spectra of asymmetric 17-level inverter*

a Voltage and current waveform
b Harmonic content of the proposed 17-level inverter

and (11), the average conduction power loss of the proposed multilevel inverter can be calculated as follows

$$P_c = \frac{1}{\pi}\int_0^{\pi} \left(N_{\mathrm{T}}(t) * P_{c.\mathrm{T}}(t) + N_{\mathrm{D}}(t) * P_{c.\mathrm{D}}(t)\right) \mathrm{d}(\omega t) \quad (12)$$

The switching losses are calculated for a typical power switch and then the results are developed to the proposed multilevel inverter. To evaluate switching losses, the linear approximation of the current and voltage during switching period is used. With the assumed approximation, energy loss during the turn-on period of a power switch can be attained as follows:

$$E_{\mathrm{on},J} = \int_0^{t_{\mathrm{on}}} v(t)i(t)\,\mathrm{d}t = \int_0^{t_{\mathrm{on}}} \left[\frac{V_{\mathrm{sw},J}}{t_{\mathrm{on}}}t\right]\left[\frac{-1}{t_{\mathrm{on}}}\left(t - t_{\mathrm{on}}\right)\right]\mathrm{d}t = \frac{1}{6}V_{\mathrm{sw},J}It_{\mathrm{on}} \quad (13)$$

where $E_{\mathrm{on},J}$ is the turn on loss of the Jth switch, t_{on} is the turn on time of the mentioned switch and I is the current through the switch after turning on.

To calculate losses at the turn-off period, it is enough that the 'on' subtitle be replaced with 'off' in the last part of (13) and I with I', in which $I'$is the current through the switch after turning off

$$E_{\mathrm{off},K} = \frac{1}{6}V_{\mathrm{sw},k}I't_{\mathrm{off}} \quad (14)$$

The switching losses are related to the number of switching transitions and also to the control method. Commonly, the average switching power loss can be calculated with the following equation

$$P_{\mathrm{sw}} = 2f\left[\sum_{J=1}^{N_{\mathrm{switch}}}\left(\sum_{i=1}^{N_{\mathrm{on},J}} E_{\mathrm{on},Ji} + \sum_{i=!1}^{\mathrm{off},J} E_{\mathrm{off},Ji}\right)\right] \quad (15)$$

where f is the fundamental frequency, $N_{\mathrm{on},J}$ and $N_{\mathrm{off},J}$ are the number of turning on and off the Jth switch during a half fundamental cycle. Also, $E_{\mathrm{on},Ji}$ is the energy loss of the Jth switch during the ith turning on and $E_{\mathrm{off},Ji}$ is the energy loss of the Jth switch during the ith turning off. Using (12) and (15), the total losses of the proposed multilevel inverter can be calculated as follows

$$P_{\mathrm{loss}} = P_{\mathrm{sw}} + P_c \quad (16)$$

6 Simulation results

To verify the performance of the proposed multilevel inverter, a nine-level structure is considered, and the simulation and

Table 4 Value of parameters in the implemented inverter

DC voltage sources in symmetric case	$V_1 = V_2 = 100$ V
DC voltage sources in asymmetric case	$V_1 = 60$ V and $V_2 = 3 * 60 = 180$ V
type of switch	BUP400D
type of IGBT driver	HCPL316j

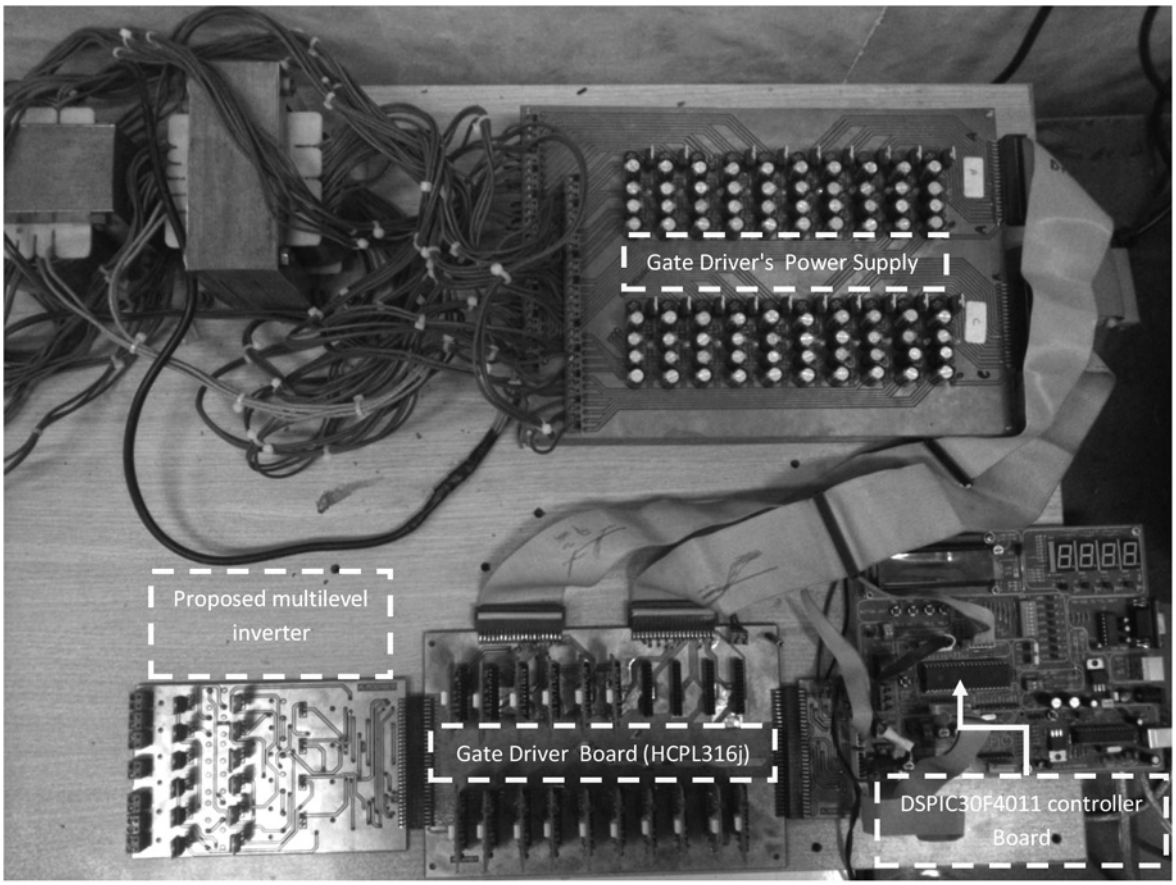

Fig. 8 *Implemented prototype setup*

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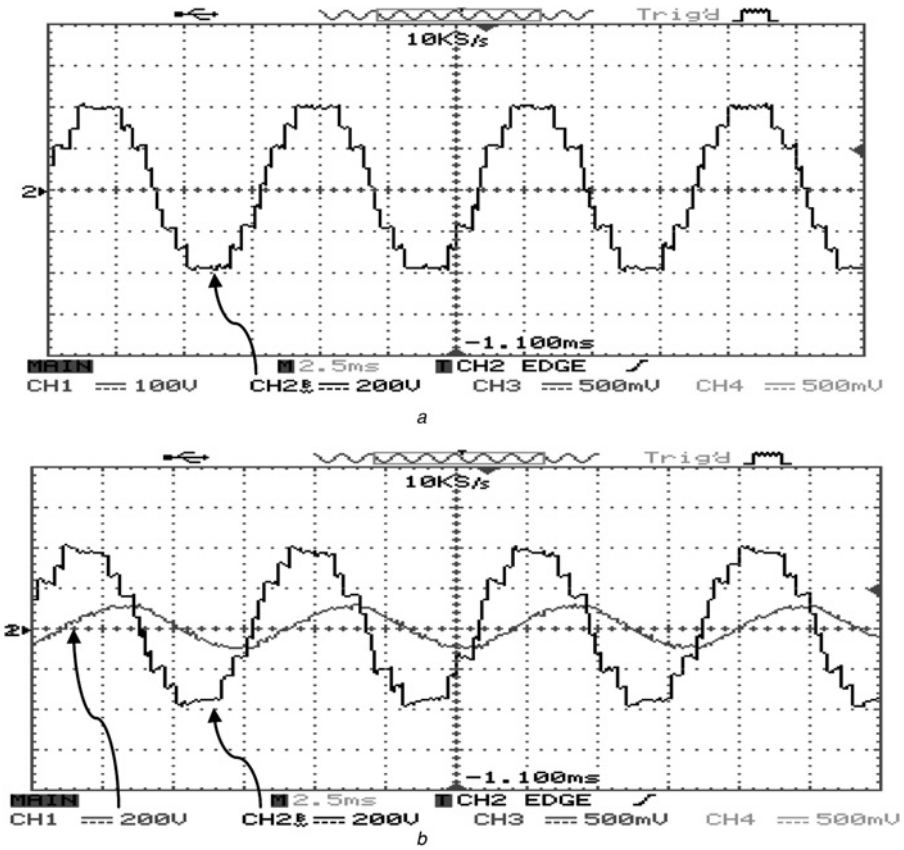

Fig. 9 *Experimental output voltage in the no-load case and load condition*

a Output voltage of the proposed symmetric nine-level inverter in no-load condition
b Output voltage and current of the proposed symmetric nine-level inverter under load condition

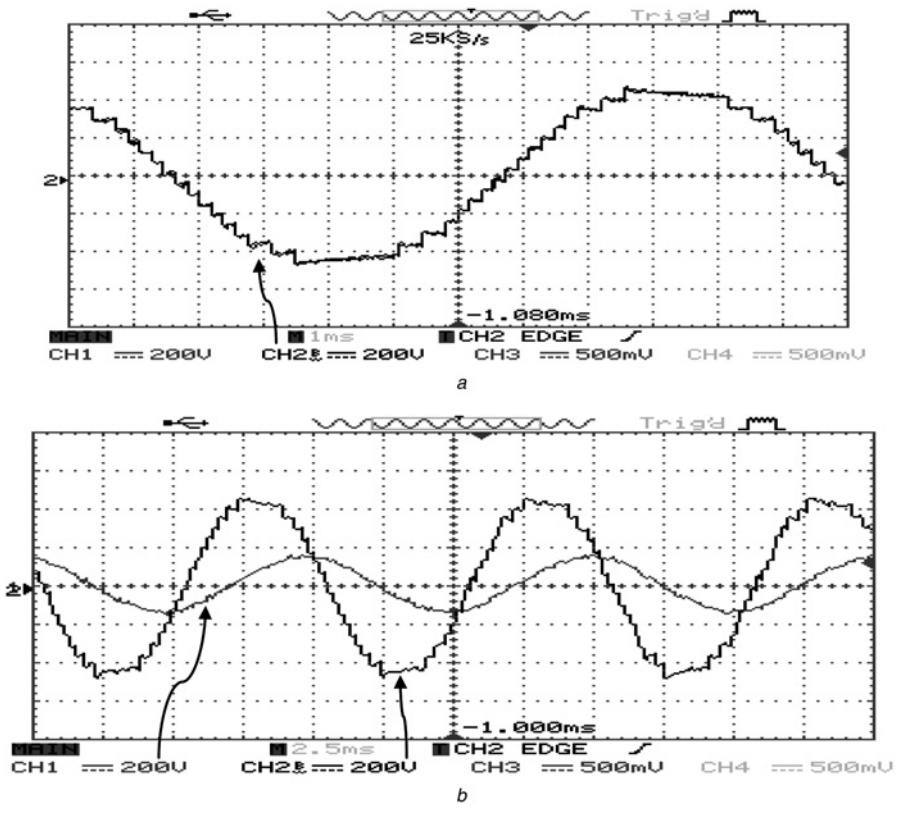

Fig. 10 *Experimental results of output voltage in no-load and loaded cases*

a Output voltage of the proposed asymmetric 17-level inverter in no-load condition
b Output voltage and current of the proposed asymmetric 17-level inverter under load condition

experimental results are obtained. The MATLAB/Simulink software has been used for simulation. A prototype of the proposed multilevel inverter which contains four DC voltage sources and 12 switches and can generate staircase waveform with maximum 120 V on output is considered. A series R–L branch with $R = 20\ \Omega$ and $L = 20$ mH is connected to the output of inverter as a load. Fig. 5 shows the output voltage of nine-level proposed inverter and load current waveform and the harmonic content.

In this section, experimental and simulation results of a nine-level proposed inverter (see Fig. 5) are presented. Table 3 defines the switching principle of symmetric nine-level proposed inverter. Fig. 6*a* shows the output voltage and load current of the proposed symmetric nine-level inverter with $V_1 = V_2 = 30$ V . Harmonic spectra of output voltage, for this case, are given in Fig. 6*b*. For increasing the output voltage quality, an asymmetric proposed inverter can be used with the same number of switches (in symmetric case) and with selecting $V_2 = 3 * V_1$ and $V_1 = 15$ V an asymmetric 17-level proposed inverter is obtained. Output voltage, load current and harmonic spectra of asymmetric 17-level inverter are given in Fig. 7. Switching scheme of the proposed inverter can be any of the switching methods defined for multilevel inverters; for instance the multilevel carrier based PWM method is used in this paper.

It can be seen from Figs. 6 and 7 that all possible levels are generated in symmetric and asymmetric structures of the proposed multilevel inverter.

7 Experimental results

For the experimental studies, the nine-level symmetric proposed inverter, as shown in Fig. 5, is implemented. Fig. 8 shows the implemented prototype proposed inverter. The control system of the proposed inverter is implemented by DSPIC30F4011 controller. To implement the proposed symmetric nine-level and asymmetric 17-level inverter four DC voltage sources and 12 IGBTs are used. The implemented circuit parameters are given in Table 4. Fig. 9*a* shows the experimental output voltage in the no-load case. Fig. 9*b* presents output voltage and current under load condition. Selecting $V_1 = 60$ V and $V_2 = 180$ V with same number of switches in nine-level symmetric structure, a 17-level asymmetric topology of the proposed inverter is obtained. The experimental results of output voltage in no-load and loaded cases are presented in Figs. 10*a* and *b*, respectively.

Figs. 9 and 10 validate the practicability of the proposed symmetric and asymmetric multilevel inverters, which can generate all voltage steps for a test case nine-level symmetric and 17-level asymmetric inverter.

8 Conclusions

In this paper, a novel multilevel inverter has been proposed. The suggested topology requires less switches and relevant gate driver circuits realising the same level in output voltage compared with traditional cascaded inverter. Therefore the suggested structure leads to reduction of installation area and cost and has simplicity of control method. It is shown that suggested inverter can be used as symmetric and asymmetric structures. The presented analyses show that the total PIV and power losses of the proposed inverter are lower to conventional multilevel inverters. Simulation and experimental results verify the validity and effectiveness of the proposed symmetric and asymmetric multilevel inverter.

9 References

1 Baker, R.H., Bannister, L.H.: 'Electric power converter', U.S. Patent 3 867 643, February 1975

2 Calais, M., Agelidis, V.G., Meinhardt, M.: 'Multilevel converters for single phase grid connected photovoltaic systems: an overview', *Elsevier J. Sol. Energy*, 1999, **66**, (6), pp. 325–335

3 Ozdemir, E., Ozdemir, S., Tolbert, L.M.: 'Fundamental-frequency-modulated six-level diode-clamped multilevel inverter for three-phase stand-alone photovoltaic system', *IEEE Trans. Ind. Electron.*, 2009, **56**, (11), pp. 4407–4415

4 Cecati, C., Ciancetta, F., Siano, P.: 'A multilevel inverter for PV systems with fuzzy logic control', *IEEE Trans. Ind. Electron.*, 2010, **57**, (12), pp. 4115–4125

5 Barbosa, P.G., Braga, H.A.C., Barbosa, M.C., Teixeria, E.C.: 'Boost current multilevel inverter and its application on single phase grid connected photovoltaic system', *IEEE Trans. Power Electron.*, 2006, **21**, pp. 1116–24

6 Ma, T.: 'P-Q decoupled control schemes using fuzzy neural networks for the unified power flow controller', *Int. J. Electr. Power Energy Syst.*, 2007, **29**, pp. 748–758

7 Liu, L., Zhu, P., Kang, Y., Chen, J.: 'Power-flow control performance analysis of a unified power-flow controller in a novel control scheme', *IEEE Trans. Power Deliv.*, 2007, **22**, (3), pp. 1613–1619

8 Ding, H., Zhang, Y., Gole, A.M., Dennis, A., Han, M.X., Xiao, X.N.: 'Analysis of coupling effects on overhead vsc–HVDC transmission lines from AC lines with shared right of way', *IEEE Trans. Power Deliv.*, 2010, **25**, (4), pp. 2976–2986

9 Haskew, S.L.T.A., Xu, L.: 'Control of HVDC light system using conventional and direct current vector control approaches', *IEEE Trans. Power Electron.*, 2010, **25**, (12), pp. 3106–3118

10 Dargahi, V., Sadigh, A.K., Abarzadeh, M., Pahlavani, M.R.A., Shoulaie, A.: 'Flying capacitors reduction in an improved double flying capacitor multicell converter controlled by a modified modulation method', *IEEE Trans. Power Electron.*, 2012, **27**, (9), pp. 3875–3887

11 Mondal, G., Sivakumar, K., Ramchand, R., Gopakumar, K., Levi, E.: 'A dual seven-level inverter supply for an open-end winding induction motor drive', *IEEE Trans. Ind. Electron.*, 2009, **56**, (5), pp. 1665–1673

12 Banaei, M.R., Salary, E.: 'New multilevel inverter with reduction of switches and gate driver', *Energy Convers. Manage.*, 2011, **52**, pp. 1129–1136

13 Nabae, A., Takahashi, I., Akagi, H.: 'A new neutral-point-clamped PWM inverter', *IEEE Trans. Ind. Appl.*, 1981, **17**, (5), pp. 518–523

14 Sadigh, A.K., Sabahi, S.H.H.M., Gharehpetian, G.B.: 'Double flying capacitor multicell converter based on modified phase-shifted pulse width modulation', *Trans. Power Electron.*, 2010, **25**, (6), pp. 1517–1526

15 Hammond, P.W.: 'A new approach to enhance power quality for medium voltage drives', *IEEE Trans. Ind. Appl.*, 1997, **33**, (1), pp. 202–208

16 Meynard, T.A., Foch, H.: 'Multi-level choppers for high voltage applications', *J. Eur. Power Electron. Drives*, 1992, **2**, (1), pp. 45–50

17 Malinowski, M., Gopakumar, K., Rodriguez, J., Pérez, M.A.: 'A survey on cascaded multilevel inverters', *IEEE Trans. Ind. Electron.*, 2010, **57**, (7), pp. 2197–2206

18 Meynard, T., Foch, H., Thomas, P., Courault, J., Jakob, R., Nahrstaedt, M.: 'Multicell converters: basic concepts and industry applications', *IEEE Trans. Ind. Electron.*, 2002, **49**, (5), pp. 955–964

19 Gateau, G., Meynard, T.A., Foch, H.: 'Stacked multicell converter (SMC): properties and design'. Proc. IEEE 32nd Annual Power Electronics Specialists Conf. Meeting, 2001, pp. 1583–1588

20 Rodriguez, J., Hammond, P., Pontt, J., Musalem, R., Lezana, P., Escobar, M.J.: 'Operation of a medium-voltage drive under faulty conditions', *IEEE Trans. Ind. Electron.*, 2005, **52**, (4), pp. 1080–1085

21 Hammond, P.W.: 'A new approach to enhance power quality for medium voltage AC drives', *IEEE Trans. Ind. Appl.*, 1997, **33**, (1), pp. 202–208

22 Banaei, M.R., Salary, E.: 'Analysis of generation symmetrical multilevel inverter', *J. Circuits Syst. Comput.*, 2011, **20**, (02), pp. 299–311

23 Kangarlu, M.F., Babaei, E.: 'A generalized cascaded multilevel inverter using series connection of sub-multilevel inverters', *IEEE Trans. Power Electron.*, 2013, **28**, (2), pp. 625–636

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