DEVELOPMENT AND INTEGRATION OF SILICON-GERMANIUM FRONT-END ELECTRONICS FOR ACTIVE PHASED-ARRAY ANTENNAS

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DEVELOPMENT AND INTEGRATION OF SILICON-GERMANIUM FRONT-END ELECTRONICS FOR ACTIVE PHASED-ARRAY ANTENNAS

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SUMMARY

The research presented in this thesis leverages silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) technology to develop microwave front-end electronics for active phased-array antennas. The highly integrated electronics will reduce costs and improve the feasibility of snow measurements from airborne and space-borne platforms.

Chapter 1 presents the motivation of this research, focusing on the technological needs of snow measurement missions. The fundamentals and benefits of SiGe HBTs and phased-array antennas for these missions are discussed as well.

Chapter 2 discusses SiGe power amplifier design considerations for radar systems. Basic power amplifier design concepts, power limitations in SiGe HBTs, and techniques for increasing the output power of SiGe HBT PAs are reviewed.

Chapter 3 presents the design and characterization of a robust medium power X-band SiGe power amplifier for integration into a SiGe transmit/receive module. The PA design process applies the concepts presented in Chapter 2. A detailed investigation into measurement-to-simulation discrepancies is outlined as well.

Chapter 4 discusses the development and characterization of a single-chip X-band SiGe T/R module for integration into a very thin, lightweight active phased array antenna panel. The system-on-package antenna combines the high performance and integration potential of SiGe technologies with advanced substrates and packaging techniques to develop a high performance scalable antenna panel using relatively low-cost materials and silicon-based electronics. The antenna panel presented in this chapter will enable airborne SCLP measurements and advance the technology towards an eventual space-based SCLP measurement instrument that will satisfy a critical Earth science need.

Finally, Chapter 5 provides concluding remarks and discusses future research directions. My publications that originated from this research are listed below.

- C. A. Donado Morcillo, C. E. Patterson, B. Lacroix, **C. T. Coen**, C. H. J. Poh, J. D. Cressler, and J. Papapolymerou, "An Ultra-Thin, High-Power and Multilayer Organic Antenna Array with T/R Functionality in the X Band," *IEEE Transactions on Microwave Theory and Techniques,* submitted for review in March 2012.

- T. K. Thrivikraman, C. E. Patterson, **C. T. Coen**, A. M. Yepes, T. Heath, B. Wilson, J. Papapolymerou, and J. D. Cressler, "Integrated, Digitally-Controlled, 64 Element SiGe on Multilayer Organic X-band Phased-Array Receiver Antenna for Snow Measurements," *IEEE Aerospace and Electronic Systems Magazine*, submitted for review in June 2012.

- C. A. Donado-Morcillo, C. E. Patterson, T. K. Thrivikraman, B. Lacroix, B. Wilson, B. Hudson, **C. T. Coen**, C. H. Poh, T. Heath, J. D. Cressler, and J. Papapolymerou, "A lightweight, 64-element, organic phased array with integrated transmit-receive SiGe circuitry in the X band," *IEEE MTT-S International Microwave Symposium Digest*, 2011.

- C. E. Patterson, T. K. Thrivikraman, S. K. Bhattacharya, **C. T. Coen**, J. D. Cressler, and J. Papapolymerou, "Development of a multilayer organic packaging technique for a fully embedded T/R module," *European Microwave Conference (EuMC)*, 2011, pp. 261-264.

CHAPTER I

INTRODUCTION

1.1 Motivation

Microwave remote sensing is an extremely powerful technique for gathering information about the Earth. The ability of microwaves to penetrate clouds, vegetation, and the ground to various frequency-dependent depths can be exploited by microwave radars and radiometers to collect data about various Earth science parameters [1]. The atmospheric absorption spectrum in Figure 1.1 shows that the X-, Ku-, Ka-, and W-bands are, in general, the frequency ranges most suitable for use in long-distance remote sensing systems. Frequency bands that contain significant molecular resonances, such as K-band and V-band, are typically used for short-range sensing applications such as automotive radar. Attenuation decreases with altitude as pressure decreases and the relative composition of the atmosphere changes. Frequency ranges for the standard IEEE radar bands can be found in Table 1.1.

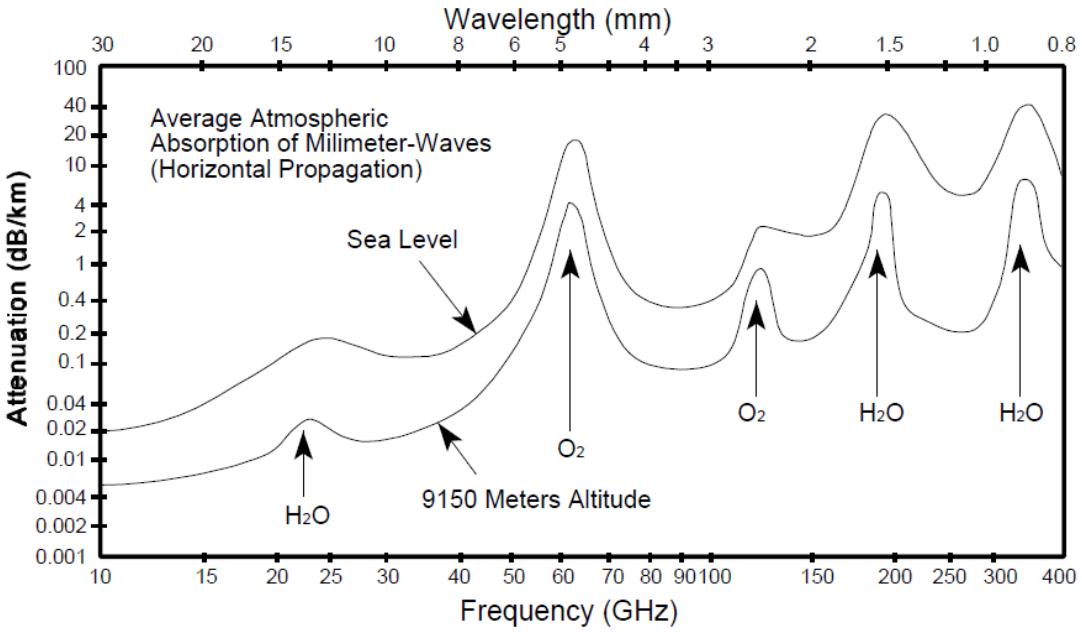


Figure 1.1: Atmospheric microwave and millimeter-wave attenuation spectrum [2].

Table 1.1: IEEE standard letter designations for radio-frequency bands [3]

L-band	1-2 GHz
S-band	2-4 GHz
C-band	4-8 GHz
X-band	8-12 GHz
Ku-band	12-18 GHz
K-band	18-27 GHz
Ka-band	27-40 GHz
V-band	40-75 GHz
W-band	75-110 GHz

The Earth science application of interest in this thesis is the measurement of snow and cold land processes (SCLP). The 2005 National Research Council (NRC) Decadal Study identifies advanced SCLP data collection as a high Earth science priority that will fill an important gap in the global water cycle observing system. This data will enable improved climate models and weather prediction and could economically benefit the U.S. by more than $1.3B per year. In order to survey the necessary area and to obtain a sufficiently high sampling density, this SCLP data must be collected from a space-based instrument [4]. In 2003, the NASA Cold Land Processes Working Group (CLPWG) outlined technological requirements for a space-based SCLP measurement mission. A constant theme in this report [5] is the need for cost reducing technologies to make a space-based SCLP measurement instrument more feasible. Instrument size, weight, and power consumption (SWaP) are the main cost drivers for any space-based remote sensing instrument. Developing highly integrated, lightweight, and low power remote sensing technologies would reduce SCLP mission costs by up to tens of millions of dollars and enable alternative mission concepts [5]. The work presented in this thesis leverages SiGe HBT bipolar complementary metal oxide semiconductor (BiCMOS) technologies to develop a robust power amplifier and integrated transmit/receive module for a highly integrated active phased-array antenna for airborne SCLP measurements. The SiGe

electronics will reduce costs and improve the feasibility of SCLP data collection from SWaP-constrained platforms.

1.2 SiGe HBT BiCMOS Technology

Silicon is an ideal semiconductor from a fabrication standpoint. It is extremely abundant on the Earth (sand), can be grown into very large defect-free crystals (300 mm wafer diameter for many new processes), and can be easily doped with both n- and p-type impurities over a large range, to name a few of its many virtues. Perhaps the most important quality is that it is simple to controllably grow an excellent oxide (SiO_2) on silicon by simply flowing dry or wet oxygen across a wafer. The resulting dielectric is extremely useful in the fabrication process and acts as an electrical isolator and as the thin gate oxide in fabricated circuits [6]. These properties of silicon have allowed silicon-based CMOS to dominate most electronic applications over the last few decades.

Despite its excellent material properties, the electrical properties of silicon are less than ideal. Carrier mobilities and saturation velocities in silicon are relatively low, which limits the usefulness of silicon-based devices in high-speed applications. III-V semiconductors such as GaAs, GaN, and InP have higher mobilities and saturation velocities which make III-V devices capable of far greater speeds than silicon-based devices. Devices in these processes are designed using advanced epitaxial growth techniques to precisely manipulate the physical and chemical structures of the semiconductor and optimize performance. This atomic-level tailoring process is known as bandgap engineering [7]. Bandgap-engineered InP devices have been shown to achieve THz speeds [8]. Although they enable excellent performance, III-V semiconductors pose significant fabrication challenges. These materials have poor native oxides, are mechanically weak, and conduct heat poorly. III-V wafers are far smaller than silicon wafers and devices have low yields, which ultimately makes III-V devices more expensive than their silicon-based counterparts. Additionally, these devices are

traditionally large compared to silicon-based devices and cannot cheaply be integrated with CMOS, which greatly complicates packaging and limits their potential for integration. An ideal high-speed technology would combine the performance of III-V devices with the economies of silicon to enable inexpensive full mixed-signal SoCs. The advent of the SiGe HBT over the last two decades has made this ideality a reality.

The theory of the HBT was originally laid out by Herbert Kroemer in 1957 [9]. In 1985 Kroemer generalized the mathematical Moll-Ross relations for carrier current density across a generalized bipolar transistor with non-uniform bandgap, putting into place key equations for designing HBTs [10]. The first SiGe HBT was demonstrated in 1987 and the technology has been rapidly advancing ever since [11]. A SiGe HBT is formed by depositing a strained SiGe alloy in the base region of a silicon BJT. This alloy is generally formed using ultra-high vacuum chemical vapor deposition (UHV/CVD). Each 10% fraction of germanium in the SiGe alloy reduces the bandgap by around 75 meV. The germanium profile is bandgap engineered to create an electric field in the base and tailor the device characteristics. A band diagram of a basic SiGe HBT is shown in Figure 1.2. The band bending in the base region indicates the presence of the electric field. This field rapidly accelerates carriers through the base, causing drift to dominate the carrier transport instead of diffusion. Drift is a much faster transport mechanism than diffusion, so this Ge-induced field greatly improves the speed of the transistors. The germanium profile is typically triangular or trapezoidal to optimize device performance and to suppress second-order device phenomena such as heterojunction barrier effects. Carbon doping is often employed in modern SiGe HBTs to prevent out-diffusion of boron dopants from the heavily doped base, which simplifies device design and fabrication and enables improved performance [6].

Introducing a strained SiGe alloy into the base of a silicon bipolar transistor improves first-order device performance in every way. The primary speed figures of

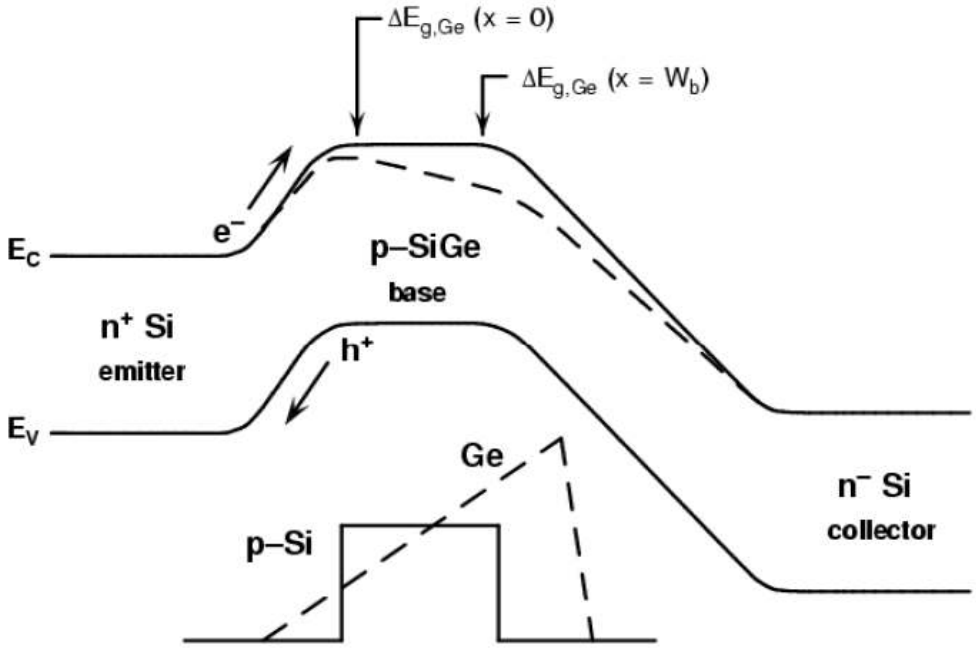


Figure 1.2: Band diagram of a SiGe HBT illustrating the Ge-induced changes [6].

merit for bipolar transistors, the unity gain cutoff frequency f_T and the maximum oscillation frequency f_{MAX}, are given by the following equations:

$$f_T = \frac{1}{2\pi\tau_{ec}} = \frac{1}{2\pi}\left[\frac{kT}{qI_C}(C_{te} + C_{tc}) + \tau_b + \tau_e + \frac{W_{CB}}{2v_{sat}} + r_c C_{tc}\right]^{-1} \tag{1.1}$$

and

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi C_{bc} r_b}} \tag{1.2}$$

These parameters are typically dominated by the base transit time τ_b. The base transit time in a SiGe HBT is given by the equation

$$\tau_{b,SiGe} \cong \frac{W_b^2}{2\widetilde{D_{nb}}} \frac{kT}{\Delta E_{g,Ge}(grade)} \tag{1.3}$$

where W_b is the vertical base width of the device, kT is the thermal energy, $\widetilde{D_{nb}}$ is the average electron diffusivity in the base (proportional to mobility per Einstein's relation), and $\Delta E_{g,Ge}(\text{grade})$ is the magnitude of the germanium-grading-induced bandgap

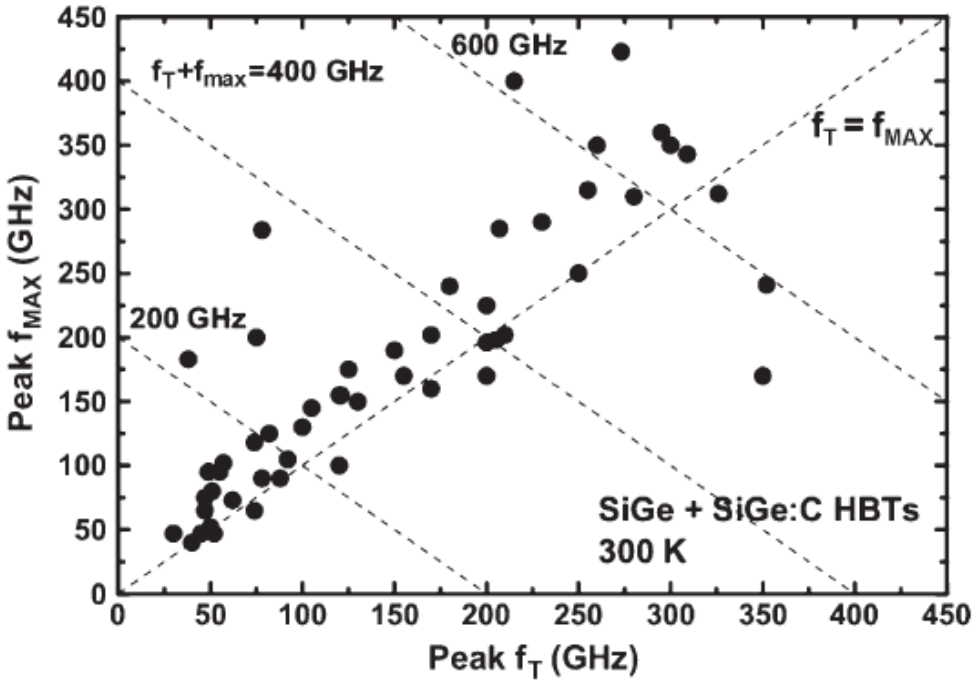


Figure 1.3: Published SiGe HBT f_T and f_{max} data showing rapidly increasing speed [12].

reduction in the base region. $\Delta E_{g,Ge}(\text{grade})$ represents the electric field generated in the base. Increasing the magnitude of this grade significantly speeds up the transit times, and in turn, the speed of the devices. Current gain and output conductance are also greatly improved by the addition of germanium; however the speed improvement is what enables the use of SiGe HBTs in microwave and millimeter-wave circuit applications.

The speed of SiGe HBTs has greatly improved over the last 25 years since the first demonstration, as shown in the speed roadmap in Figure 1.3. Modern third-generation SiGe BiCMOS processes generally offer multiple HBT variants (high-speed and high-breakdown) along with advanced CMOS, full suites of passives (including MIM capacitors and optimized spiral inductors), and even millimeter-wave components such as hybrids and couplers. Relevant HBT specifications for a high-speed SiGe HBT in a mature third-generation SiGe technology are listed in Table 1.2. Emerging fourth-generation processes are pushing SiGe HBTs toward half-terahertz speeds [13, 14]. As shown in Figure 1.4, the speeds of emerging SiGe HBTs are comparable to those of even

Table 1.2: Relevant specifications for a 3rd-generation SiGe HBT [15]

W_E	0.12 μm
Peak β	400
BV_{CEO}	1.7 V
Peak f_T	207 GHz
Peak f_{max}	285 GHz
J_C at peak f_T (mA)	10-15 mA/μm^2

the best InP devices. SiGe HBTs have even been projected to eventually achieve a peak f_T/f_{max} of 782/901 GHz at the 32 nm node [16]. Clearly SiGe is becoming an increasingly strong contender to III-V technologies for microwave and millimeter-wave circuit applications.

1.3 Phased Array Antennas

Antennas in classical detection radars were steered mechanically. Such antennas tend to evoke images from black-and-white war films. Although mechanical beam steering is relatively simple (and cheap!), it is slow and not precisely controllable. The sluggish pace of mechanical antennas makes it difficult if not impossible to track small, fast-moving objects. Additionally, mechanical systems such as these are prone to reliability issues (burnt out motors, etc.). The advent of the phased array antennas in the 1970s solved these shortcomings (for radars with a swath width less than 180°). Phased arrays consist of arrays of near-identical radiating elements that combine energy in free space to form a single equivalent aperture. Most phased arrays are specifically designed to be uniform linear arrays, where the elements are equally spaced so optimum phase adjustments result in constructive interference [17]. The far-field pattern of an array is defined by the normalized radiation pattern of the individual elements, the spacing between the elements, and the relative amplitude and phase distributions across the elements. It is this last parameter, the phase, that is adjusted in order to steer the beam

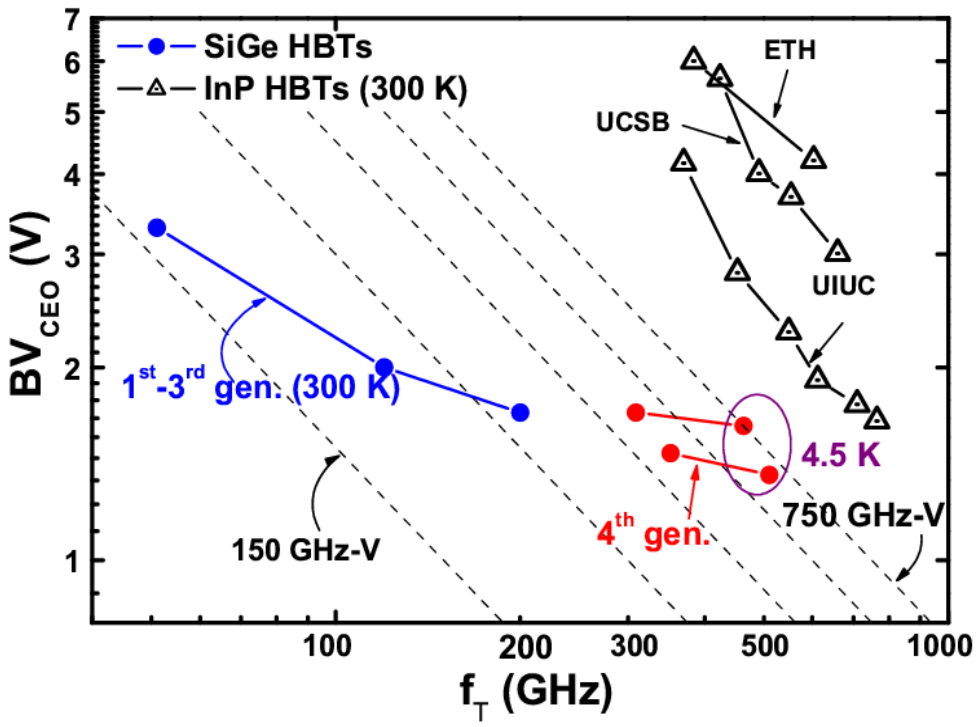


Figure 1.4: Generational evolution of SiGe HBT performance (peak f_T and BV_{CEO}) with respect to InP HBTs [12].

[1]. Increasing the number of elements in the array increases the directivity of the beam and suppresses undesired sidelobes.

The original and most simple type of phased array is a passive phased array, also known as an electronically scanned array (ESA). Such an antenna contains a passive phase shifter in the beamforming path for each element. A single high-power source such as a traveling-wave tube (TWT) amplifier provides RF input power which is split up by the beamforming network, adjusted in phase by the phase shifters, and re-combined in free space to form a beam in the desired direction. An illustration of this process is shown in Figure 1.5. A more advanced variant is the active phased array antenna, or active electronically scanned array (AESA). An AESA combines active amplifying circuitry along with the phase shifting for each element. The active electronics and the phase shifter are contained what is called a transmit/receive module, or T/R module.

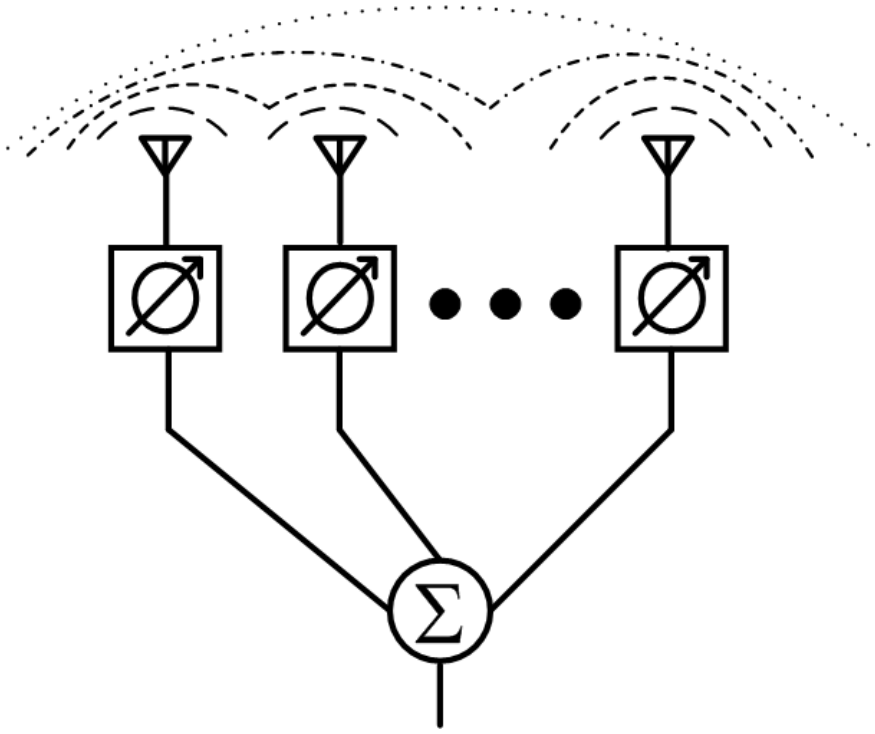


Figure 1.5: Representative drawing of a passive phased array.

Both types of phased arrays steer far more quickly and accurately (often on the order of micro or nanoseconds) than mechanically steered antennas. This increased speed and accuracy allows for operators to shape transmit and receive beams differently, which is desirable if there is a significant amount of RF interference (RFI) impingent from a given direction. The ability to rapidly switch between transmit/receive and phase states makes phased arrays capable of rapidly tracking and detecting moving objects as well [18].

Front-end T/R modules are one of the main bottlenecks in implementing AESA antennas. A block diagram of a typical T/R module is shown in Figure 1.6. Low noise amplifiers (LNAs) close to the elements minimize input line losses and help preserve the signal to noise ratio (SNR) of the received signal. Power amplifiers (PAs) close to the elements mitigate power losses introduced by the beamforming networks, which improves the output power and transmit efficiency of the antenna. The duplexer in the T/R module generally is implemented using a ferrite circulator or a SPDT switch.

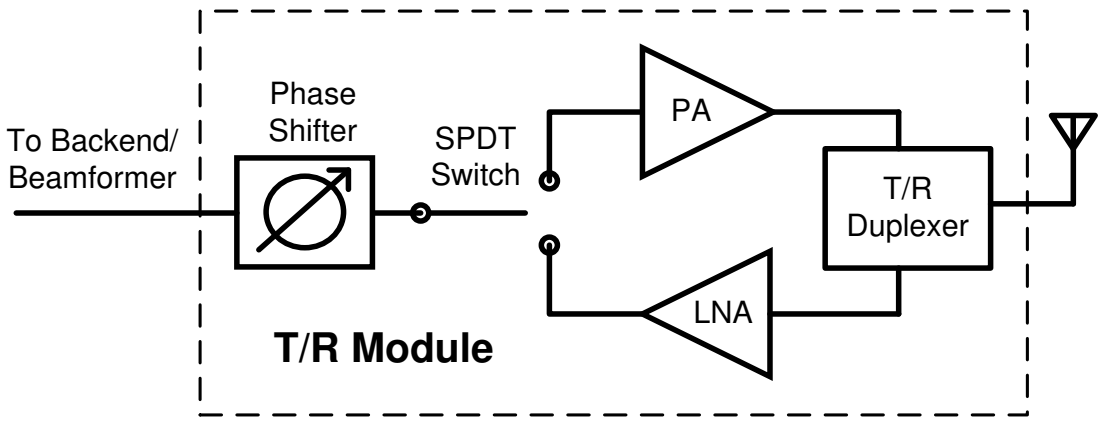


Figure 1.6: Block diagram of a simple T/R module.

Circulators allow the antenna to transmit and receive simultaneously (full duplex operation) and provide roughly 15 to 20 dB of isolation. If the output power of the PA is high, a limiter circuit may be required at the LNA input to protect the LNA while the PA is transmitting [19]. An alternative duplexer is a SPDT switch, which cannot simultaneous allow transmitting and receiving (half duplex operation) but generally provides above 30 dB in isolation. Although not shown in Figure 1.6, T/R modules generally contain digital electronics to control the phase shifter and additional circuitry to generate bias voltages for the individual circuits. Typical T/R modules contain a collection of GaAs MMICs along with some hybrid components, some ferrites, and silicon-based digital control. These elements can clearly be seen in the image shown in Figure 1.7, a T/R module developed by EADS.

The presence of T/R modules in AESA antennas significantly improves their performance with respect to passive ESA antennas, but this added performance introduces significant technical challenges. In order to generate the application-required output power, many AESA antennas have hundreds to thousands of radiating elements, requiring hundreds to thousands of T/R modules. These T/R modules consume huge amounts of power, sometimes requiring the use of large diesel generators capable of generating megawatts of power. These large power requirements lead to significant

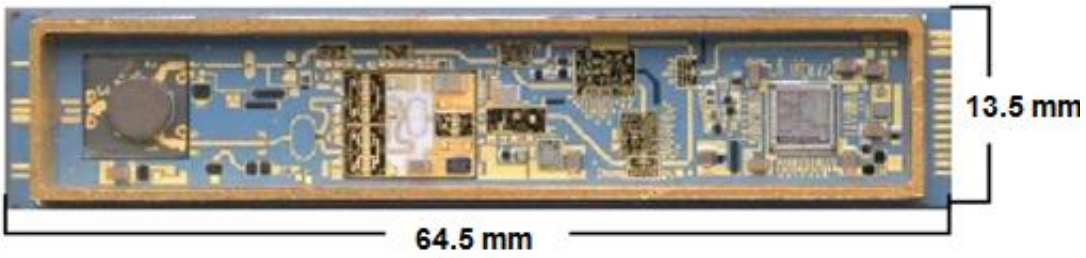


Figure 1.7: Photograph of a typical radar T/R module developed by EADS.

thermal issues with these T/R modules, greatly complicating the module and array designs [20]. These issues make existing AESA radar systems impractical for heavily SWaP constrained airborne or space-borne platforms.

Perhaps an even greater issue in implementing AESA antennas is their high cost. A T/R module with an output power of 10 W typically costs between $1,000 and $3,000 [18]. If hundreds or thousands of these modules are used, costs can become enormous and prohibitive. Roughly 25% of the cost of an AESA antenna is the GaAs MMIC chips, another 25% of the cost is the T/R modules not including the MMICs, and the other 50% is the antenna itself [21]. Costs could be greatly reduced by using a cheaper MMIC technology, reducing the amount of chips and components required in each module, and increasing the integration. This is a problem begging for a silicon-based solution!

The relatively new concept of low-power-density (LPD) arrays enables the use of low-power silicon technologies in T/R modules [20]. LPD arrays allow for the use of T/R modules with relatively low output powers (~1 W or less), which SiGe has achieved up through X-band [22]. The output power is increased at the array level by scaling up the number of array elements, which results in an AESA that has a high output power and is more efficient than arrays using III-V MMICs in hybrid modules [20, 23]. Integrated SiGe T/R modules containing all RF blocks along with digital control and bias references on a single chip greatly simplifies packaging and reduce the footprint of the modules. The SiGe T/R module shown in Figure 1.8 occupies less than 2% of the surface area of

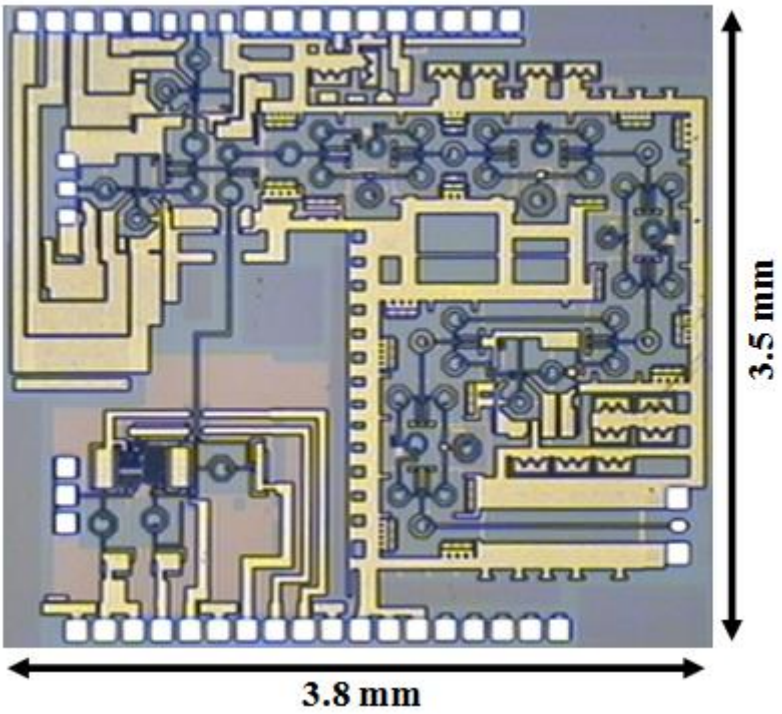


Figure 1.8: Photomicrograph of a SiGe T/R module SoC.

the module shown in Figure 1.7 and is extremely lightweight as well. Heat dissipation is much less of an issue in SiGe than in III-V hybrid modules due to the lower output power of the individual T/R modules and the high thermal conductivity of silicon. SiGe enable the development of lightweight, low-power radars that make AESA radar systems far more practical and feasible for airborne and space-borne platforms.

Due to the economies of silicon (high yield, mature processing techniques, large wafers, etc.) it is projected that SiGe T/R modules could each cost $10 or less [20]. A quick cost analysis shows that for $1000, one could purchase 100 0.5 W SiGe T/R modules and a single $1000 10 W GaAs hybrid module. That equates to 50 W of power using SiGe (assuming 100% free space combining efficiency) versus 10 W of power in GaAs for the same price. This is an admittedly rough analysis, but when one takes into account packaging and heat dissipation considerations, SiGe is clearly a more attractive option. The rapidly increasing speed of SiGe HBT technologies combined with their

integration with CMOS and the economies of silicon make SiGe BiCMOS the optimal technology for smart phased arrays [17].

1.4 Organization of Thesis

This thesis focuses on the development and integration of SiGe front-end electronics for a highly integrated AESA antenna. Chapter 2 will discuss design considerations for SiGe HBT power amplifiers, specifically focusing on basic PA theory, power limitations in SiGe HBT technologies, and techniques for improving the output power of SiGe HBT PAs. Chapter 3 will discuss the design process, measurement results, and measurement-to-simulation correlation of a self-biased SiGe PA for X-band radar. Chapter 4 will discuss the development of a very thin, lightweight LPD AESA antenna for airborne SCLP measurements using custom SiGe T/R modules. The SiGe electronics enable the very high degree of integration and low form factor achieved by the antenna. Chapter 5 will provide concluding remarks and discuss future research directions.

The antenna was the final result of a three-year collaborative effort between Dr. John D. Cressler's SiGe Devices and Circuits Group, Dr. John Papapolymerou's MiRCTECH group, and the Sensors and Electromagnetic Applications Lab (SEAL) at the Georgia Tech Research Institute (GTRI). The MiRCTECH group developed the antenna arrays and led the packaging efforts. The SiGe group (including me) developed and characterized the SiGe T/R modules and supported the antenna testing and integration. The SEAL lab developed testing equipment, provided antenna testing facilities, and provided testing and integration support. I joined the project at the beginning of the third and final year. My responsibilities in this project consisted of designing the PA for the final T/R module (Chapter 3), assisting in the design of the T/R module, fully characterizing the T/R module, and assisting in the characterization of the final array (Chapter 4).

CHAPTER II

SIGE HBT POWER AMPLIFIER DESIGN CONSIDERATIONS

2.1 Introduction

Power amplifiers (PAs) are typically the most challenging circuit blocks to design in wireless systems. PAs are highly nonlinear circuits by their nature, and as such are extremely difficult to accurately model and simulate using traditional microwave circuit design tools. Designing PAs in SiGe poses additional challenges due to the inherent power limitations of the platform. Despite these challenges, PAs in SiGe instead of III-V platforms are desirable due to the economical and integration advantages of silicon (described in great detail in Chapter 1).

This chapter will discuss SiGe power amplifier design considerations for radar systems. Radar PAs generally transmit maximum power when the radar is transmitting and are turned off when the radar is receiving (in a half-duplex system). The primary design goal in most radar PA designs is thus output power. Wireless communication PAs, on the other hand, experience high peak-to-average power ratios and are generally implemented in heavily power constrained platforms (cellular phones), so efficiency is the primary design goal in cellular PAs. Section 2.2 of this chapter will discuss fundamental PA design concepts, focusing on load-line theory developed by Dr. Steve Cripps. Section 2.3 will discuss power limitation mechanisms specific to SiGe HBTs and SiGe BiCMOS processes, focusing on breakdown voltages and current limitations in SiGe along with lossy passive elements. Lastly, Section 2.4 will discuss techniques for increasing the output power of SiGe HBT PAs with a focus on the hybrid cascode topology.

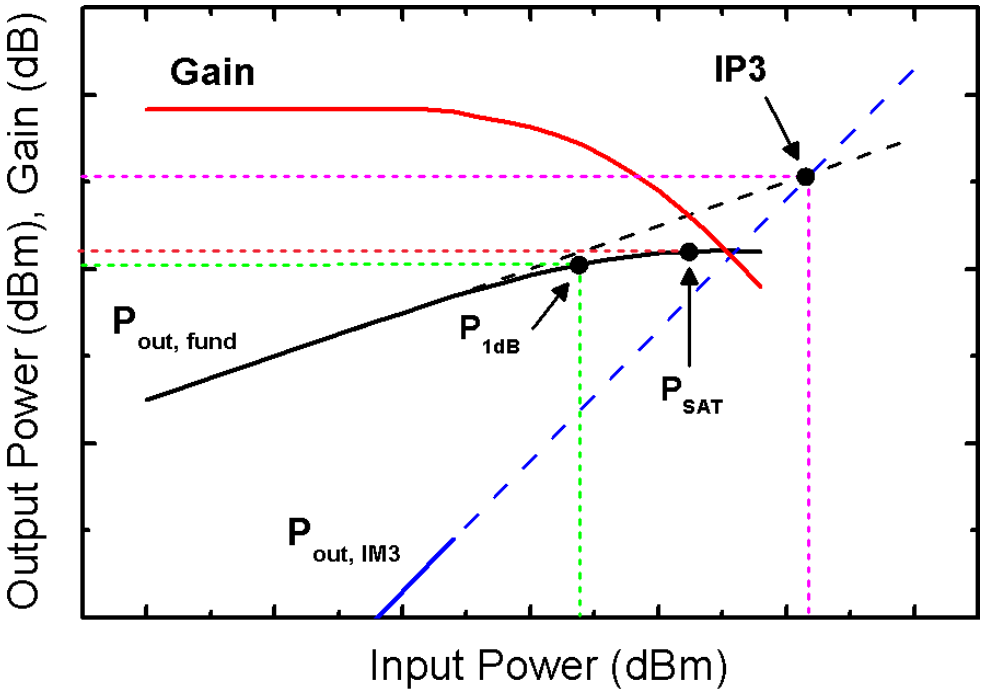


Figure 2.1: Large signal compression behavior of an example PA, showing the main nonlinearity figures of merit.

2.2 Power Amplifier Design Theory

2.2.1 Nonlinearity Fundamentals

The goal of a power amplifier in a wireless system is to deliver a high amount of power to an antenna to maximize the transmitted signal power. In order to design such a circuit, one must understand the inherent nonlinearities of the devices used to design PAs. No physical device is capable of outputting an infinite amount of power—there will always be physical mechanisms that limit the power output to a certain level. For example, high electric currents generate heat and can lead to thermal runaway, which can destroy devices. High voltages can cause avalanche and/or dielectric breakdown, resulting in blown devices. Practical power limitations for SiGe HBTs will be discussed in Section 2.3.

The large signal swept power behavior of a generic device or amplifier is shown in Figure 2.1. RF output power at the fundamental frequency increases linearly with input power until a threshold is reached where the gain decreases and the output power levels off. This gain reduction phenomenon is called gain compression. The power level at which the gain is compressed by 1 dB versus the small-signal value (referred to as P_{1dB}) is treated as the maximum power level up to which the device or amplifier behaves linearly. The maximum possible output power of the device or amplifier, where the fundamental tone's output power is flat with respect to input power, is referred to as the saturated output power P_{SAT}.

The quickly rising IM3 tone in Figure 2.1 is caused by intermodulation distortion (IMD). IMD products will be present in the PA output when the input signal is of the form

$$x(t) = A\cos(\omega_1 t) + A\cos(\omega_2 t). \tag{2.1}$$

Where A is the amplitude and ω_1 and ω_2 are closely spaced frequency tones. When the output signal is modeled as a power series it will contain the terms

$$\begin{aligned} y(t) = &\left(k_1 A + \frac{3k_3A^3}{4} + \frac{3k_3A^3}{2}\right)\cos(\omega_1 t) + \cdots \qquad \text{(fundamental)} \\ &+ \frac{3k_3A^3}{4}\cos(2\omega_2 - \omega_1) + \ldots \qquad \text{(intermodulation)} \end{aligned} \tag{2.2}$$

where k_1 and k_3 are coefficients of the power series terms. The mixing of the two input tones produces unwanted tones ($2\omega_2 - \omega_1, 2\omega_1 - \omega_2$) in the bandwidth of the amplifier that cannot be filtered out [6]. These unwanted tones rise three times as quickly (proportional to A^3) as the fundamental tones, so as input drive increases these IMD products rapidly becomes more of an issue. The intersection of the extrapolated first-order and third-order terms is known as the third-order intercept point, or IP3. The input power at IP3 is referred to as IIP3, and the output power is referred to as OIP3. These are the primary IMD figures of merit for a circuit. IMD products can cause digital signal

corruption and are of great concern in wireless communication PAs and especially receiver systems. In radar receivers IMD products can interfere with received Doppler shifted frequency components and corrupt the measured data. In radar transmitters, on the other hand, the input tone to the PA is normally generated by a local oscillator (LO) with only a single frequency component, so IMD products are normally not a concern in radar PAs.

2.2.2 Power Matching and Load-Line Theory

The PA design theory presented in this section was largely developed and formalized by Dr. Steve Cripps in [24]. The output power of a device is heavily influenced by the impedance presented to the output of the device. Basic circuit theory states that in order to achieve maximum power transfer, the output impedance presented to a transistor should be the conjugate match of the output impedance. This resonates out the reactive component of the device output impedance and results in maximized resistive power transfer. This line of thinking is fallacious when it comes to PA design, however. The output resistance of a well-designed device biased in the operational region (forward-active mode for a BJT, saturation mode for a FET) will be very high. When a device is conjugately matched to a high load resistance, the slope of the load-line will be low, as shown by the R_{GAIN} line in Figure 2.2. I_{MAX} and V_{MAX} are the maximum current and voltage limits of the device in question. V_{KNEE} is the "knee voltage" of the I-V characteristics, which is the transition from saturation to forward-active mode in a bipolar and the transition from the linear region to the saturation region in a FET. The load-line swings through the full voltage range but through only a small current range, resulting in a sub-optimal output power for the device. Conjugate output matching results in maximum power transfer, not maximum power output.

In order to maximize output power, the device load-line should follow the R_{OPT} line shown in Figure 2.1. Since power is the product of voltage and current, output

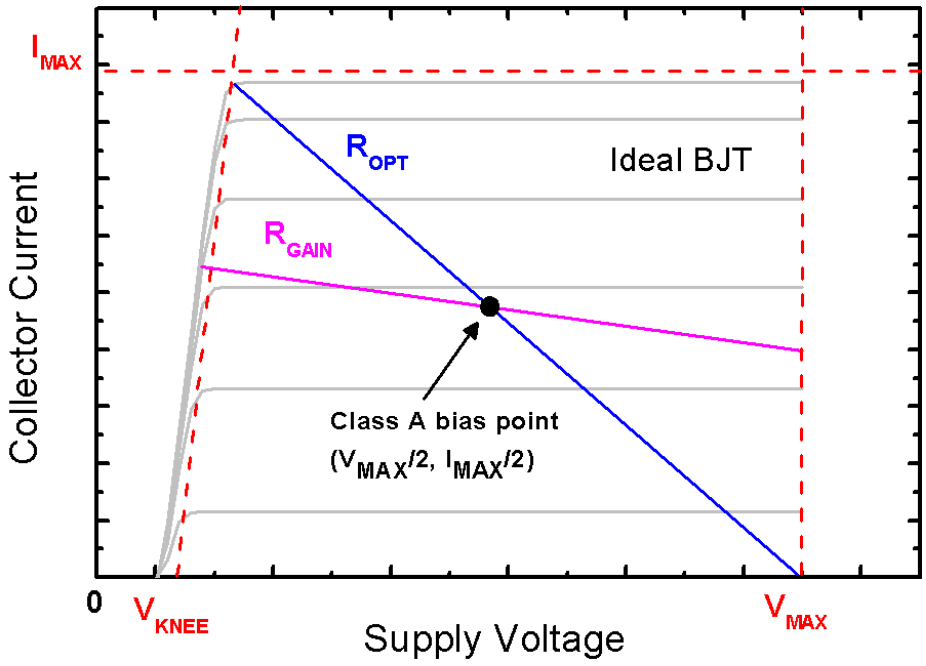


Figure 2.2: Non-ideal and optimal power load-lines for a sample bipolar transistor.

power is maximized when the load-line traverses the maximum voltage and current swings of the device. The load impedance required to achieve this desired load-line is clearly different from the conjugate impedance, so the device is be intentionally mismatched to maximize power output. Intentional mismatching a device is typically taboo in circuit design, but this is the fundamental principle in PA design. Gain and matching are traded off in order to attain more linear output power. Gain compression characteristics of a conjugately matched and a power matched device are shown in Figure 2.3. Clearly the gain of the power matched device is reduced, but the output power is significantly improved.

The optimal power matching resistance is given by the equation

$$R_{OPT} = \frac{(V_{MAX} - V_{KNEE})}{I_{MAX}}. \tag{2.3}$$

The knee voltage is usually small but can significantly change the optimal resistance and the output power and cannot be neglected. The maximum voltage V_{MAX} is generally

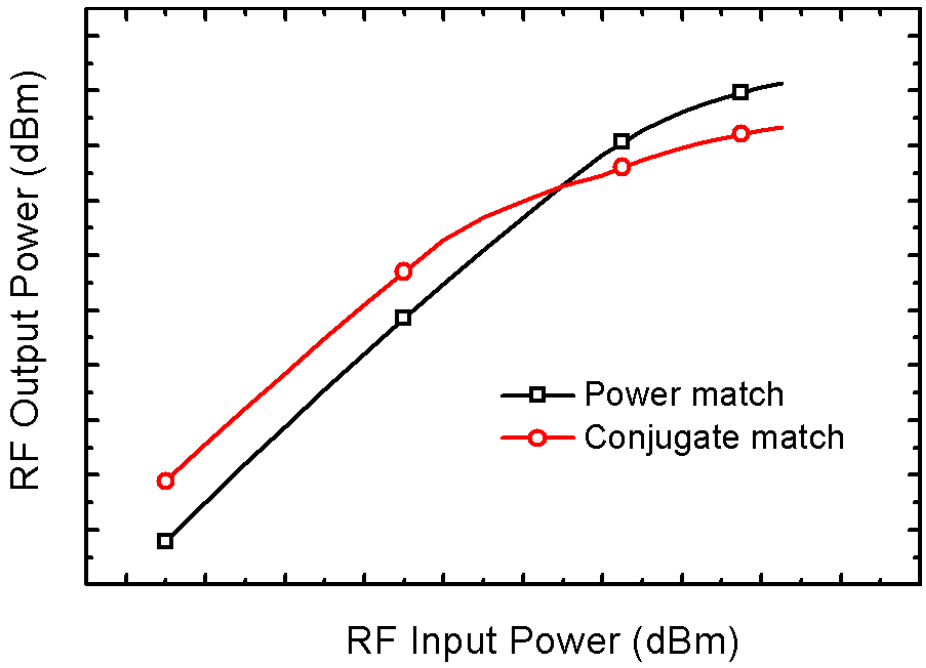


Figure 2.3: Effect of output match impedance on gain compression characteristics.

defined as the breakdown voltage of the device. The maximum current I_{MAX} is not clearly defined. Peak linear performance is achieved when devices are biased at the peak f_T / f_{MAX} current, although high performance can still be attained at currents past this peak. Practical devices generally do not exhibit hard current saturation until they are very heavily driven, so nonlinear high-injection effects and reliability concerns often practically set the limits of I_{MAX}. Because of this, I_{MAX} is often determined experimentally.

Typically when designing a PA it is desirable for the transistor core to have I_{MAX}, V_{MAX} and V_{KNEE} values that result in easily "matchable" impedances. If R_{OPT} is low or high, it can be very difficult to create practical matching networks to present this resistance to the device. The reactive component of the power match is typically tuned to the conjugate of the reactive (or susceptive) component of the device output impedance. This prevents any "looping" behavior in the dynamic load-line caused by reactive components and maximizes power output.

In order to correctly position the load-line for maximum current and voltage swings, the bias point of a power device is generally set to $((V_{MAX}-V_{KNEE})/2, I_{MAX}/2)$, as shown in Figure 2.2. This bias point maximizes fundamental tone output power. Rising input drive levels increase the ranges of the current and voltage swings, extending the dynamic load-line from the central bias point towards the corners of the I-V characteristics. When the voltage swing reaches the V_{MAX}, soft breakdown nonlinearities distort the voltage peaks. Similarly, when the voltage swing reaches the V_{KNEE} the device is slowed down by saturation region (triode region for a FET) operation and distortion occurs at the peaks. High-injection effects distort the current when the current swing reaches I_{MAX}. When the current swings towards negative infinity, the device effectively turns off and hard clipping occurs at the negative peaks. As the input drive increases, the amount of clipping/distortion at these limits increases and a larger proportion of the fundamental tone power is converted into undesired harmonics. The distorted waveforms for a compressed Class A PA are shown in Figure 2.4. The clipped peaks will clearly introduce strong odd harmonic components into the PA output spectrum

The significant nonlinearities in compressed devices and the resulting spectral content in distorted output signals are very difficult to model and simulate, which greatly complicates the design of PAs. The output voltages and currents of compressed devices are not purely sinusoidal, so the concept of a well-defined output impedance breaks down in such a situation. The *ac* impedance represented by V = IZ is only defined for purely sinusoidal signals. Impedances for heavily driven devices can only be defined as rough voltage-to-current ratios, so output impedances for these devices must be derived from the voltage and current waveforms [24]. Harmonic balance simulations are typically used to derive these waveforms. These simulations are notoriously slow and often suffer from convergence issues, making simulation-based PA design extremely difficult (and frustrating!).

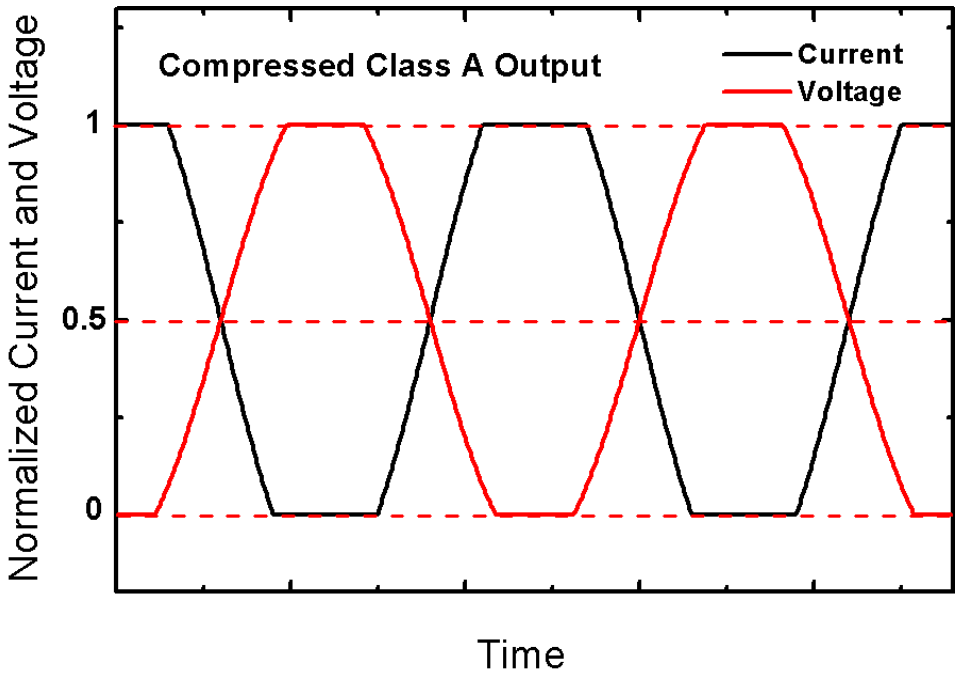


Figure 2.4: Output voltage and current waveforms of a heavily compressed example Class A PA. The clipped waveform peaks introduce a strong odd harmonic content into the output spectrum.

The most accurate way to determine the desired output impedance is to use measurement-based load-pull techniques. An impedance tuner is used to define the impedance presented to the output of a power device. Desired power characteristics (gain, output power, IMD, etc) are measured at this impedance, preferably through a power sweep. These measurements are repeated across a large constellation of points on the Smith chart. Once the measurement is completed, contours for each parameter can be imposed on a Smith chart showing where the optimal impedances for output power, gain, etc. are and how quickly those parameters degrade as the impedance is moved away from those points. Example contours are shown in Figure 2.5. Designers can use load-pull contours to determine the optimal output impedance to meet design specifications. Power contours are generally not purely circular due to the heavy nonlinearities inherent in heavily driven devices. After load-pull measurements are completed, the load tuner can be tuned to the desired point and source-pull measurements can be performed to

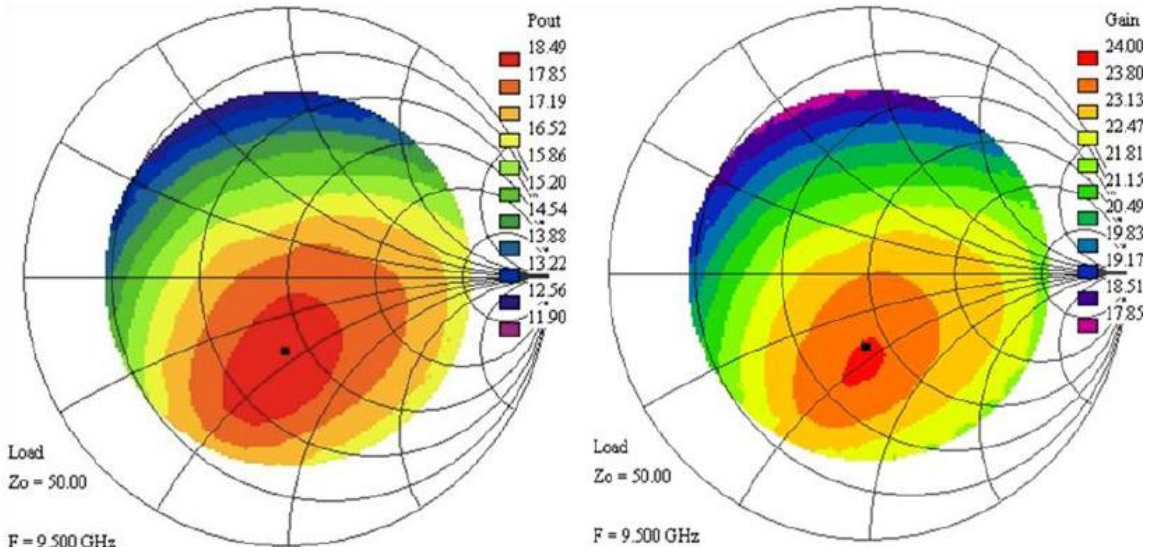


Figure 2.5: Load-pulled output power and gain contours for an example SiGe amplifier.

determine the optimal source impedance as well. The optimal source impedance for output power is generally near the conjugate match because the input side behaves linearly due to the lower signal levels present (assuming the device has high gain). Tuned measurements such as these are time-consuming, but they are far more accurate (and sometimes faster) than simulations and are very useful tools for designing PAs.

2.2.3 Efficiency and Classes of Operation

PA efficiency is an extremely important design consideration in many wireless systems. In heavily power-constrained applications such as cellular phones, power consumption must be minimized and the inherently inefficient performance of simple Class A PAs will not suffice. The original efficiency metric used for PAs, output efficiency (also referred to as collector efficiency for bipolar PAs or drain efficiency for FET-based PAs) is defined by

$$\eta = \frac{P_{out,fund}}{P_{dc}} \tag{2.4}$$

where $P_{out,\,fund}$ is the output power at the fundamental frequency and P_{dc} is the dc power consumption. The more commonly used efficiency metric which takes gain into account is power added efficiency (PAE), which is defined by

$$PAE = \frac{P_{out,fund} - P_{in}}{P_{dc}} = \frac{P_{in}}{P_{dc}}(G - 1) \tag{2.5}$$

where P_{in} is the input power and G is the amplifier gain. According to this metric, an amplifier is not truly efficient if it is not adding a significant amount of power to the signal. The PAE for an amplifier will tend to be low until high input drive levels are reached, when the RF output power is on the order of the dc power and the gain adds a significant amount of absolute power to the signal. Peak PAE for a PA is often reached in moderate to deep compression while the input power is rising more rapidly than the gain is compressing. Even if an amplifier has high gain, it will generally have low PAE at low input drive levels because it is adding an insignificant amount of RF power compared to the dc power used to bias the circuit.

The efficiency of a PA is limited by its class of operation. The class of a PA is defined by its nominal bias point and the resulting voltage and current waveforms. A snapshot of device I-V curves showing the bias points for basic PA classes is shown in Figure 2.6. The simplest PA is a Class A PA, which was described in great detail in the previous section. A Class A PA is biased at (V_{MAX}/2, I_{MAX}/2) to maximize output power. However, the output power for an optimally matched Class A PA is

$$P_{opt} = \frac{V_{dc}I_{dc}}{2} = \frac{(V_{MAX} - V_{KNEE})I_{MAX}}{8}, \tag{2.6}$$

which shows that the maximum efficiency of a Class A PA using ideal devices is 50%. Real PAs will not achieve this maximum efficiency due to power losses in passive elements and device nonlinearities (Early effect and channel length modulation, etc.) that are unavoidable in practical circuits [24]. Devices with high knee voltages have severely limited voltage swings and significantly reduced efficiencies as a result. Highly scaled

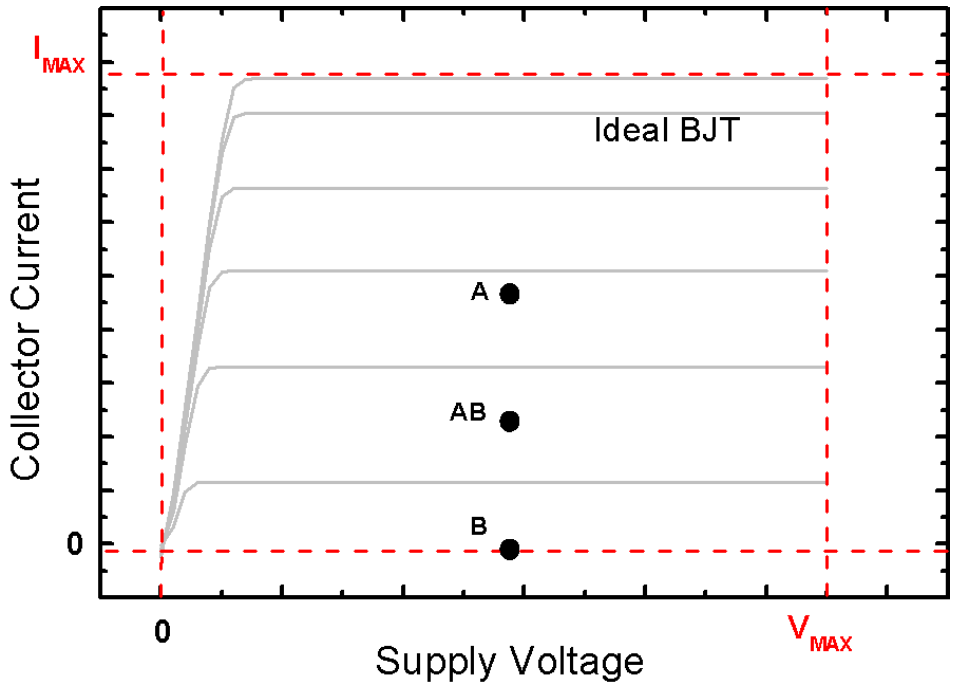


Figure 2.6: Nominal operating points for Class A, AB, and B operation imposed on ideal device I-V curves.

SiGe HBTs often have knee voltages of over 0.8 V and open-base common-emitter breakdown voltages of less than 2 V. The knee voltage in such a device effectively reduces the maximum output power by a factor of two over an ideal device with no knee voltage. A common rule-of thumb is that one should only design a Class A PA if a PAE of less than 25% is acceptable. Class A PAs have the highest output power and most linear performance of all PA classes, but they are theoretically the least efficient.

Class B PAs are nominally biased at an extremely low current as shown in Figure 2.6. The supply voltage is still set to $V_{MAX}/2$ for Class B and most other classes of operation. The nominal power consumption of a Class B PA is zero, but since the devices in the PA are effectively turned off, Class B PAs don't have any gain at low drive levels. As the drive level increases the PA current is swung into conduction for 50% of the cycle and swung back into zero-current cutoff for the other 50% of the cycle (corresponding to the positive and negative peaks of a sinusoidal input voltage). The RMS current of the PA becomes non-zero with increasing drive levels, so the gain and *dc*

power consumption increase accordingly. Eventually the gain will compress and the output power will saturate. The maximum theoretical efficiency of a Class B PA is 78.5%, which is clearly a large improvement over a Class A PA. This improvement comes at a cost, however. The gain is reduced from Class A operation and a significant amount of harmonics are generated by the 50% duty cycle current waveform. Class B PAs presents design challenges as well, for it is quite difficult to simulate the voltage and current waveforms of devices that are swung into operation entirely by the input drive. Class B PAs are quite nonlinear and have very different load-lines from Class A PAs, making simulation-based design of Class B PAs difficult. A common compromise between Class A and Class B operation is the Class AB PA, which is biased between Class A and Class B operation as shown in Figure 2.6. Class AB PAs trade off some linearity for significantly improved efficiency and are commonly employed in radar systems [24].

Numerous classes of operation have been proposed and are commonly used (all the way through Class S) in the pursuit of higher efficiency. Waveforms are increasingly distorted in order to further improve efficiency, and techniques such as envelope tracking, pre-distortion, and feed-forward are employed to re-linearize the PAs while maintaining high efficiency. Cellular PAs routinely attain efficiency in the range of 70-80% while maintaining the necessary output power. Radar PAs rarely employ these linearization techniques and typically operate in Class A or Class AB to maximize linearity, output power, and simplicity.

2.3 Power Limitations in SiGe HBTs

Designing high power PAs in SiGe BiCMOS processes presents unique challenges due to inherent power limitations of silicon-based technologies. The following subsections will discuss voltage (V_{MAX} and V_{KNEE}) and current limitations (I_{MAX}) in SiGe HBTs and the lossy nature of passives on silicon.

Table 2.1: Critical breakdown parameters for common semiconductors [25]

Material	Si	GaAs	GaN	InP	Ge
E_g (eV)	1.12	1.42	3.36	1.35	0.66
$\mathcal{E}_{crit}$ (MV/cm)	0.3	0.61	8.08	0.52	0.061
K_S	11.9	12.9	9.7	12.5	16.0

2.3.1 Voltage Limitations

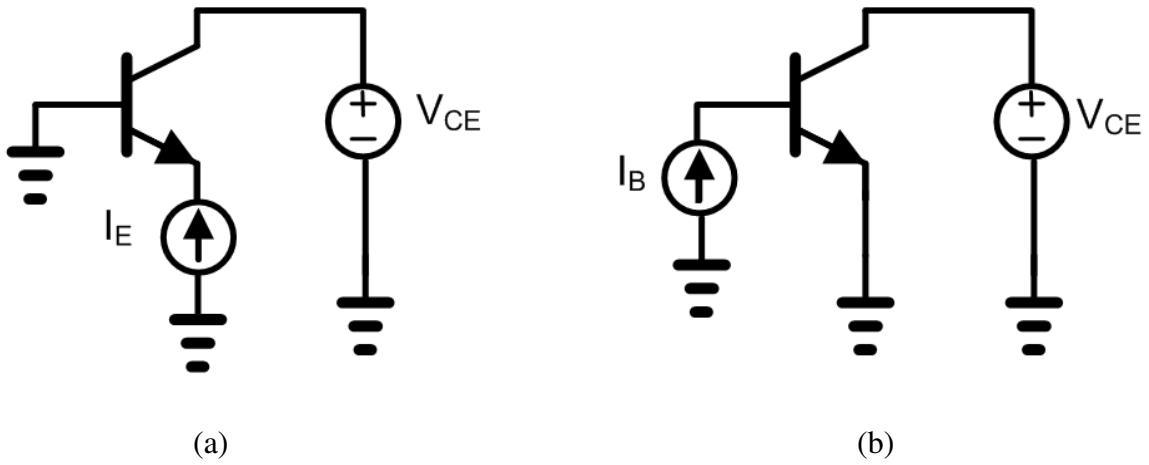
Breakdown voltages in *pn* junctions (and hence bipolar transistors) are fundamentally limited by properties of the semiconductor. Avalanche breakdown in a *pn* junction occurs when the breakdown voltage is reached per the following equation:

$$V_{br} = \frac{\mathcal{E}_{crit}^2}{\frac{2q}{K_S \varepsilon_0}\left(\frac{N_A N_D}{N_A + N_D}\right)} \tag{2.7}$$

where q is the fundamental electric charge, K_S is the dielectric constant of the semiconductor, ε_0 is the dielectric constant of free space, N_A is the acceptor doping on the *p*-side of the junction, N_D is the donor doping on the *n*-side of the junction, and $\mathcal{E}_{crit}$ is a material-dependent critical electric field [26]. The breakdown voltage is proportional to $K_s\mathcal{E}_{crit}^2$, which is determined by material properties. Wang [25] showed that the critical electric field in semiconductors is proportional to the bandgap cubed:

$$\mathcal{E}_{crit,semi} = 1.36 \text{ x } 10^7 \left(\frac{E_g}{4.0}\right)^3 \tag{2.8}$$

Bandgap values, critical breakdown voltages, and dielectric constants for common microwave semiconductors are listed in Table 2.1. Due to the low bandgap and subsequently low critical electric field of silicon, SiGe HBTs have lower breakdown voltages than devices on more advanced semiconductors. The low bandgap of germanium slightly reduces the bandgap and critical electric field of SiGe, but the change in small so the breakdown voltages of SiGe HBTs are nearly identical to those of same-sized silicon BJTs [6].



(a) (b)

Figure 2.7: Bias configurations for measuring (a) BV_{CBO} and (b) BV_{CEO}.

The breakdown voltage for a common-base configured HBT with an open emitter (forced emitter current bias) is referred to as BV_{CBO}. The bias configuration for measuring BV_{CBO} is shown in Figure 2.7(a). The open circuit looking out of the emitter effectively removes the emitter-base junction from the circuit, so BV_{CBO} is the breakdown voltage of the collector-base junction. Carriers gain energy with increasing voltages and generate additional carriers through impact ionization. Once BV_{CBO} is reached, avalanche multiplication occurs and the current goes to infinity, breaking down the junction. Although BV_{CBO} is the maximum limit for common-base operation, SiGe HBTs cannot be safely biased up to that limit due to common-base pinch-in instabilities. As the collector-base reverse bias increases, eventually the base current reverses direction and current begins to flow out of the base. This is caused when soft avalanche multiplication begins and avalanche holes flow out of the base terminal. The increasing reverse base current induces current crowding at the center of the transistor. The collector current becomes unstable at this point, creating kinks in the output characteristics. The reverse voltage at which pinch-in occurs can be considered to be the maximum stable bias point for common-base HBTs [27, 28].

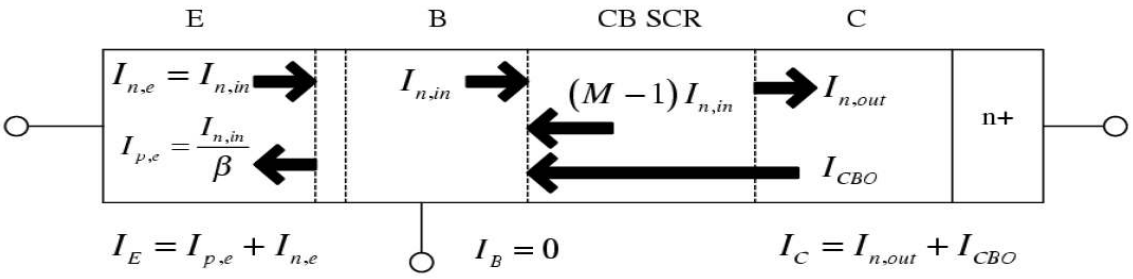


Figure 2.8: Illustration of the open-base avalanche multiplication process in a bipolar transistor [6].

The worst-case breakdown voltage for an HBT is BV_{CEO}, which is the case when a common-emitter HBT is biased with a forced base current (open base), as shown in Figure 2.7(b). Electrons injected from the emitter flow through the base into the collector-base space charge region. When a sufficiently high reverse bias is applied, impact ionization occurs in this space charge region. A reverse hole current that is equal to (M-1) times the injected electron current flows back into the base, where M is the carrier multiplication factor. The generated reverse hole current cannot directly exit the base due to the open circuit, so this current flows directly into the emitter. This produces an electron current in the emitter that is β times the injected hole current into the emitter. These multiplied electrons flow back into base. This positive feedback process causes avalanche breakdown to occur when (M - 1) = $1/\beta$, whereas (M - 1) must go to infinity for BV_{CBO} breakdown to occur [6, 26]. BV_{CEO} can be represented by the equation

$$BV_{CEO} = \frac{BV_{CBO}}{\beta^{1/n}} \tag{2.9}$$

where *n* is an empirical fitting factor that is typically between 3 and 6 [29].

HBTs can often be safely biased past BV_{CEO} in actual circuits. The actual breakdown voltage depends on the resistance presented to the base. If the base is open circuited the feedback mechanism will be unhindered and the breakdown voltage will be BV_{CEO}. If the base is shorted, the multiplied holes will all flow out of the base and the

open-base feedback mechanism will not occur, making the breakdown voltage BV_{CBO} (or more accurately, BV_{CES}). If a finite resistance is presented to the base, the breakdown voltage BV_{CER} will be somewhere between BV_{CBO} and BV_{CEO}. For base resistances less than around 1 kΩ, the positive feedback is negligible and BV_{CER} is effectively equal to BV_{CES} [29]. There is no known non-empirical equation for BV_{CER}, so although BV_{CEO} is not a hard limit and circuits should be designed with that in mind, care must be exercised so BV_{CER} is not exceeded, depending on the resistance presented to the base.

While BV_{CER} or BV_{CBO} set the maximum PA voltage V_{MAX}, the knee voltage is a significant power limitation in SiGe HBT PAs as well. The knee voltage is the transition between saturation mode and forward-active mode in bipolar transistors. From an I-V curves perspective, the knee voltage is the voltage where V_{CE} and V_{BE} are equal. The knee voltage in SiGe HBTs tends to be higher in SiGe HBTs than in silicon BJTs, around 0.8 – 0.9 V instead of 0.6 – 0.7 V. This voltage increases with scaling as well. The built-in voltage (turn-on voltage) in a base-emitter junction is defined by the following equation:

$$V_{bi} = \frac{kT}{q} \ln \left(\frac{N_{DE}^{+} N_{AB}^{-}}{n_i^2} \right) \tag{2.10}$$

where kT/q is the thermal voltage, N_{DE}^{+} is the donor doping in the emitter, N_{AB}^{-} is the acceptor doping in the base, and n_i is the intrinsic carrier concentration [26]. The intrinsic carrier concentration is proportional to $N_C N_V$ (the effective conduction and valence bands density-of-states product), which is lower in SiGe than in silicon because the effective masses of electrons and holes are reduced by adding germanium. This concentration is exponentially dependent on the bandgap, so the slight Ge-induced reduction in the bandgap further reduces n_i. The emitter is generally doped to solid solubility limits, which further reduces the bandgap and n_i due to bandgap narrowing. These Ge-induced reductions in n_i clearly result in an increased turn-on voltage (and in

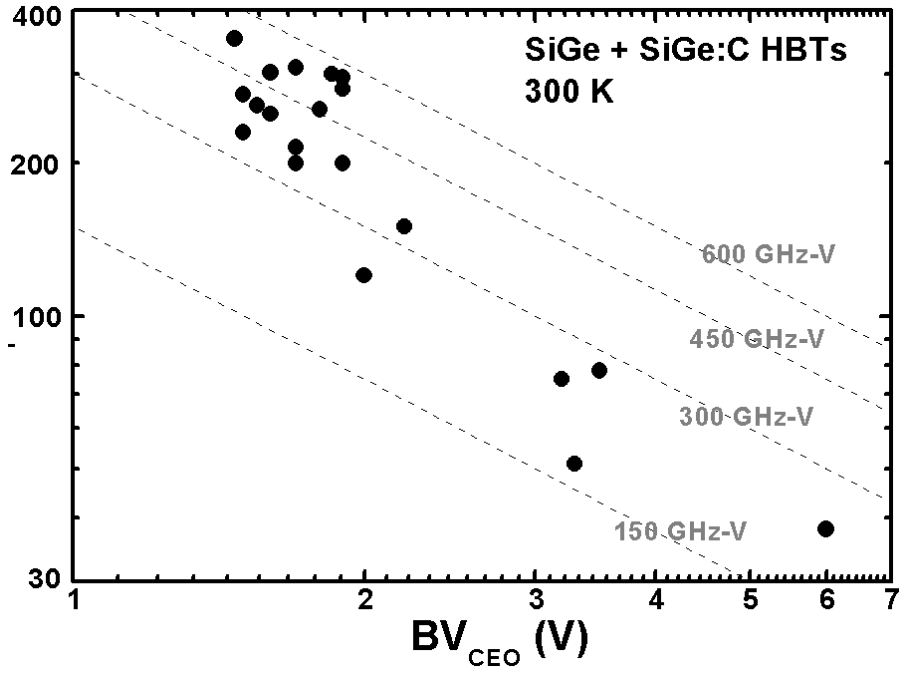


Figure 2.9: Published device data showing the fundamental speed-breakdown tradeoff in SiGe HBTs [12].

turn, knee voltage) for SiGe. As SiGe HBTs are scaled the germanium fraction increases, resulting in further reductions in $N_C N_V$, E_g, and n_i and ultimately increased knee voltages. Scaling both increases knee voltages and reduced breakdown voltages, significantly compressing the voltage swing range in SiGe HBTs [6].

Despite their numerous advantages, SiGe HBTs are fundamentally limited in their ability to generate significant amounts of power at high frequencies. Figure 2.9 contains published device f_T and BV_{CEO} data which shows the reciprocal speed-breakdown limitations in silicon-based bipolar transistors. In 1965, E. O. Johnson proposed that the maximum attainable f_T - BV_{CEO} product in silicon transistors is roughly 200 GHz-V, as dictated by the dielectric breakdown field and the saturated drift velocity [30]. This value is known as the "Johnson Limit." Many of the data points shown in Figure 2.9 clearly exceed the Johnson limit, so this is clearly not a hard limit. This reciprocal speed-power relationship is more accurately described in terms of BV_{CES}, which is truly a "hard"

bipolar power limit instead of BV_{CEO}, which is a worst-case power limit. Practical doping-dependent limits for the maximum f_T - BV_{CEO} product in silicon have been recently proposed to be around 300 GHz-V and 950 GHz-V for collector doping levels of 10^{16} and 10^{18} cm^{-3}, respectively [29].

These voltage limitations clearly complicate the design of PAs in SiGe, making it quite difficult to design high-power PAs for high-frequency applications in SiGe. As shown in Figure 1.4, III-V transistors simply have a higher speed-breakdown limit due to higher saturation velocities and breakdown fields. Improved device design techniques such as the use of superjunction collectors [12] have been proposed to improve this limit in silicon. Despite their voltage limitations and the ensuing design challenges, SiGe-based PAs are still extremely attractive due to their potential for high integration and low cost fabrication.

2.3.2 Current Limitations

The primary current limitation mechanism in SiGe HBTs is the Kirk effect [31]. The mechanism of the Kirk effect is as follows. Under high injection conditions, a large current density flows through a device. As the current increases, the high density of carriers will begin to collapse the electric field in the base-collector space charge region, causing the effective base width to increase. This slows down the device and causes the current gain and f_T to collapse. The current density at which the electric field collapses completely is given by the equation

$$J_{C,Kirk} \approx q v_{sat} \left(N_{DC} + \frac{2\varepsilon(V_{CB} + V_{bi})}{q W_{epi}^2} \right) \qquad (2.11)$$

where W_{epi} is the width of the epitaxial collector layer [6]. $I_{C,\,Kirk}$ is very close to I_{MAX} for most bipolar transistors. Saturation velocities for the primary microwave semiconductors are listed in Table 2.2. Silicon has the lowest saturation velocity of these materials, meaning the Kirk effect will occur at lower current densities in silicon than in these other

Table 2.2: Electron saturation velocities for common microwave semiconductors

Material	Saturation Velocity (cm/s)
Si	1×10^7
GaAs	1.2×10^7
GaN	2.5×10^7
InP	2.2×10^7

materials. V_{bi} decreases with increasing intrinsic carrier concentration n_i as shown in (2.10), and n_i is proportional to the inverse exponential of the bandgap [26]. Therefore, because silicon has the smallest bandgap of these semiconductors as listed in Table 2.1, silicon will have the smallest doping-independent V_{bi} which results in a relatively lower $J_{C,Kirk}$. Increasing the collector doping in a device increases the peak electric field in the B-C space charge region. This increased field requires a greater current density to generate sufficient charge to collapse the field. However, increasing N_{DC} reduces the breakdown voltage so the output power does not increase.

Equation (2.11) shows clear scaling implications for maximum SiGe HBT current densities. Device scaling increases speed and reduces device sizes and breakdown voltages. This translates to a reduced W_{epi} and increased N_{DC} and V_{bi}, resulting in a higher $J_{c,\,Kirk}$ for scaled devices. Although the maximum current density is increased, the maximum allowable device size is reduced with scaling. Therefore the maximum absolute current through devices is only slightly changed (often reduced) with scaling. Additionally, the higher operating current densities pose thermal and reliability concerns for SiGe HBTs. In order to achieve increased current levels without sacrificing speed or reliability, many HBTs must be combined in parallel. This causes issues with impedance matching and "current hogging" across groups of parallel devices.

The other potentially significant current limitation in SiGe HBTs is gain collapse caused by heterojunction barriers effects (HBE). In a well-designed HBT operating at low current densities at room temperature, the heterojunction barrier will be buried in the

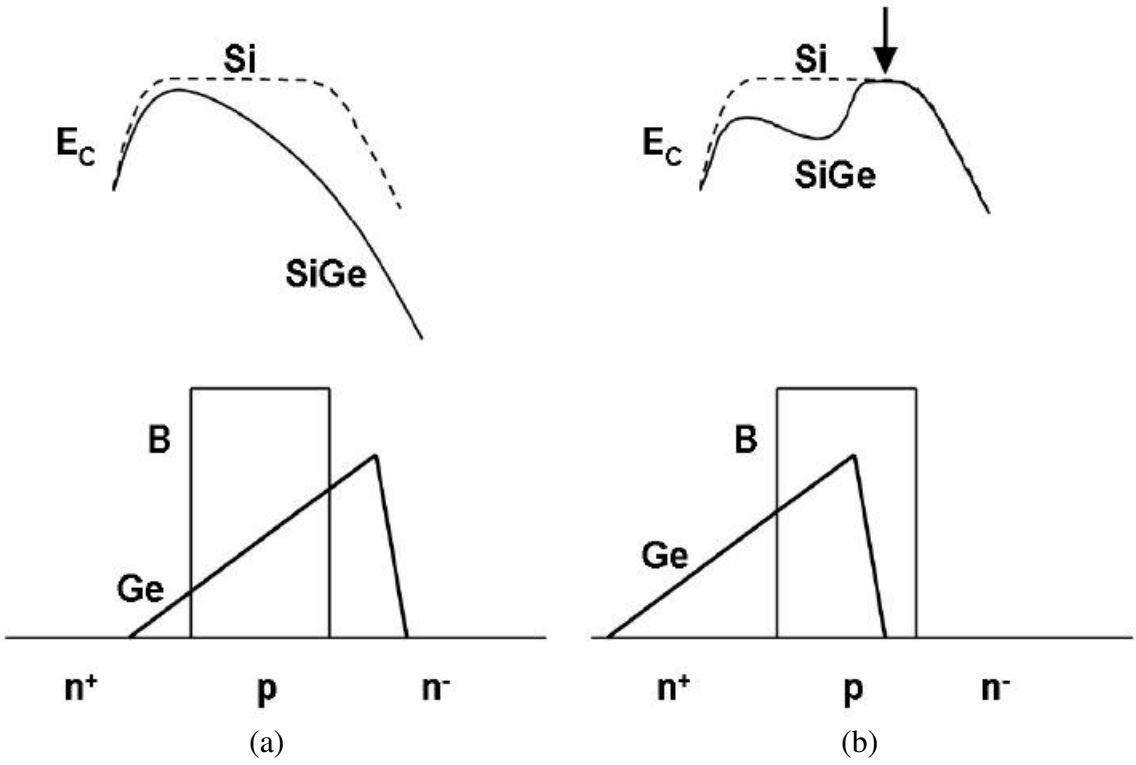


Figure 2.10: Illustration of (a) an unexposed heterojunction and (b) an exposed heterojunction barrier in the bandgap of a SiGe HBT [6].

B-C space charge region and will not manifest itself in the bandgap, as shown in Figure 2.10(a). As current densities increase and the B-C space charge region shrinks, this heterojunction can become exposed and appear as an electron barrier in the conduction band, as shown in Figure 2.10(b). This barrier greatly impedes electron drift through the base and leads to a strong premature collapse of β and f_T. This effect occurs at around the same current density as the Kirk effect in low-voltage (high-speed) SiGe HBTs operating at room temperature. HBE tends to dominate the high-injection cutoff behavior of SiGe HBTs as temperature decreases, so HBE are a major concern for cryogenic high-current applications of SiGe HBTs [6].

2.3.3 Passive Elements

The third fundamental power limitation in silicon-based RFICs is the lack of high-quality factor (Q) passives. For a given point on the Smith chart, Q is the ratio of the reactive or susceptive component to the resistive or conductive component. Points near the center of the Smith chart have low Q values and points near the edges (particularly near the upper- and lower-center regions) have high Q values. In order to match to an impedance with a given Q (denoted by Q_{match}), matching elements with Q ($Q_{element}$) equal to or larger than Q_{match} need to be used to design the matching networks. In other words, matching components with low $Q_{element}$ values can be used to match to "moderate" impedances (low Q_{match}) on the Smith chart, but high values of $Q_{element}$ are required to match to highly reactive or susceptive impedances near the edges of the Smith chart. High power PAs on silicon often employ transistor cores with a large amount of devices combined in parallel. This results in low resistance and high capacitance values looking into the input and output of the transistor core. Such a core has a high Q_{match} and requires high-Q inductors to resonate out the capacitance and make the core "matchable."

This high Q requirement exposes a fundamental challenge in SiGe PA design—the challenge of obtaining high inductor Q on silicon. Attainable inductor Q values are generally on the order of 15 to 20 in a silicon-based process. These values are quite low. Typical metal-insulator-metal (MIM) capacitors in SiGe technologies attain Q factors of around 70-80, which is far lower than typical values for off-chip capacitors. Although these capacitors are not ideal, they are relatively simple to implement in layout and do not impose any significant impedance matching challenges. Properly designing and laying out inductors is widely regarded as one of the most challenging aspects of designing RF circuits in a silicon technology.

Integrated inductors on silicon are typically implemented as planar spirals in the top metal layer. The standard compact model for an inductor on silicon is shown in Figure 2.11 [32]. One of the primary loss mechanisms in monolithic inductors is metal

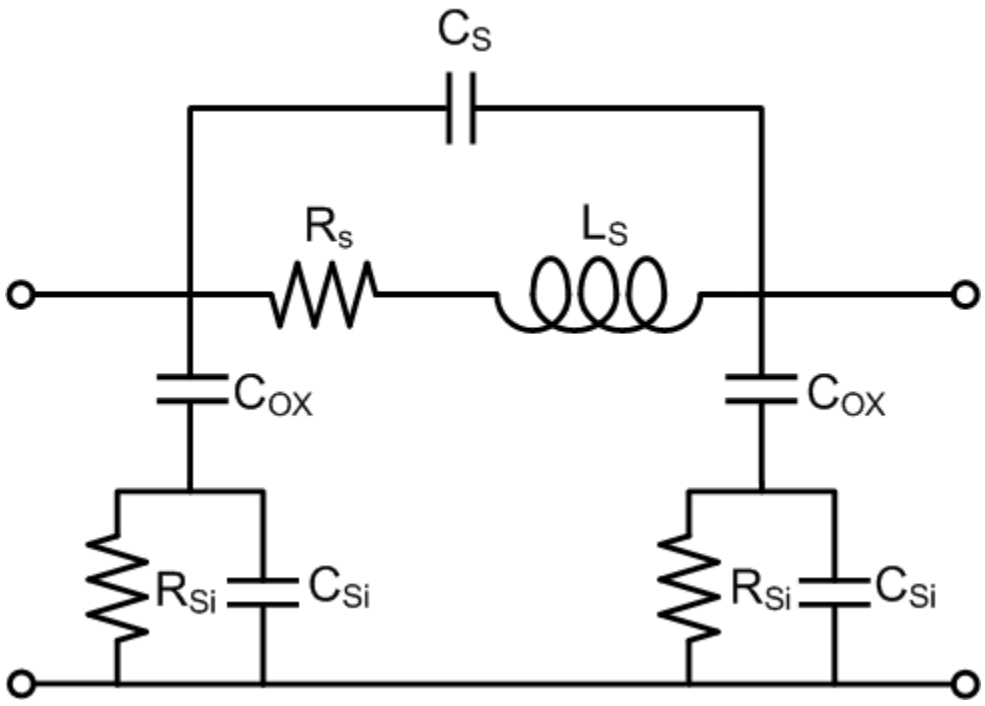


Figure 2.11: Standard compact model for a spiral inductor on silicon, neglecting eddy current losses [32].

trace resistance enhanced by the skin effect. As frequency increases, the current in a conductor is increasingly concentrated on the edges of the conductor, lowering the effective cross-sectional area seen by the current and increasing the resistance. Inductors on silicon are generally over 100 microns in diameter, and the long trace lengths and low trace widths often result in significant series resistances and reduced Q for inductors. The typical metallization used on silicon is aluminum, whose sheet resistance of around 10-100 Ω per square is relatively high [6]. The series capacitance C_S accounts for both crosstalk between adjacent traces in the inductor and capacitance between the metal traces and the underpass connection. This capacitance tends to be small and is most troublesome at high frequencies [32]. The oxide capacitance tends to be quite large since inductors are often up to hundreds of microns in diameter and the oxide thickness is generally less than 20 microns. This large capacitance results in a low self-resonant frequency for most inductors.

The losses in the silicon substrate are primarily accounted for by R_{SI} and C_{SI}. R_{SI} is the conductivity of the silicon substrate which is set by the background doping. The resistivity of silicon wafers tends to be on the order of 10-50 Ω-cm. This low resistivity provides for a conductive path for currents to bypass the desired inductor element, which increases loss and decreases Q. C_{SI} accounts for capacitance in the bulk silicon itself. The model in Figure 2.11 neglects another key loss mechanism in inductors on silicon – eddy currents. Magnetically induced eddy currents in the substrate reduce the effective inductance of the inductor and are difficult to model. The magnitude of the induced eddy currents increases as the substrate is moved closer to the inductor [33]. These loss mechanisms reduce inductor Q and self-resonance frequency and make the layout of inductors quite challenging. The resistivity of III-V wafers tends to be much larger than that of silicon wafers due to typical fabrication techniques in those technologies which greatly reduce substrate losses and results in higher-performance inductors.

Emerging methods to counteract these inductor loss mechanisms promise increased quality factors and self-resonant frequencies. The primary methods to reduce the metal trace resistance are to use thicker top metal layers and/or more conductive metals such as copper. Many high-speed commercial SiGe processes have thick top metal layers (~ 4 μm) and employ some copper metallization. The oxide capacitance can only be realistically decreased by increasing the oxide thickness, which is primarily a mechanical challenge [34]. The use of high resistivity silicon substrates greatly reduces inductor losses but is difficult to implement if CMOS fabrication compatibility is to be maintained [6]. Deep trench meshes in the substrate under inductors have been shown to improve Q by increasing the effective substrate resistivity and preventing the flow of eddy currents [35]. Another popular technique for suppressing eddy currents is to design patterned ground shield in the polysilicon or bottom metal layers that prevent the propagation of eddy currents and increase Q at the expense of a reduced self-resonant frequency [33]. These techniques give designers some flexibility in overcoming the

inductor Q limitations in silicon, and these challenges look to become more manageable as new SiGe processes often feature increased oxide thicknesses, thick copper traces, and new improved inductor layout configurations.

2.4 Increasing Output Power in SiGe HBT PAs

Given the aforementioned power limitation mechanisms in silicon-based technologies, there are three main approaches to improving the output power in high-frequency SiGe HBT PAs [28]. The first method is to increase V_{MAX} by using devices with higher breakdown voltages. This increases the allowable voltage swing, but in order to improve the breakdown voltage the collector doping must be decreased. This decreased doping results in a larger collector-base space charge region, which slows down the devices per Equation (1.1). If high gain is required at high frequencies, this approach is likely not an option. The second approach is to increase I_{MAX}, which is easily done by combining transistors in parallel. However, combining increasing amounts of transistors in parallel rapidly decreases the input and output resistances due to parallel resistor division and greatly increases the capacitive reactances due to capacitance addition. Only so many devices can be paralleled until the impedances are too close to the edge of the Smith chart to match with low-Q on-die passives. Matching can be achieved if is implemented with high-Q off chip passives, but this approach greatly reduces integration. Another method to improve output power is to drive the devices with a higher collector voltage and allow them to swing into weak breakdown. This trades off reliability, which is required for most practical applications [28]. An ideal option would be to use a device topology that increases the allowable supply voltage while preserving device reliability.

The cascode topology is a step toward this goal. A schematic of a cascode pair is shown in Figure 2.12. The addition of the upper device boosts the output resistance of the pair by a factor of β—a very large improvement. Both transistors share the same

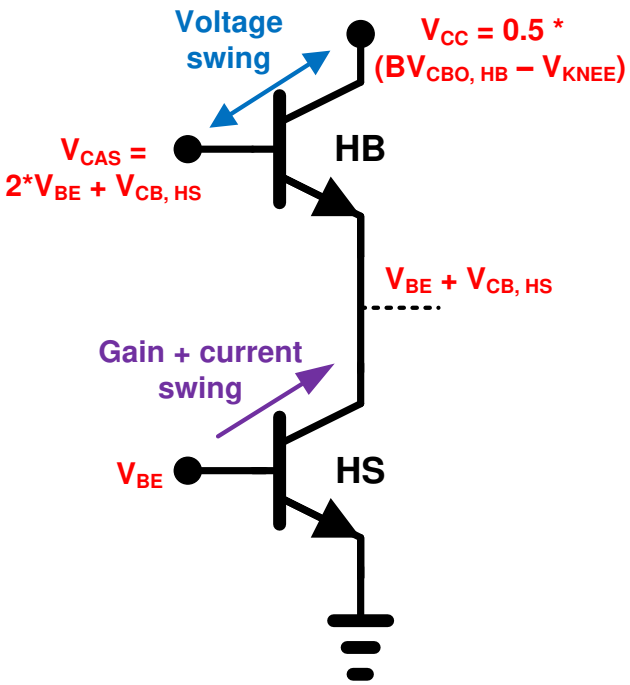


Figure 2.12: Schematic of a hybrid cascode SiGe HBT pair showing functionality of each device and nominal bias voltages.

collector current, so there is effectively no current gain in the upper device (common-base current gain α is less than unity). This implies that both the transconductance and current swing of the cascode pair will be set by the common-emitter device. The operation of the upper device is effectively that of a common-base device driven with a fixed emitter current. The gain characteristics of the pair are dominated by the bottom transistor; the upper transistor is primarily utilized to improve output resistance and to increase the allowable supply voltage. An additional benefit from the cascode topology is that the Miller effect is effectively negated. Looking out of the collector of the common emitter device, the resistance is equal to $1/g_m$. This low resistance means that very little voltage swing will ever be present at the node between the two devices. The voltage gain across the base-collector capacitance C_μ is nearly unity, so this capacitance will have a negligible impact on the high-frequency performance [36]. One drawback of cascode pairs is that they are prone to instabilities at the upper base node. This is caused

by a potentially negative resistance at the upper base ($\Gamma > 1$) being presented to an *ac* short circuit ($\Gamma = -1$), which is a recipe for oscillation. This tendency for oscillation can be mitigated by providing ample capacitance on the upper base and by inserting a small series resistance [37].

This topology can be further improved for use in PAs. Because the gain characteristics of a cascode are dominated by the bottom device, the primary function of the upper device in a PA is to provide maximum voltage swing. When the upper device is driven with a fixed emitter current and the upper base is presented with a short, the breakdown voltage of the cascode transistor is BV_{CES}. This upper device can be replaced with a high-breakdown HBT variant to further improve the voltage swing and to improve the power handling capability of the cascode pair. This is known as the hybrid cascode configuration [38]. Output characteristics of a common-emitter high-breakdown device and a hybrid cascode pair are shown in Figures 2.13 and 2.14, respectively. These plots illustrate the large improvement in breakdown voltage provided by this topology. The primary difference between high-speed and high-breakdown devices is collector doping. High-breakdown devices require low collector doping, whereas high-speed devices require high collector doping to decrease the width of the C-B space charge region and to increase speed per equation (1.1) [6].

The typical bias voltages for a cascode PA are annotated on the schematic in Figure 2.12. The upper base voltage is generally set to slightly over twice the V_{BE} of the lower device in order to minimize the knee voltage required to keep both devices in forward-active mode. The knee voltage of cascode pairs is higher than that of a single device but is generally lower than the extra voltage that is gained by using a cascode pair. This topology has been used to achieve the maximum power output demonstrated in a SiGe HBT PA at X-band to date [22]. Additionally, it has been shown that cascode SiGe cores have excellent reliability. The large voltage swing across the upper device

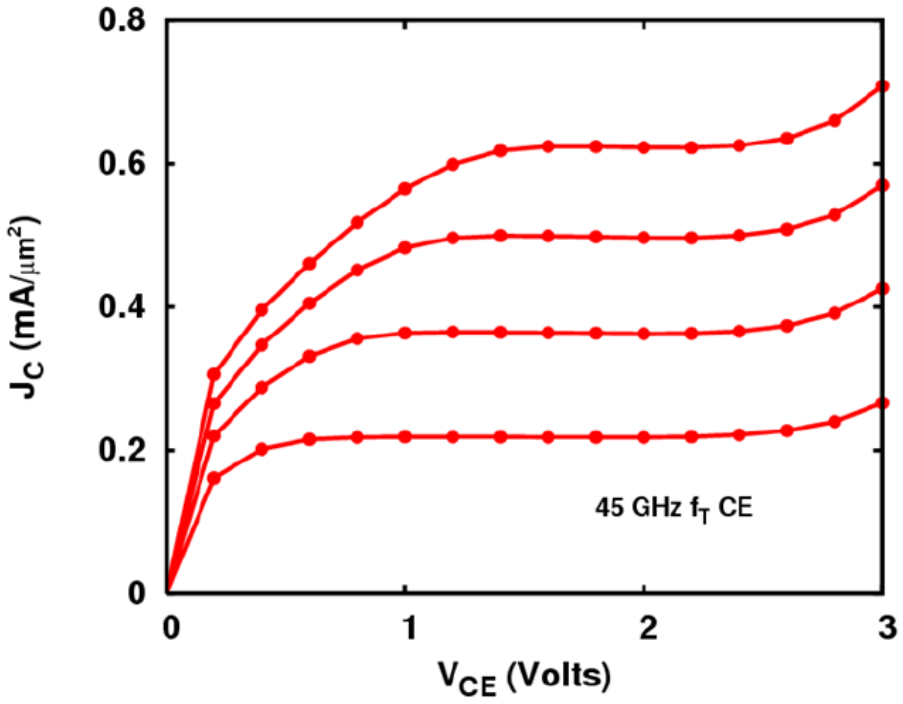


Figure 2.13: Output curves of a common-emitter high-breakdown third-generation SiGe HBT showing a low breakdown voltage [38].

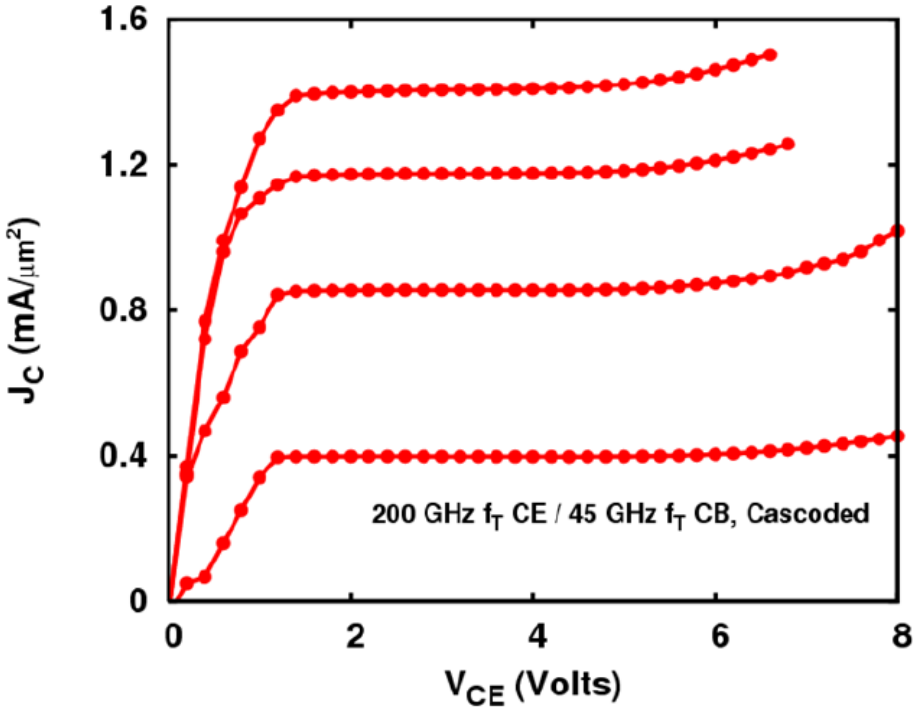


Figure 2.14: Output curves of a third-generation hybrid cascode SiGe HBT pair showing a significantly improved breakdown voltage [38].

increases the leakage and degrades β at low voltages, but this leakage has no impact on gain, output power, or linearity [39]. The improved voltage swing, high gain, and high reliability of the hybrid cascode topology make it an excellent device for high-frequency PA applications.

2.5 Summary

In this chapter we reviewed the primary considerations for designing SiGe HBT PAs. Basic concepts of PAs were reviewed, focusing on nonlinearity concepts, load-line design theory, classes of operation, and efficiency considerations. These concepts were then tied into the practical design of SiGe HBT PAs. Voltage breakdown mechanisms in silicon were presented along with the current-limiting HBE and Kirk effects. The lossy nature of passives on silicon was briefly discussed as well, focusing on how inductors complicate the design of SiGe PAs and limit the bandwidth of on-die matching networks. The final section discussed strategies for increasing the output power in SiGe PAs and presented the hybrid cascode topology as a method to overcome the shortcomings of the usual power-enhancement techniques. Chapter 3 will discuss the design and characterization of a SiGe PA for X-band radar with an emphasis on the considerations presented in this chapter.

CHAPTER III

X-BAND SIGE PA DESIGN AND CHARACTERIZATION

3.1 Introduction

This chapter discusses the design, characterization, and measurement-to-simulation correlation of an X-band hybrid cascode SiGe PA. The PA was designed for integration into a SiGe T/R module for an LPD AESA antenna panel. This antenna will be presented in detail in Chapter 4, but the characteristics of the antenna that drove the design requirements of the PA will be outlined henceforth. Each panel contains 64 radiating elements and 32 T/R modules, with one T/R module per two elements. The final multi-panel array will contain 2,304 radiating elements and 1,152 T/R modules (and integrated PAs). Therefore, it is very important that the PA is stable, does not have greatly varying performance from die-to-die, and does not require bias tuning. Tuning the bias of over 1,000 PAs is clearly impractical. A robust on-die self-bias network must be designed as part of the PA to satisfy this requirement. Additionally, there must be a capability to switch off the PA in order to save power and to prevent damage to the T/R switch and LNA while the radar is in receive mode.

Section 3.2 describes the PA design procedure and presents the simulation results. The characterization process and measurement results are outlined in Section 3.3. Finally, Section 3.4 will discuss an in-depth investigation to determine the source of shifted matching and degraded performance in the PA.

3.2 X-band PA Design

The technology used for designing the PA is IBM's BiCMOS8HP, a mature 3rd-generation commercially available SiGe process. Relevant specifications for this process are listed in Table 1.2. Design specifications for the PA are shown in Table 3.1. The

Table 3.1: Design specifications for the X-band SiGe PA

Center Frequency	9.5 GHz
Bandwidth	500 MHz
Gain	>20 dB
Output Power	15 dBm
PAE	>30%

specifications are not overly ambitious for a X-band PA design in this process. 20 dB of gain at X-band should be readily achievable using a single stage amplifier with high-speed HBTs variants as the primary gain elements. The required output power of 15 dBm can be considered "medium" and is not particularly ambitious at X-band in this technology. The >30% PAE requirement implies that this PA should be designed to operate in Class AB.

3.2.1 Transistor Core Design

The first step in the design process is to choose the topology and design the transistor core. The topology chosen for this PA was the single stage hybrid cascode due to the high gain and improved voltage swing this topology provides. In order to maximize the performance of each hybrid cascode device, it is important to ensure that both the high-speed and the high-breakdown devices are operating at the same proportional current densities. The onset of the Kirk effect occurs at a lower current density in high-breakdown devices than in high-speed devices, as explained in Chapter 2. If the high-speed and high-breakdown devices are the same size, the high-breakdown device will compress before the high-speed device. When the high-speed device is approaching peak gain, the high-breakdown device is compressed and will likely have low or negative gain. This results in wasted performance and is undesirable. The size of the high-breakdown device should be increased so the onset of the Kirk effect occurs at the same bias current in both devices. This maximizes the gain of the pair so performance is not wasted.

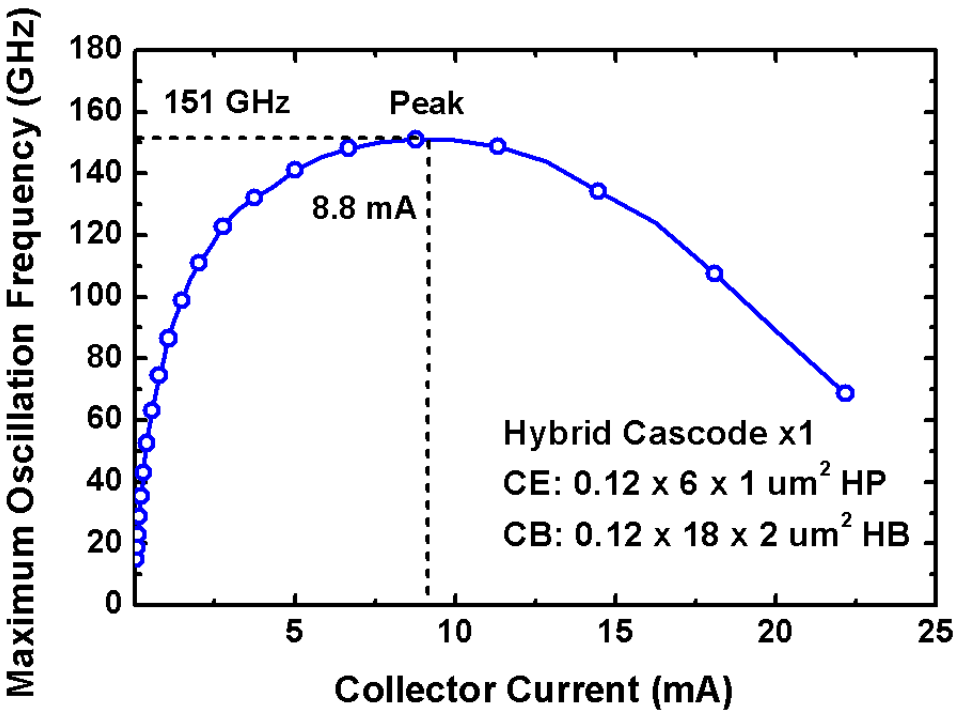


Figure 3.1: Maximum oscillation frequency (f_{MAX}) plotted versus linear collector current for the hybrid cascode device.

In the 8HP process, high-speed (HS) devices reach peak f_T at a current density around 12 mA/μm^2 while high-breakdown (HB) devices peak at around 2 mA/μm^2. This means that the high-breakdown device area should be six times that of the high-speed device. The actual sizes of each device should be sufficiently large to drive the desired amount of current per cascode. The selected device sizes were 0.12 x 6 μm^2 for the common-emitter device and 0.12 x 18 x 2 μm^2 for the common-base device. Two high-breakdown devices were used for each high-speed device so each cascode could drive sufficient current levels, which slightly complicated the layout. Figure 3.1 contains a plot of simulated f_{MAX} against linear bias current for the designed hybrid cascode. Typically f_T and f_{MAX} are plotted versus logarithmic current. Linear current, however, is more relevant for designing PAs, which normally operate at high dynamic current levels. It should be noted that f_{MAX} is a more relevant metric for RF circuit design than f_T, but the current density at which peak f_{MAX} and f_T occur is almost identical. The current density

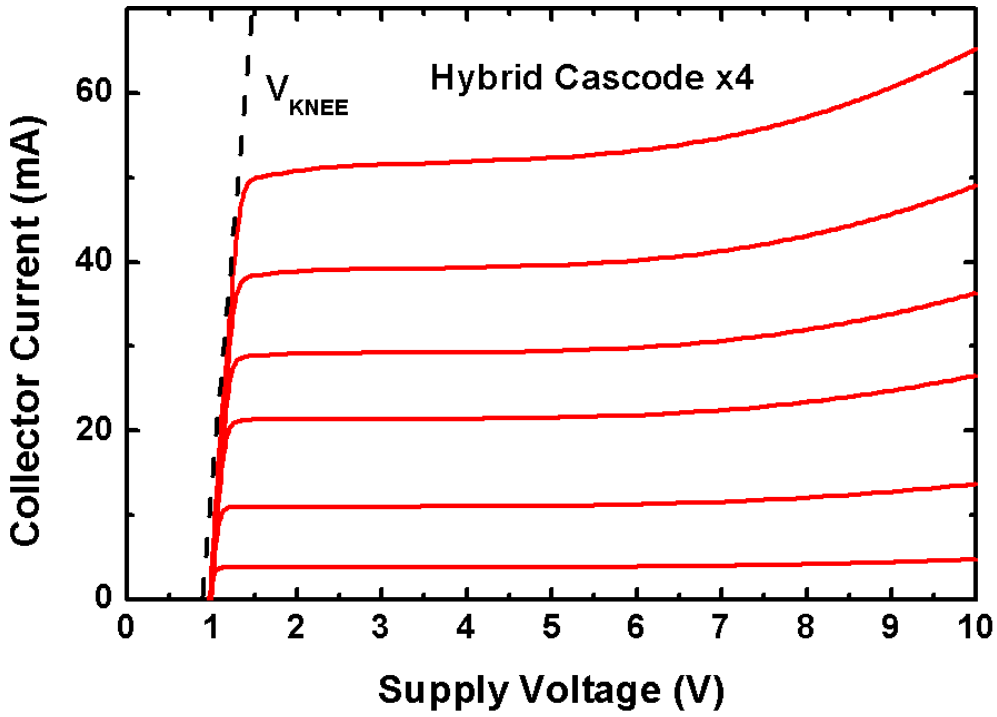


Figure 3.2: Simulated output characteristics for the four-cascode PA core.

at which peak performance occurs is more relevant to PA design than the actual values of f_T or f_{MAX}.

Because the output power specification is not particularly aggressive, only a few parallel cascodes are required to achieve the necessary current swing. If lower voltage devices were used more parallel devices would be required to achieve the required output power. This would complicate the design of the input and output matching networks because the resistive components of the impedances would be reduced and the reactive components would be increased, requiring the use of higher-Q passives and limiting the matching bandwidth. Using a low number of hybrid cascodes makes the input and output matching simpler and allows for a larger bandwidth. Initial large-signal simulations indicated that four of the hybrid cascodes in parallel should be sufficient to achieve the desired output power of 15 dBm using on-chip matching elements.

3.2.2 Biasing

The next step in the PA design process is to choose the nominal bias point and to design the bias networks. A plot of simulated I-V curves for the PA core is shown in Figure 3.2. The knee voltage is over 1 V for this core, which is quite high. The supply voltage was chosen to be 5 V for this design. This rail allows a swing of 4 V down to the knee and around 5 V towards the breakdown voltage. The output power could most likely be increased by using a larger supply voltage, but the use of a lower voltage ensured ensure robust and reliable performance which was the primary design goal. The nominal bias current was chosen to be 5.4 mA, which corresponds to deep class AB operation per the I-V curves in Figure 3.2.

The cascode voltage was generated from an on-die bandgap reference (BGR). BGRs are voltage sources that balance the opposite temperature dependences of the diode turn-on voltage and the fundamental thermal voltage kT/q to generate a stable, precise, nominally temperature-independent voltage [40]. The simple BGR implemented in this PA generates a reference voltage of 2.66 V. This voltage is driven through an op-amp buffer and divided down to 1.77 V before reaching the upper base node of the PA core. This buffer makes the BGR appear as an ideal voltage source to the transistors. The resistance introduced by the resistor divider helps to ensure RF stability at the cascode node as well [37].

The lower base bias for the PA was generated by a complementary-to-absolute-temperature (CTAT) current source. As temperature increases, the voltage generated by a CTAT source decreases. This behavior is desirable because the turn-on voltage in bipolar transistors exhibits a CTAT behavior. The on-die CTAT source generates a 290 μA reference current which is passed into a f_T-doubler circuit. f_T-doublers have high gain and therefore high reverse isolation. This purpose of the f_T-doublers in this PA is to prevent any RF from leaking into the reference circuit [41]. A resistor divider was used at the output of the f_T–doubler to implement an RF choke and to set the bias voltage and

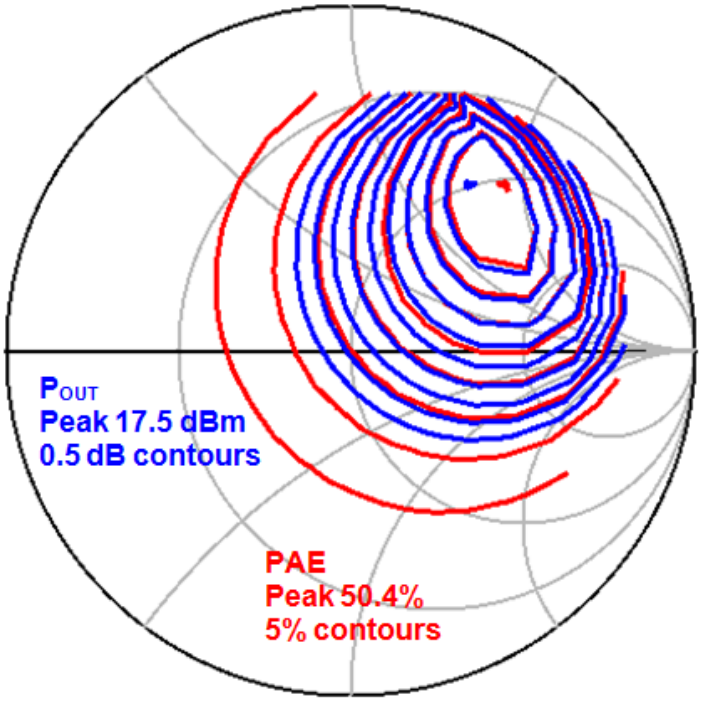


Figure 3.3: Simulated load-pull contours for the PA core with self-bias network and emitter inductor.

current at the lower base of the cascode core. The CTAT source can be disabled when an external signal of 2.5 V is applied. This satisfied the requirement that the PA can be turned off when the radar is receiving. The BGR and CTAT source require a single 3.5 V supply to generate the lower base and upper base bias references, so no bias tuning would be required in this PA design. A separate 5 V signal must be supplied to the circuit in order to generate the PA rail voltage.

3.2.3 Impedance Matching

In order to simplify the matching impedances a small inductor was placed between the emitter node of the PA core and ground. Emitter inductance reduces the capacitance seen looking into the input and output of the core, which makes those impedances more resistive and therefore easier to create high-bandwidth matching networks for. Emitter inductance improves two-tone linearity as well [42]. It is very

important to not place too much inductance on the emitter, because at high current levels a V = I x Z drop across the inductance can cause the phenomenon of "ground bounce," where the potential at the emitter "bounces" with the swinging current. Ground bouncing often results in degraded performance and oscillatory behavior. Devices are very sensitive to emitter impedance, so this inductor was considered to be part of the amplifying core for the rest of the design process.

Next, load-pull simulations were performed to determine the optimal load impedance. These simulations were performed in Agilent Advanced Design System (ADS). The user specifies an RF input power, fundamental frequency, and an impedance range on the Smith chart to simulate. A harmonic balance simulation is performed at each load impedance point, and the output power and PAE are calculated from the simulated waveforms at each point. The results are then plotted as contours on the Smith chart. In order to ensure maximum simulation accuracy, the load-pull simulation was performed on the cascode core with the emitter inductor and the self-bias network connected. The input signal had an amplitude of -5 dBm at 9.5 GHz, which was chosen so a core with 20 dB of gain would saturate at a power level of at least 15 dBm per the design specifications. The simulated contours are shown in Figure 3.3. The peak output power of 17.5 dBm and PAE of 50.4% both exceed the design specifications. It is fortuitous that the optimal impedances for both power and efficiency are extremely close on the Smith chart, occurring at impedances around $61 + j72\ \Omega$. The output power and PAE will both be reduced from the peak values when matching networks are designed using on-silicon passives, so safety margins between the load-pulled and actual output power and PAE of the final PA were necessary to meet the design specifications.

The output match was implemented as a standard L-C high-pass filter. Such a topology is highly desirable in matching networks because the inductor acts as an RF choke and the capacitor acts as a *dc* block, so the matching network both matches the impedance and functions as a bias tee. The network was designed to match the

impedance 61 + *j*72 Ω to 50 Ω. In integrated RF systems it is often more efficient to match to impedances other than 50 Ω between circuit blocks to reduce losses. However, this PA was to be fabricated as both part of a T/R module and a stand-alone test structure so it was matched to 50 Ω in order to minimize mismatches between the test setup and the test structure output. A 2 Ω resistor was inserted between the 5 V rail and the load inductor in order to damp out any potential oscillations. This resistor slightly reduces performance to help ensure stability, one of the primary requirements of the circuit. Capacitance was placed between the inductor and this resistor to ensure a good RF ground at this node, so that no RF energy would leak into the power supply.

The last step in the schematic-level design process was to design the input matching network. As mentioned in Chapter 2, the input match is typically designed to conjugately match the input impedance to achieve maximum power transfer. High gain lower-power PAs behave linearly on the input side due to the low impingent power levels, so a conjugate source match is desirable. The input match was implemented as a C-L-C "tee" bandpass filter. Three-element matching networks are lossier than simple two-element networks but have lower Q and allow for a larger bandwidth. Previous PA designs for this project had experienced unwanted and unexpected matching shifts from simulation to measurement. The improved bandwidth provided by a three-element matching network was an attempt to mitigate the performance degradation from matching shifts if they were to occur again. A schematic of the final PA including the core, self-bias circuitry, and matching networks is shown in Figure 3.4. Table 3.2 contains a list of values for the elements in Figure 3.4.

3.2.4 Simulation Results

The simulated S_{11} and S_{22} of the full PA are shown in Figure 3.5. The PA is clearly matched at 9.5 GHz. The quality of the match is not ideal (around -15 dB), but this is to be expected due to the intentional mismatch on the output and the higher-

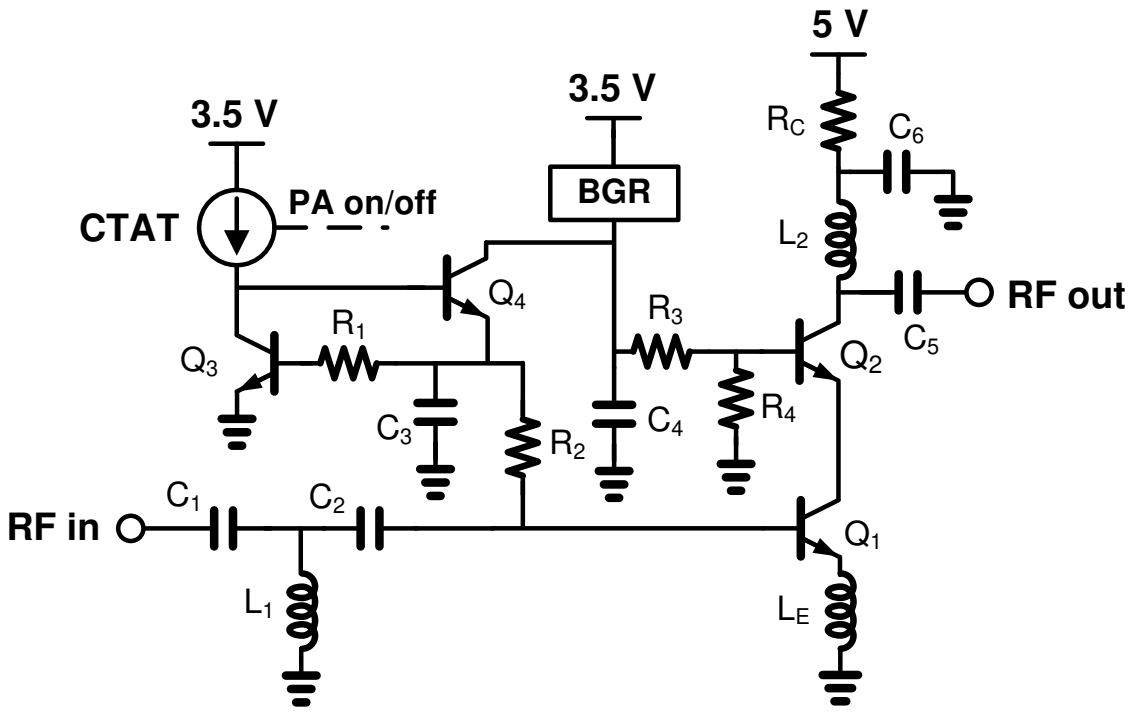


Figure 3.4: Top-level schematic of the X-band SiGe PA.

bandwidth lower-Q matching network at the input. Figure 3.6 shows that the simulated S_{21} (gain) of the PA is over 20 dB across the design bandwidth and peaks at over 23 dB. This clearly meets the design specifications. The simulated stability parameters are shown in Figure 3.7. The Rollett stability factor K is above unity and the stability measure is positive, which indicates unconditional stability for the PA. It should be noted that this K-factor test does not take stability at internal nodes into account. Potential instabilities at the cascode node are not reflected in these curves, so additional measures must be taken to ensure no instabilities arise at that node. Swept power simulation results are shown in Figure 3.8. The saturated power is 15 dBm and peak PAE exceeds 30%. The simulation results therefore indicate that this PA meets and/or exceeds all design specifications.

Table 3.2: Component values for the X-band SiGe PA

Q_1	0.12 x 6 x 4 HP
Q_2	0.12 x 18 x 8 HB
Q_3	0.12 x 1.2 x 1 HP
Q_4	0.12 x 1.2 x 1 HP
C_1	320 fF
C_2	2 pF
C_3	2 pF
C_4	5.8 pF
C_5	190 fF
C_6	2 pF
R_1	5 kΩ
R_2	500 Ω
R_3	10 kΩ
R_4	20 kΩ
R_C	2 Ω
L_1	658 pH
L_2	928 pH
L_E	42 pH

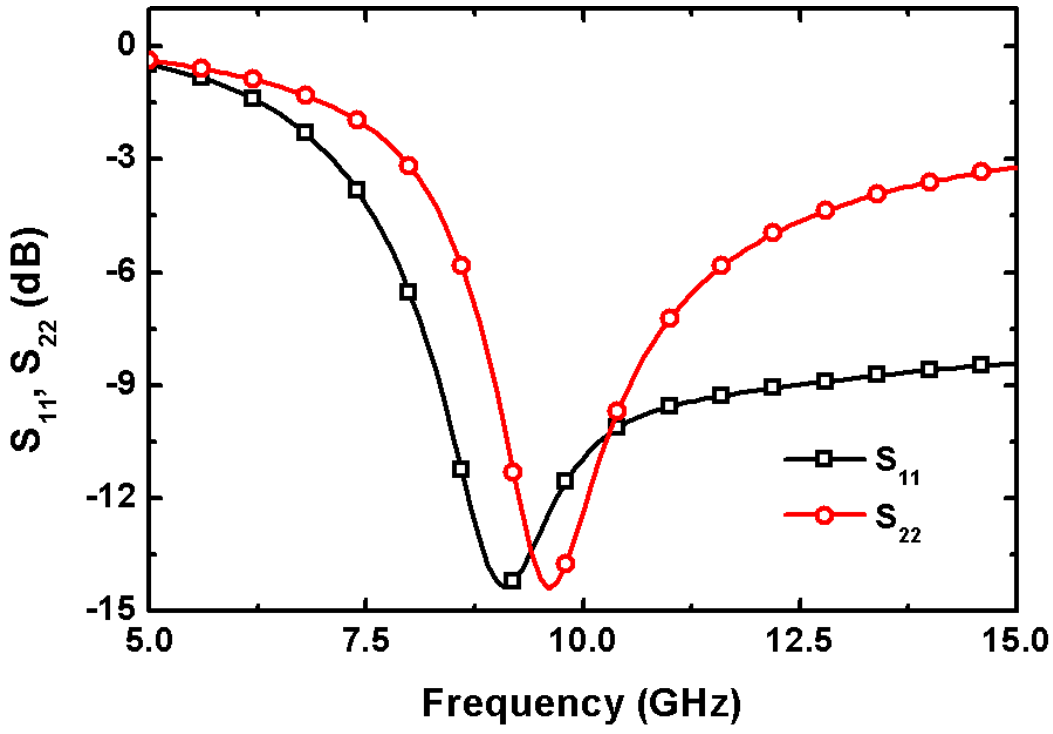


Figure 3.5: Simulated S_{11} and S_{22} (input and output match) of the X-band SiGe PA.

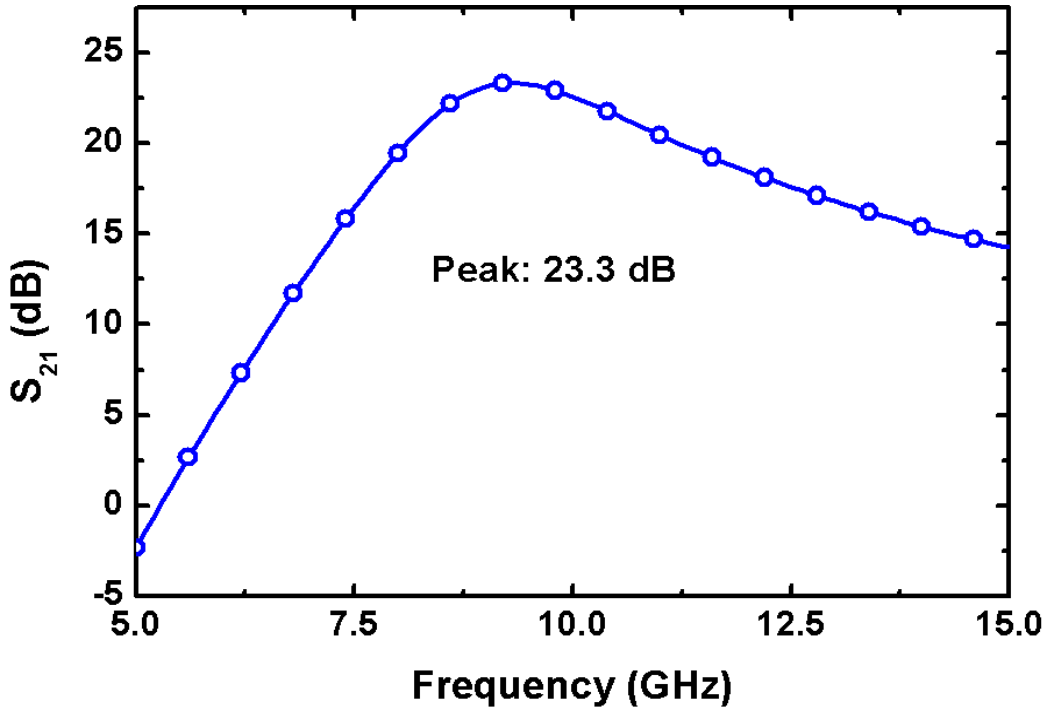


Figure 3.6: Simulated S_{21} (gain) of the X-band SiGe PA.

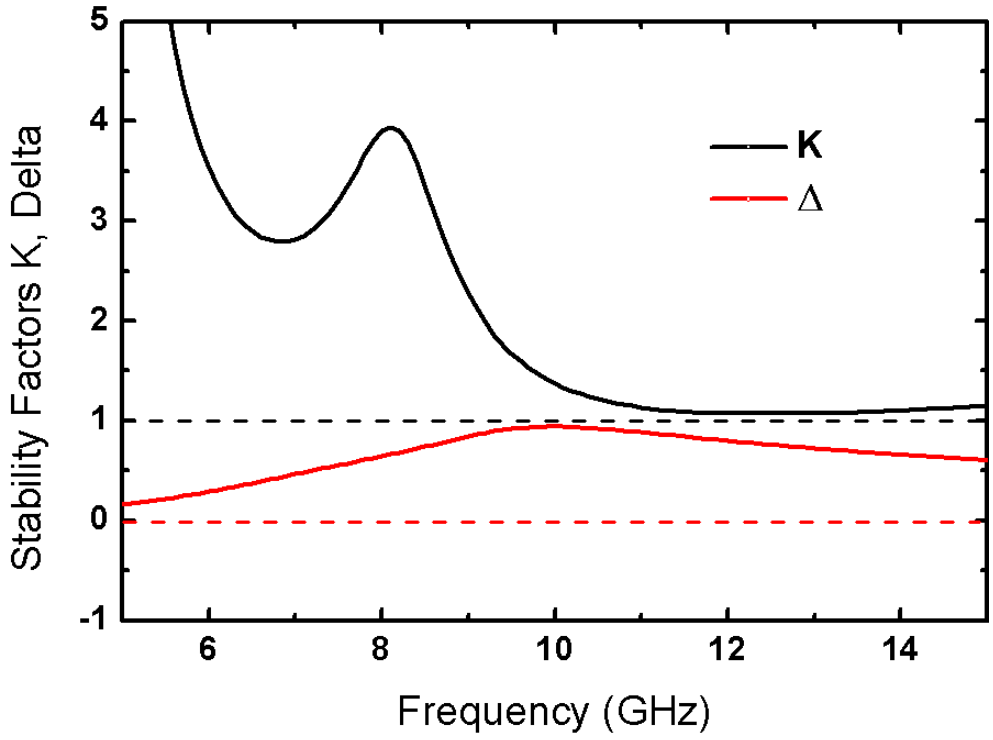


Figure 3.7: Simulated stability parameters of the X-band SiGe PA showing unconditional stability across the range 5-15 GHz.

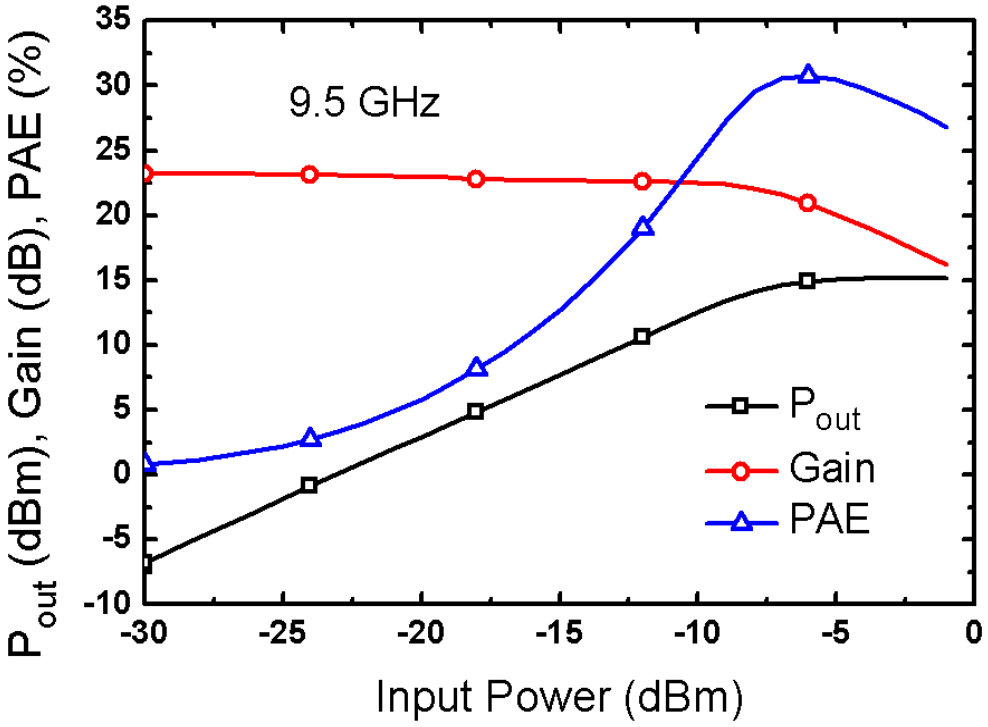


Figure 3.8: Simulated large signal performance of the X-band SiGe PA.

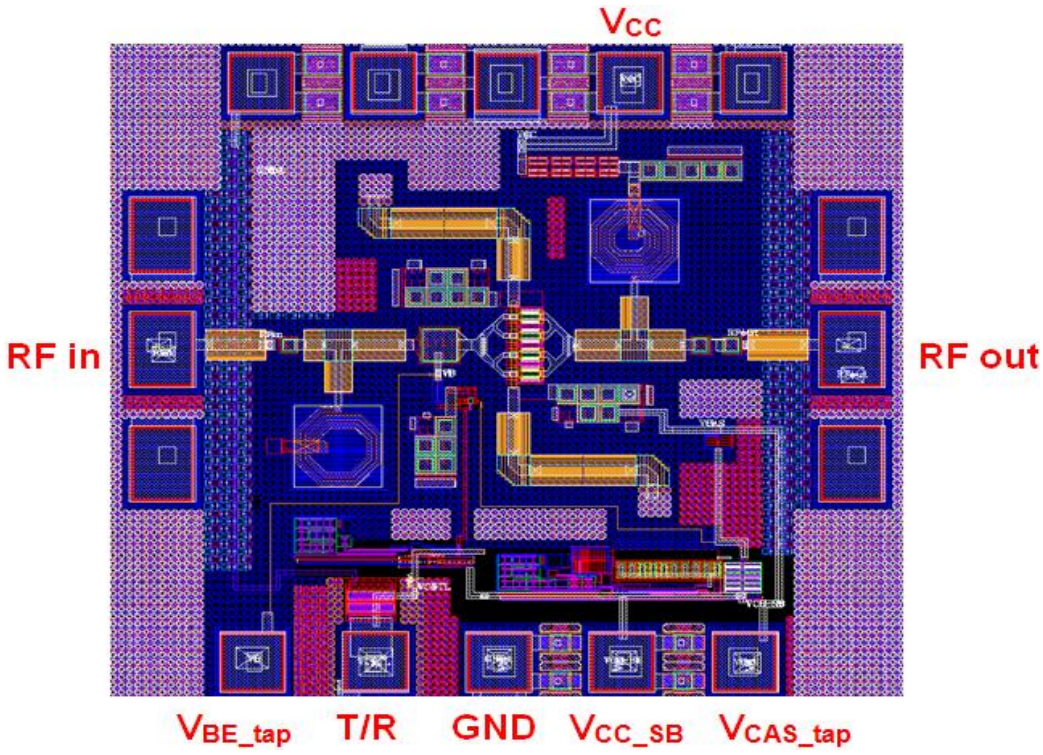


Figure 3.9: Layout of the PA test structure showing pad labels.

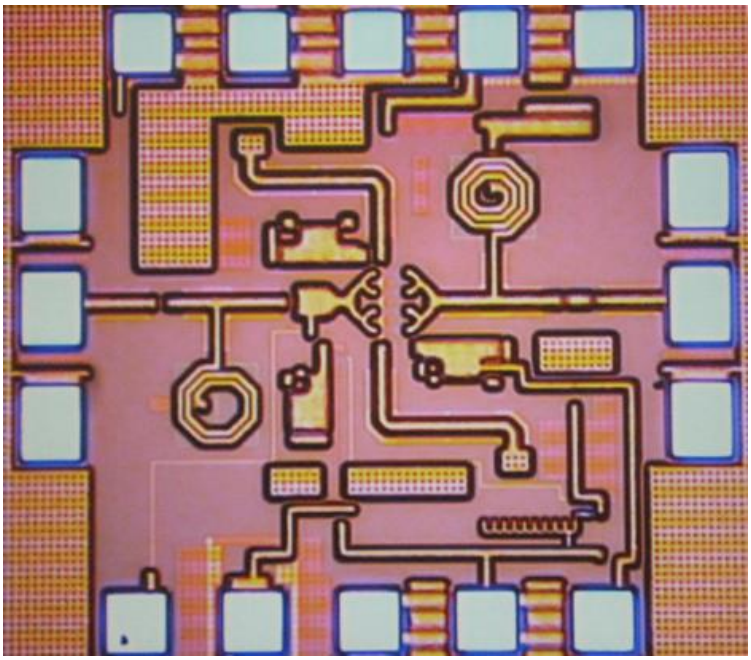


Figure 3.10: Photomicrograph of the fabricated self-biased PA test structure.

3.2.5 Layout Considerations

The layout of the standalone PA test structure showing padouts is shown in Figure 3.9. The size of the PA layout including pads is 0.92 x 0.98 mm^2. The "tap" pads allow for direct measurements of the voltages generated by the self-bias networks. The unlabeled pads at the top of the layout are unused. The RF pads are intended to be probed with traditional ground-signal-ground wafer probes with a pitch of either 150 μm or 250 μm.

The PA was laid out with a ground mesh on the bottom metal layer (M1) so ground is well-defined across the whole circuit. Substrate contacts are included with each mesh element to ensure that the substrate itself is well-grounded and to help meet process-required density specifications. All RF path interconnects are implemented as 50 Ω microstrip lines to ensure good signal control in the critical transmission path. The emitter inductor was implemented as two separate 50 Ω microstrip lines to achieve the low inductance and to minimize the parasitic resistance on the emitter that could cause

Table 3.3: Measured versus simulated PA self-bias voltage and current values.

	Simulated	First PA	Second PA
V_{BE}	0.841 V	0.846 V	0.847 V
V_{CAS}	1.777 V	1.83 V	1.73 V
I_C	5.34 mA	6.11 mA	6.22 mA

ground bounce. All spiral inductors utilized M1 ground shields to prevent the flow of eddy currents and to increase L and Q at the expense of higher oxide capacitance and a reduced self-resonant frequency. The capacitor in the output matching network was implemented as two series capacitors in order to physically implement the small capacitance required to obtain a good impedance match.

3.3 PA Characterization

A die photo of the fabricated SiGe PA is shown in Figure 3.10. The first step in the characterization process was to ensure the self-bias networks functioned correctly. Bias values were measured for two separate PAs, and the results are shown in Table 3.3. The voltages and currents shifted somewhat from the simulated values, but the shifts were too small to have a significant effect on the performance of the PA. The bias points of the two PAs were quite close, which is necessary to ensure uniform gain and output power across the final antenna array. The goal of minimizing bias variations between die is therefore considered to be met.

The performance of the SiGe PA was measured on a custom on-wafer measurement station designed in conjunction with Focus Microwaves, Agilent Technologies, and Suss Microtech. This station can perform S-parameter, noise figure, and load- and source-pull measurements up to 40 GHz with a single probe contact. An image of this measurement station is shown in Figure 3.11.

Measured and simulated S-parameters for the PA are shown in Figure 3.12. The peak gain was reduced by nearly 10 dB from simulation and was shifted out of the design

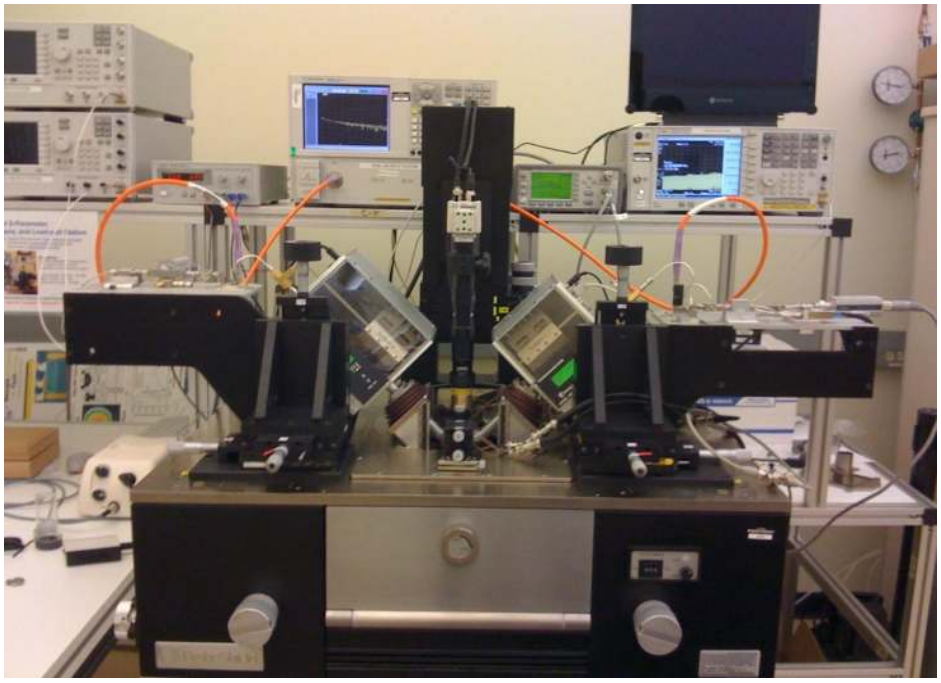


Figure 3.11: Photo of the integrated S-parameter, noise figure, and load-pull measurement station.

bandwidth. The output resonance was shifted from around 8.5 to 10 GHz but is still reasonably well matched across the design bandwidth. The input match, on the other hand, is shifted much higher in frequency and is poorly matched at both the design frequency and higher frequencies. This shifted input match is the most likely source of the degraded performance in measurement. Figure 3.13 shows that the PA is unconditionally stable from 8-20 GHz.

Measured large-signal performance of the PA at 9.5 GHz is shown in Figure 3.14. The small signal power gain is 11.7 dB, the output power is 14 dBm, and the peak PAE is 14%. The output power is slightly reduced from the design specification. This may have been caused by the slight shift in the output match or by inaccuracies in the large-signal models used for load-pull simulations. The PAE is reduced from simulation as a result of the reduced gain and output power. Although none of these power metrics met the design specifications, the PA was stable, self-biased, and exhibited little die-to-die variation which made it acceptable for integration into a T/R module.

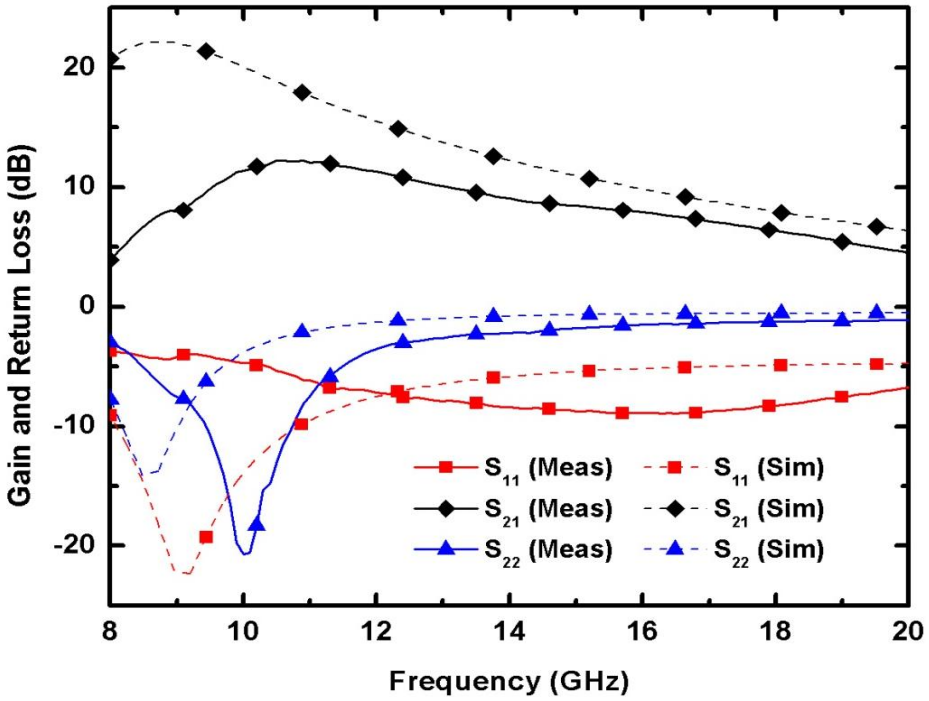


Figure 3.12: Measured versus simulated S-parameters for the X-band SiGe PA.

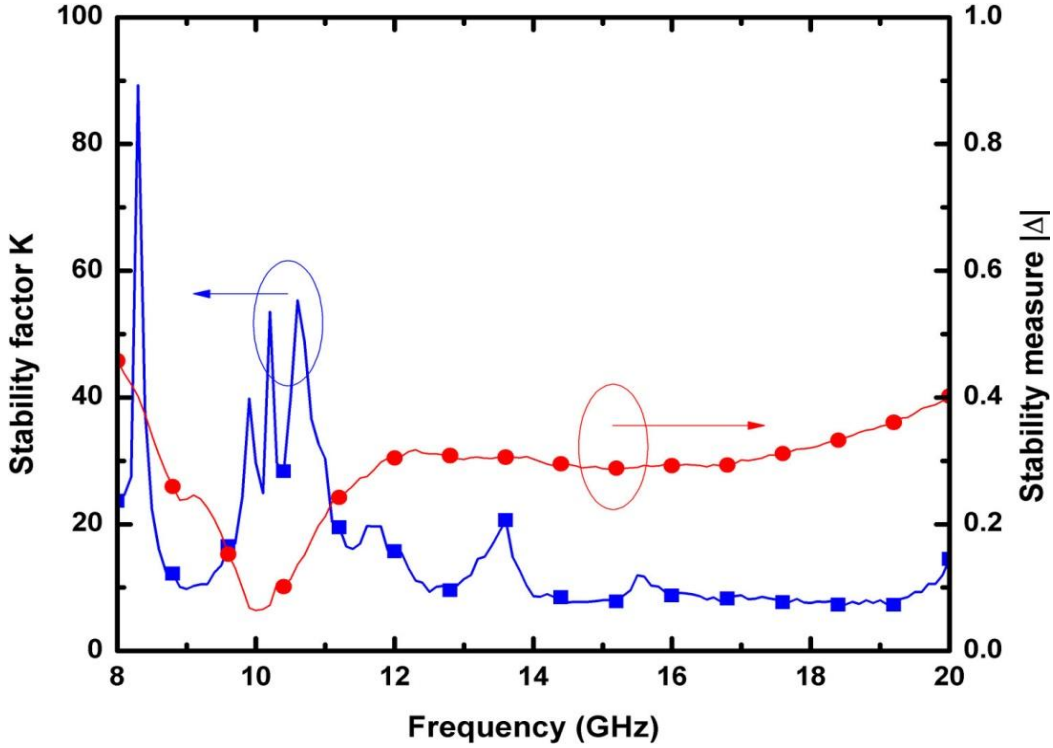


Figure 3.13: Measured stability parameters of the SiGe PA showing unconditional stability.

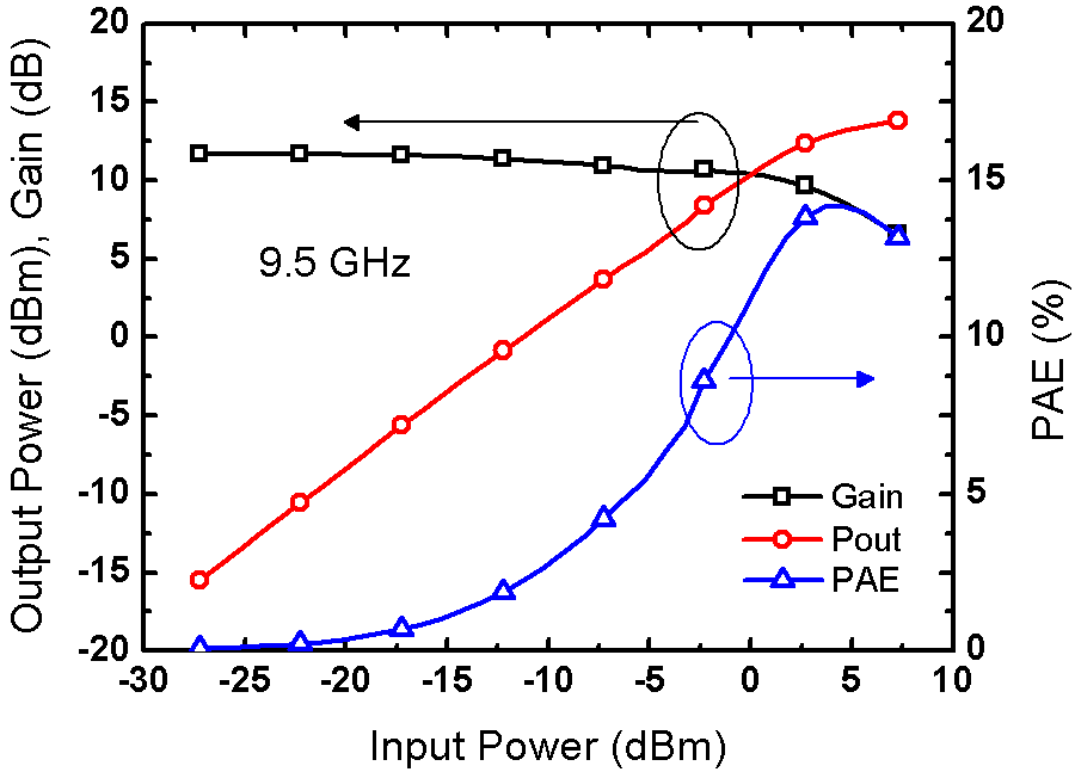


Figure 3.14: Measured large-signal performance of the PA.

Load-pull and source-pull measurements were performed on the PA to determine if a higher output power could be attained by shifting the external impedances away from 50 Ω. Measured load-pull contours are shown in Figure 3.15. The maximum power contour does encircle 50 Ω, and although this contour is large and is not centered at 50 Ω, only a slightly increased output power could be attained by changing the load impedance presented to the PA. Source-pull contours are shown in Figure 3.16. Output power and gain could be slightly increased by shifting the source impedance, but 50 Ω is inside the highest power contour so little improvement could be attained. The performance degradation therefore occurs inside the PA structure and cannot be significantly improved off-die.

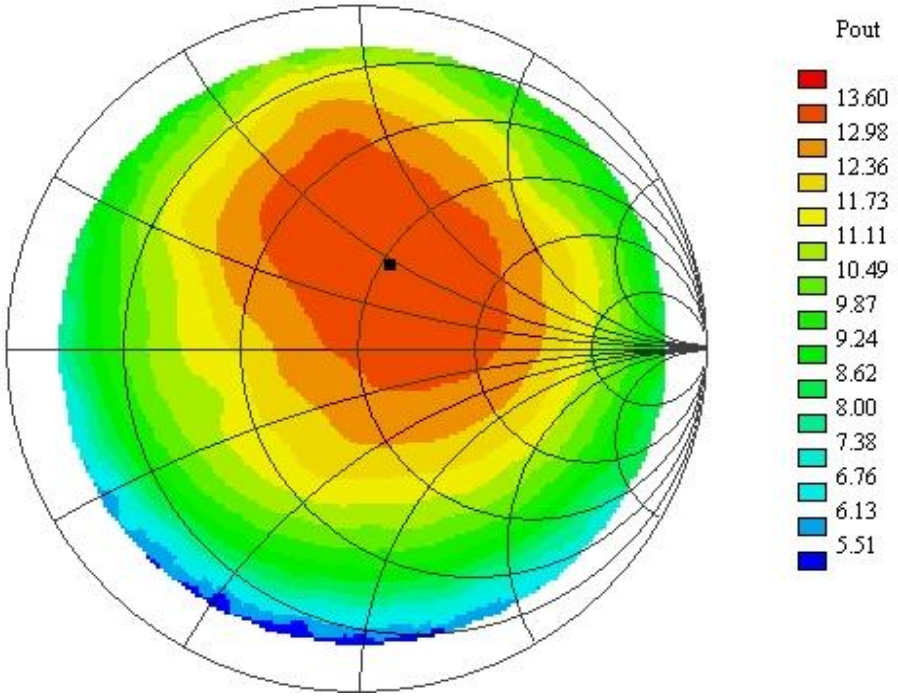


Figure 3.15: Load-pull contours of the X-band SiGe PA.

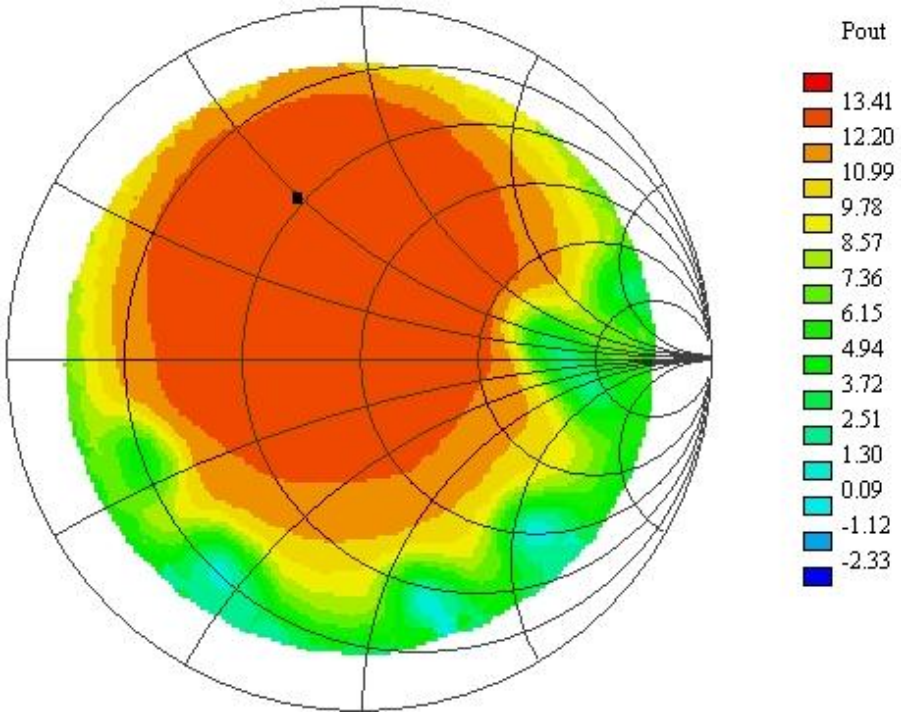


Figure 3.16: Source-pull contours of the X-band SiGe PA.

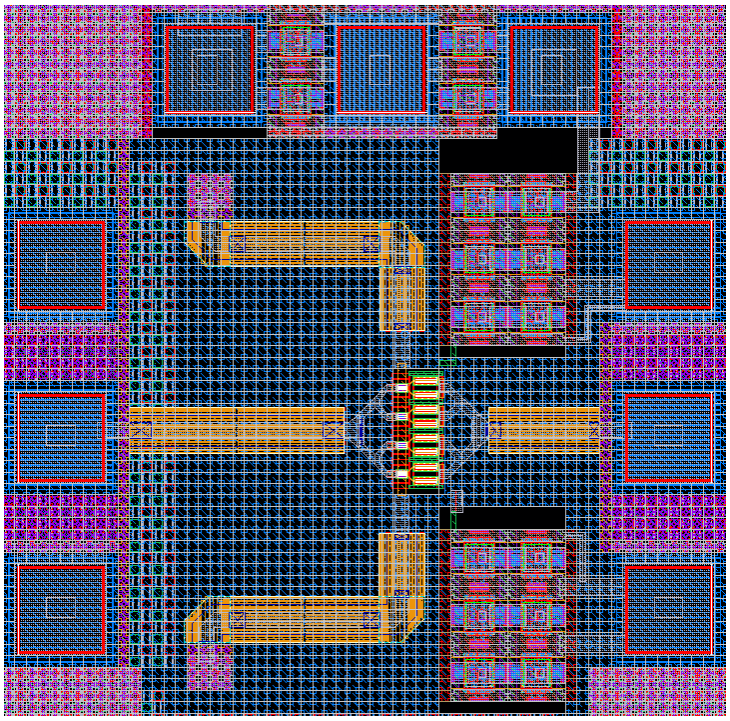


Figure 3.17: Layout image of the PA core with emitter inductor test structure.

3.4 Measurement to Simulation Correlation

The final step in the PA design process was to determine the source of the large discrepancies between the simulated results and the measured data. Test structures of the PA core were included on the test tile with the full amplifier, so these structures were measured to determine if either the transistor core or the emitter inductor caused the shifted performance. A layout capture of the PA core with emitter inductor test structure is shown in Figure 3.17. Figure 3.18 shows the measured and de-embedded S-parameters of this PA core biased at the nominal operating point of the full PA. The simulated data closely matches the measured results. The small noticeable differences were probably caused by layout parasitics or by the use of non-ideal de-embedding structures. Load-pull measurements were then performed on the PA core to verify its large signal performance. Figure 3.19 shows that the output power and gain of the core are very close to those of the simulated PA, so clearly the design kit models were valid. However, the

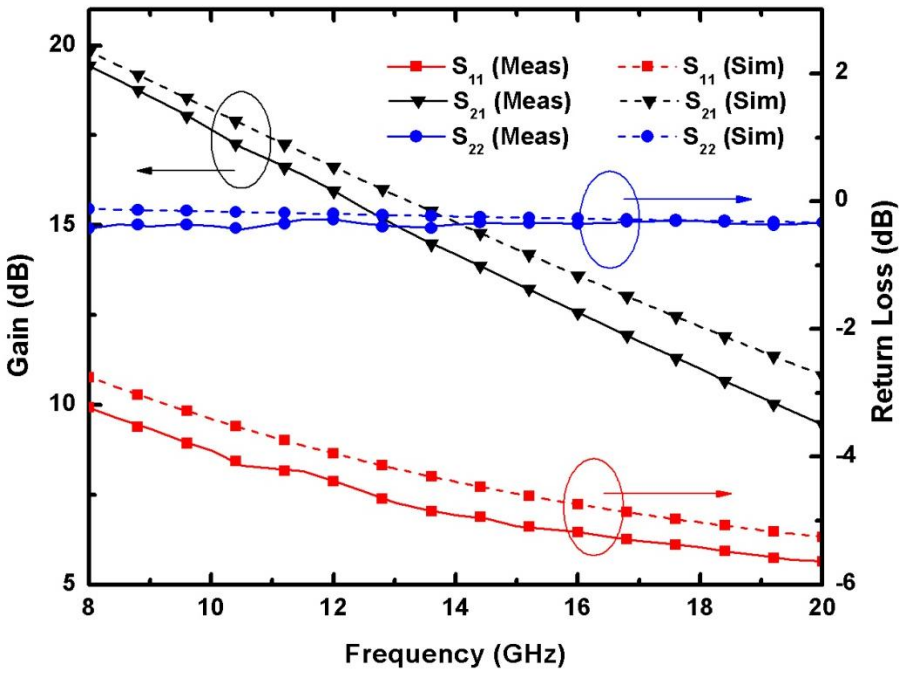


Figure 3.18: Measured and de-embedded S-parameters of the PA core with emitter inductor test structure biased at the nominal operating point.

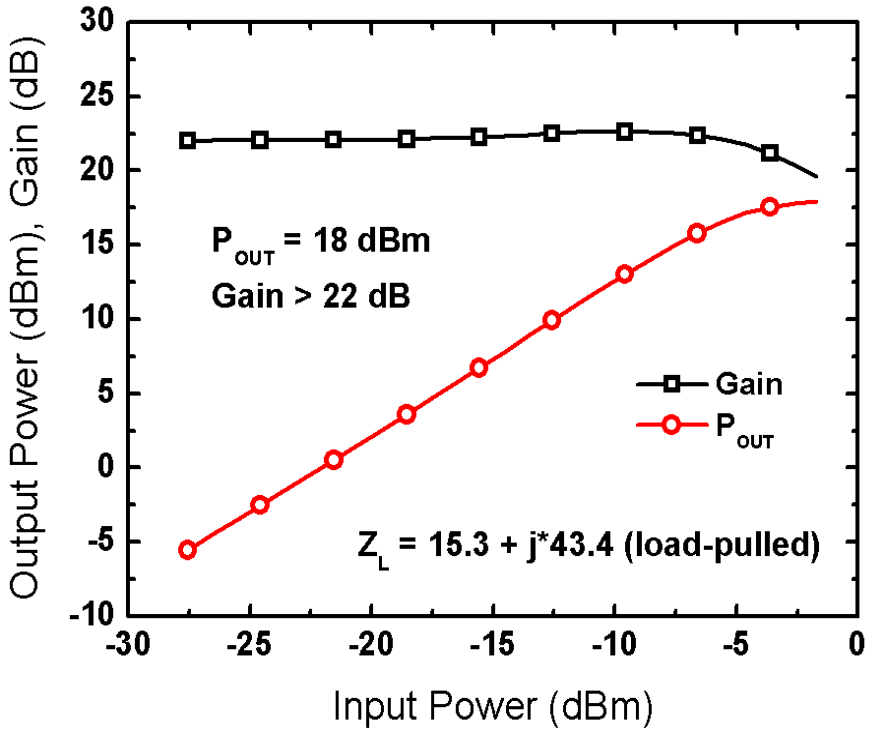


Figure 3.19: Measured large-signal gain and output power of the PA core test structure biased at the nominal operating point and tuned to the optimal power load impedance.

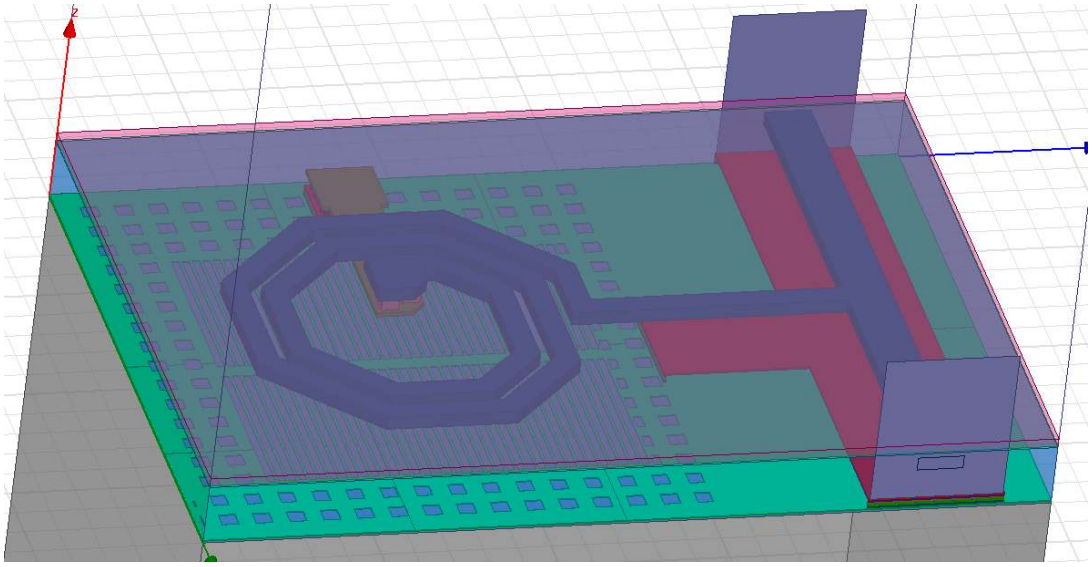


Figure 3.20: HFSS model of the input matching inductor in the SiGe PA.

load-pulled impedance of 15.3 + j*43.4 Ω is significantly different from the simulated impedance of 61 + *j*72 Ω. This impedance difference would definitely reduce the output power of the amplifier, but it would probably not cause the drastic gain reduction observed in the full PA measurements. Some other mechanism is therefore responsible for the large shift in the input matching of the PA.

The other suspected cause of the shift was the inductor layouts. Inductors are quite sensitive to improper layout techniques and are notoriously difficult to accurately simulate. Because the input side of the PA showed the largest shift, the subsequent analysis focuses on the input inductor. The input inductor was modeled in Ansoft HFSS, a powerful 3-D electromagnetic simulator. An image of the modeled inductor is shown in Figure 3.20. The S-parameters of this inductor were simulated and extracted from the following equations:

$$L = \frac{Im\{Z_{11}\}}{\omega} \tag{3.1}$$

$$Q = \frac{Im\{Z_{11}\}}{Re\{Z_{11}\}} \tag{3.2}$$

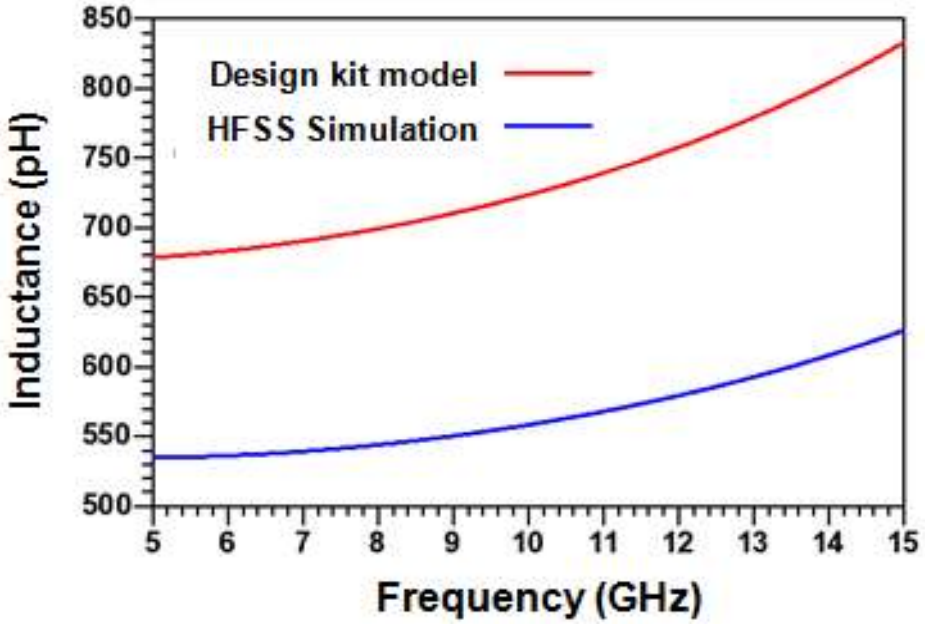


Figure 3.21: Comparison between the EM-simulated and design kit-modeled inductance of the input-side inductor in the SiGe PA.

HFSS and design kit model inductance and quality factor simulations for this inductor are shown in Figures 3.20 and 3.21, respectively. The HFSS-simulated inductance and quality factor are reduced from the model values. This is because the M1 ground shield is shorted by the surrounding metal fill, forming a closed loop. The ground shield is meant to suppress eddy currents and reduce substrate losses. The closed loop allows eddy currents to flow and reduces the inductance, Q, and self-resonant frequency.

In an attempt to solve this mystery, various refined S-parameter simulations of the full PA are plotted in Figures 3.23 and 3.24. In addition to nominal design kit simulations and measured data, the refined simulations include a design kit simulation with extracted layout parasitics, a simulation with extracted layout parasitics and EM-simulated inductor data, and a simulation using extracted parasitics, EM-simulated inductors, and measured transistor core S-parameter data. Despite all these refinements, this shifted performance still is not accounted for. The large performance discrepancy between the refined simulations and the measured data implies that there are additional un-simulated effects that caused the shifted performance.

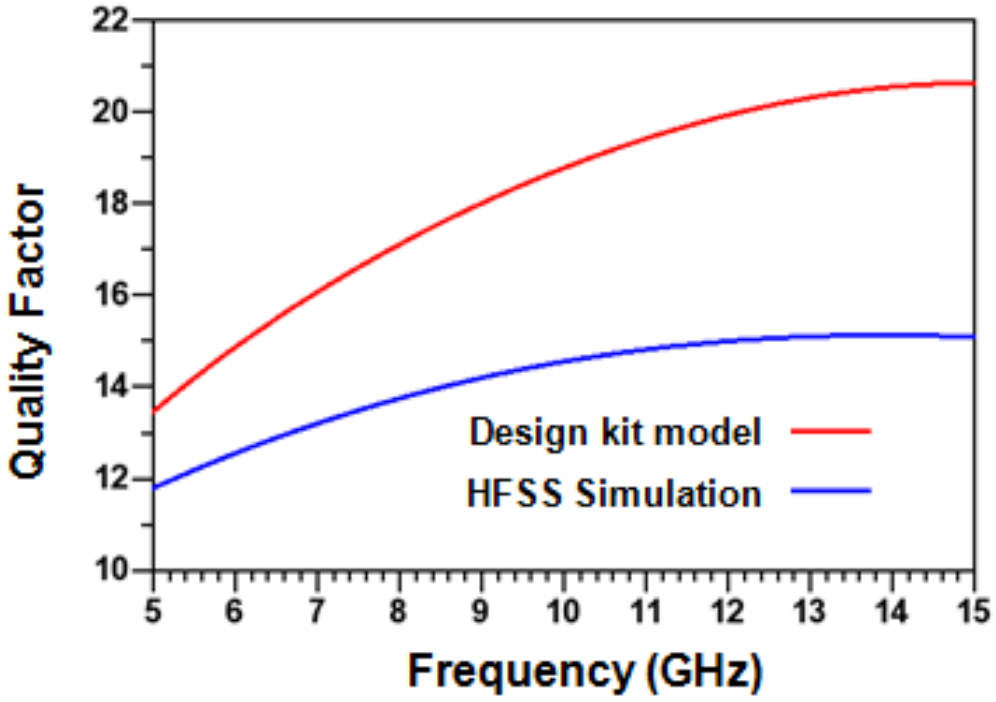


Figure 3.22: Comparison between the EM-simulated and design kit-modeled quality factor of the input-side inductor in the SiGe PA.

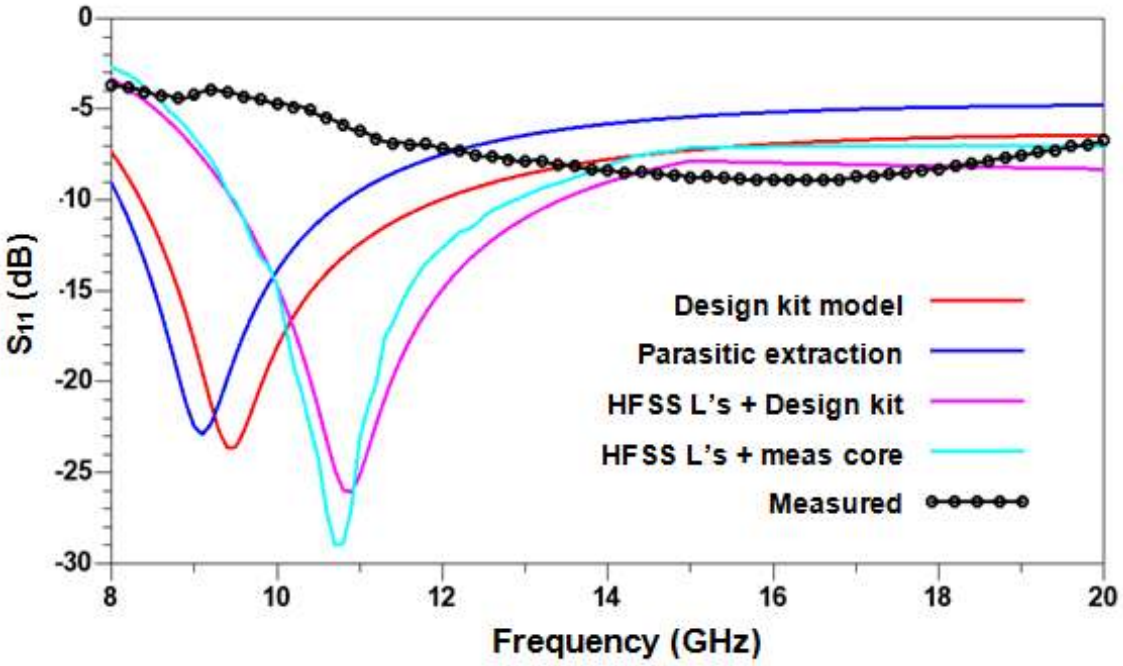


Figure 3.23: Comparison of various refined S_{11} simulations of the SiGe PA, showing that the matching shift still is not modeled.

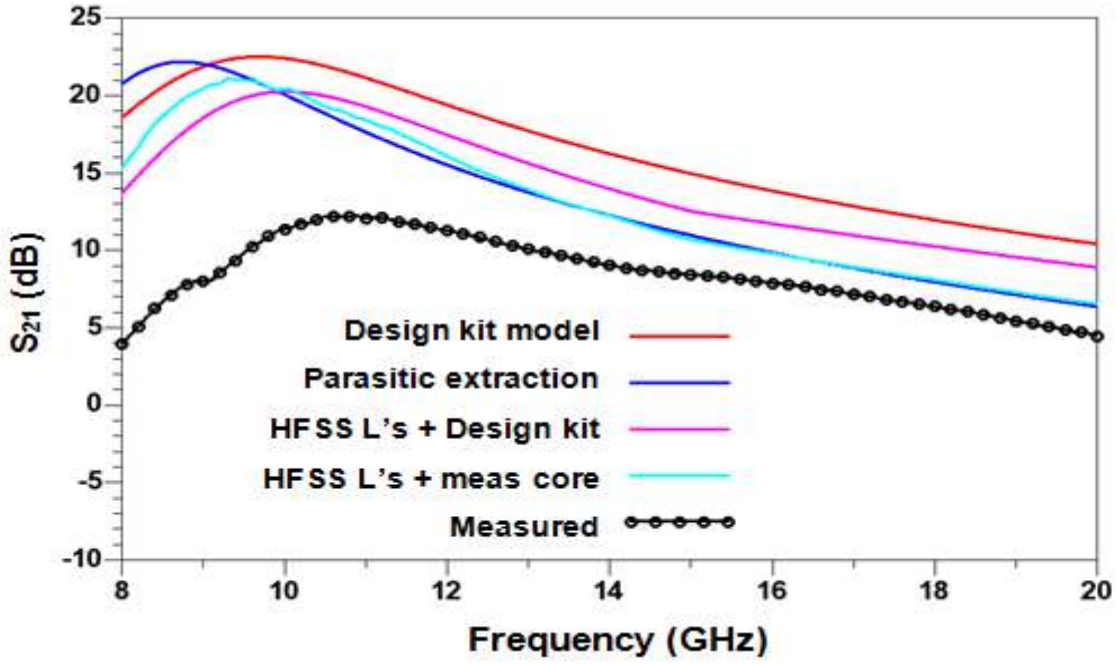


Figure 3.24: Comparison of various refined S_{21} simulations of the SiGe PA, showing that the matching shift still is not modeled.

It is believed that the large shift in the input match was caused by the substrate contacts surrounding the inductor. A layout image of the input inductor is shown in Figure 3.25. The blue layer is the lowest metal layer and the substrate contacts are in the center of each green square (active). The IBM 8HP design manual states that substrate contacts should not be placed within 50 μm of inductors. The inductor in Figure 3.25 is surrounded by substrate contacts, some of which are only 15 μm away from the inductor spirals. An inductor's quality factor can either be improved or degraded when surrounded with substrate contacts, depending on how the contacts are connected and on the inductor configuration (one-port or two-port) [43]. In addition, the self-resonant frequency is decreased as substrate contacts are placed increasingly close to an inductor [44].

After much investigation, it is believed that the 1-port configuration of the input inductor is what caused the drastic shift in the input match. We further believe that the output match was not majorly shifted because that inductor was implemented in a two-

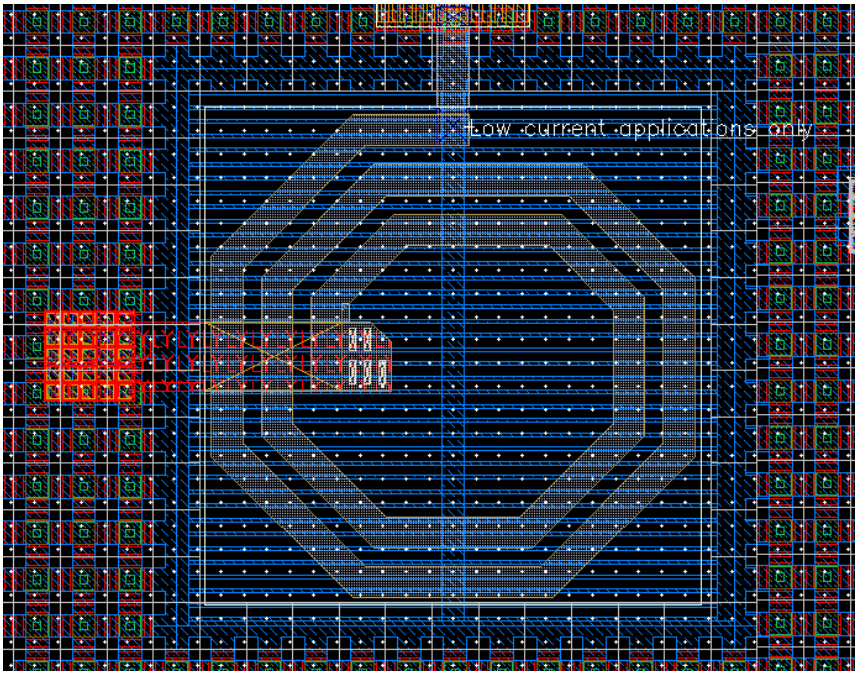


Figure 3.25: Layout capture of the input-side inductor showing surrounding M1 fill and substrate contacts.

port configuration which is inherently less sensitive to the proximity of substrate contacts [43]. Unfortunately, we knew of no way to accurately incorporate the effects of substrate contacts into inductor EM simulations. Based on measured results from other circuits on the same die as this PA, it can be confidently stated that the inductor layouts were to blame for the degraded performance of this PA. In order to avoid this issue in future circuit designs, inductors should be laid out like the example inductor in Figure 3.26.

3.5 Summary

In this chapter we discussed the design and characterization of a medium-power Class AB SiGe PA for an X-band T/R module. The PA design process was explained in detail, focusing on the design of the transistor core, bias selection and self-bias network design, impedance matching, and layout consideration. Simulations indicated that the PA should have over 23 dB of gain, over 30% PAE, and 15 dBm of output power at 9.5 GHz. The fabricated PA, however, had only 12 dB of gain, 14 dBm of output power, and 14%

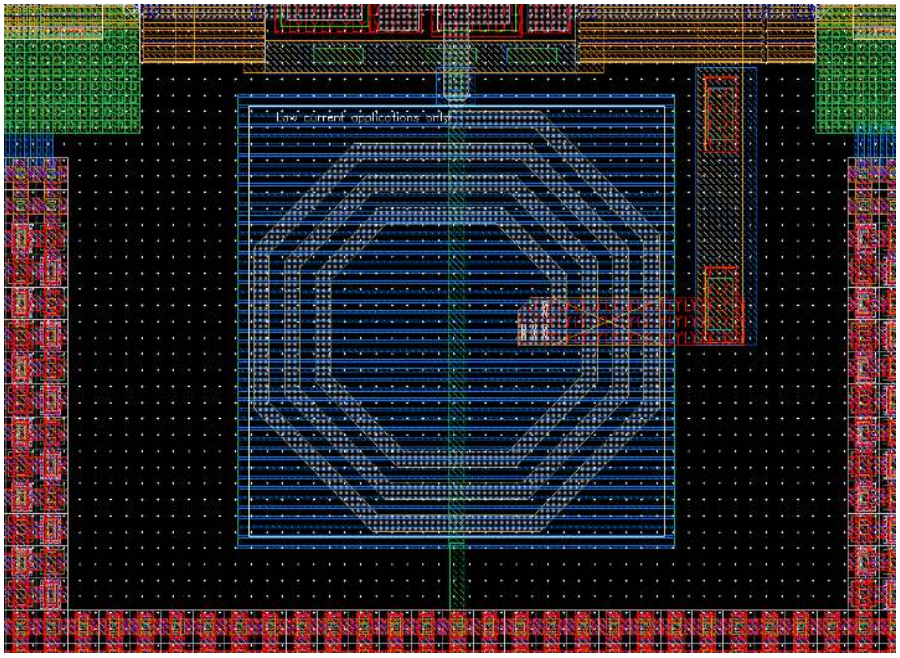


Figure 3.26: Image of a properly laid out inductor that is not closely surrounded by metal fill and/or substrate contacts.

PAE at the fundamental frequency. Fortunately the PA was robust and stable as intended, making it acceptable for integration into the T/R module for the target antenna panel. The measurement to simulation correlation of the PA was investigated and we deduced that the inductor layouts are to blame for the shifted performance.

Chapter 4 will discuss the development and characterization of the X-band SiGe T/R module that this PA was developed for. The integration of these T/R modules into a lightweight, highly integrated AESA antenna will also be discussed.

CHAPTER IV

DEVELOPMENT OF AN ACTIVE PHASED-ARRAY ANTENNA USING INTEGRATED SIGE T/R MODULES

4.1 Introduction

This chapter discusses the development of a very thin, lightweight active phased array using highly integrated SiGe T/R modules. The system-on-package (SoP) antenna combines the high performance and integration potential of SiGe BiCMOS technologies with advanced substrates and packaging techniques to develop a high performance scalable antenna panel using relatively low-cost materials. Multiple panels can be scaled together at the array level to implement a high efficiency, relatively low price antenna [20]. The antenna panel presented in this chapter will enable airborne SCLP measurements and advance the technology towards an eventual space-based SCLP measurement instrument that will satisfy a critical Earth science need.

Section 4.2 will discuss the design of the full array and the sub-array panels, focusing on how these set the requirements for the SiGe chips. The design and characterization of the SiGe T/R module will be presented in Sections 4.3 and 4.4, respectively. Packaging considerations for the flip-chipped T/R modules are outlined in Section 4.5. Finally, Section 4.6 will discuss the integration and characterization of the completed sub-array. My responsibilities in this project consisted of designing the PA block for the T/R module (discussed in Chapter 3), assisting in the integration of the T/R module, fully characterizing the T/R module, and assisting in the characterization of the final array.

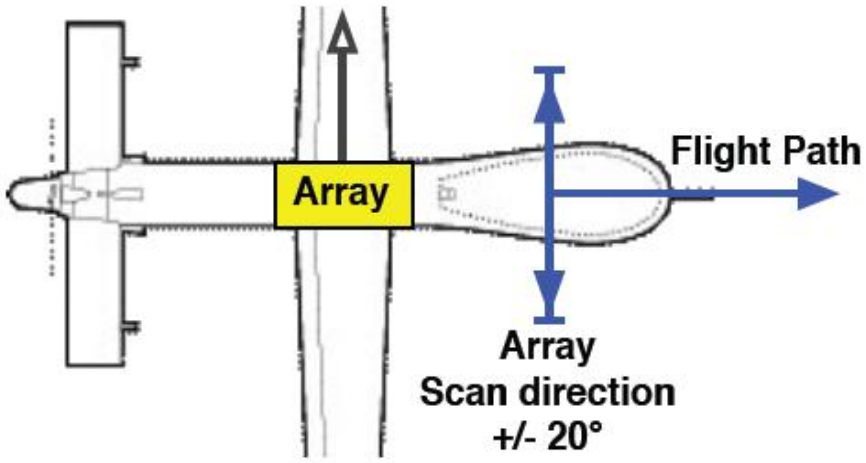


Figure 4.1: Cartoon of the desired aircraft-mounted panel array showing scanning configuration [45].

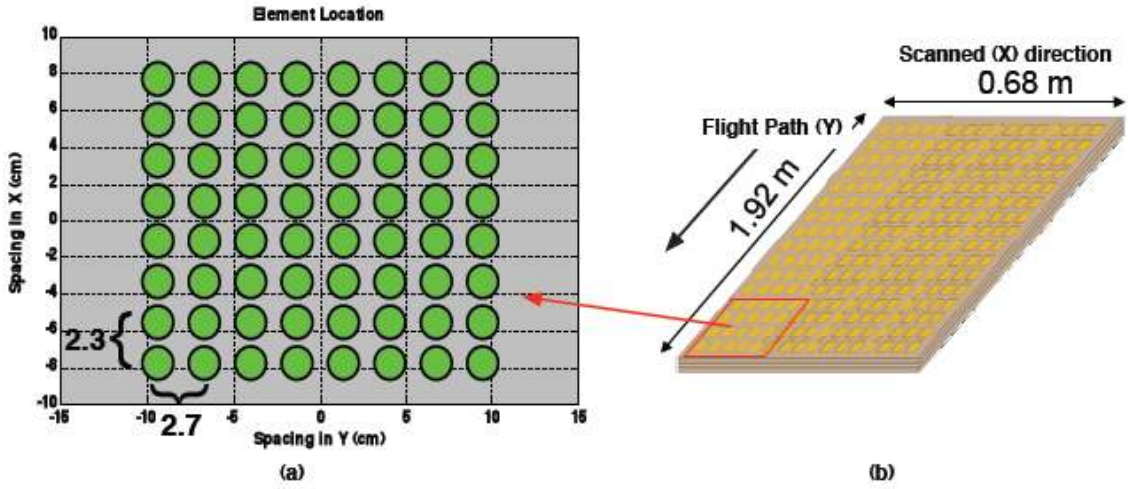
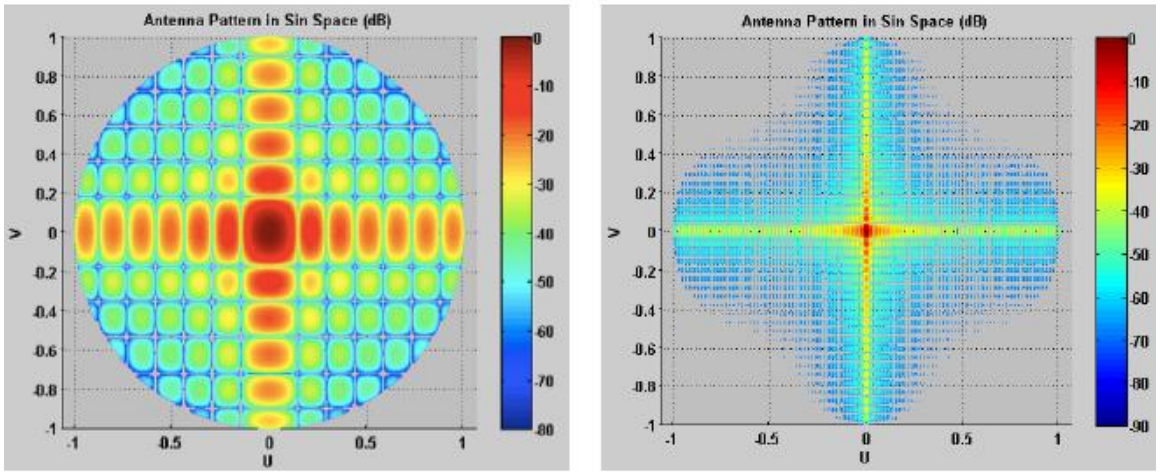


Figure 4.2: Illustration showing the dimensions of the 8x8 sub-array and the full array (from [45]).

4.2 Array Requirements and Design

The design of the full array was driven by the SCLP measurement requirements. This array design in turn set the requirements of the sub-array panel and the SiGe T/R modules. The array design is presented in detail in [45], although the main elements will be discussed presently to provide context. The full array was designed to be mounted on an aircraft or UAV flown at an altitude of 8 km, as shown in the illustration in Figure 4.1.



(a) (b)

Figure 4.3: Simulated antenna patterns of (a) the 8x8 sub-array and (b) the full array (from [45]).

The beam was set to be scanned ± 20° in the horizontal direction to set a swath width of 6 km. The spacing of the array elements was chosen to avoid undesired grating lobes over the steering range. In order to achieve sufficient directivity, antenna gain, and spatial resolution, the beamwidth of the array was chosen to be 2.2° in the x-direction and 0.8° in the y-direction. The beamwidth and the element spacing specifications were used to determine the final array size of 0.68 m in the x-direction and 1.92 m in the y-direction. The required number of radiating elements was chosen to be 2,304. Implementing such a large array as a single panel would require challenging and expensive fabrication, so the use of smaller sub-arrays greatly simplified the implementation. The size of each sub-array was chosen to be 8 x 8 elements, as illustrated in Figure 4.2. The final array would therefore contain 36 sub-array panels. A MATLAB simulation of the antenna patterns for the sub-array and the full array are shown in Figures 4.3(a) and 4.3(b), respectively. Clearly the simulated beamwidth of the full array is much smaller than that of the sub-array, meaning that it has much higher gain. This large array size and high gain would greatly increase the output power of the array, which would compensate for the main inherent limitation of using SiGe T/R modules.

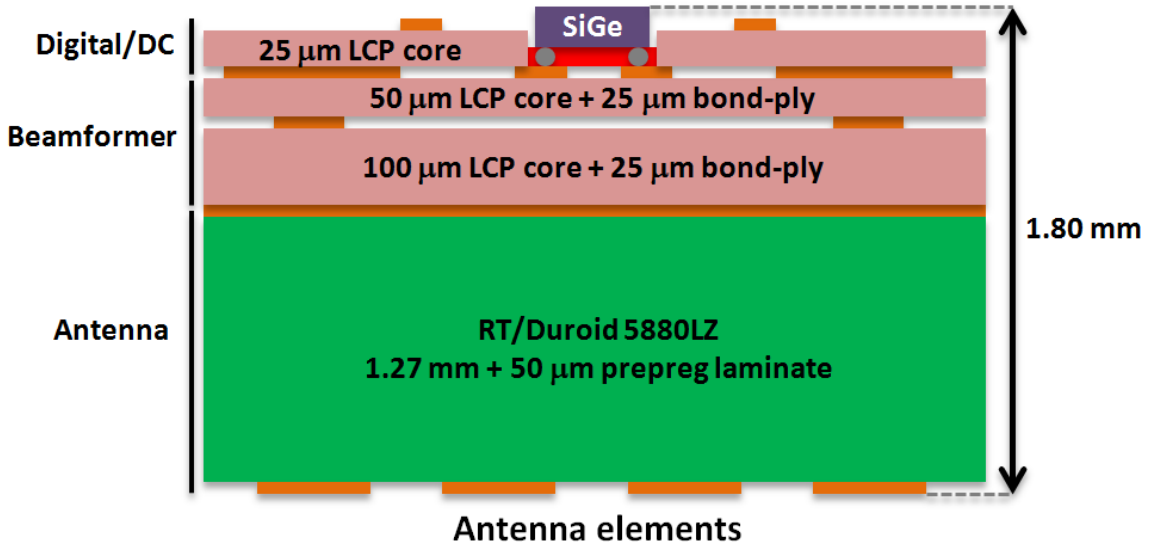


Figure 4.4: Simplified substrate stackup of the final antenna sub-array (not to scale).

. The remainder of this chapter will focus on the design of the 8x8 sub-array. Previous efforts that this array is based off of are described in [46], [47], and [48]. The construction of the final array described here is presented in [49]. Figure 4.4 shows a simplified diagram of the substrate stackup in the final sub-array. The base of the substrate stack is a relatively thick layer of RT/Duroid 5880LZ which provides the requisite bandwidth for the antenna. The patch antennas are electrically isolated from the T/R modules and beamforming network by a solid copper ground plane on the backside of the Duroid. Thin layers of liquid crystal polymer (LCP) compose the dielectric used on the beamforming and digital/DC layers of the stack. LCP is a flexible organic microwave substrate that has low loss, a low dielectric constant, is compatible with traditional PCB processing techniques, and perhaps most importantly, is relatively inexpensive [50]. The beamforming network is constructed from embedded microstrip lines between the T/R modules and the radiating elements and from striplines between the panel input and a stripline-to-CPW transition at the input of each T/R module.

The packaging of the SiGe T/R modules was a major focus of this project. Initial developmental boards packaged the T/R modules simply using conductive epoxy and

traditional wirebonds [47]. In order to reduce losses and to protect the T/R modules, the next revision of the board placed the T/R modules in recessed cavities before wirebonding, which resulted in greatly reduced inductive bond lengths [48]. To further reduce parasitic losses, we explored flip-chip bonding the T/R modules by placing gold studs on the bondpads using a wire ball bonder. A novel packaging technique was developed to embed flip-chipped SiGe T/R modules in LCP to create a planar profile for the antenna exterior and to create a near-hermetic seal to protect the SiGe chips from the external environment [51]. The final revision of the board implemented standard flip-chip packaging for the T/R modules using solder balls. Mechanical stability of these bonds was improved at the expense of slight RF performance degradation by injecting an epoxy underfill under the chips, as shown in Figure 4.4. The embedded packaging could not be implemented for the final array due to issues that will be described in Section 4.6. These packaging efforts resulted in low-parasitic, mechanically stable connections to the T/R module that maximized integration and minimized losses in order to improve the efficiency of the array.

Figure 4.5 is a schematic of the final array. The previous version of this array implemented one T/R module per row of eight elements, whereas this array implemented one T/R module per two elements. Using more T/R modules increases the output power at each element. From a receiver point of view, placing the T/R modules closer to the elements reduces the amount of SNR degradation introduced by the input feed lines. The initial plan was to implement one T/R module for each element in the array, but simulations indicated that the incremental performance improvement from 32 to 64 T/R modules was small and not worth the added packaging complexity that doubling the amount of T/R modules would introduce.

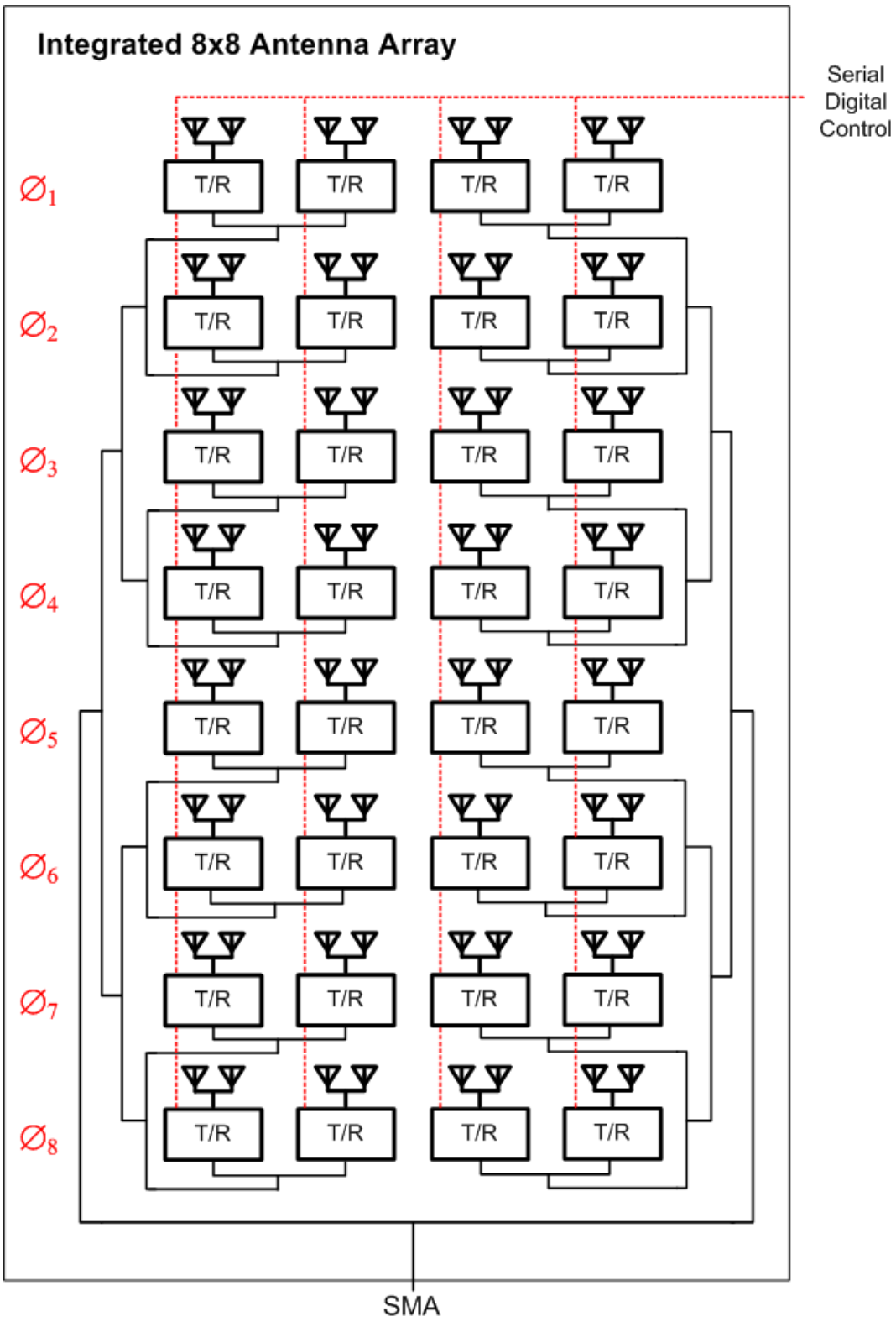


Figure 4.5: Schematic of the final 8x8 sub-array with 32 T/R modules. The operation of the digital control network and the T-junction beamforming network are illustrated.

The power splitters/combiners implemented in the final board were simple T-junctions, as shown in Figure 4.5.

The digital control interconnections are shown in red in Figure 4.5. One of the primary goals of this final board was to minimize the amount of external connections required. To achieve this, the phase state of each T/R module is controlled serially. An external computer-controlled FPGA sends buffered digital signals to the board which are fanned out into four columns of eight T/R modules. Each row of four T/R modules (eight elements) is therefore set to a given phase state in order to steer the beam to the desired angle, as denoted by the symbols $\varnothing_1 \ldots \varnothing_8$. The board could have been implemented with all 32 chips controlled in one serial row, but four identical control columns were implemented to minimize the impact of one or more chips in the serial path failing. Chip-to-chip serial control reduced the interconnect complexity of the board and minimized external wiring complexity, which simplified the board layout and made the board more easily implementable for the target application.

4.3 SiGe T/R Module Development

The SiGe T/R module developed for this final array was based off of previous X-band modules developed by our group. These previous modules were not designed or optimized for integration into an antenna array like the new design presented here [23, 45]. The primary requirements of the T/R module for the final array were full transmit/receive functionality, high-speed duplexing, on-die digital control for the phase shifter, and on-die bias references. Additionally, the T/R module needed to be robust, have little die-to-die variation, and be optimized for flip-chip packaging. The T/R module was designed in IBM's BiCMOS8HP process, the same as the PA in Chapter 3.

Figure 4.6 contains a block diagram of the new T/R module. The PA is exactly the same as the one presented in Chapter 3. The LNA, phase shifter, and T/R switches are described in [45]. The LNA is similar to the inductively-degenerated cascode design

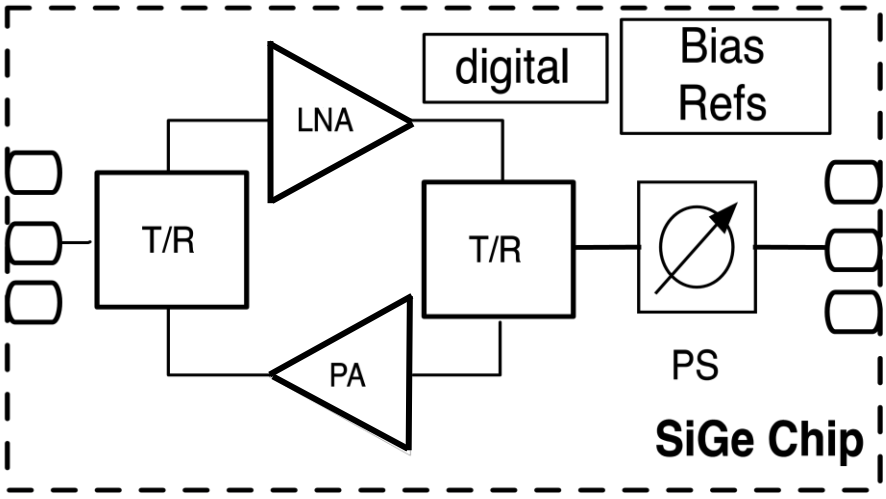


Figure 4.6: Block diagram of the new SiGe T/R module.

presented in [52]. It has over 16 dB of gain, a noise figure (NF) of less than 1.5 dB, and consumes 35 mW of *dc* power. Like the PA, the LNA has an internal bias reference that can be switched off so minimal power is wasted while the antenna is transmitting. The three-bit phase shifter (45°, 90°, and 180°) consists of hi-pass and low-pass filter sections for each phase bit that are controlled by CMOS switches. The entire shifter has approximately 8 dB of loss and draws a negligible amount of power.

The T/R switches were implemented as simple triple-well MOS series-shunt SPDT switches that consume almost no power and have an insertion loss of approximately 3 dB. The shifter-side switch was designed to provide extra isolation between the center pole and the PA input to ensure sufficient isolation while the LNA is potentially receiving high powers. This extra isolation was achieved by using a second series FET. Integrating the antenna-side T/R switch on-die was a major change to this T/R module design. The previous array used a low-loss MEMS switch to minimize receive-side SNR degradation and transmit-side output power losses. However, this low loss came at a price of reduced integration and slow switching time. The CMOS switch in the final T/R module is more lossy and has a lower power-handling capability than the

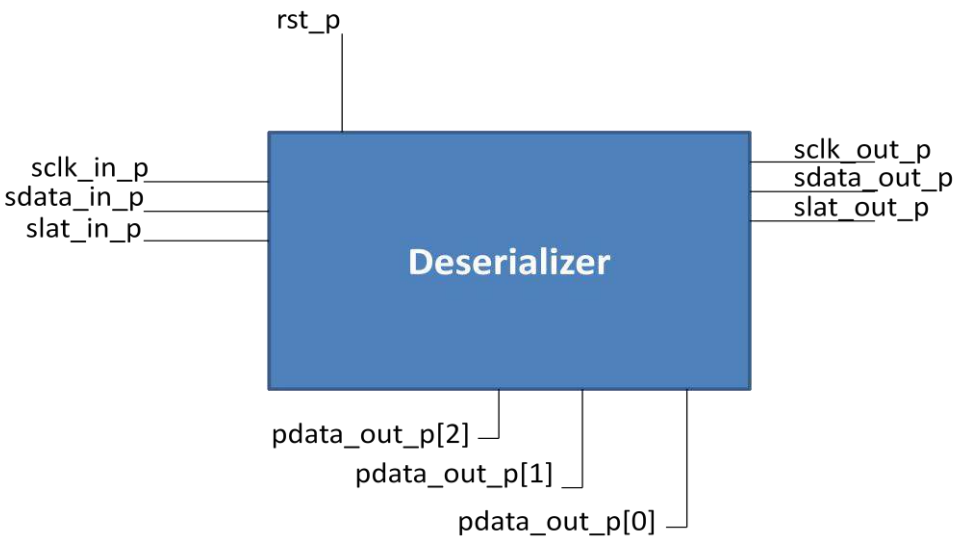


Figure 4.7: Input and output signals of the on-die serial-to-parallel converter/deserializer.

MEMS switch but is fully integrated on-die and switches extremely rapidly. Using this low power switch limits the PA output power to around 15 dBm to ensure sufficient reliability for the output switch. The output T/R switch was designed to ensure sufficient isolation between the PA output and the LNA input. The insertion loss of the FETs in this process is not well modeled, so simulation results predict lower loss for these switches than is typically measured (~0.5 dB more lossy per device in measurement). Therefore, the insertion loss of the output T/R switch is estimated to be 2.5-3 dB.

Figure 4.7 shows the input and output signals of the digital deserializer implemented in the T/R module. The input signals for the deserializer are intended to be generated by a computer-controlled FPGA. Four input signals are required for each deserializer – a serial clock, serial data stream, serial latch, and a global reset. The deserializer acts as a First-In-First-Out (FIFO) buffer which holds three bits at a time. Each clock cycle the earliest bit is kicked out of the buffer to the data output line. The data output is buffered on-die and passed on to the subsequent deserializers in the chain, so the data output is simply a delayed version of the input stream. When the

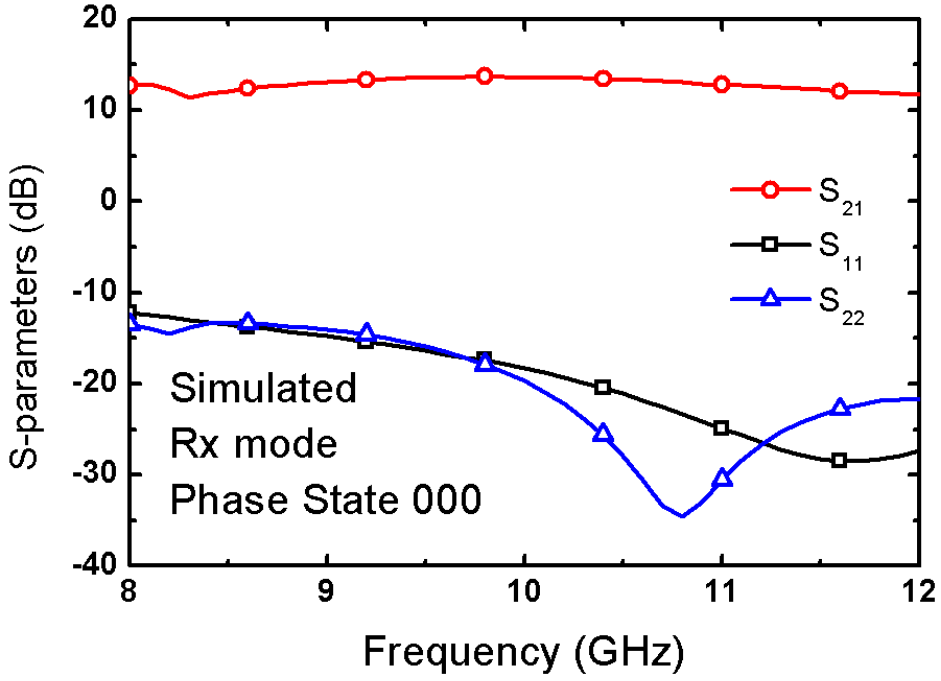


Figure 4.8: Simulated receive path S-parameters of the T/R module.

latch signal is set high, the data in the buffers is latched and the three parallel output signals set the bits of the phase shifter.

The code for the deserializer was written in VHDL and mapped to 8HP digital parts with corresponding Verilog files using Synopsis Design Vision. The layout was synthesized automatically in Cadence and parasitic extraction was performed to take interconnect delays into account. Simulations indicated that the deserializer should work correctly up to clock frequencies of 416 MHz, which is far faster than required by the application.

Simulated receive path S-parameters and NF are shown in Figure 4.8 and 4.9, respectively. The receive path is well-matched across X-band and has over 13 dB of gain and a NF of less than 2.1 dB across the array design bandwidth. Due to the inaccurately modeled FET insertion losses, however, it is presumed that this gain and NF will degrade in measurement. Simulated transmit path S-parameters and swept power results are shown in Figures 4.10 and 4.11, respectively.

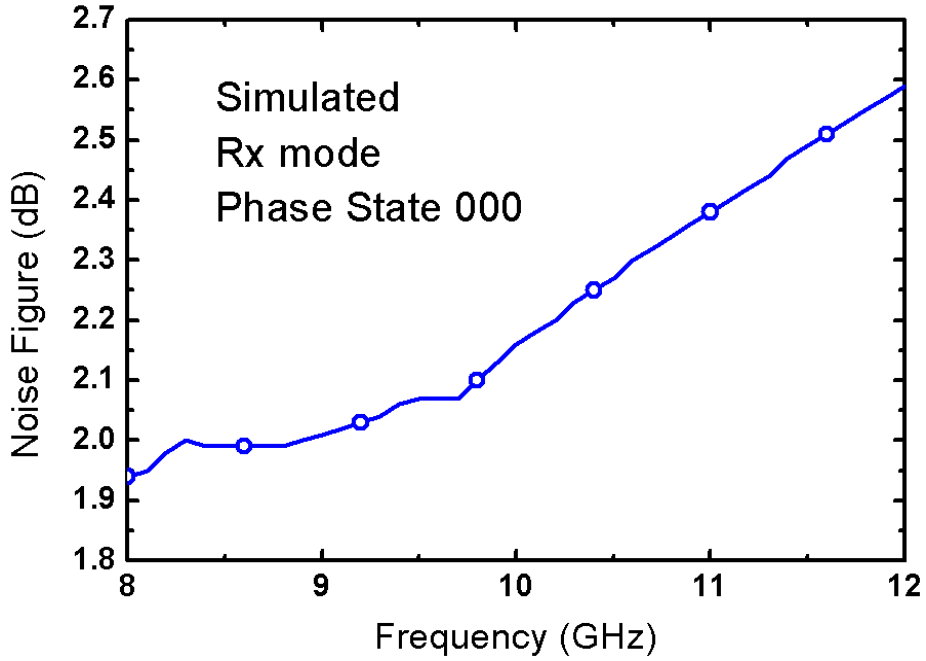


Figure 4.9: Simulated receive path NF of the T/R module. The measured NF will most likely be higher due to poorly modeled insertion loss of FETs in 8HP.

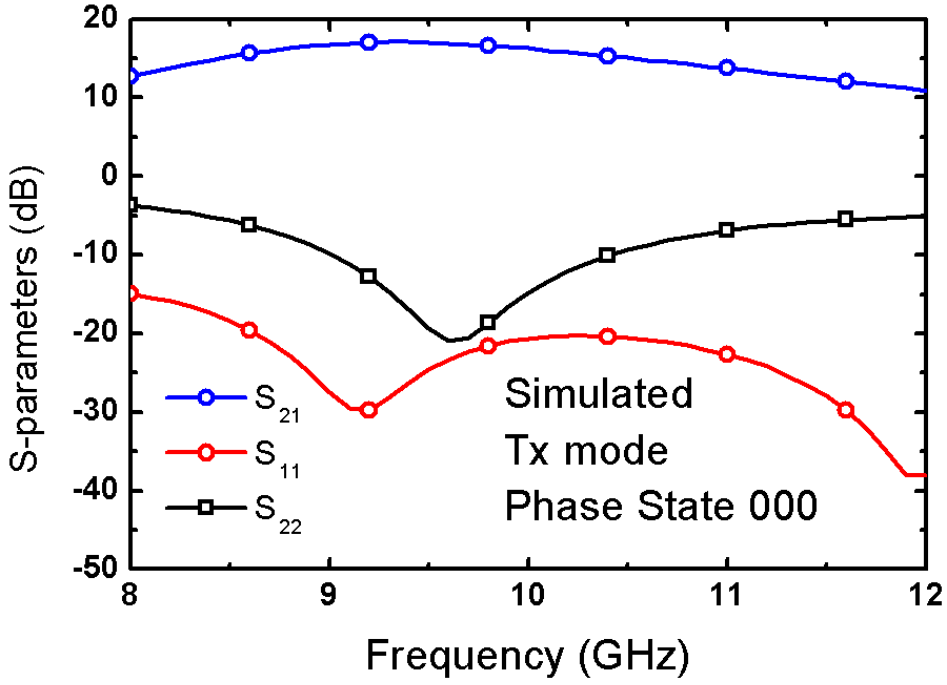


Figure 4.10: Simulated transmit path S-parameters of the T/R module. The measured results will most likely be shifted and degraded due to the inductor layout issues discussed in Chapter 3.

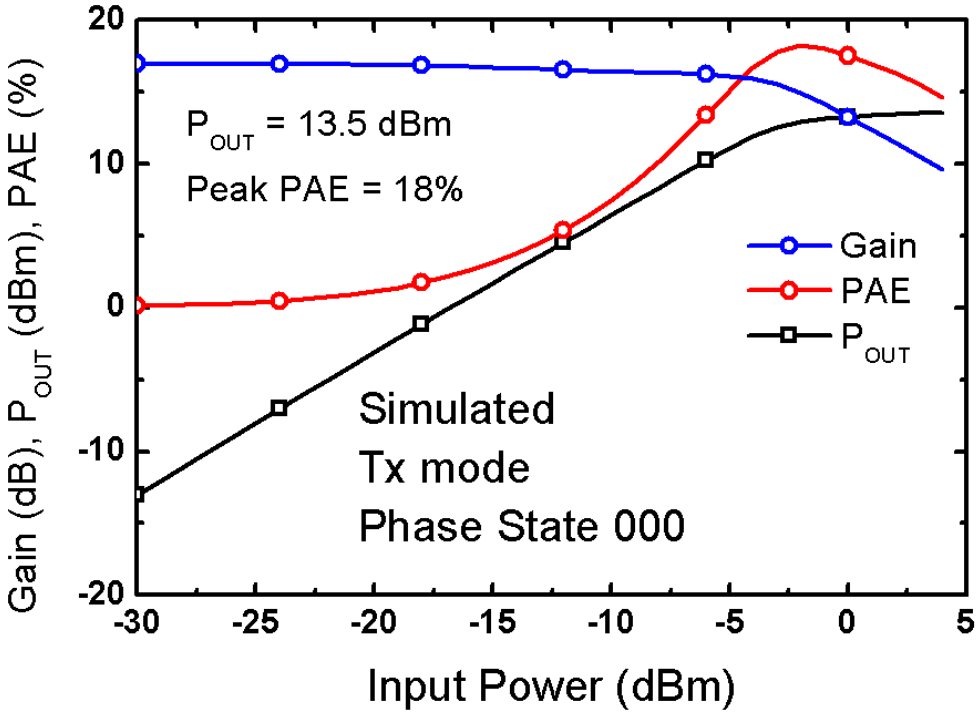


Figure 4.11: Simulated large-signal performance of the T/R module transmit path. All metrics will most likely be degraded in measurement due to the PA performance and the poorly modeled switch devices.

Although the S-parameters appear to be well-matched with a gain over over 16 dB, these results would most likely be degraded in the fabricated T/R module due to the inductor layout issues discussed in Chapter 3. The T/R module output power of 13.5 dBm is 1.5 dB lower than the simulated PA output power. When the measured output power of the PA and the switch device insertion losses are taken into account, it is projected that the output power of the transmit path will be around 11 dBm. The gain and PAE would most likely be significantly reduced in measurement as well.

The final layout of the T/R module chip is shown in Figure 4.12 with padout signals annotated. The size of the die is 2.13 x 3.7 mm^2. In order to facilitate the flip-chip packaging, IBM's C4 (Controlled Collapse Chip Connect) bondpads were used with a "4 on 9" pad pitch with a pad size of 125 μm and minimum pad spacing of 225 μm. The C4 bumps are electroplated 97Pb:3Sn solder balls with a melting temperature of 215 -255 C for organic packages. The RF path inputs and outputs are meant to receive CPW input signals and the

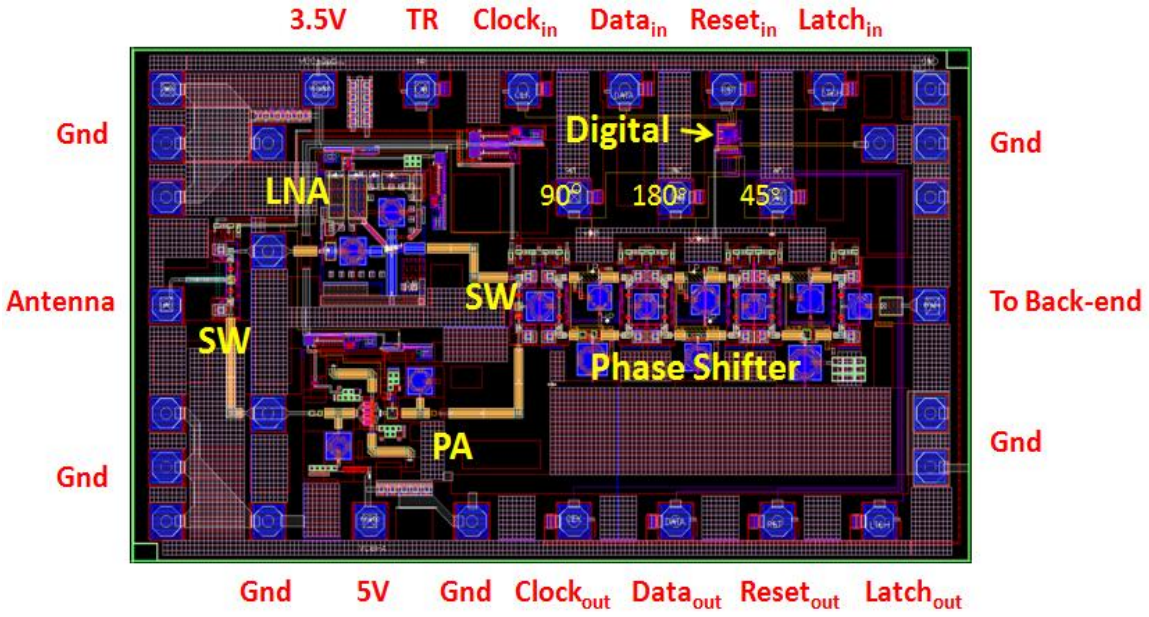


Figure 4.12: Layout image of the full T/R module showing all circuit blocks and padouts.

ground (Gnd) pads for the sides are uneven per the C4 bump process requirements. C4 pads were placed at the input of the LNA and the output of the PA so the output T/R switch could be diced off if required for testing. HFSS simulations indicated that the loss of a series C4 bump is less than 0.1 dB across X-band, so the loss of these extra test pads would not significantly degrade performance. Pads were included for each phase bit so the phase state could be read out during digital testing and manually set for simplified RF testing. Each digital input requires voltage levels of zero or 2.5 V. The T/R module is set to transmit mode (LNA off/PA on) when the TR is low and is set to receive mode (LNA on/PA off) when TR is high. The 3.5 V line supplies powers for the LNA, all switches, and the digital block while the 5 V supply only functions as the rail voltage for the PA. Due to the low number of *dc* and digital inputs for each T/R module along with the serial chip-to-chip protocol, only a single nine pin cable is required to provide *dc* power and digital control to the full array of 32 T/R modules. This is an extremely low number of inputs for 32 sophisticated SiGe chips and truly demonstrates the array's high level of integration.

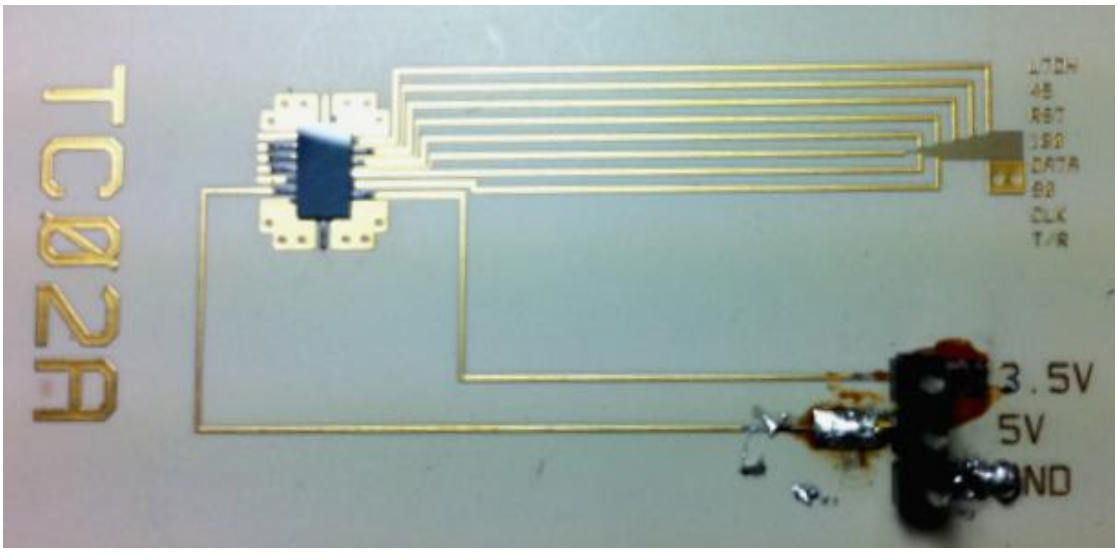


Figure 4.13: Photograph of a SiGe T/R module flip-chip bonded to an LCP/Duroid test coupon.

4.4 Module Packaging

Due to the intended flip-chip packaging configuration, the fabricated T/R modules could not be directly probed on-wafer and needed to be bonded to custom test coupons so they could be characterized. Figure 4.13 shows a photograph of a SiGe T/R module flip-chip bonded to an LCP/Duroid test coupon. Supply voltages and ground were applied through header pin connections and the digital signals and phase states were applied through a nine-pin DC probe. RF probes with a 500 μm pitch were used to probe the gold-plated copper pads on either side of the T/R module. Thru-reflect-line (TRL) calibration structures elsewhere on the board allowed for VNA calibration to the reference planes of the C4 bumps.

A seemingly innocuous mechanical anomaly with the boards became a major, nearly prohibitive packaging challenge. All of the fabricated test coupons were vertically bowed out. When placed on a horizontal surface, the center of the test coupon would be raised a few millimeters in the air while only the corners of each board were resting on the surface. This flexing was caused by differing coefficients of thermal expansion (CTEs) between the LCP and Duroid materials. LCP has a higher CTE than Duroid, so

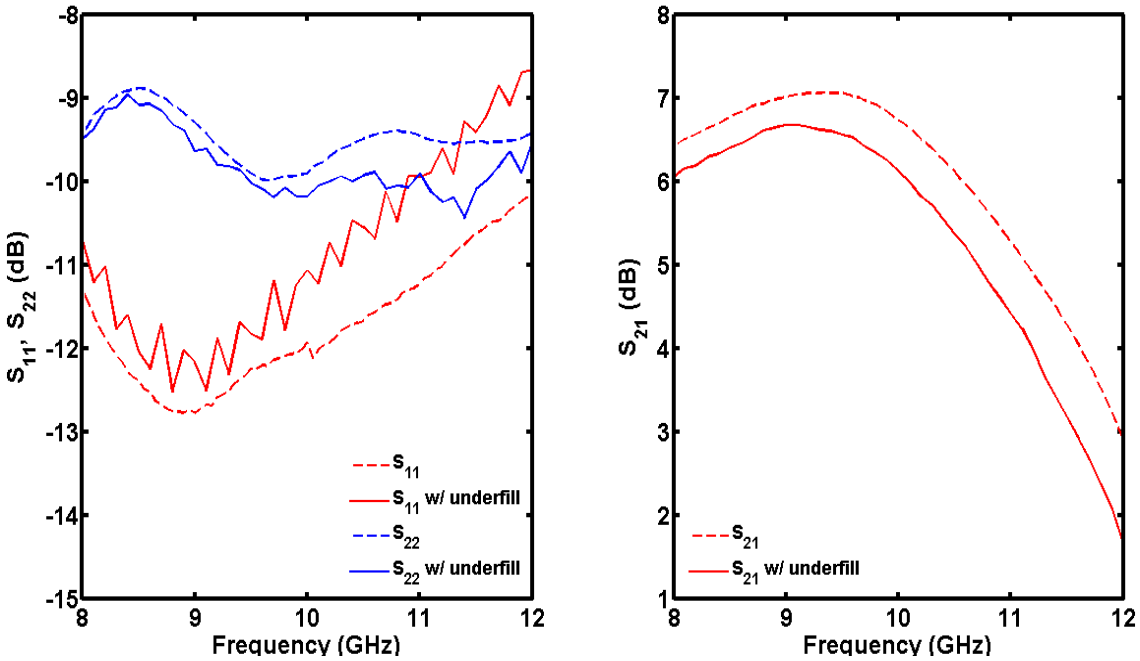


Figure 4.14: Effect of the epoxy underfill on the measured receive path S-parameters.

when heated during lamination the top LCP layers expand laterally and cause the Duroid to bow in. Heating and cooling cycles are essential to the lamination process, so there was no way to completely avoid this effect [49].

In order to characterize the test coupon using wafer probes, a planar surface was required. The flexed board could only be planarized by physically compressing it onto the chuck, either by using vacuum suction and/or tape. This compression placed stress on the flip-chip bonds and caused them to fail often during testing. In order to improve the mechanical strength of the flip-chip bonds, an underfill epoxy was injected under the T/R modules. This made the bonds far more reliable. However, this epoxy has a non-unity dielectric constant. This dielectric is "seen" by the top-metal passives on the T/R module and results in degraded performance. Measured S-parameters with and without epoxy underfill are shown in Figure 4.14 for the receive path and Figure 4.15 for the transmit path. The receive path gain was reduced by around 0.5 dB and the matching is barely affected. The transmit path gain, on the other hand, was reduced by almost 1 dB.

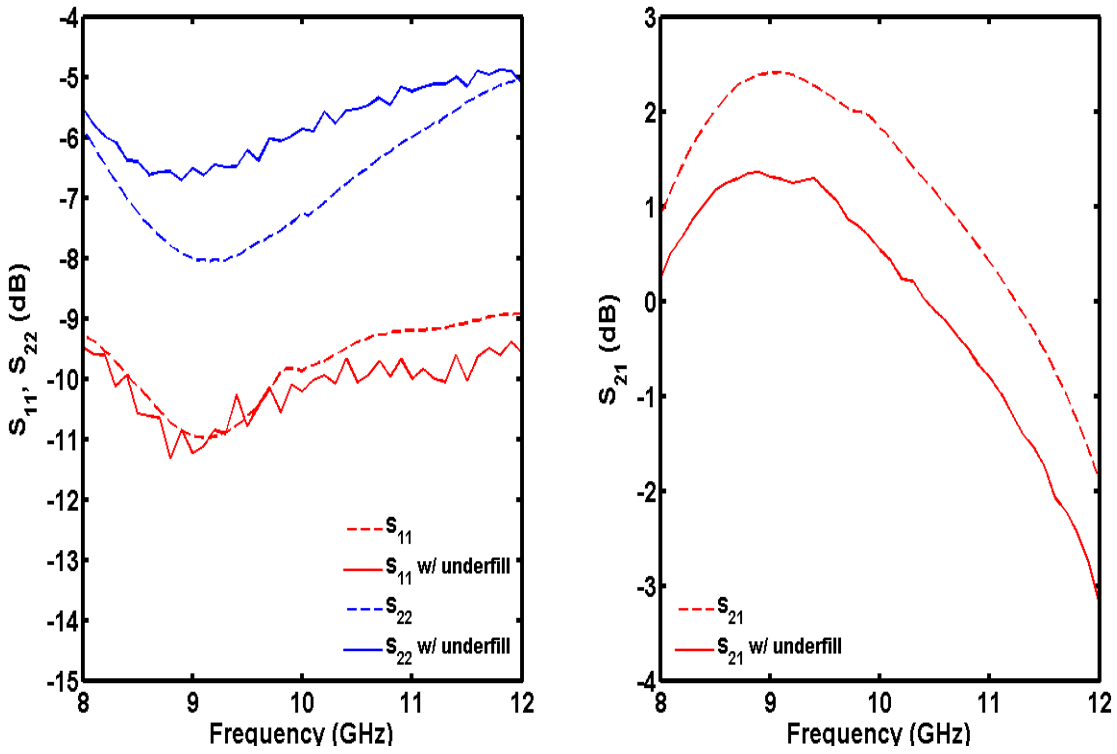


Figure 4.15: Effect of the epoxy underfill on the measured transmit path S-parameters.

The different gain reductions for each path must be caused by interactions between the top-level passives and the epoxy dielectric in the LNA and the PA. The C-L-C input matching network in the PA may be inherently more sensitive to an epoxy underfill because any shift in the inductor performance would be exacerbated by the subsequent impedance shift induced by the second capacitor. The underfill-induced performance degradation must be tolerated to ensure robust packaging, so this additional loss mechanism could not be avoided.

4.5 T/R Module Characterization

4.5.1 RF

An image of the fabricated T/R module with C4 bumps is shown in Figure 4.16. All measured data presented in this section is for a T/R module with epoxy underfill. Figure 4.17 shows the measured receive path gain and phase for each phase state.

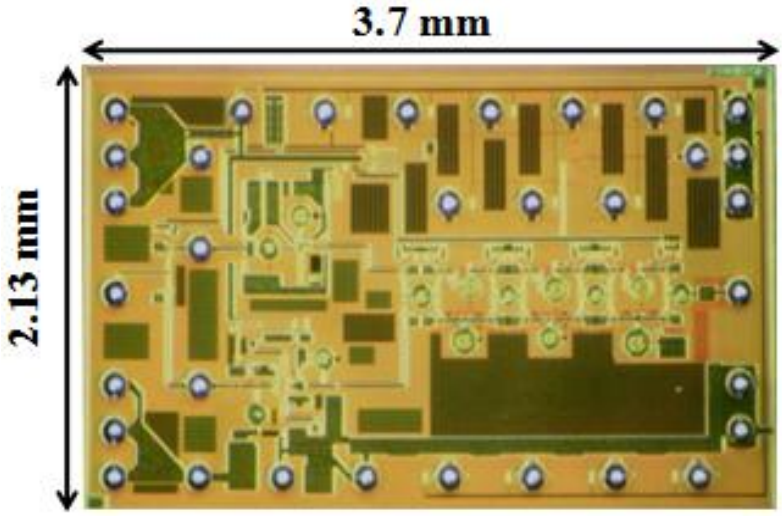


Figure 4.16: Photomicrograph of the fabricated SiGe T/R module.

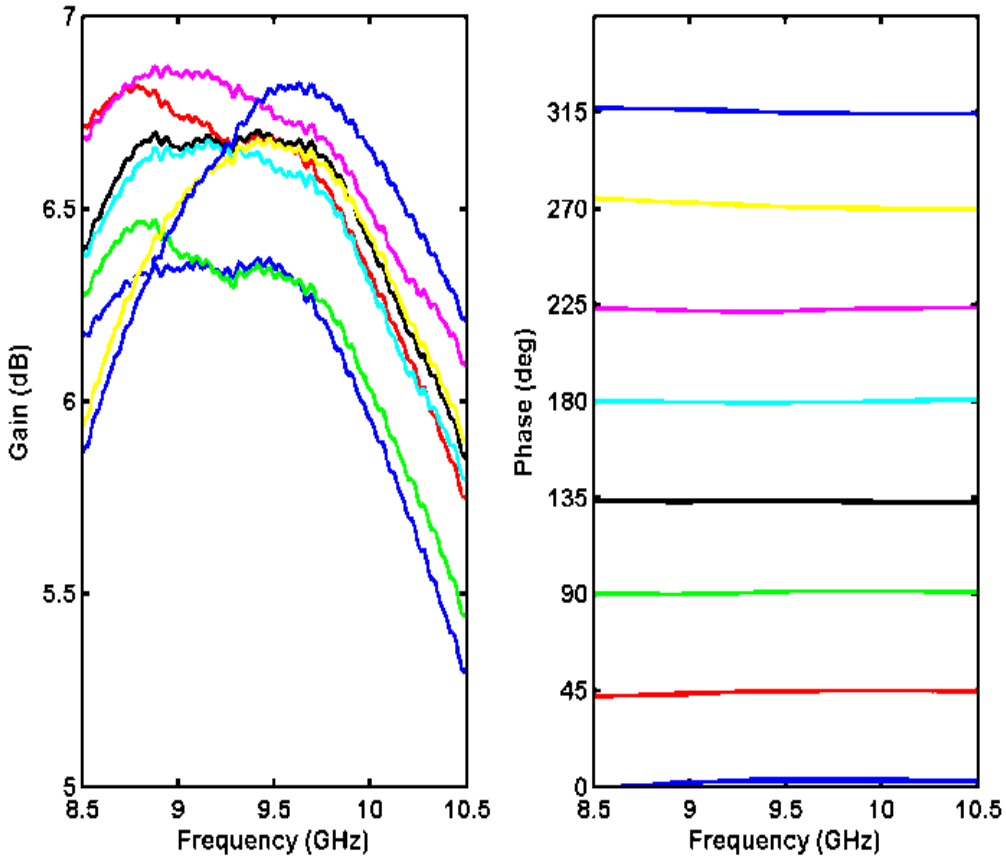


Figure 4.17: Measured receive path gain and phase states of the T/R module.

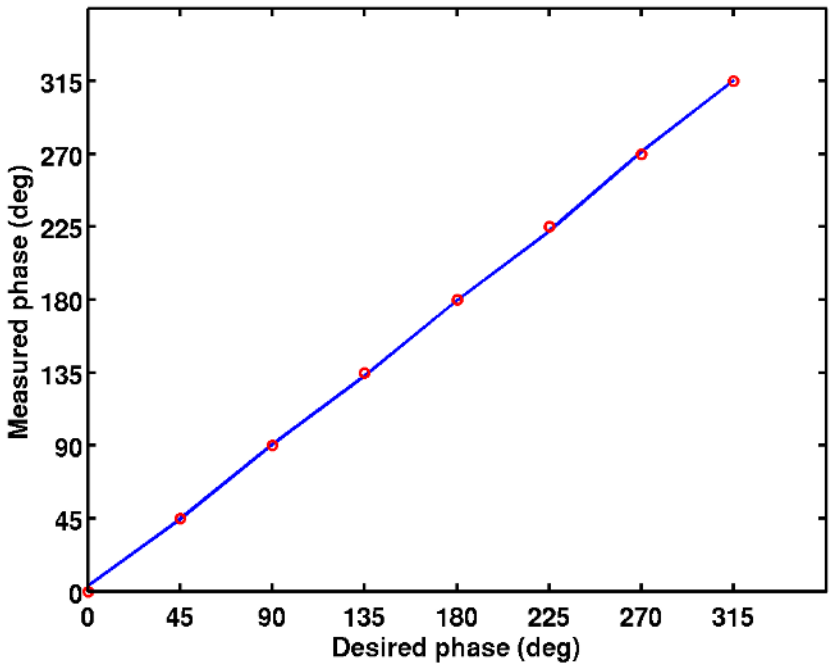


Figure 4.18: Receive path phase state linearity showing excellent phase shifting accuracy.

The total gain variation is approximately 1.5 dB across the design bandwidth and 1 dB across the phase states. The phase varies very slightly across the bandwidth. The gain is centered around 6.5 dB, which is around 7 dB lower than simulated. These un-modeled losses primarily come from the FET switch devices, the epoxy underfill, and other flip-chip packaging parasitics. Figure 4.18 shows that the phase shifter very accurately set the desired phase states. The measured receive path noise figure is shown in Figure 4.19. The average of around 5.6 dB is far higher than the simulated values ofaround 2 dB. This reduction is also most likely caused by the switch devices and packaging parasitics. The transmit path gain and phase states are shown in Figure 4.20. The gain of 1 dB is around 7 dB lower than that of the measured PA test structure and almost 16 dB lower than that of the simulated transmit path. Much of the transmit path gain loss is caused by the PA inductor layouts, and again the packaging and the switches introduce additional loss. The transmit path linearity is shown in Figure 4.21. The output power is reduced to 11 dBm as expected. The PAE was miniscule due to the very low gain and is not plotted.

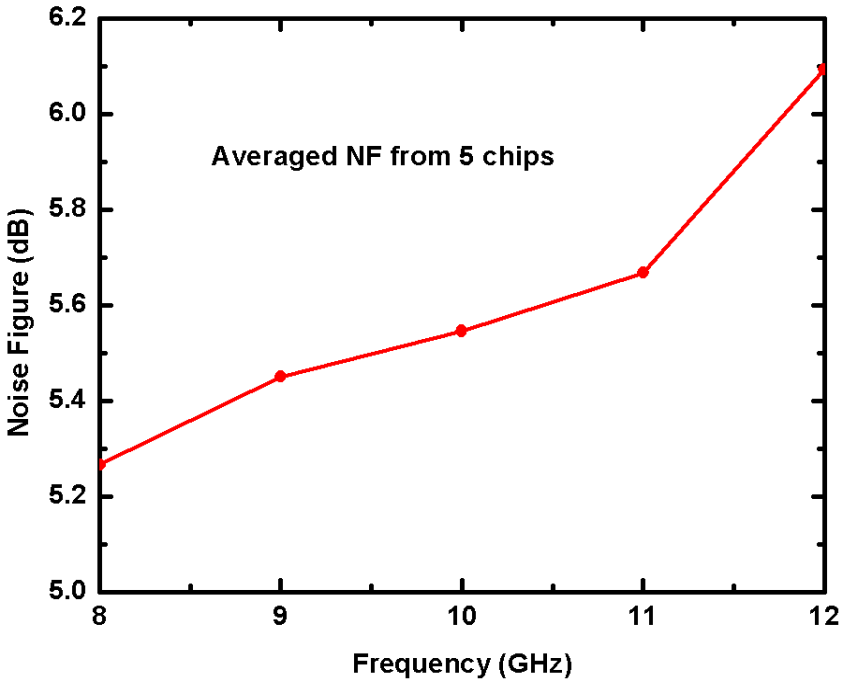


Figure 4.19: Measured receive path noise figure across X-band.

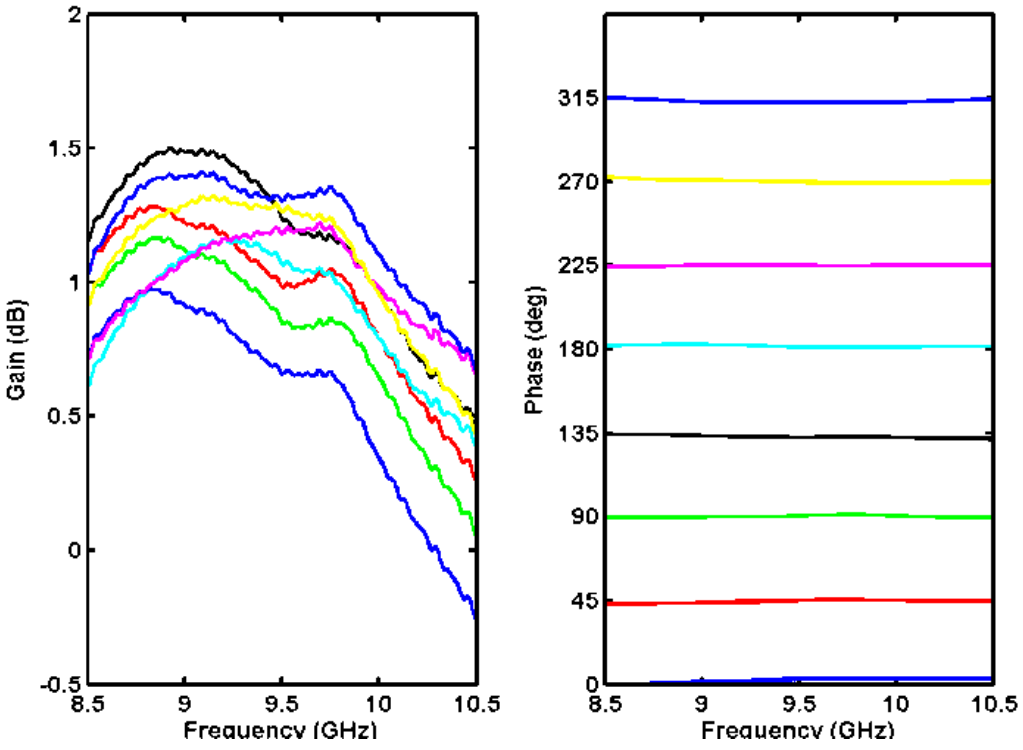


Figure 4.20: Measured transmit path gain and phase across X-band.

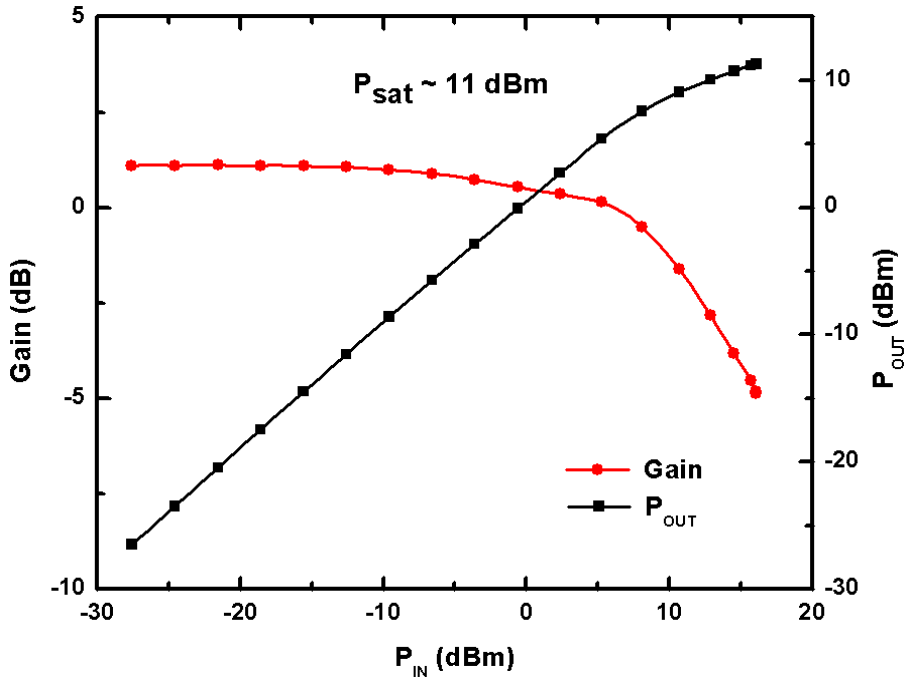


Figure 4.21: Measured large signal performance of transmit path at 9.5 GHz.

4.5.2 Digital

In order to test the serial control, a digital test board for a single row of eight T/R modules was fabricated as shown in Figure 4.22. An external FPGA sent serial data into the first T/R module and the serial outputs were tested by probing directly on the board traces using a multimeter and oscilloscope. The first T/R module in the chain was always set to the correct state. Every other chip in the serial chain, however, would be set to an unpredictable and incorrect phase state. These other chips would only be set to the correct state if the command was to set the phase shifters to an "all 000" (phase of 0 degrees) or an "all 111" (phase of 315 degrees) state.

The main cause of these issues is shown in the scope captures in Figure 4.23. The input data stream from the FPGA changes the data signal on the falling clock edge, which allows the signal to settle before the new data bit is clocked in to the shift register. On the output of the T/R module, however, the data stream changes on the rising clock edge. Figure 4.24 shows that the offset between the clock and data edges on the output stream

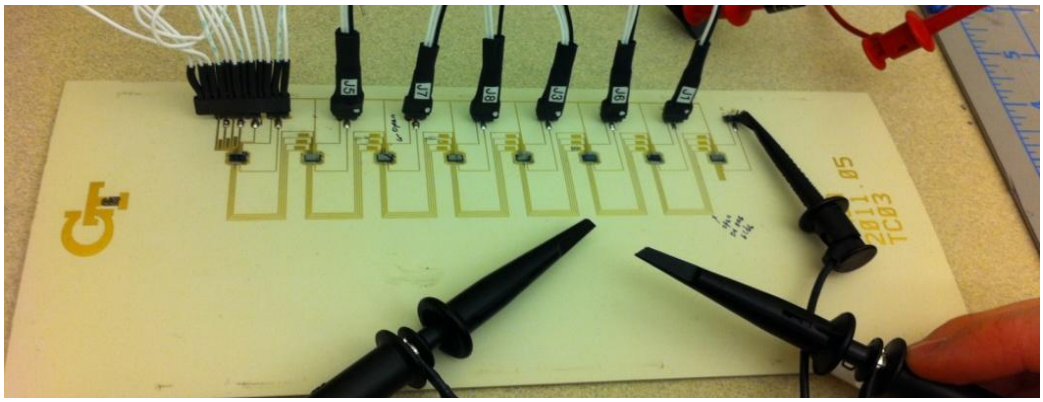


Figure 4.22: Digital test board populated with eight T/R modules.

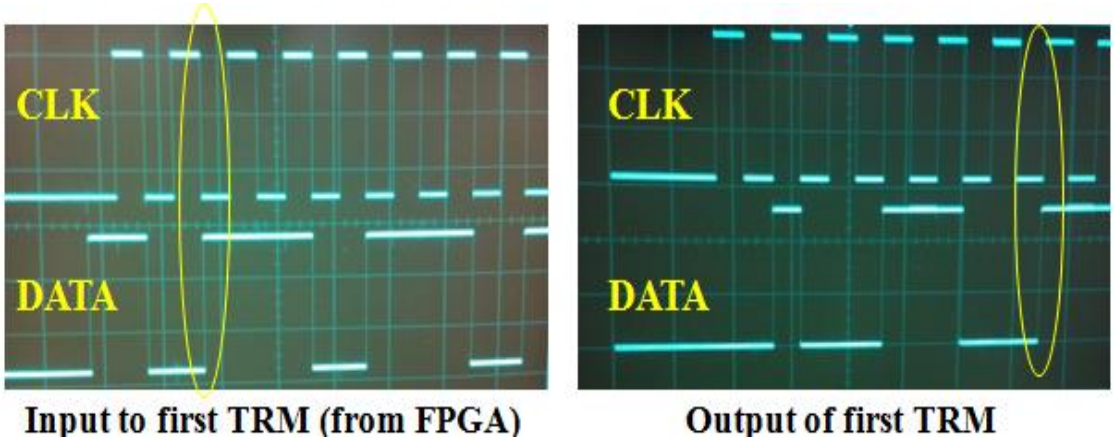


Figure 4.23: Oscilloscope captures of T/R module input and output data streams.

is around 200 ps. Such a short delay makes shift registers sensitive to noise and effectively puts them into a metastable state. Additionally, the rising edges in Figure 4.24 are distorted and effectively slowed down by parasitics resistances and capacitances. Data can "slip through" shift registers if the first latch is clocked before the second, which can happen when clock edges are distorted/slowed like this. Due to these issues, the new T/R modules as fabricated could not be controlled in a serial chain.

Simulations of the VHDL code used to synthesize the digital block showed that changing the data output on the rising clock edge was written into the VHDL. The chain of these deserializers functioned correctly in simulation, but these simulations did not sufficiently account for parasitics and noise. The VHDL code should be changed in

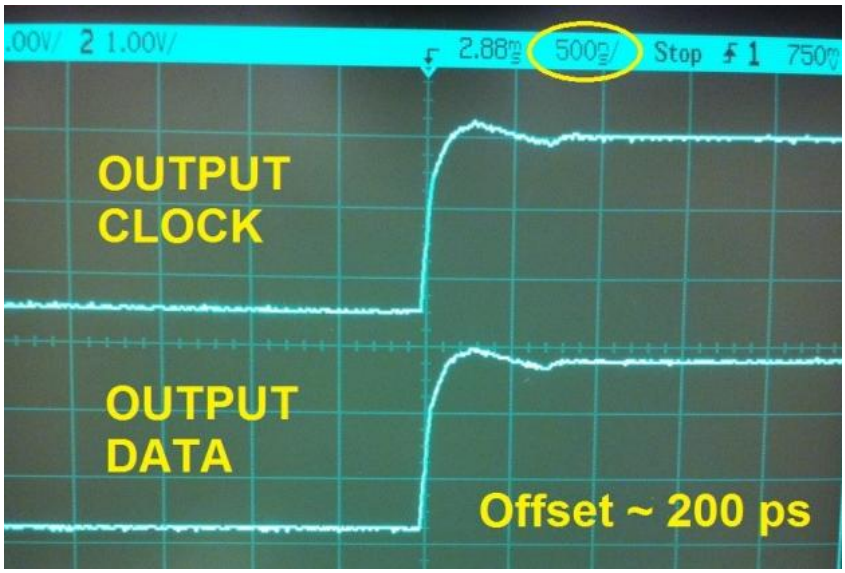


Figure 4.24: Oscilloscope capture of the clock and data transitions at the output of the first T/R module.

future designs so data changes on falling clock edges. This would ensure that the data signals settle before they are read into the shift registers. Larger buffers on each digital input and output pin would prevent the signal edges from being distorted and slowed down. Schmitt triggers could be added to each data input to make the input registers immune to noise (using hysteresis). The shift registers could be designed so each of the two latches in a register is activated on opposite clock cycles, which would prevent data from "slipping" through the registers due to slow clock edges.

4.6 Array Integration and Characterization

Once the T/R modules were fully characterized and the packaging process was improved, the final 8x8 array was assembled. The array fabrication and assembly process is fully described in [49]. Even though the flip chip bonds were fairly robust due to the injection of epoxy underfill, embedded packaging could not be demonstrated for this array because laminating an embedding array onto the board would have required compressing the array and risked breaking the flip-chip bonds. Broken bonds in the embedded antenna would be very difficult and time-consuming to debug and repair.

Figure 4.25: Fabricated array populated with 32 T/R modules and connected for near-field chamber measurements.

Figure 4.25 shows an image of the final 8 x 8 array populated with 32 T/R modules. The dc/digital and RF distribution networks can be clearly seen along with the simple required external connections. The coaxial cable was taped to the array mounting fixture to prevent the cable from placing mechanical stress on the panel which could damage the fragile bonds.

The radiation pattern of the antenna was measured in a near-field range chamber. A waveguide antenna probe scanned vertically while the antenna mount was rotated ±180° to perform a full cylindrical scan. A photograph of the chamber test setup is shown in Figure 4.26. Software provided by Nearfield Systems, Inc. was used to automate the measurements and calculate the far-field antenna patterns from the measured near-field cylindrical data.

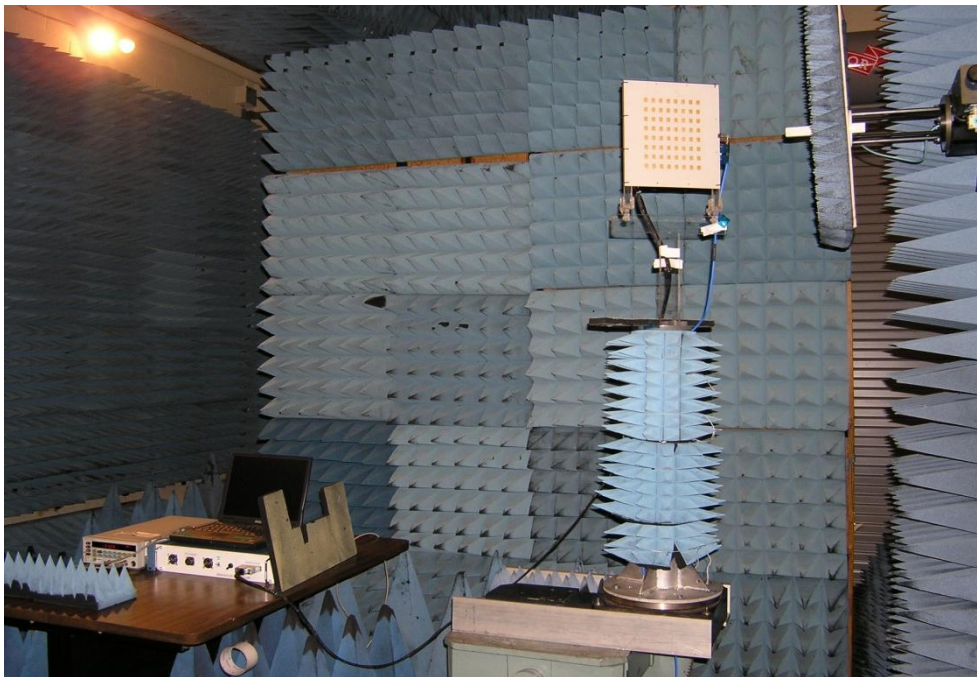


Figure 4.26: Near-field range chamber test setup for characterizing the antenna radiation patterns.

The measured antenna gain patterns across azimuth are shown in Figure 4.27. Measurements were only performed at the zero phase state for both transmit and receive due to the issues with the chip-to-chip serial control. The broadside gain in receive mode is 20.1 dBi and the gain in transmit mode was 14.6 dBi at 9.5 GHz. The gain difference between receive and transmit modes is very close to the difference observed between the gains of the T/R module transmit and receive paths, as expected. The gain variation across frequency for each path is minimal. This array has lower gain than previous implementations due to the implementation of a relatively lossy (vs. MEMS) T/R switch in the T/R modules, the degraded gain of the PA, and the lossy stripline beamforming network [49].

The effective isotropic radiated power (EIRP) was significantly improved from the previous implementation. EIRP is calculated from the equation

$$EIRP = P_T G_T \tag{4.1}$$

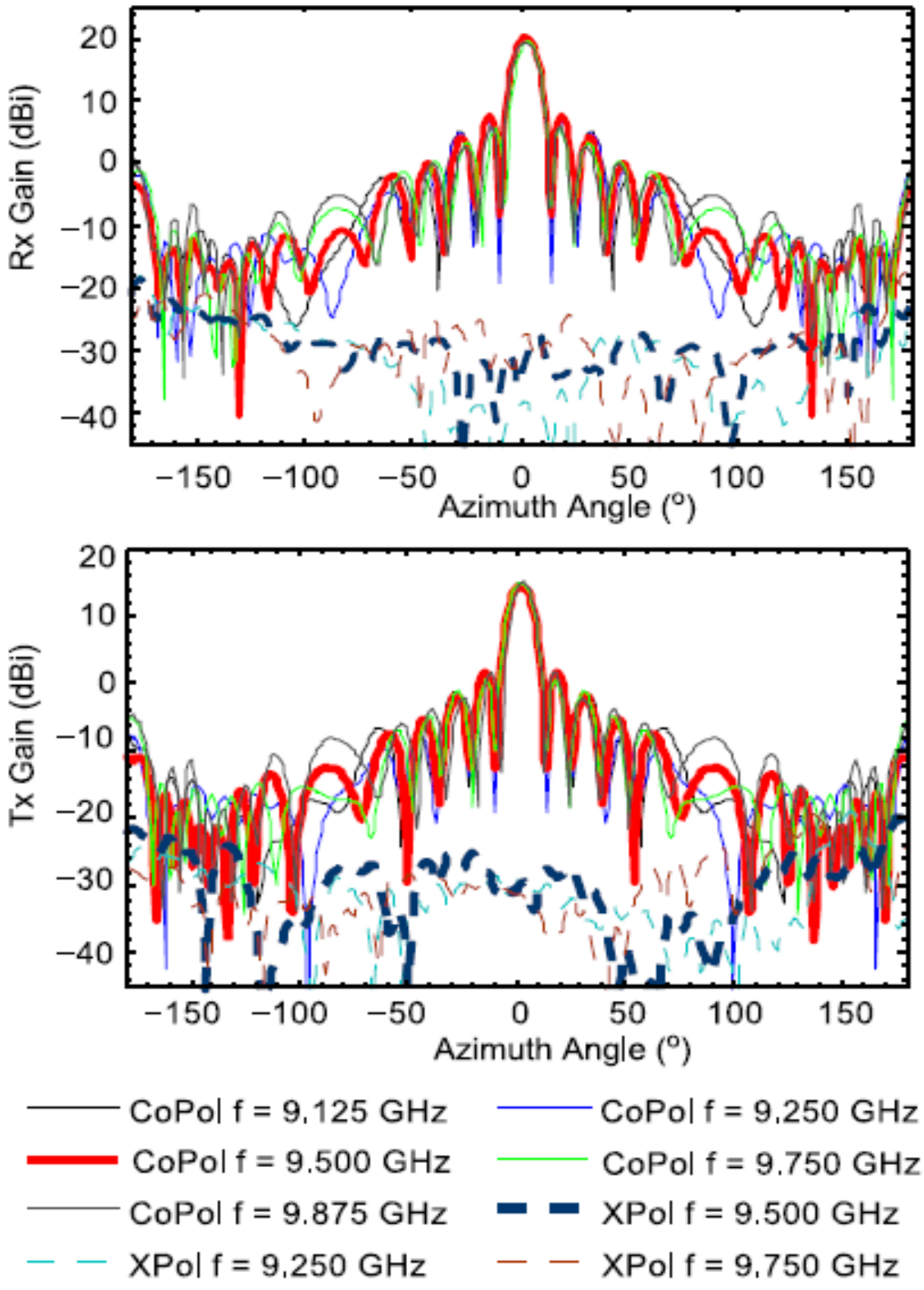


Figure 4.27: Measured far-field response of the 8x8 antenna array at the zero phase state [49].

where P_T is the transmitted power of the antenna and G_T is the antenna transmit gain. EIRP is typically measured in the far-field of the antenna, which required separate measurements described in [49]. The EIRP of this array was measured to be 47.1 dBm (51.3 W). The previous implementation of this antenna described in [48] had an EIRP of 42.5 dBm (17.8 W). Even though the output power of each T/R module was only 11 dBm (12.6 mW), combining 32 of these T/R modules in a high gain antenna resulted in far higher output powers. The EIRP would be even higher if the T/R modules had higher output powers like the implementation in [48].

The primary figure of merit for receiver antennas is the gain to system noise temperature ratio G/T, which is defined by the following equation:

$$\frac{G}{T} = 10\log\frac{G}{T_A} \tag{4.2}$$

where G is the receive gain of the antenna and T_A is the system noise temperature. T_A was calculated from the measured T/R module noise figure and simulated interconnect losses. The G/T of this array was calculated to be -6.64 dB, which is slightly reduced from the array presented in [48] due to the lossier components and interconnects in this final implementation.

4.7 Summary

This chapter presented the development, characterization, and integration of SiGe T/R modules into a thin organic X-band antenna sub-array for airborne SCLP measurements. The requirements of the applications dictated that the T/R modules be robust, low-power, and highly integrated with digital control on-die. The performance of the T/R module was degraded from simulation to measurement due to the shifted PA performance and poorly modeled switch devices. Packaging difficulties greatly complicated the characterization of the T/R module and prevented the embedded flip-chip packaging from being demonstrated at the array level. Despite these difficulties, a

very thin, lightweight, highly integrated, and high power antenna constructed from organic packaging materials and silicon-based T/R modules was demonstrated. This project shows the potential of SiGe as an alternative to III-V platforms for use in heavily SWaP-constrained radar applications.

CHAPTER V

CONCLUSION

5.1 Concluding Remarks

The research presented in this thesis demonstrates the potential of SiGe electronics for use in highly integrated radar applications. Microwave radar electronics are typically implemented using expensive and inefficient III-V semiconductor platforms that are difficult and expensive to integrate. SiGe HBT BiCMOS technologies provide a high-performance low-cost alternative to these traditionally dominant technologies. The high integration and high efficiency provided by SiGe technologies enable the development of lightweight, low-power, relatively low-cost radars for heavily SWaP-constrained platforms such as aircraft and satellites.

The primary limitation of SiGe PAs is their low achievable output powers at microwave frequencies. Chapter 2 discussed the fundamental power limitation mechanisms in SiGe BiCMOS technologies and presented methods for improving the output power in SiGe PAs. The concepts presented here were applied to the design of a robust self-biased medium-power X-band SiGe PA for an integrated T/R module. The measured performance of the PA was shifted from simulation and an in-depth investigation revealed that improper inductor layout techniques were to blame for the degraded performance.

The development of a very thin and lightweight organic X-band antenna using SiGe T/R modules was presented in Chapter 4. The application requirements drove the design of the sub-array panels and the SiGe T/R modules. The final sub-array integrated 32 SiGe T/R modules into a thin substrate stackup using advanced packaging techniques to realize a relatively inexpensive, easily transportable phased-array antenna panel. The performance of the T/R modules was degraded due to the PA layout issues and the

problematic chip-to-chip serial digital control, but these issues could be easily corrected in future designs. The SiGe T/R modules and the antenna array presented in this thesis show that SiGe is truly an enabling technology for relatively low-cost, highly integrated microwave phased array radar antennas.

5.2 Future Research Directions

A natural extension of the research performed in this thesis is to explore the design of low-power, robust SiGe electronics for space-based radar systems. Synthetic aperture radars in orbit endure temperatures up to 120° C while facing the sun and down to -110° C during the night while constantly being bombarded by intense radiation. Commercial radar systems on Earth are not exposed to these extreme environment conditions. Electronics in space are typically contained in temperature-controlled "warm boxes" which are bulky, expensive, and consume large amounts of power. Remote sensing systems function best when the front-end electronics are located very close to the antenna. If the electronics are inside a warm box, the long distance between the antenna and the T/R module will introduce noise and reduce signal integrity, reducing the dynamic range of the system. The electronics systems used in these missions are generally comprised of III-V components packaged in bulky multi-chip modules. Reducing the SWaP of these systems and eliminating the need for warm boxes and radiation shielding would improve the performance of the electronics and greatly reduce mission costs.

SiGe HBTs have been shown to have excellent performance in cryogenic environments and to be highly tolerant to ionizing radiation [53]. Space-based satellites are extremely SWaP-constrained platforms, so SiGe is a very attractive technology for space-based radar systems. Space-based radar systems need to have high output powers to overcome the attenuation caused by the long transmission distances between satellites and the surface of the Earth. Therefore, developing SiGe PAs suitable for space-based

radar is a high technical priority. I will focus on the design of SiGe PA variants optimized for temperature-invariant operation in space. This will require device-level characterization to understand the changing device performance at cryogenic temperatures, specifically the effects of temperature on operating voltage and current limitations and device impedances. Passive elements will need to be characterized over temperature as well so matching networks can be optimized for wide-temperature operation. Potential techniques for ensuring temperature-invariant performance are adaptive biasing networks and over-temperature tunable matching networks using varactors.

I will also explore developing SiGe electronics for space-based radiometer systems. Radiometers are highly sensitive receivers designed to precisely detect and measure microwave blackbody radiation. These receivers typically receive very low power levels, so the power challenges imposed by SiGe pose minimal design challenges for radiometers. I will specifically focus on the design of a SiGe radiometer calibration source which will consist of an avalanche diode noise source (hot noise temperature), a resistor at the ambient temperature (medium noise temperature), and an active cold noise source (cold noise temperature). These noise sources will be connected together by a low-loss high-isolation switch and fed into an LNA and receiver chain. These components will demonstrate similar performance to typical radiometer calibration sources with a much smaller form factor and lower power consumption. The low SWaP required by the SiGe radiometer electronics will reduce costs and improve the feasibility of future space-based remote sensing missions.

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