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Development and Testing of an Approach to Anti-Islanding in Utility-Interconnected Photovoltaic Systems

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Development and Testing of an Approach to Anti-Islanding in Utility-Interconnected Photovoltaic Systems

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Abstract

This report documents the development of an inverter control method that detects and avoids islanding in utility-interconnected photovoltaic installations. This method is applicable to single and multiple inverters connected to a single utility distribution line. The anti-islanding approach is described and its performance is demonstrated on both a theoretical basis and with results from tests conducted at Sandia National Laboratories and Ascension Technology, a division of Applied Power Corporation. It has been demonstrated that this approach is effective for single and multiple photovoltaic inverter installations for the special case where the inverter contains a version of anti-islanding software compatible with IEEE Std 929-2000. The report also describes the anti-islanding technique so that it can be incorporated into photovoltaic systems lacking this feature. A test procedure that ascertains whether an anti-islanding capability exists in a PV inverter is also presented.

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1. Introduction

Islanding of photovoltaic systems (or of any non-utility controlled generating system) has long been a concern of both utilities and generating equipment owners because of the potential for safety hazards and equipment damage. Islanding is a condition in which a portion of the utility system, which contains both load and operating generation, remains energized when utility operational procedures require that it be de-energized. If the generation is under the direct control of the utility, then it is not a concern in the context that this report addresses. If, however, the generating source(s) supplying the loads within the island is not within the direct control of the power system operator, then there is a concern for several reasons. Perhaps the most significant of these is the potential safety hazard of a lineworker, or a passerby, coming in contact with a line that is presumed to be de-energized, but is actually energized because of a home or business owner leaving a grid-tied renewable source energized and tied into the grid.

This report describes an anti-islanding control technique for use in utility-interconnected photovoltaic systems. The technique can be used to prevent islanding in any distributed generation resource that uses a static inverter as the interface device.

The report presents background, test results that helped direct the formulation of the final islanding prevention approach, and test results of the final anti-islanding technique.

One of the significant objectives of this project was to define a test procedure that can be used to confirm that a satisfactory anti-islanding technique is incorporated in an inverter. It was necessary to develop a standardized test that a single inverter with an adequate anti-islanding technique can pass, but which one that lacks such a technique will fail. This report describes such a test, and provides a discussion of why the test is adequate.

2. Background

Islanding of photovoltaic systems (or of any non-utility controlled generating system) has long been a concern of both utilities and generating equipment owners because of the potential for safety hazards and equipment damage. In the mid-1980s, Sandia National Laboratories contracted four electric utilities[1] for the purpose of identifying their areas of concern with photovoltaic systems. One of the areas identified as a concern was islanding. These four utilities then proceeded to perform islanding testing, under Sandia sponsorship, to determine the extent of the islanding problem. As documented in reference 1, some potential for islanding was found during these tests. This led several of the utility contractors to suggest that better understanding of the islanding phenomenon should be pursued, and more robust anti-islanding techniques should be developed.

A new generation of inverters was available in the mid-1990s. At this same time an upsurge in interest in utility-interconnected PV systems generated fresh interest in the topic of islanding. In addition, the developmental work on two standards required an improved understanding of islanding. These two standards were an IEEE standard on utility interconnection of PV systems (IEEE Std. 929-2000) and the Underwriters Laboratories safety standard for photovoltaic inverters (UL 1741). Because of the renewed interest in islanding and the need for test data to confirm anti-islanding capabilities of modern inverters, Sandia National Laboratories initiated a test program to investigate the propensity for islanding in today's inverters. To this end, several inverters from different manufacturers were subjected to islanding testing at Sandia. One important finding resulting from these tests was that the various approaches for preventing islanding utilized by different manufacturers interfered with each other thus allowing islanding to occur. Another finding was that even single inverters did not respond fast enough to meet the newly proposed IEEE Std. 929-2000 requirements. As a result of these findings Sandia undertook an anti-islanding development program in cooperation with U.S. PV inverter manufacturers.

Sandia sponsored a meeting for interested PV inverter manufacturers to develop a consensus on an approach for preventing islanding. Eight manufacturers were invited, of which seven sent representatives to the meeting. Several other people (outside of Sandia and the inverter manufacturers) also attended the meeting because of their specific knowledge of, or interest in, islanding. Since islanding

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[1] Public Service Electric and Gas Co. (New Jersey), Georgia Power Co., Salt River Project (Arizona), and Southern California Edison Co

was perceived by these manufacturers as a problem where cooperation among manufacturers was more productive than development of proprietary techniques (that is, techniques that could possibly interfere with each other) consensus was reached that a common technique was in the interest of all inverter manufacturers. An approach was then proposed for developing such a technique. This approach will be discussed further in this report.

Islanding prevention techniques other than that described in this document are certainly possible. However, any islanding prevention technique should be capable of passing the non-islanding inverter test described herein. Additionally no anti-islanding technique should be allowed to interfere with the techniques described in this document.

A Brief Discussion of Line-Commutated Versus Self-Commutated Inverters

When discussing an inverter's propensity to island, the question is often asked, "Is it a line-commutated or self-commutated inverter?" This is because of the erroneous perception that line-commutated inverters cannot island, while self-commutated inverters can. In fact either type can island. Whether or not they will is a function of the controls designed into the inverter.

There is some understandable confusion regarding the terms "self-commutated" and "line-commutated" when used with regard to inverters. There is a natural tendency to want to classify an inverter as either one or the other. Actually many inverters are really a hybrid of both, and shouldn't be classified as either one or the other.

Most PV inverters are line-commutated when viewed strictly from a dc to ac conversion perspective. Many inverters have a full bridge "unwrapper" where the dc/ac conversion takes place. An unwrapper is essentially a reverse rectifier. The unwrapper takes a string of positive half sine waves and flips alternating halves to negative sine waves, thus producing a full sine wave. The unwrapper operation is based on zero crossings of the line voltage waveform - hence it is line-commutated.

BUT, there is a second converter in many designs that controls the shape of the output current waveform, that is, the shape of the half sine waves that the unwrapper operates on. This converter is truly "self-commutated." The switching frequency is independent of the utility frequency. This converter is used to control the shape of the output current to be a 1/2 sine wave. This second converter is a dc/dc converter that functions before the line-commutated dc/ac inverter bridge unwrapper. The self-commutated operation of this second converter is what allows designers to achieve low harmonic distortion, typically

< 2% THD, which would never be achieved with a purely line-commutated design. Also, the self-commutated portion of the inverter allows the controls to be more sophisticated than a pure line-commutated design, as will be seen in the body of this report.

3. Islanding - Why the Concern?

Exactly what are we referring to when we use the term islanding? Islanding is a condition in which a portion of the utility system, which contains both load and operating generation, remains energized while isolated from the remainder of the utility system. If the generation is under the control of the utility, then it is not a concern in the context that this report addresses. If, however, the generating source(s) supplying the loads within the island is not within the direct control of the power system operator, then there is a concern for reasons that are discussed below. PV generation normally fits this latter condition. Although it is conceivable that PV generation could be controlled by the utility, that is not the normal case and is certainly not true with small dispersed systems such as those found on residential rooftops. Islanding of these small dispersed systems is the topic addressed by the work described in this report.

There has been some discussion that islanding under certain circumstances may be desirable. For example, if a utility experiences a disturbance that results in inadequate generation being available, it may be desirable to have all non-utility generation remain online to assist the utility in recovering from the disturbance. However, in today's world the penetration of utility-interconnected PV generation is not high enough to support entire sections of utility systems, so this issue is ignored for now, but may be revisited at a later time. Therefore, for the reasons discussed below, islanding of PV systems is to be avoided.

How an Island Might Occur

If a segment of a utility system is established as a PV-powered island, then there is no utility control over the voltage and frequency of that island. This situation could occur for the following reasons:

- as a result of a fault that is detected by the utility protection equipment, and results in opening a fault interrupting device, but which is not detected by the PV inverter (see "Undetected Line Faults" which immediately follows);
- as a result of accidental opening of the normal utility supply by equipment failure;
- as a result of utility switching of the distribution system and loads, such as for maintenance operations; or,
- as a result of human error or malicious mischief.

Why Islands are Undesirable

Non-utility controlled generation islanding should be avoided because:

- The utility cannot control voltage and frequency in the island. Voltage or frequency excursions can cause damage to customer equipment. Utilities are concerned that they might be found liable for electrical damage to customer equipment connected to their lines which is the result of voltage or frequency excursions outside of the acceptable ranges.

- Islanding may interfere with the restoration of normal service by the utility.

- Reclosing into an island may result in re-tripping the line or damaging the dispersed generation equipment, or other connected equipment, because of out-of-phase closure. (See "Reclosing," which follows.)

- Islanding may create a hazard for utility line-workers by causing a line to remain energized when it is assumed to be disconnected from all energy sources.

Undetected Line Faults

It is generally thought that a PV inverter will have no problem with islanding when the reason for the utility open-circuit condition is a utility line fault. The reasoning behind this misconception is that there will always be a voltage disturbance associated with the fault. While this will usually be the case with three-phase PV systems, it is not always the case with single-phase PV systems.

The majority of rooftop PV systems will be connected to a single phase of the utility's three-phase line. The majority of devices that utilities use to clear faults are three-phase devices. Many single-phase fuses are employed in utility systems, as well as single-phase reclosers, but these devices all have a three-phase fault-clearing device somewhere upstream. Single-phase fuses are usually coordinated with an upstream circuit breaker so that the breaker operates first, with the intent that it will clear temporary faults, then the line can be reclosed, thus limiting the time of the outage. The fuse only blows if the reclosing effort fails to clear the fault. This combination of single-phase inverters and three-phase fault interrupters leads to the potential for situations where a fault can exist on a line which results in the opening of a circuit breaker, but without an adequate voltage disturbance to impact the single-phase inverter.

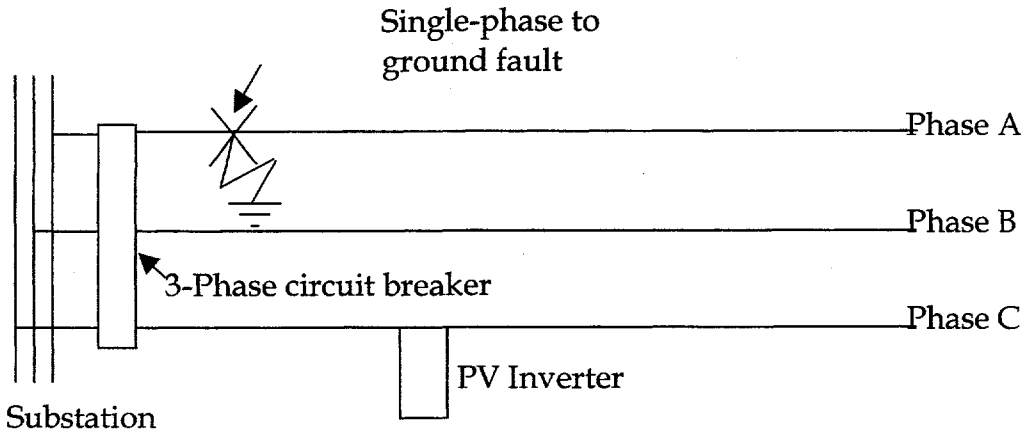

Figure 1. Single-phase fault on a three-phase system.

An example of such a situation is illustrated in Figure 1, where a single-phase-to-ground fault exists (an extremely common type of fault) on phase A while the PV system is on phase C. In this case, it is possible that the fault-clearing device (that is, the circuit breaker) will open and the single-phase PV inverter will not have seen sufficient voltage disturbance to cause it to trip. A three-phase inverter in this same situation will probably (depending on fault location and severity) have seen the voltage disturbance and will trip.

Reclosing

The vast majority (over 90%, by utility industry estimates) of utility outages in areas with overhead lines are caused by something that is transient in nature, such as a branch being blown into the lines, or a flash-over caused by a lightning surge. A technique that most utilities use to limit the outage time associated with these transient faults is known as "reclosing." This involves opening of the fault-interrupting device (circuit breaker or recloser), and then rapidly reclosing it. The time that the device is opened often allows the fault to clear, and then the reclosing operation restores normal service. If the first reclosing operation doesn't clear the fault, the reclosing procedure is normally repeated 2 or 3 times with increasingly longer "open" periods. If the fault can't be cleared by this succession of reclosing operations, then the interrupting device opens and stays open, requiring service personnel to visit the site, determine and remedy the cause of the problem, and then manually reclose the breaker.

What has this to do with islanding? If the line is opened, then reclosed, and a PV inverter remains active during the open period, two things might occur, neither of which is good.

First, the energy output from the inverter could conceivably maintain the fault arc so that the reclosing operation will fail and a long outage requiring service personnel will result. Two things make this possible. The PV system can energize a phase that it is not connected to by backfeeding various three-phase devices such as large motors and distribution transformers. Also the energy necessary to maintain a fault arc is much less than the energy required to initially establish the fault.

Second, a phase difference may develop between the inverter and utility during the outage so that, when the line is reclosed, the phase difference is adequate to damage the inverter. This is not expected to be a problem with reclosing intervals on the order of less than a second, but longer reclosing intervals are common for the final reclose attempts before lockout.

4. Basic Anti-Islanding Techniques

Most islands can be easily avoided by monitoring ac voltage and frequency at the inverter output terminals and only allowing inverter operation when these parameters are within acceptable limits. When an island is created, unbalance between islanded load and islanded generation will result in either frequency or voltage (or both) drifting outside of their normal operating range, causing the PV inverter to disconnect. It is possible, however, that the power requirements of the load match the instantaneous output of the PV system so closely that voltage and frequency limits would not be exceeded if the system were islanded. The existence of this "nondetection zone," where the load and generation balance is such that an inverter utilizing only voltage and frequency detection can continue to operate, is discussed in reference 2. This paper also discusses an interesting statistical analysis of the probability of having a load-to-generation match such that operation is in the nondetection zone. The analysis is based on correlation of simulated PV output with actual measured load data on specific feeders in various parts of the U.S. The paper indicates that, at certain times of day, with specific PV penetration levels (there must be connected PV system power ratings of at least 70% of the line's average loading), the probability of the load being in the nondetection zone can be as high as 30%. This non-zero probability suggests the need for additional controls to detect this potential islanding condition and remove the PV system from the circuit until the utility system is restored to normal voltage and frequency.

Tightening voltage and frequency windows of allowable inverter operation has been suggested as a means to eliminate islanding, but this only reduces the probability of an island occurring, rather than eliminating the possibility. A tighter operating window also increases the occurrence of nuisance tripping.

A more satisfactory solution to the problem of detecting a balanced dispersed-generation island is the use of an inverter that incorporates an adequate, anti-islanding technique.

What is a Desirable Response to Islanding Conditions?
During an island condition the inverter should stop energizing the line. However, a connection must be maintained for the sensing and control circuitry so that the inverter will be able to reconnect when the utility has returned to normal conditions. Throughout this report the term "disconnect" will be used for the situation where the inverter ceases to energize the line, even though the sensing circuitry to allow inverter control remains connected to the utility.

If the intention is to be certain that a downed line is de-energized in sufficient time that a lineworker or other person doesn't come in contact with an energized line, then an inverter that will disconnect in several seconds is adequate. A much more demanding requirement is to have the inverter disconnect rapidly enough that it will be off-line before the first "reclose" is initiated. Since high-speed reclosing often results in the line being reclosed within 12 to 15 cycles (0.20 to 0.25 seconds for a 60Hz system) of the initial opening, then an anti-islanding technique that can disconnect the inverter in less than 12 cycles is desirable. The intent of the work described in this report was to have an anti-islanding technique that will disconnect in 10 cycles (0.167 seconds) or less under most load-to-generation ratio conditions.

It should be noted that any utility condition that results in either frequency or voltage being out of specification at the inverter terminals is easily detected and responded to by the basic inverter voltage and frequency functions. Modern inverter designs can readily detect and respond to such situations in times significantly less than 10 cycles. Response in significantly less than 10 cycles is not desirable because it would result in nuisance tripping.

The only situation that presents some potential for difficulty occurs when the utility is disconnected and there is no associated perturbation of frequency or voltage at the inverter terminals. In most such situations, the voltage or frequency at the inverter terminals will eventually deviate from allowable values, causing the inverter to trip. Generally speaking, if the ratio of the real power of the islanded load to the real power of the PV inverter output is less than 0.5 or greater than 1.5, or if the islanded load has a power factor of less than 95% leading or lagging, then most inverters will not maintain both voltage and frequency inside the normal operating windows and the inverter will rapidly disconnect from the line.

The islanding condition that is most challenging to detect is the condition where the utility has disconnected, the inverter has seen neither a voltage nor a frequency disturbance, and the resulting islanded load has a close match to the PV output, both in terms of real and reactive power. A discussion of this situation is presented in Section 6, "The Non-Islanding Inverter," of this report.

5. Establishing the Need - Testing of Existing Hardware

Sandia's islanding-investigation program began with some basic testing to establish the state of islanding protection in commercial PV inverters available at the time (1997). This testing was performed by subjecting five inverters (from five different manufacturers--four U.S. and one Japanese) to a variety of basic islanding scenarios. This testing was performed with individual inverters and with various combinations of multiple inverters. The test setup is shown in Figure 2. The inverters tested would respond to an island in a satisfactory fashion if tested one inverter at a time. However, when tested in parallel, significant run-on times were seen. In this testing, some of the inverters were manually turned off after a run-on time of greater than 30 seconds. These results agreed with other theoretical and experimental work as reported by Ropp in reference 3, and indicated that further work on anti-islanding was needed.

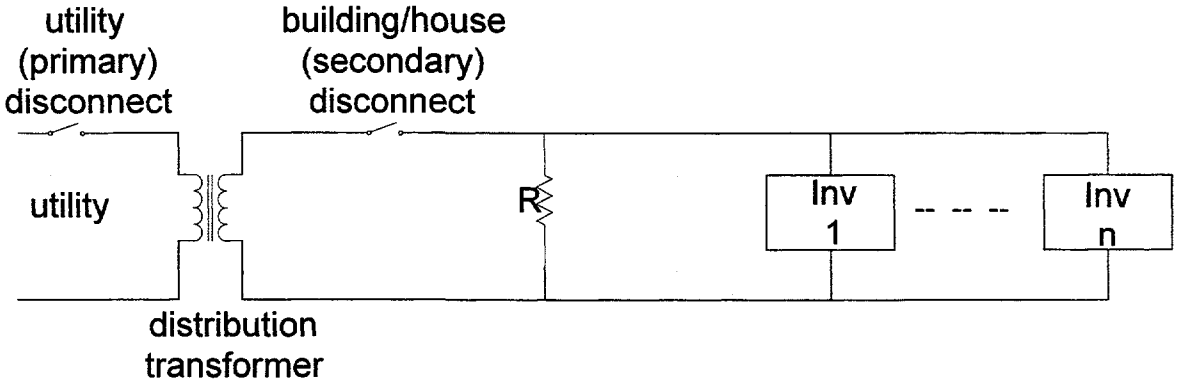

Figure 2. Test circuit configuration at Sandia Labs.

The Anti-Islanding Working Group

During this initial testing, conversations were held with the inverter manufacturers to discuss findings and determine future direction. Following the initial tests, the inverter manufacturers, and selected other individuals with interest or expertise in islanding, were invited to a meeting at Sandia National Laboratories to convene the Anti-Islanding Working Group and discuss the islanding issue. Most of the U.S. PV inverter manufacturers chose to attend this meeting. At the meeting, test results were discussed in detail along with a discussion of what desirable test results should be. It was decided that the requirements of IEEE P929, a draft of what is now IEEE Std 929-2000, the standard for utility interconnection of PV systems, should be the target. These requirements are given in section 6, "The Non-Islanding Inverter," of this report. As a result of these discussions, the PV inverter manufacturers agreed that a

common anti-islanding technique, one that all manufacturers could adopt if they chose to do so, was in the best interests of the PV industry. The working group made recommendations regarding the approach that was to be pursued. Active methods that perturb the utility and measure a coincident change in voltage or frequency were rejected by the working group because it was felt that there would need to be synchronization between units for this type of scheme to work in high penetrations. Utility members of the P929 working group had expressed the concern that such synchronized perturbations can be undesirable for the interconnected utility by degrading power quality.

As a result of this agreement, an effort was undertaken to establish such a technique. Ascension Technology was selected as the contractor to develop the technique. Lab testing of the new design (using dc power supplies instead of PV arrays) would be performed at Ascension Technology's Boulder, Colorado, laboratory and verification testing with actual PV arrays would be performed at Sandia National Laboratories.

6. The Non-Islanding Inverter

The efforts of the Anti-Islanding Working Group were to develop an anti-islanding technique which could be incorporated into any manufacturer's inverter and make it a non-islanding inverter. It is important to note that a non-islanding inverter cannot be expected to provide anti-islanding protection for other distributed generators on the same circuit that don't incorporate adequate islanding protection measures. That is, if some other distributed generator on the same circuit as the non-islanding inverter regulates voltage and frequency inside of the non-islanding inverter's trip limits during an island, then the non-islanding inverter has no means to distinguish whether the voltage and frequency are being maintained by the utility or by a non-utility generator.

What is a Non-Islanding Inverter?
A non-islanding inverter is defined in IEEE Std. 929-2000 as:

> An inverter that will cease to energize the utility line in 10 cycles or less when subjected to a typical islanded load in which either of the following is true:
>
> 1. There is at least a 50% mismatch in real power load to inverter output (that is, real power load is less than 50% or greater than 150% of inverter power output) or,
> 2. The islanded-load power factor is less than 95% (lead or lag),
>
> If the real-power-generation-to-load match is within 50% AND the islanded-load power factor is greater than 95%, then a non-islanding inverter will cease to energize the utility line within 2 seconds whenever the islanded load has a quality factor of 2.5 or less.

Note that the above definition includes two cases. Case 1 is for a "typical" island in which load and generation <u>are not</u> closely matched, and case 2 is for an island in which load and generation <u>are</u> closely matched. In case 1, where load and generation are not closely matched, disconnect is required to be in 10 cycles or less. For case 2, two seconds are allowed for the inverter to recognize the island and disconnect. Note that the 10 cycle disconnect for case 1 is the value that was discussed in the section titled "What is a Desirable Response to Islanding Conditions?" in order to eliminate problems associated with high-speed reclosing. Although the 2-second disconnect associated with case 2 is longer than the time required to not interfere with high-speed reclosing, this is not seen as a problem because of the low probability of occurrence. That is, in order to qualify for the 2-second disconnect time, both real and reactive power of the load must match real and reactive output of the PV system.

What Is Q and Why Does It Matter?

The IEEE definition for a non-islanding inverter also specifies that the closely matched load case has a quality factor, or Q, of 2.5 or less. (Unfortunately, "Q" can be confusing because it is used for different quantities in electrical engineering. It is used for the reactive component of complex power, as in the equation S = P+jQ, and also as the quality factor of a resonant circuit. The latter use is what is intended in this discussion.) Q is defined as 2π times the ratio of the maximum stored energy at the resonant frequency to the energy dissipated per cycle at that frequency. Resonant frequencies near the utility operating frequency, 60Hz in the US, are the only resonant frequencies of concern in this discussion. If a circuit is resonant at some frequency other than the utility operating frequency, it will have a tendency to move the island frequency outside of the normal frequency-operating window. This will trip the inverter.

If the resonant circuit, such as a load on a power system, comprises an inductance, L, a capacitance, C, and an effective resistance, R, all in parallel, then the value of Q is:

$$Q = R\sqrt{C/L} \qquad (1)$$

or, noting that for the resonant case where □, *the angular frequency is*

$$\omega = 1/\sqrt{LC}\,, \qquad (2)$$

then

$$Q = R/\omega L. \qquad (3)$$

On a power system, where real power, P, and reactive powers, var_L for inductive load, and var_C for capacitive load are measured at 60Hz:

$$Q = (1/P)\sqrt{var_C \times var_L} \qquad (4)$$

Note that in this report, "var" (often written VAr) is used to designate reactive power. This is for convenience even though it is technically incorrect, as "var" is a *unit* of reactive power. In addition, "var" is used as a *magnitude* in this report, not a signed value. Thus, for the resonance case the notation $var_C = var_L$ is used, rather than [capacitive reactive power] = -[inductive reactive power].

Also note that equation (4) assumes the load can be modeled as a parallel RLC load. Reality is much more complicated. Test results and theoretical modeling [3] have shown that this simple model works well in predicting worst-case islanding test conditions. Also note that the quantities var_C and var_L actually vary as a function of power system frequency. For example, as frequency increases, var_C increases and var_L decreases. At the resonant frequency var_C and var_L are equal. When var_C and var_L are equal, the RLC load appears resistive with unity power factor. This will be discussed further in a later section.

Since $var_C = var_L$ in the resonance case, then equation (4) simplifies to:

$$Q = var/P, \tag{5}$$

$$\text{where } var = var_C = var_L. \tag{6}$$

The higher Q is, the stronger the resonance. The reason that Q is important to this discussion is that strong resonance (high Q) results in a circuit with a strong tendency to move toward, or remain at, the resonant frequency. Thus the higher Q, the more difficult it is for an anti-islanding technique that uses frequency shifting to actually shift the frequency, a necessary action for proper response to an island. Therefore, when defining a non-islanding inverter, the maximum value chosen for Q is important. Too low of a value for Q is unrealistic and may result in "passing" an inverter design that will island under real-world conditions. Too high of a value for Q is also not realistic, and results in an island for which an anti-islanding technique may not be able to respond properly. Utility engineers agree[2] that $Q > 2.5$ is unlikely on an actual distribution feeder.

An Association between Q and Power Factor

Associating Q with power factor provides a useful means for putting Q in terms that are familiar to most power engineers. That is, most power engineers have no reason to know what the Q is of a distribution line, but they will have an instinctive feel for what the power factor of that line is. The Q of a parallel RLC circuit can be mathematically associated with the power factor of a distribution line using the following logic:

1. Begin with a known, or assumed, circuit load and load power factor, <u>without any power factor-correction capacitors present</u>, i.e. the "uncorrected" circuit load. These data, along with the circuit voltage and frequency, define R (circuit resistance) and L (circuit inductance). Since the power system frequency is known, ωL is also known ($\omega = 2\pi f$).

[2] This maximum value for Q is the result of discussions within the IEEE P929 working group. This working group included 9 members who are currently electric utility company engineers, as well as 6 others who had previously worked as utility company engineers.

2. Assume that through good planning, or bad luck, power factor-correction shunt capacitors are added just adequate to correct the total circuit power factor to unity. This assumption is basic to obtaining the "worst case scenario" for the anti-islanding protection, since it makes the resonant frequency equal to the power system frequency. Any other resonant frequency would tend to aid, rather than hinder, the anti-islanding protection. (Note that once this assumption is made, L and C are no longer independent; they have a fixed relationship of $\omega L = 1/\omega C$.)
3. With this parallel resonant RLC circuit, $Q = R/\omega L$, as stated in equation (3) above. Note that, given Assumption 2, one doesn't need to know C explicitly in order to calculate Q. It can be calculated simply from R and ωL obtained from step 1.

With the above to establish the thought process, it can be seen that, even though the line may have shunt capacitors connected to improve power factor, the following calculation is performed using the power factor of the line as it would be without the capacitors connected.

$$Q = \tan(\arccos[PF]) \qquad (7)$$

where PF is the power factor of the distribution line with no shunt capacitors connected.

The selected Q of 2.5 equates to a power factor of 0.37. As power factor increases, Q decreases. Thus, the requirement that Q = 2.5 or less in the IEEE definition equates to lines with uncompensated power factors from 0.37 to unity. This will cover all practical distribution line power factors.

The Non-Islanding Inverter Technique

Two distinct, but related, techniques were developed in this program for avoiding islanding of PV inverters. These techniques must be used in conjunction with the traditional over- and under-frequency and voltage techniques. These new techniques are referred to as the Sandia Frequency Shift (SFS) and Sandia Voltage Shift (SVS) methods. Both methods can be employed in an inverter, but the design of some inverters makes it more reasonable to employ one of the techniques rather than the other. Employing both techniques in an inverter yields the best results, as will be shown later in this report.

Sandia Frequency Shift (SFS)

The frequency shift method is an accelerated frequency drift with positive feedback [4]. The positive feedback in the frequency control makes the island frequency unstable when there are no other mechanisms present to regulate island frequency. When the utility or other generators that control frequency are

connected, the SFS unstable frequency controls are not strong enough to affect frequency. When the utility is disconnected, the SFS method forces the frequency to shift outside of the frequency-operating window, causing the inverter to disconnect. The frequency shift is not in a fixed direction, but can be either up or down depending on generation and load characteristics.

When an island exists, the SFS unstable frequency controls will cause the inverter frequency to deviate from 60Hz. If the island frequency starts to move up, the reference frequency of the inverter moves up at a faster rate. If the island frequency moves down, the reference frequency of the inverter moves down at a faster rate. In order to prevent out of phase operation between the inverter output and the utility during operation in the normal frequency window, the inverter reference signal is reset at every zero crossing of the voltage waveform, a characteristic of line-commutated inverters. More detail on the implementation of SFS will be given later in this report. This method can be implemented digitally in inverter firmware.

Sandia Voltage Shift (SVS)

The voltage shift method is similar to the SFS method. Amplitude of the output current waveform is adjusted in response to utility voltage fluctuations. When voltage increases, output current is increased. When voltage decreases, output current is decreased. The control signal is based upon the difference between filtered average voltage and cycle-by-cycle measurements of voltage. During normal operation, the utility voltage will fluctuate slightly. If the positive feedback gain is chosen as 2.0, then when the utility voltage fluctuates by 1%, the output current will fluctuate by 2%. The SVS method was suggested as an alternative to the SFS method by two of the U.S. inverter manufacturers in an IEEE P929 meeting where the merits of the SFS method were being debated.

Voltage & Frequency Trip Set Points

Table 1 lists the voltage and frequency trip set points that were used during all of the tests. The values in this table are not in total agreement with IEEE Std. 929-2000 and UL 1741 May 1999 Edition, which are shown in Table 2. These tests were performed before the values in the standards were finalized. However, these trip points are adequate to demonstrate the SFS/SVS principles.

Much discussion surrounded the selection of trip points during the standards-writing process. For example, allowing the PV system frequency to go as low as the inverter can tolerate will result in leaving generation on line at a time when the utility presumably needs generation. However, many utility power pools have requirements that under-frequency trip points of generators and loads must be coordinated. Thus, the frequency trip points were selected to coordinate with existing trip points with the thought in mind that these points may be changed as

distributed resources increase to the point that they have a larger impact on utility system operation.

Trip points in an inverter can be changed to those required by the standards by making a change in firmware. In the final implementation tested, these trip set points were the only means for shut down of the inverters. (That is, the SFS/SVS technique forces the voltage and frequency to these points, and then the voltage and frequency trip settings actually activate the inverter disconnect.)

Table 1. Trip Set Points used in Ascension Technology testing. (Not in agreement with 929 trip points, which were established after this testing was complete.)

	Set Point	Time to Operate (cycles)
Frequency	> 63.0 Hz	½
	> 60.5 Hz	5
	< 59.5 Hz	5
	< 57.0 Hz	½
Voltage	> 145 V	1
	> 132 V	100
	< 110 V	100
	< 60 V	5
	< 30 V	1

Table 2. IEEE 929/UL 1741 trip points.

	Set Point	Time to Operate (cycles)
Frequency	> 60.5 Hz	≤6
	< 59.3 Hz	≤6
Voltage	≥ 165 V	≤2
	> 132 V	≤120
	< 106 V	≤120
	< 60 V	≤6

Note that the above operating times have been selected to allow ride through of brief voltage and frequency excursions to minimize nuisance tripping.

7. Testing Considerations

Before beginning a discussion of the test results obtained using the SFS/SVS techniques, a discussion of the significance of magnetic components and associated distortion on test results is needed. This discussion will help explain some of the results that otherwise might not be clear, as well as helping to understand the final testing technique selection.

Magnetic Components Result in Faster Disconnect

An observation during initial testing of balanced loads was that the presence of a 50kVA distribution transformer in the island significantly reduced the islanding times. All disconnects with the transformer in the circuit were in less than 0.5 seconds, while similar tests that did not include a transformer ran on indefinitely. Note that the resistance and inductance of the transformer were included in calculating the R, L, and C needed for a balanced island. The capacitance included those capacitors that were added to the circuit to cancel the 60Hz inductive reactance of the transformer (Figure 3).

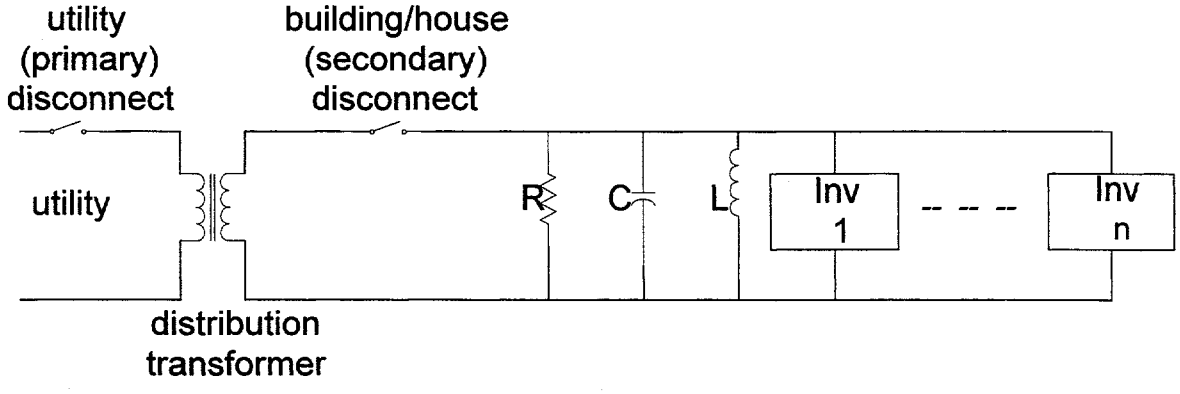

Figure 3. Test configuration that revealed impact of distribution transformer on test results.

Investigation led to the conclusion that the reduction in run-on time seen with the transformer in the test circuit was caused by the distortion in the combined transformer/capacitor load, which resulted in a harmonic-rich load that the PV inverters could not support. Figure 4 shows the transformer magnetizing current, the capacitor charging current and the combined current of the transformer and capacitor. (Figure 4a shows the values for the specific 50kVA transformer used in the test. Figure 4b shows similar values for a 15kVA distribution transformer for comparison.)

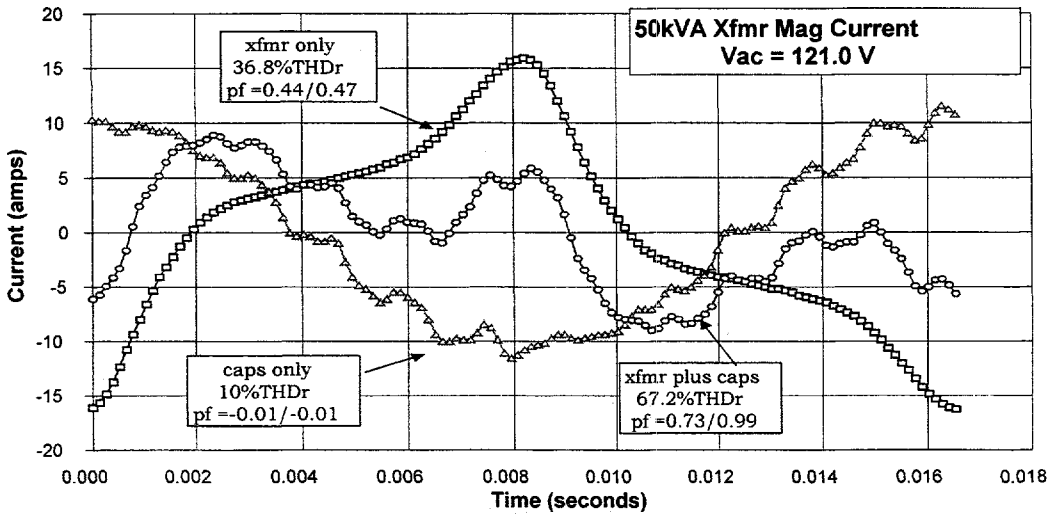

Figure 4a. Distortion and power factor associated with a 50kVA distribution transformer.

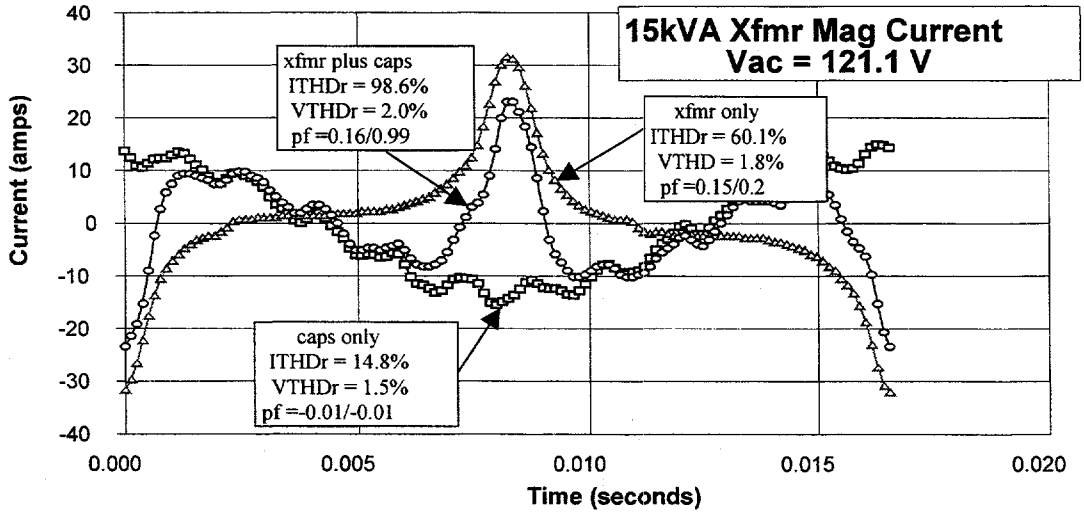

Figure 4b. Distortion and power factor associated with a 15kVA distribution transformer.

Note that Figure 4 also indicates power factor for magnetizing current, capacitor charging current, and total current. The first power factor value for each current is total power factor and the second value is displacement power factor. (That is, the first value is power factor when all frequencies are considered, the second is power factor of the 60Hz component only.) The capacitors cancel only the 60Hz component of transformer magnetizing current. The combination of 50kVA transformer and capacitors results in a load current that has 67% distortion and 73% total power factor, a harmonic-rich load at a power factor that the PV inverters aren't designed to supply.

Repeatability and predictability of the impact of magnetic circuits on testing is difficult to achieve because of the non-linearity of the saturation curve (*B-H* curve) of magnetic circuits. Excitation voltage affects distortion of a particular magnetic component, as does the manufacturer's selection of the magnetic material. For economic reasons, manufacturers of inductive components, such as distribution transformers, design the magnetic circuit so that operation is near the point at which the relation between voltage and current becomes highly non-linear. Thus, repeating the test with a small difference in excitation voltage can have a large impact on distortion. (Westinghouse's *Electrical Transmission and Distribution Reference Book*, fourth edition, indicates that an increase from 100% to 102% voltage will increase magnetizing current from 100% to 120% in commercial distribution transformers.) Other factors that impact the repeatability of such tests include design tradeoffs made in both the sizing of the magnetic circuit and in magnetic materials used.

Even though one may not be easily able to predict the impact of a particular magnetic component in an islanding test, it is clear that the more magnetics are involved in the island, the more distortion will be seen in the islanded load. In addition, an increase in magnetics in the islanded load decreases total power factor even if an attempt is made to cancel the magnetizing current requirements of the load with capacitors (which only impacts displacement power factor, not total power factor.) The characteristics of "off the shelf" PV inverters are such that they will not be able to support an islanded load which contains significant magnetic components, whether or not the magnetizing current is compensated by capacitors. (Custom-designed inverters capable of operating with variable power factor can be built. See "A Variable-Power-Factor-Inverter Consideration" in chapter 10 for a brief discussion regarding these inverters.) This leads to the conclusion that the fewer the magnetic components in the circuit, the more meaningful the resulting test. This is because the most difficult islanding test for an inverter is one with an undistorted, unity power factor load and circuit resonance at 60Hz.

Another nonlinear effect that is seen in inductors is the result of the magnetic core nonlinear B-H curve, which results in inductance varying as a function of applied voltage as discussed earlier. Because of this, any mismatch in real power, which causes a shift in voltage when the island is formed, will also affect inductance. This, in turn, affects reactive power balance, which affects island frequency. Because of this real world effect, it is more difficult to achieve the balance necessary for islanding with magnetic components in the circuit.

Because of the above, it was determined that worst-case testing excludes the distribution transformer from the islanded load. Therefore, all further testing discussed in this report is performed without the transformer.

Relation to Actual Utility Conditions

The above discussion might lead one to wonder if testing without a distribution transformer in the island represents a real islanding situation on a utility distribution line. Rather than examine various scenarios to determine the probability of islands without distribution transformers, it is better to examine the interaction of distribution transformers and utility line distortion.

Transformer magnetizing current, which remains constant and is independent of load current, is only a couple of percent of the transformer rated full-load current. (Actual distortion from this magnetizing current can vary quite a bit based on transformer core design, core material, and operating voltage. However, these factors are still providing variation on a value that is a couple of percent of load current.) If the transformer is energized, but not loaded, then the transformer draws a highly distorted current. That is, its current contains high total harmonic distortion (THD). As total load on the transformer is increased, the load current offsets the distorting effect of the magnetizing current, and THD is decreased. Therefore, the same 67% current THD that was seen for an unloaded transformer becomes only a couple of percent for a reasonably loaded transformer. (Clearly, if the combined distortion from capacitors and transformers on operating distribution lines resulted in 67% distortion, utility companies would be forced to alter the design of these components in order to meet the distortion requirements of their customers.)

Any islands that contain distribution transformers will also contain the loads on those transformers, resulting in reasonable distortion values. Thus, the islanding testing without a distribution transformer results in low distortion values, which are more like those actually seen on utility systems. The current distortion values seen with the unloaded transformer and associated capacitors are uncharacteristically high for operating utility systems.

Anti-islanding work performed by Japanese researchers around 1990 actually used this impact of distortion from distribution transformers as an indicator for an anti-islanding scheme. The scheme took advantage of the fact that the distortion from distribution transformers apparently increased during an island situation, and used the measured third and fifth harmonic voltage distortion increase as a signal that an island had been created and that the inverters should trip [9].

Is a Motor a Necessary Part of Islanding Testing?

Early in this testing, it was anticipated that a motor load might constitute a worst-case load. The motor has inertia that should help to maintain both voltage and frequency. As will be seen later in this report, induction motors were used

in much of the "proof of concept" testing done at both Ascension Technology and at Sandia. The motors were chosen specifically to have a "flywheel" effect. In most of these tests a ½ horsepower induction motor with capacitors and grinding wheels attached was used. As will be seen, the addition of these motors with flywheels did not, in general, result in an islanded load that was more difficult to detect than a tuned RLC circuit without a motor. A theoretical discussion of induction motors in islanded situations can be found in [3].

The motor did, however, add a variety of parameters to the test procedure that change from one motor to the next, making repeatable tests extremely difficult. For example, motor core materials, winding patterns, quality and condition of bearings, and inertia all impact the electrical characteristics of the motor in an island. Repeatability of testing with a tuned RLC load was excellent.

Testing Consideration Summary

Using only resistive, inductive, and capacitive components tuned to the power system frequency in the islanded load results in a well-defined, repeatable test. Motors and transformers were eliminated from the load to reduce harmonics and because of the difficulty in defining all the parameters associated with them (that is, impacts of differing core materials, winding patterns, motor inertia, etc.) How much these difficult-to-define parameters affect islanding depends very much on details of inverter design.

A final point, in addition to repeatability, that makes it desirable to define a satisfactory islanding test that does not require motor loads is scalability. The test method should be able to be used for a 100-watt inverter or a 100kW inverter.

8. Preliminary Test Results

Testing was performed at the Ascension Technology Boulder, Colorado, office and at Sandia National Laboratories in Albuquerque. The Ascension Technology testing was done in a "bench test" fashion, with power to the inverter being provided by a dc power supply, and with loads being varied as needed to match inverter output and the specific test conditions being examined. Testing at Sandia was done using PV arrays and laboratory loads.

The Ascension Technology testing allowed a greater number of tests to be performed in a given time period, as the inverter output could be fixed (by fixing the dc power supply output) which meant that a test could be repeated many times without having to make changes. The Ascension Technology testing examined one inverter and its associated load.

The testing at Sandia used multiple inverters in parallel. The Sandia testing included more variables than the Ascension Technology testing, as the inverter outputs continually varied as the sun varied, requiring frequent adjustment of the load to maintain balance between load and inverter output. It was important to do the Sandia testing to examine the response of multiple inverters in parallel, as well as to confirm that the inverters behaved the same way in a "field" environment as they did in the tightly controlled environment provided at Ascension Technology.

Worst Case Loads

During the preliminary testing before SVS and SFS were implemented, two types of loads were found to present the longest islanding times. These were RLC loads, with a resonant frequency of 60 +/- ½ Hz, and induction motor loads with capacitive var correction. The theoretical modeling described in [3] also indicated that this would be the case. In both the RLC and motor load cases it was necessary to balance load to output (both in magnitude and phase angle) in order to get long islanding times.

Preliminary tests included a wide range of generation to load ratios and load conditions. During the final testing, efforts concentrated on worst-case load testing only.

Single Inverter Tests at Ascension Technology

Tests conducted at Ascension Technology were done with a single modified SunSine™ 300 inverter. A dc power supply was used to provide controlled input power. Since the tests were conducted in the manufacturer's facilities, it was possible to control the inverter through a diagnostics interface. This allowed a

much faster test cycle time than is possible in field-testing. Firmware version 1.46 of the SunSine™ 300 utilized the SFS and SVS methods for anti-islanding.

Initial RLC Load Tests

The resistance in these tests was a result of the losses in the inductor only. For this set of tests, only inductance and capacitance was used for the load. The goal was to achieve a resonant load with the highest possible Q. This resulted in Q = 3.7. During the tests, the inverter was operated over a range of power levels to get a range of generation/load ratios, which varied from 0.68 to 1.19. Figure 5 shows the voltage trajectories for the various generation-to-load ratio tests and Figure 6 shows the frequency trajectories for this same set of tests. In these figures, the island is initiated at time equal to zero. Note that both the voltage and frequency are unstable and not able to sustain an island. In this set of tests the inverter shut down within 10 cycles due to frequency trips.

Other RLC load combinations were tested, but are not presented here. The tests presented represent the worst-case tests.

In Figures 5 and 6, the endpoints of the trajectories represent the last full cycle of voltage or frequency measurement. At some time during the following cycle the inverter shut down. The measurement system only made measurements on a full cycle of data, but the inverter makes measurements every half cycle. Therefore, the inverter may trip before a full cycle of data is taken. For example, all high-frequency trajectories in Figure 6 end below 63 Hertz. If the next complete cycle of data were taken, then it would show the trajectory passing 63 Hertz.

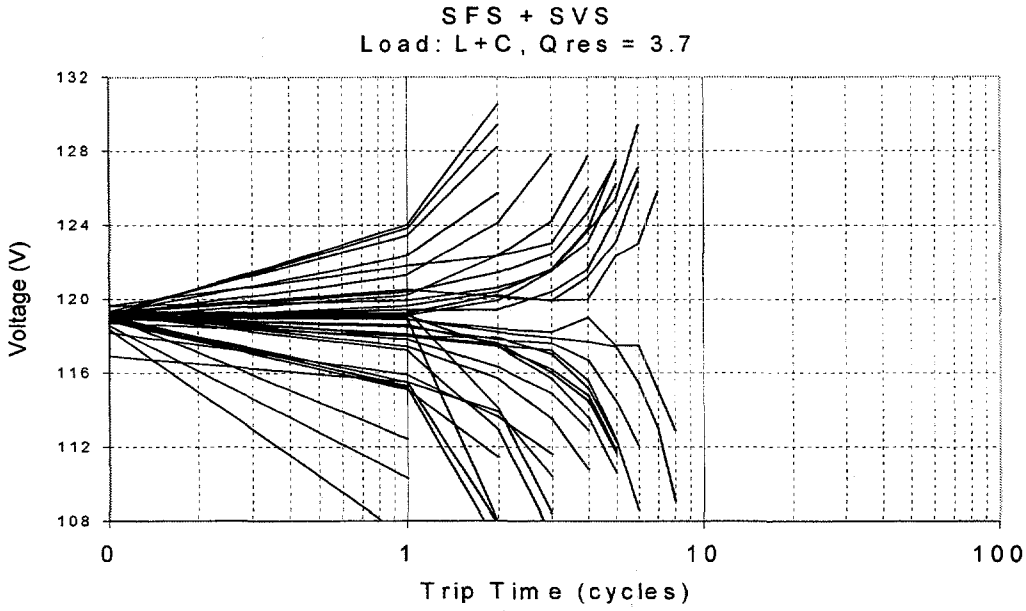

Figure 5. Voltage trajectories for a family of generation-to-load ratios for an RLC load. Trip points – 110V and 132V. (100 cycle maximum trip time).

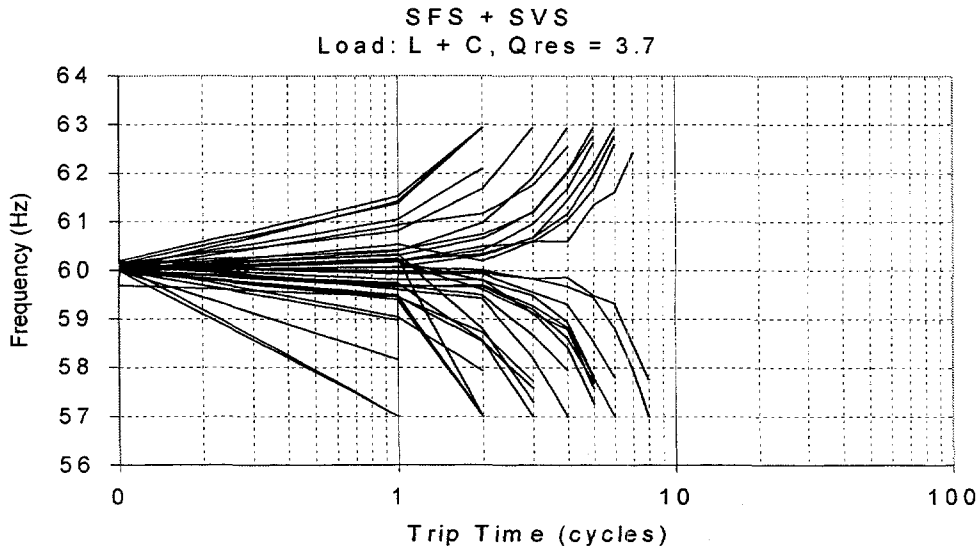

Figure 6. Frequency trajectories for a family of generation-to-load ratios for an RLC load. Trip points – 59.5Hz and 60.5Hz (5-cycle maximum trip time) and 63Hz and 57Hz (½-cycle trip time).

Induction Motor Load Test

A ½ HP induction motor with grinding wheels was used for the next series of tests. Capacitance of 261 vars was added to correct power factor of the motor to 1.00. No additional resistance was added to the test circuit, but the no-load

losses of the motor (that is, the power required to maintain motor speed) were 119 watts, resulting in Q = 2.2. Again, a range of inverter power levels was used to achieve a range of generation/load ratios that varied from 0.88 to 1.15. In these tests, no island exceeded 70 cycles, well below the 2 seconds required by IEEE/UL standards, and all trips were due to frequency trips. The power-factor-corrected motor voltage would drop by ½ in 42 cycles after disconnect of all sources of power. Figures 7 and 8 show the voltage and frequency trajectories for motor load tests. Figure 9 shows that the time to trip is heavily influenced by the generation-to-load ratio.

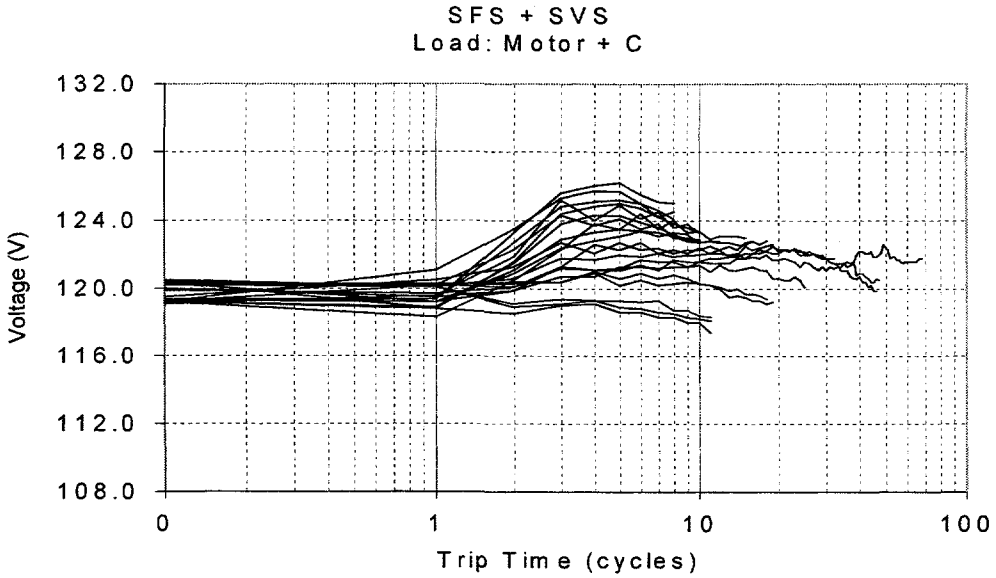

Figure 7. Voltage trajectories for a family of generation-to-load ratios for a PF corrected motor. Trip points – 110V and 132V. (100 cycle maximum trip time).

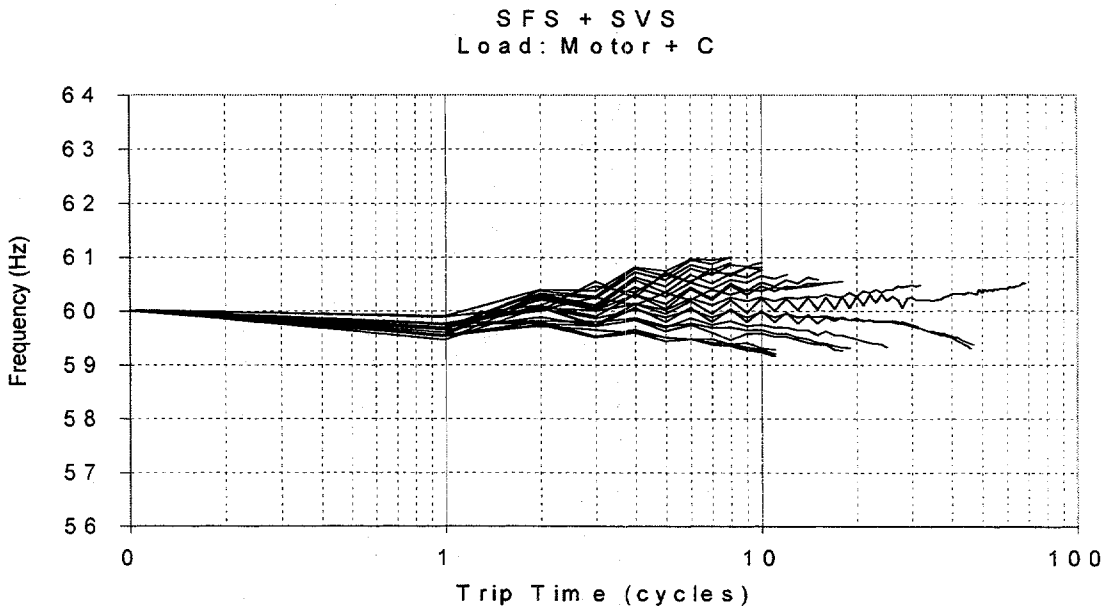

Figure 8. Frequency trajectories for a family of generation-to-load ratios for a PF corrected motor. Trip points – 59.5Hz and 60.5Hz. (5 cycle maximum trip time).

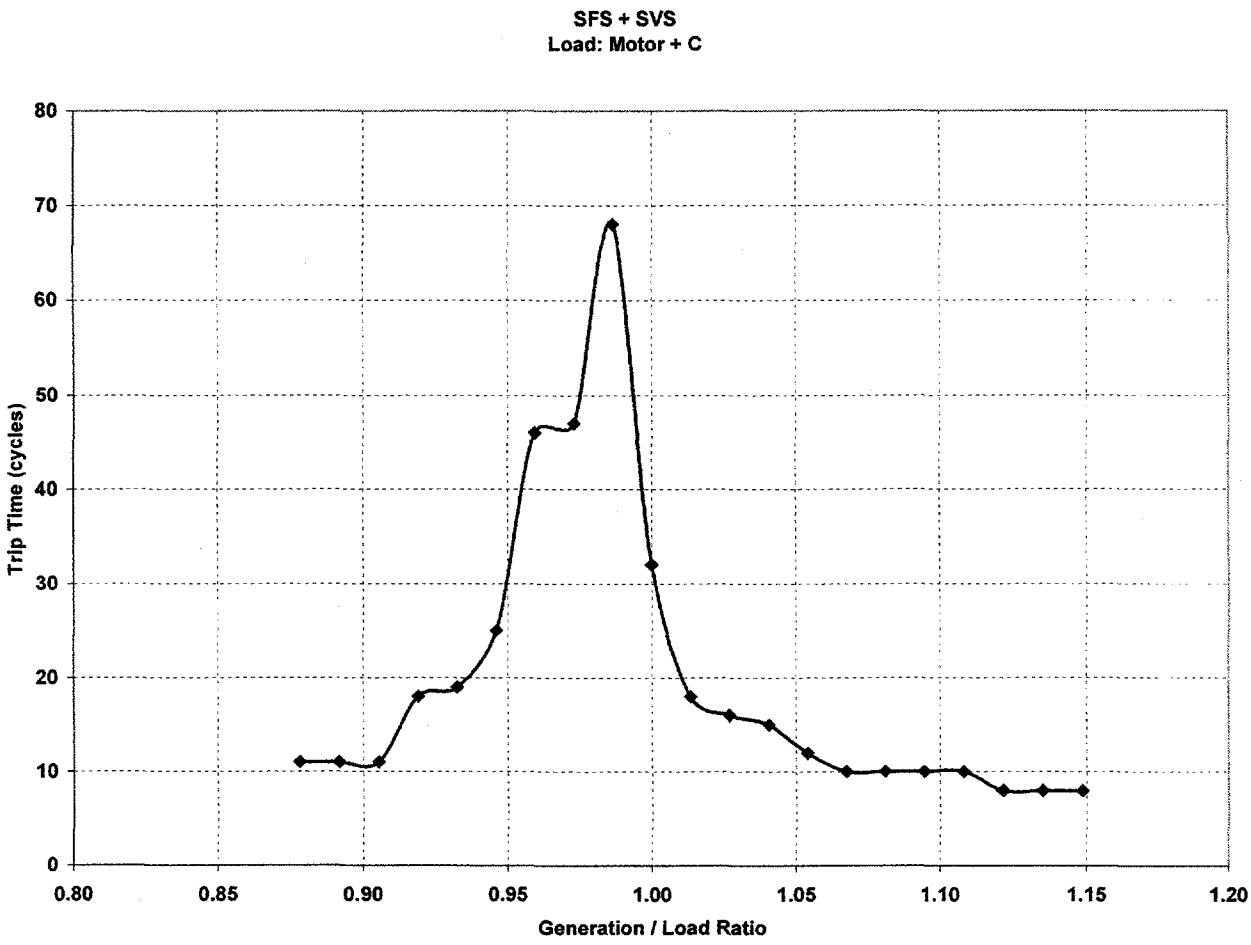

Figure 9. Trip time is heavily influenced by generation-to-load ratio.

Test Results from Sandia National Laboratories

Configuration.

Three of the specially modified SunSine™ 300 AC Modules were connected in parallel with various loads in an outdoor array field for the evaluation of the SVS/SFS anti-islanding technology. The circuit configuration is shown in Figure 10. The various loads were configured as required for each test and included R, RL, RLC, RC, motor, and motors with C. The ½ HP induction motor load included a flywheel (based on the concept that the flywheel can store energy, then transfer it back to the island through generator action). Parameters varied included power factor, $P_{generation}/P_{load}$, and Q. One of the two disconnects shown was used to interrupt the utility power. Because of the nonlinearity of the magnetizing currents in the transformer, as previously discussed most tests were performed using the secondary disconnect.

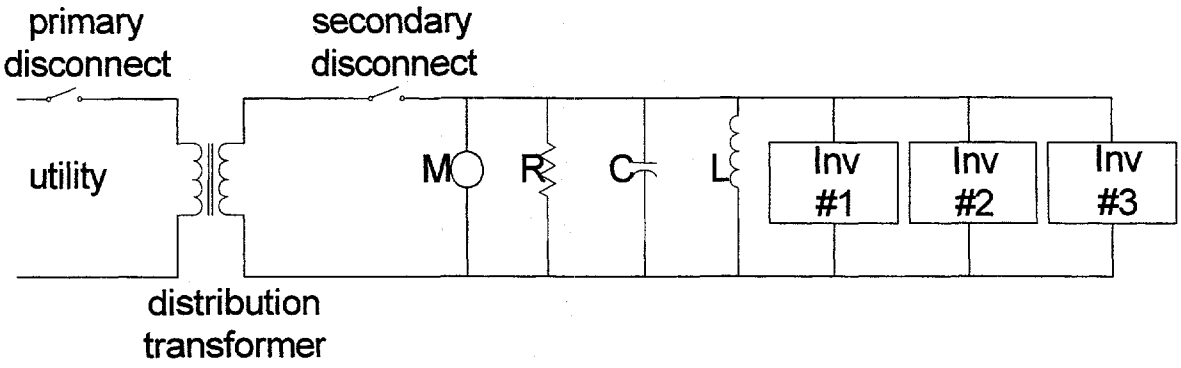

Figure 10. Configuration for testing at Sandia National Laboratories.

The test loads were selected based on a variety of input. The first discussions that indicated that an RLC circuit tuned to the power system frequency would be a good islanding test load occurred during an International Energy Agency workshop on PV/grid interconnection that was held in Zurich, Switzerland, in September of 1997. In addition, testing at Sandia and the theoretical results in [3], indicated a problem with high-Q loads. The "distribution transformer" used for those tests that included a primary side disconnect was unusually small (2 kVA) for a distribution transformer. That size was used to maintain an appropriate scale for the three 300 watt, module scale inverters. This approach resulted from the thought that two 4 kW inverters connected to a 15 kVA distribution transformer would be representative of two residential PV systems and would operate in a similar manner.

Initially the value of C in the RLC circuit was fixed at 301 microfarads (1.63kvar at 120Vac) and L was selected to provide 60 Hz resonance. The value of R was then sized to dissipate power equal to that produced by the three parallel inverters. This was a necessary condition for islanding. The value of R also determines Q. Since, with $var_C = var_L = var$, and $Q = var/P$ (as stated earlier in equation 5), it follows that high Q is achieved by operating the inverters at low power, as shown in Table 3. Thus the circuit could be islanded only for particular combinations of inverter output power and values of R, L and C.

Table 3. Q associated with various power levels when var_C=var_L=1.63kvar.

Q	Power (watts)
2	839
5	328
10	164
20	81

Test Results.
Three sets of data are presented in Table 4. The first column of data was the result of extensive testing of the SFS anti-islanding approach. (That is, SFS only, no SVS). This was an extensive series that evaluated a full range of load types. The results of the evaluation show that the SFS approach was very successful for all cases with the exception of certain RLC loads with strong resonance at 60 Hz. The run-on time is related to the circuit Q, with run-on times of about 6 cycles (approximately 100 milliseconds) for a Q equal to 1.5. For $1.5 < Q < 7$, the inverter shut down in less than 0.5 seconds (although relatively long for this series of tests, still less than the 2 seconds required in IEEE Std. 929-2000 case 2). For two of the higher Q cases (Q of 8 and 11), the circuit using only SFS islanded until operator intervention.

Table 4. Islanding times in seconds.

Load	SFS only	SFS & SVS 301 μ F	SFS & SVS 641 μ F
R	.068	-	-
RL	.028	-	-
RC	.036	-	-
RLC	.100 for Q = 1.5 .500 for Q = 1.5 to 7 Island* for Q = 8, 11	.32, Q = 7	.78, Q=8
Motor + C	.228	.53	-

*operator intervention required

The second column of data in Table 4 includes both the SFS and the SVS anti-islanding methods. This series of tests was limited to the previously identified worst cases, RLC and a ½ HP induction motor load (with flywheel and capacitor). This series of tests shows that the islanding associated with RLC resonance has been eliminated, the longest time being .32 seconds for a Q = 7 case.

The third column of data in Table 4 expands on the second set by doubling the available capacitance and hence increasing the allowable power output from the inverters for a specific value of Q. While this doubled the islanding time to .78 seconds, the islanding time is still not lengthy and the Q of 8 is very high, equivalent to having a line with uncorrected power factor of 12.5% or less. This very high Q condition is unlikely to occur in a normal distribution circuit

Motor Load Testing at Sandia
The motor load tests that were performed at Ascension Technology were repeated at Sandia. This was to provide confirmation that the motor, as a load,

presents no unusual obstacles to the SFS/SVS anti-islanding technique. The testing with three parallel inverters, and the sun as the energy source, was felt necessary to give a complete picture of the interaction of the SFS/SVS technique with motor loads.

The tests were configured as shown in Figure 10. The load consisted of the motor (with its associated inductance and resistance), plus additional resistive load to balance the output of the PV arrays, and adequate capacitance to balance the inductance of the motor. The motor is a ½ HP induction motor that runs a bench grinder. The grinder has two grinding wheels attached to enhance the flywheel effect of the motor. The secondary disconnect switch was used to initiate the tests. Ten tests were run with this configuration, with all shutoff times substantially less than the 2 seconds required by case 2 of IEEE Std. 929-2000. Five of the tests were run with the motor and flywheel "freewheeling," in which case the motor consumed 270 watts to maintain speed. The other five tests were operated with a steel bar pressed against one of the grinding wheels to increase the load on the grinder motor. In this condition, the motor consumed 420 watts to maintain speed. (The nameplate rating of the ½ HP motor was 480 watts.) The resistance was adjusted for these tests so that the balance between load and generation was maintained. That is, the 3 inverters combined were producing about 750 watts during these tests, so the total load needed to be about 750 watts whether the motor was consuming 270 watts or 420 watts.

For both the loaded and unloaded grinder tests, the fastest inverter trip times were 0.172 seconds. For the loaded grinder tests, the maximum run-on time was 0.196 seconds, while the maximum run-on time for the unloaded grinder test was 0.22 seconds, as shown in Tables 5 and 6. Clearly, the two-second trip time limit was easily met.

Table 5. Trip times for ½ HP grinder motor with load.

	Trip Times (sec.)		
Generation/Load	Inverter 1	Inverter 2	Inverter 3
0.989	0.18	0.18	0.18
0.996	0.172	0.188	0.188
1.022	0.172	0.196	0.196
1.031	0.18	0.172	0.172
1.141	0.196	0.196	0.196

Table 6. Trip times for ½ HP grinder motor without load.

	Trip Times (sec.)		
Generation/Load	Inverter 1	Inverter 2	Inverter 3
1.058	0.204	0.204	0.204
1.059	0.22	0.212	0.212
1.069	0.172	0.172	0.196
1.099	0.18	0.204	0.196
1.125	0.204	0.204	0.204

9. The Non-islanding Inverter Test

An important part of the development of non-islanding inverters is development of a technique for testing inverters that will identify the incorporation of a suitable anti-islanding technique in an inverter. Ideally, such a test will allow testing of one inverter at a time and will provide a screen that passes inverters that incorporate a suitable anti-islanding technique, while failing those without such a technique. Recall that, in the preliminary testing at Sandia National Laboratories, single inverters were able to pass islanding tests that those same inverters, when paralleled with other manufacturers' inverters, failed. A good non-islanding inverter test should be capable of being performed on a single inverter, rather than requiring multiple inverters, so that independent-testing laboratories, such as Underwriters Laboratories, can readily perform the test when evaluating new inverter designs.

The task, then, was to develop a test that will be meaningful when applied to single inverters. This test should identify inverters that have an anti-islanding scheme that will assure that the inverter will not island if tested with multiple inverters. This is where the concept of a load that is resonant at the power system frequency (60Hz in the U.S.) with a Q of 2.5 is important. If the load in the island under test is simply a resistance, and load and generation are not well balanced, then basic frequency and voltage trip limits provide satisfactory islanding protection. However, the addition of inductance and capacitance, tuned to 60Hz, will tend to keep the frequency at 60Hz. Additionally, balancing load and generation will maintain voltage within operational limits. Therefore, an islanding test with balance between load and generation (ratio of load to generation between 0.5 and 1.5) and a 60 Hz resonant circuit with Q = 2.5 constitutes a satisfactory single-inverter non-islanding test.

Non-Unity-Power-Factor Inverters

An additional complication arises with inverters that are designed to be able to operate in either the utility-tied mode or the stand-alone mode. These inverters are understandably popular because of their ability to provide the PV system owner with power even when there is a utility outage. This type of inverter typically has two ac tie points – one that is tied to the utility and one that is tied to those loads that the owner has chosen to keep energized during a utility outage. The owner's other loads are energized conventionally through the main distribution panel, the same place that the PV system ties into the utility system. The utility tie connection is the one to which the anti-islanding scheme applies. During a utility outage, the inverter opens this tie, disconnecting the customer and his PV system from the utility. At this time all loads in his house are dropped except those that are tied to the second inverter ac tie point. The

inverter maintains the connection to these loads, which the owner has selected for operation during outages. Conceivably, the owner could choose to connect the entire house to this second tie point so that the entire house would maintain power during a utility outage. The owner would just need to be certain that the PV system, and its battery backup, has the capacity to carry the load of the entire house.

The fact that the inverter can source reactive power adds a complicating factor to any islanding testing. One of the key features of an islanding test is that the real power and the reactive power must be balanced independently at the point where disconnection will take place. That is, the islanded real power load and the islanded real power generation must equal each other, resulting in zero real power current flow out of the island. The same must be done independently with the reactive power.

Balancing real power load and generation is straightforward in a laboratory setting. The same is not true of reactive power. Inductors and capacitors draw non-60Hz current (distortion current) which complicates the test procedure. Measurement of reactive power flow then becomes more complex, as the 60Hz component of this distorted reactive power is what must be balanced in the island. The test procedure that follows may seem a bit cumbersome, but it was found through many trial and error tests to produce consistent results.

The following is the test procedure that was developed to identify a non-islanding inverter. This procedure is also included as an annex in IEEE Std. 929-2000:

Test Procedure to Verify Non-Islanding Inverters

Begin by verifying that the frequency and voltage trip points function properly, as these are what actually disconnect the inverter. Once the fixed frequency and voltage limits have been verified, test to determine the inverter cannot maintain stable operation without the presence of a utility source. A utility source means any source capable of maintaining an island within the recommended voltage and frequency windows. Because of the uncertainty associated with the need to sink both real and reactive power from the inverter, this test is best performed with a utility connection, rather than a simulated utility. (Note that frequency and voltage variation are not required for this testing.)

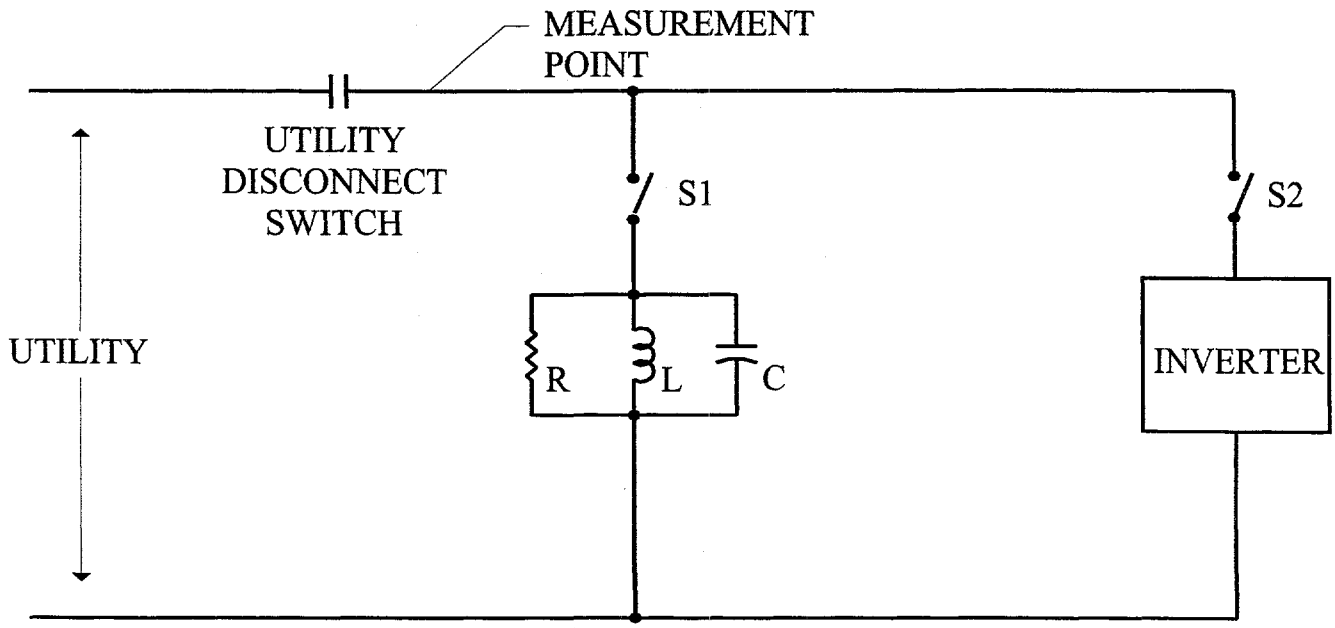

Figure 11. Non-islanding inverter test circuit.

This test procedure is based on having the Q of the islanded circuit (including load and inverter) set equal to 2.5. Recall the following equations from section 6 of this report (also recall that "var" is used to represent the magnitude of reactive power):

$$Q = (1/P)\sqrt{var_C \times var_L}$$

Note also that, in the resonant case

$$var = var_C = var_L$$

Therefore, in the resonant case,

$$Q = var/P,$$

Test procedure background: This test procedure is designed to be universally applicable to both unity-power-factor inverters and non-unity-power-factor inverters. With unity-power-factor inverters, the second step (step b, below), where inverter reactive power output, $P_{q\text{-inverter}}$, is measured, will result in a value of $P_{q\text{-inverter}}$ that is zero, simplifying the remainder of the procedure. For inverters where $P_{q\text{-inverter}}$ is not zero the test is complicated by the presence of reactive power in the inverter.

Harmonic current that flows between the utility, the loads and the inverter, further complicates the situation by making it appear that current is flowing

when the 60 Hz component of current has been zeroed. Thus, it is important, when adjusting inductive and capacitive reactance, to use instruments that can distinguish the 60Hz component of current and power from other frequencies.

The sequence of the steps below is suggested for several reasons. The inductance is measured first because that measurement is low in harmonics. The capacitance is added second so that the voltage is stable when the resistance is added. The resistive parallel load is then added and adjusted. Note that this resistance will be in addition to the resistance that will be part of the inductive load.

This test procedure assumes that a non-unity-power-factor inverter will be sourcing, not sinking, reactive power. The procedure refers to a circuit that is configured as shown in Figure 11. Details of this circuit may be changed to suit the specific hardware available to the tester. For example, it may be convenient to replace switch S1 with individual switches on each leg of the RLC load. For each inverter/load power combination the following procedure is suggested to achieve the proper generation-to-load complex power balance.

Non-islanding inverter test procedure:
(Note: This test procedure uses the terminology from IEEE Std 929-2000, including the use of P_{qL} and P_{qC} for inductive and capacitive reactive power. These terms are used in the same manner as the terms var_C and var_L have been used throughout this report. That is, they are used as magnitude values, not signed values.)

a) Determine inverter test output power, P_{inv}, that will be used.
b) Operate the inverter at P_{inv} and measure inverter reactive power output, $P_{q\text{-}inverter}$. This is accomplished by:
   Close the utility disconnect switch. With no local load connected (that is, S1 is open so that the RLC load is not connected at this time), and the inverter connected to the utility (S2 is closed), turn the inverter on and operate it at the output determined in step a). Measure real and reactive power flow at the measurement point. The real power should equal P_{inv}. The reactive power measured in this step is designated $P_{q\text{-}inverter}$.
c) Turn off the inverter and open S2.
d) Adjust the RLC circuit to have Q = 2.5. This is accomplished by:
   1) Determining the amount of inductive reactance required in the resonant RLC circuit using the relation $P_{qL} = 2.5\ P_{inv}$.
   2) Connecting an inductor as the first element of the RLC circuit and adjusting the inductance to P_{qL}.
   3) Connecting a capacitor in parallel with the inductor. Adjust the capacitive reactance so that $P_{qL} - P_{q\text{-}inverter} = P_{qC}$

4) Connecting a resistor that results in the power consumed by the RLC circuit equaling P_{inv}.

e) Connect the RLC load configured in step d) to the inverter by closing S1. Close S2 and turn the inverter on, making certain that the power output is as determined in step a).

(**Note**: The purpose of the procedure up to this point is to zero out the 60 Hz components of real and reactive power, or to zero out the 60 Hz component of current flow, at the utility disconnect switch. System resonances will typically generate harmonic currents in the test circuit. These harmonic currents will typically make it impossible to zero out an RMS measurement of power or current flow at the disconnect switch. Because of test equipment measurement error and some impact from harmonic currents, it is necessary to make small adjustments in the test circuit to achieve worst case islanding behavior. Step g) is performed to make these small adjustments.)

f) Open the utility-disconnect switch to initiate the test.

g) After each successful test, one parameter is adjusted by approximately 1.0% per test, within a total range of ±5% of the operating point determined in step d) above. The parameter that is adjusted may be load inductance, L, or load capacitance, C. After each adjustment, an island test is run and time to trip is recorded. If any of these tests results in islanding for longer than 2 seconds, the unit fails the test and the test sequence is considered complete.

This test should be performed with the following ratios of real load to inverter output, where both values are given as a percent of inverter full output rating:

Real Load	Inverter Output
25%	25%
50%	50%
100%	100%
125%	100%

Note that the final test, where load substantially exceeds generation, was included in the IEEE test procedure at a time when there was no experience with the non-islanding inverter. Testing since that time has shown that this is not a useful test, and it will probably be deleted from the IEEE test procedure when IEEE Std 929-2000 is revised in its next 5-year cycle.

Test Procedure Verification

Testing was performed to verify that the above procedure is adequate to separate non-islanding inverters from those that do not employ an adequate anti-islanding technique. Preliminary testing at Ascension Technology was performed by running the above tests with both the SFS and the SVS either activated or de-activated. Results are as follows:

SFS on, SVS on (Ten tests at each power level)

25%Load 25% Inverter
Min: 4 cycles, Max: 8 cycles, Avg 6 cycles to trip PASS

50% Load 50% Inverter
Min 5 cycles, Max: 14 cycles, Avg 8 cycles to trip PASS

100% Load 100% Inverter
Min 3 cycles, Max 7 cycles, Avg 6 cycles to trip PASS

125% Load, 100% Inverter
Min 2 cycles, Max 3 cycles, Avg 3 cycles to trip PASS

SFS off, SVS off (Ten tests at each power level)

25%Load 25% Inverter
Min: >1000 cycles, Max: >1000cycles, Avg >1000cycles to trip FAIL

50% Load 50% Inverter
Min >1000 cycles, Max: >1000 cycles, Avg >1000 cycles to trip FAIL

100% Load 100% Inverter
Min >1000 cycles, Max >1000 cycles, Avg >1000 cycles to trip FAIL

125% Load, 100% Inverter
Min 5 cycles, Max 7 cycles, Avg 6 cycles PASS

Note that the inverter without SFS and SVS passed the last test. This test was performed with a mismatch between load and generation that was adequate to cause the inverter to trip. Also note that the average trip time is 6 cycles, which indicates a frequency trip. (Recall that the first levels of voltage trips are allowed 120 cycles.) The mismatch in real power caused the island voltage to drop. The load demanded more power than the PV could supply. Changing the voltage, in this case dropping the voltage, affects the reactive power balance. This is because inductance is typically very nonlinear with voltage, but capacitance is more likely to be linear. In this case, the drop in voltage has the effect that the var_C now exceeds the var_L and the resonant frequency drops quickly, causing the inverter to trip on under-frequency.

Additional Testing of the Non-Islanding Inverter Test Procedure

In order to gain more confidence in the capability of the non-islanding inverter test procedure, testing was performed on a previous-generation anti-islanding technique, which had initially looked very promising. The test procedure described above was used, with the required ten tests at each load level. The testing was performed by Ascension Technology in their Boulder facility. The results of these tests are illustrated in Figures 12a through 12d.

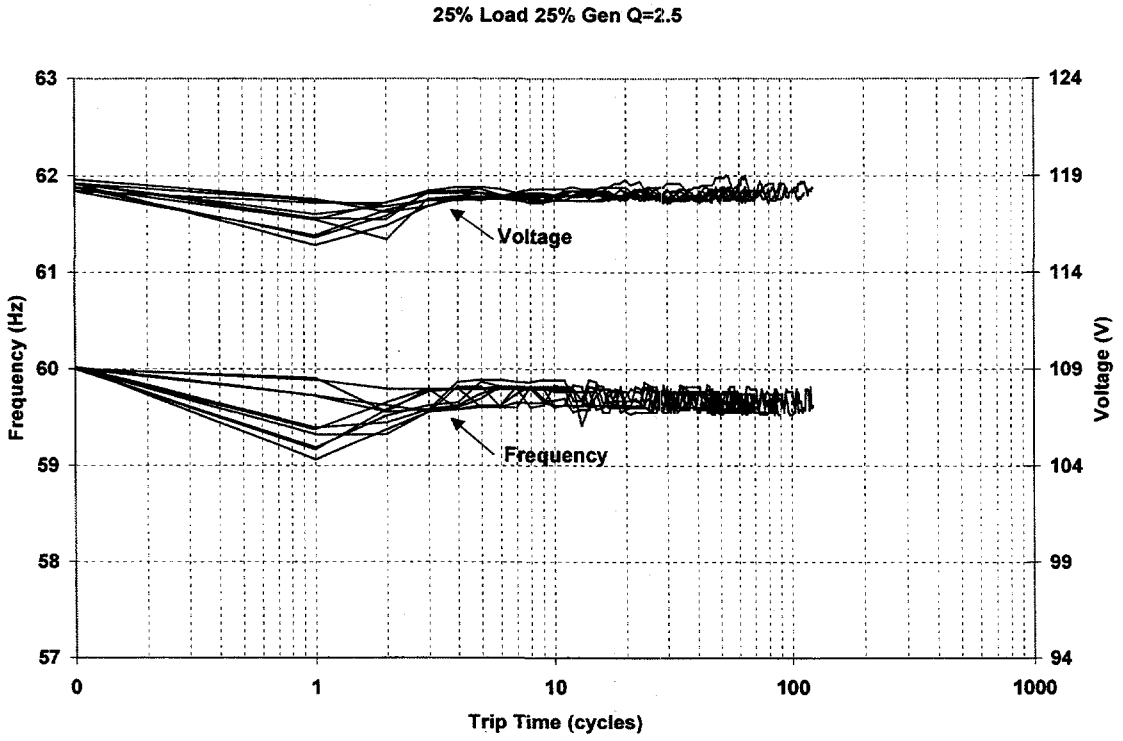

Figure 12a. Previous generation (non SFS/SVS) anti-islanding test - inverter voltage and frequency trajectories for 25% inverter output and matched load case. Trip points – 59.5Hz, 60.5Hz, 106V, 132V.

The inverter under test almost passed the first test scenario where the inverter is producing at 25% of its rated capacity, and the load equals the output, as shown in Figure 12a. Of the ten tests performed, only one exceeded the allowed 120 cycles to trip, and that test tripped in 123 cycles. The quickest trip time in this test series was 14 cycles.

The test sequences shown in Figures 12b and 12c reveal the shortcoming of this particular anti-islanding technique. Recalling that the maximum trip time for these test scenarios is 120 cycles, it is seen from these two figures that many of the tests went to 1000 cycles, where manual intervention terminated the test.

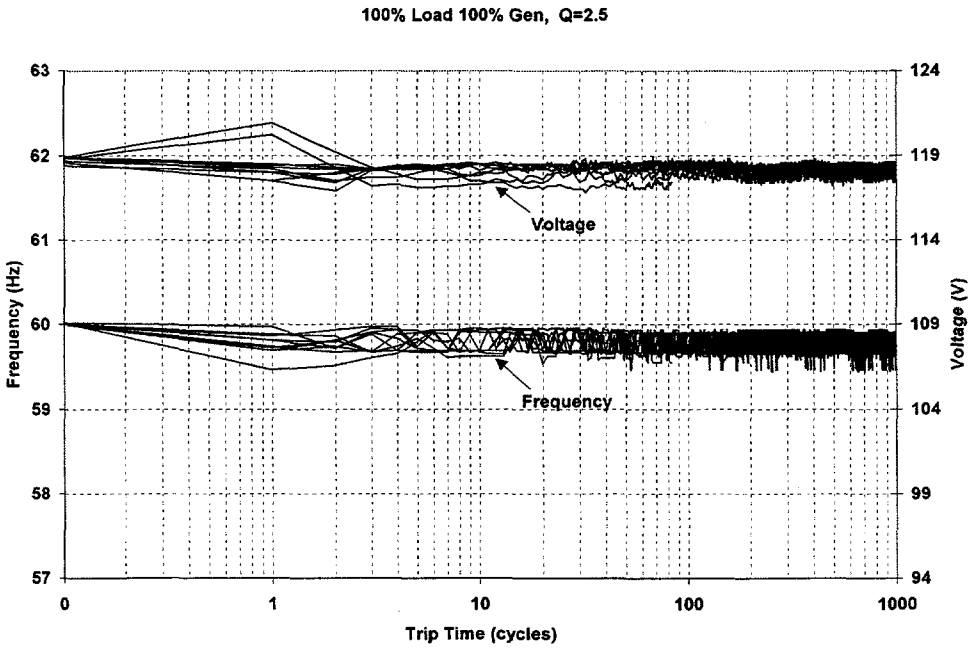

Figure 12b. Previous generation (non SFS/SVS) anti-islanding test - Non SFS/SVS inverter voltage and frequency trajectories for 50% inverter output and matched load case. Trip points – 59.5Hz, 60.5Hz, 106V, 132V.

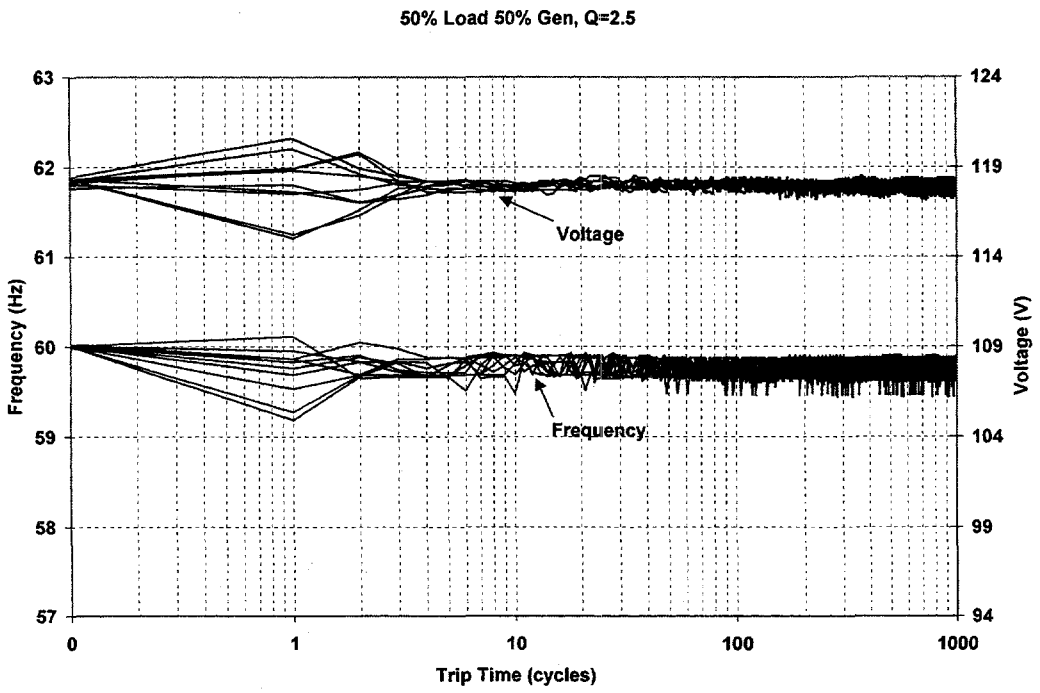

Figure 12c. Previous generation (non SFS/SVS) anti-islanding test - inverter voltage and frequency trajectories for 100% inverter output and matched load case. Trip points – 59.5Hz, 60.5Hz, 106V, 132V.

In this particular set of tests, the inverter under test easily passed the last test scenario, shown in 12d. In this test, the inverter is operating at full capacity, and is loaded at 125% of capacity. In each of the ten tests in this scenario, both voltage and frequency went beyond the initial trip points. Since frequency has a quicker trip time than voltage at the first trip point (six cycles for frequency, versus 120 cycles for voltage), all the tests illustrated in Figure 12d resulted in under-frequency trips.

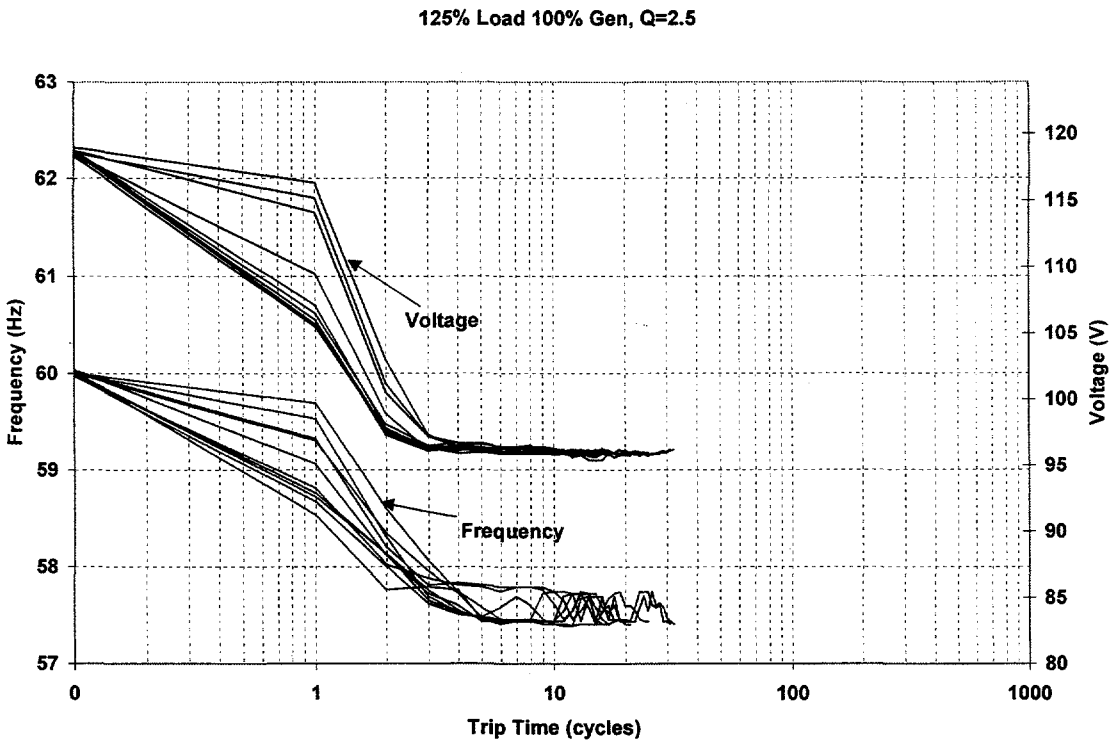

Figure 12d. Previous generation (non SFS/SVS) anti-islanding test - inverter voltage and frequency trajectories for 100% inverter output and 125% load case. Trip points – 59.5Hz, 60.5Hz, 106V, 132V.

As a final confirmation that the test procedure was sufficient to distinguish between non-islanding inverters and those that do not employ an adequate anti-islanding technique, several tests were conducted at Sandia with a variety of inverters. Some of these inverters were known to include the SFS/SVS technique, some were purported by their manufacturer to include an adequate anti-islanding technique, and the anti-islanding capabilities of some were unknown. These inverters were tested with a variety of different loads, including pure resistive (balanced with inverter output), motor loads (also balanced load and output), and the Non-Islanding Inverter test described above.

Many of the inverters were able to pass both the resistive and motor load test, but failed the Non-islanding Inverter test. These results supported use of the Non-islanding Inverter test to distinguish between non-islanding inverters and those that do not employ an adequate anti-islanding technique.

Multiple-Inverter Testing

Although multiple-inverter testing is not included in IEEE Std. 929-2000 or UL 1741, Sandia Laboratories will continue to perform multiple-inverter and single-inverter evaluations. The purpose of the tests is to continue to expand our knowledge base and to ensure that the single-inverter test is adequate for new inverter models.

10. Implementing SVS & SFS Islanding Protection in a Static Utility Interactive Inverter

Islanding protection is needed in utility interactive inverters when those inverters are outside the control of utility system operators and it is desired to have the inverter shut down when the rest of the utility shuts down as well. In a majority of situations, voltage and frequency operating limits are sufficient to prevent a persistent island of an inverter with a section of the grid that has been 'shut down'.

The method presented below uses those same voltage and frequency trip setpoints to decide when to shut down the inverter. No additional sensing mechanisms, such as sensing a phase shift in the voltage waveform, sensing changes in utility impedance, sensing changes in voltage harmonic content or rates of change of utility frequency are used by the inverter to decide when it is time to shut down.

In order to provide a complete explanation of how to implement islanding protection it is important to present some issues about how voltage and frequency are sensed, since the method of sensing can affect the islanding protection efficacy. In this section, references will be made to the actual implementation of this method in the SunSine® AC Module firmware.

Voltage Sensing

AC voltage is measured by sampling the ac voltage waveform 64 times per cycle, a sample rate of 3,840 samples per second. The timing of these samples is synchronized with the zero crossing of the ac voltage using software methods. A hardware phase lock loop is not used. A signal, representative of the ac voltage, is added to a fixed dc offset and enters an 8-bit a/d converter. The ac signal is added to a dc offset so that a unipolar 0.0 to 5.0-volt a/d converter can be used. The microprocessor computes the ac voltage based on the following formulas.

$$RMS^2 = DC^2 + V^2$$

$$V = sqrt(RMS^2 - DC^2)$$

The dc component is found by averaging the samples. The RMS^2 component is found by squaring the samples and averaging the results. The computation of V is done every ½ cycle, shortly after each zero crossing of the voltage waveform.

The need for an RMS-type computation of V may be questioned with the thought that the average of the rectified voltage should be sufficient. This is certainly

true for the purposes of SVS operation. However, we have used an RMS method because measurement inaccuracies can arise when averaging is used to compute ac voltage in the presence of changing voltage harmonic distortion.

The important point to note from this section is that ac voltage is measured and computed every ½ cycle.

Voltage Trip Points
During the testing of these methods the following trip set points were used.

$V > 144V$	Trip in ½ cycles
$V > 132V$	Trip in 100 cycles
$V < 104V$	Trip in 100 cycles
$V < 60V$	Trip in 5 cycles
$V < 30V$	Trip in ½ cycles

As can be seen, there are fast, medium, and slow speed trip times. Any number of trip settings and times to operate could be programmed into such a unit. The intent is to trip faster on the more severe voltage changes, but to ride through the less severe excursions, hence minimizing nuisance tripping of the unit during normal power system operation.

For any particular trip speed there is a counter, *Slow_count* for example. If the voltage exceeds the slow trip limit, the counter is incremented. If the voltage is in the satisfactory range, the counter is decremented. The counter is never allowed to 'roll over' or go past the limit for an 8 bit counter of 255; nor is the counter allowed to 'roll under', or decrement a step backwards from 0 to 255. This increment/decrement operation is performed once every ½ cycle. A counter larger than 8 bits could be used if desired times to operate exceeded 127 cycles.

When a counter exceeds its allowed number of steps, the inverter is shut down.

Frequency Sensing
The ac voltage signal is passed into a Zero Crossing Detect (ZCD) circuit. This circuit has filtering to filter out the effects of high frequency noise on the power line. The output of the circuit is a square wave logic signal that passes into the microprocessor. A 16-bit timer running at 5.0 MHz captures the rising and falling edges of the ZCD signal in the microprocessor. This timer rolls over every 13.1 milliseconds, enough time to measure the period of each ½ cycle to a resolution of 200 nanoseconds.

Once every cycle, the period measurement from the last two ½ cycles is combined to determine the period of the last cycle of ac voltage. The resulting

period measurement is then converted to a frequency and compared to the stored frequency trip limits once per full cycle.

Again, it is important to note that frequency, F, is measured over a full cycle of the ac voltage waveform.

Frequency Trip Limits
During the testing of these methods the following Frequency Trip set points were used.

F > 63.0Hz	Trip in 1 cycle
F > 60.5Hz	Trip in 5 cycles
F < 59.5Hz	Trip in 5 cycles
F < 57.0V	Trip in 1 cycle

The 1 cycle trips don't need a counter. The counter for the 5 cycle trips is implemented in the same manner as the counters for the voltage trips.

Voltage, Frequency and Current Regulation
These methods were implemented on an inverter that regulates output current. This output current regulation maintains a low distortion sinusoidal current waveform, regardless of utility voltage and frequency. The inverter relies on the utility to regulate system frequency and voltage. Utility interactive inverters are designed to be connected to the utility through relatively low impedance. This is important for the utility to be able to maintain voltage regulation. When that low impedance connection to the utility is broken, it is expected that utility interactive inverters will shut down.

Under most circumstances, when the utility is disconnected, voltage and/or frequency regulation is lost. Most commonly this is because there is more load than generation connected and system voltage collapses. There are, however, circumstances in which load and generation are balanced closely enough to maintain voltage and frequency regulation for a period of time. To the authors' knowledge, these circumstances have only been created in controlled experimental environments where researchers were attempting to create such circumstances. It is under these circumstances that the SVS and SFS methods operate to prevent islanding.

The SVS and SFS methods add positive feedback to the output current controls of the inverter such that system operation under these circumstances is destabilized. It is important not to make the positive feedback so strong that it destabilizes the utility grid. Fortunately, not much positive feedback is needed to destabilize even strong islands.

Sandia Voltage Shift (SVS)

The measurement of ac voltage, V_i, is the starting point of the SVS method, and is described above. The voltage measurement is first scaled to obtain high resolution between 90.0 to 154 volts.

$$Vps_i = (V_i - 90.0) \times 256 / 64.0$$

Vps_i is the power system voltage. This high-resolution measure of voltage is then digitally filtered with a simple IIR filter. The filtered result, designated Vf_i, is a measure of the average recent ac voltage. Vf_i does not fluctuate very much because it is a filtered parameter. The subscript $_i$ indicates data from the most recent ½ cycle. A subscript $_{i-1}$ is data from the ½ cycle before that.

$$Vf_i = (1-kv) \times Vf_{i-1} + kv \times Vps_i$$

The parameter kv determines the time-constant of the IIR filter, and in our implementation was 1/256. This filter computation is made every ½ cycle.

An error signal, Ev_i, is computed as the difference between the most recent measurement of ac voltage and the filtered ac voltage.

$$Ev_i = Vps_i - Vf_i$$

If Ev_i is positive, that means that the most recent voltage is greater than the average voltage, that is, voltage is rising. If Ev_i is negative, voltage is dropping. During normal operation of the power system, there will be normal cycle by cycle fluctuations in Vps_i, thus creating fluctuations in Ev_i. As long as the grid is connected, these fluctuations are small.

When the voltage appears to be rising, the output current control is increased. When the voltage is dropping, the output current control is decreased. As long as the grid is connected, operation of the inverter will not affect system voltage. Thus, even though the output current is fluctuating a small amount, it will not sustain a trend. When the grid is no longer connected, any fluctuation in voltage will cause the inverter to react. Since the utility is no longer maintaining system voltage, the inverter will continue to push voltage either up or down until a voltage trip shuts down the inverter.

One of the benefits of this method is that multiple inverters on the system will support each other in destabilizing the island. If system voltage at one inverter is rising, it is likely that it is also rising at other inverters on the island. Island operation with inverters controlled in this manner is inherently unstable.

Output Current Control

The control of the magnitude of the output current of the inverter is done depending upon the application. In photovoltaic applications, output current is increased or decreased to track the maximum power of the photovoltaic power source. This maximum power tracking has a slow time constant compared with the cycle by cycle variations mentioned above. For the purpose of destabilizing an island, one may assume that the maximum power tracking output current magnitude command signal, designated Pmpt, is constant during operation of the islanding protection method. In the SunSine® 300 inverter, the value of Pmpt varies from about 0 to 200, and is stored in an 8 bit register. For purposes of these discussions, a value of Pmpt of 200 represents 100% inverter output. Ev_i ranges from -127 to +127 and represents an error voltage of -32 to + 32 volts ac.

The command that directly controls output current magnitude, Pcmd, is a function of both Pmpt and Ev_i as follows.

$$Pcmd_i = Pmpt_i + Ev_i / 12 + Ev_i \, x \, (Pmpt_i / 200) \, x \;\; 0.57$$

When Ev_i is zero, $Pcmd_i = Pmpt_i$. As the magnitude of Ev_i increases we know that the voltage is moving either up or down and will eventually reach one of the trip limits. In other words, high gain is needed to destabilize the system.

Sandia Frequency Shift

The SFS method is similar in principle to the SVS method. The SFS method acts to destabilize system frequency.

The measurement of frequency, F_i, is the starting point of the SFS method, and is as described above for voltage measurement. The frequency measurements are digitally filtered with a simple IIR filter. The filtered result, call it Ff_i, is a measure of the average recent ac frequency. Ff_i does not fluctuate very much because it is a filtered parameter. The subscript $_i$ indicates data from the most recent ½ cycle. A subscript $_{i-1}$ is data from the ½ cycle before that.

$$Ff_i = (1\text{-}kf) \, x \, Ff_{i-1} + kf \, x \, F_i$$

The parameter kf determines the time-constant of the IIR filter, and in our implementation was 1/256.

An error signal, Ef_i, is computed as the difference between the most recent measurement of frequency and the filtered frequency.

$$Ef_i = F_i - Ff_i$$

If Ef_i is positive, that means that the most recent frequency is greater than the average frequency, that is, frequency is rising. If Ef_i is negative, frequency is dropping. During normal operation of the power system, there will be normal cycle by cycle fluctuations in F_i, thus creating fluctuations in Ef_i. As long as the grid is connected, these fluctuations are *very* small.

When the frequency appears to be rising, the output current control frequency is increased. When the frequency is dropping, the output current control frequency is decreased. As long as the grid is connected, operation of the inverter will not affect system frequency, so even though the output current is fluctuating a small amount, it will not sustain a trend. When the grid is no longer connected, any fluctuation in frequency will cause the inverter to react. Since the utility is no longer maintaining system frequency, the inverter will continue to push frequency either up or down until a frequency trip shuts down the inverter.

One of the benefits of this method is that multiple inverters on the system will support each other in destabilizing the island. If system frequency at one inverter is rising, it is also rising at other inverters on the island. Island operation with inverters controlled in this manner is inherently unstable.

How can Inverter Frequency be Different than Grid Frequency?
A natural question to ask at this point is 'How can the inverter frequency be different than the grid frequency?' At every zero crossing of the voltage, the inverter time base is reset to zero. When the inverter current output frequency is higher than the grid frequency, the output current will finish forming a ½-sine wave before the next voltage zero crossing occurs, resulting in output current remaining at zero until the voltage zero crossing occurs. At this point output current resumes at the beginning of another ½ cycle of sine wave current output. If the inverter current output frequency is lower than the grid frequency, then the voltage zero crossings will occur before the current waveform finishes a full ½ cycle. At that point the output current waveform is reset to zero, switches polarity, and starts at the beginning of another ½-sine wave cycle.

The effect of such operation in an island is that the inverter quickly causes island frequency to move outside the trip limits. When the inverter is connected to the utility, these small fluctuations do not affect system frequency.

Inverter Frequency Control
The sine wave frequency, Finv, of the output current waveform is determined based upon the grid frequency, Fgrid, and the frequency error Ef_i (also called frequency deviation).

$$Finv = Fgrid + fn2(Ef_i)$$

The function, fn2(), is shown in the chart below. The steps seen in the graph are due to digitization and resolution effects in the digital implementation

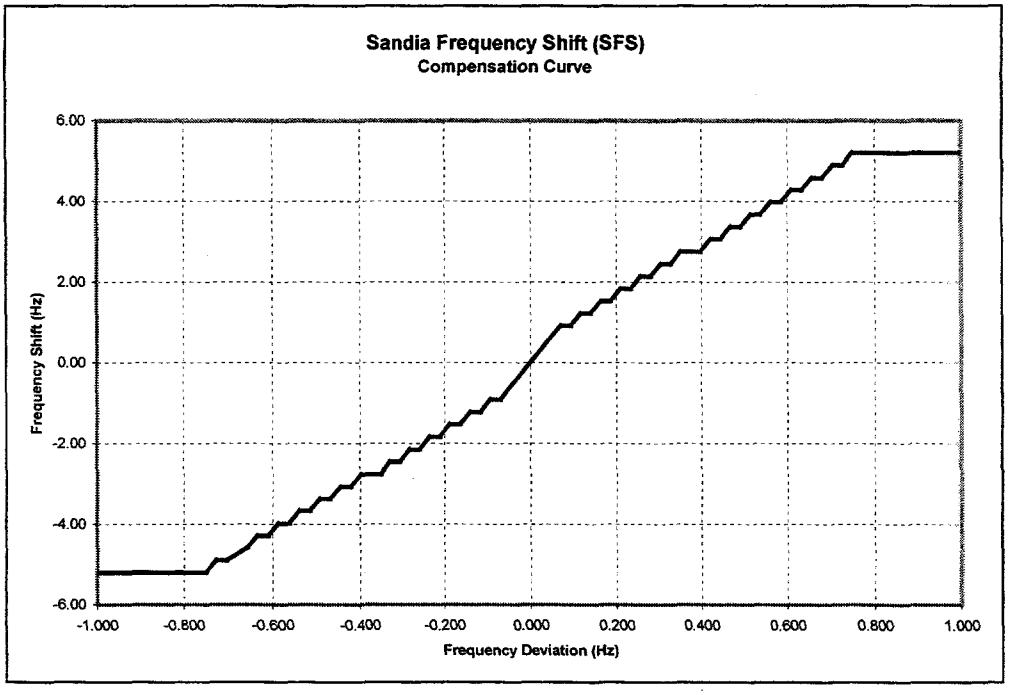

Figure 13. SFS compensation curve, showing the relation between measured frequency deviation and the shift that SFS will apply.

Fast Response, It is Critical !

The ability of the SVS & SFS methods to react quickly in shutting down an island is partly due to fast and accurate measurement and control. Accurate measures of voltage and frequency are made on the order of 1 cycle. Computation of the output current controls is made during the next ½ cycle before being applied to the output current waveform. This implies an average delay time of about 1 cycle in the destabilizing control loop.

If measurement of voltage were taken over multiple cycles, then measured fluctuations in voltage would be much smaller. Trip times would increase significantly in such a design. This has implications in how the inverter measures ac voltage. For example, it would probably not work to measure ac voltage through a circuit with a response time on the order of 100 to 1000 milliseconds. Circuits such as RCD filters or RMS/DC converters may cause problems here because of the long response time. This was not investigated in the project reported on here.

A Variable-Power-Factor-Inverter Consideration

PV inverters can be designed to operate at power factors other than unity, and an interconnecting utility may request that an inverter for a large PV system operate at some non-unity power factor. However, the IEEE and UL standards for inverters rated 10kW or less requires that they operate at greater than .85 power factor, and most are designed to operate at unity power factor. The SVS and SFS methods could work with a variable power factor inverter as long as the power factor of the inverter changes slowly enough that it is nearly constant over the time period that anti-islanding controls need to operate. We would suggest an order of magnitude difference in response times between the power factor response and the anti-islanding response to provide a comfortable degree of margin. Thus the power factor tracking feature of such an inverter should have a response time no faster than 20 seconds. If a power-factor-tracking inverter were able to change power factor to match the load, and did so with a response time faster than 2 seconds, it is quite possible that such operation would interfere with SVS and SFS operation. However, this would depend very much on the details of exactly how such power factor correction operation is implemented.

Digital or Analog Implementation?

The implementation tested in this project was a digital implementation. It might be possible to build a successful analog implementation, but it would probably be very difficult. The anti-islanding controls were integrated with the other inverter controls in the same microcontroller used to control the inverter. This microcontroller costs about $5 in production quantities. No additional hardware was needed in the inverter design beyond that already needed for inverter operation.

11. Conclusions

Implementation of the combination of SVS and SFS has proven to be sufficient to achieve a Non-islanding Inverter. SVS and SFS are likely to work with high penetrations of distributed generators. They do not require synchronization between inverters to operate. Other active methods that perturb the utility and measure a coincident change in voltage or frequency will not work in high penetrations unless the perturbations are synchronized. Such synchronized perturbations can be undesirable for the interconnected utility.

The SVS and SFS methods have been fairly easy to implement. The only modifications necessary to implement them in the inverters used for testing were changes in firmware. No changes to the hardware were required. This may not be true in general for all inverter designs.

Results presented here are far superior to results of other anti-islanding tests conducted over the last 18 months both at Ascension Technology and at Sandia National Laboratories. This work was supported by a consensus of U.S. inverter manufacturers. Although not guaranteed, it is likely that the results of this work will move toward a *defacto* standard for anti-islanding in the United States. It is hoped that by sharing these results, similar methods will be considered in the international community.

A significant product of this work was the establishment of a test procedure that can be used to distinguish between inverters that have satisfactory anti-islanding techniques and those that do not.

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