Development of a Digital Array Radar (DAR)

B. Cantrell & J. de Graaf, *Naval Research Laboratory*
F. Willwerth & G. Meurer, *MIT Lincoln Laboratories*
L. Leibowitz, SFA, *Advanced Technology Division*
C. Parris & R. Stapleton, *Naval Surface Warfare Center*

ABSTRACT

Twenty-first century littoral and open-sea missions present US Navy (USN) shipboard-radar systems with the challenge of detecting small targets in severe clutter and against multiple sources of interference. In Fiscal Year 2000 (FY00), the Office of Naval Research (ONR) sponsored a program to develop an active array radar that includes a digital beamforming (DBF) architecture. The DBF radar system has the potential for improved time-energy management, improved signal-to-clutter (S/C) ratios, improved reliability and reduced life-cycle costs. This paper summarizes the latest developments of the program during FY00.

PROGRAM BACKGROUND

In FY00, ONR sponsored the Digital Array Radar (DAR) program, to develop state-of-the-art technologies for insertion into an active-array radar system with a full DBF architecture. Three organizations have been involved: MIT/LL, NRL/DC and NSWC/DD. This paper presents the work performed in this program during FY00 and provides some hardware test results from each organization.

USN RADAR CHALLENGES IN THE 21ST CENTURY

USN operations in both littoral and open-sea areas continued to grow in complexity during the last decade. Land clutter, multiple jammers, and commercial wireless links across the globe present increasing challenges to current radar systems onboard USN surface combatants. Twenty-first century USN surface combatants will require surveillance radars with high-clutter rejection, rapid beam steering, increased resistance to interference, and low life-cycle costs. Various phased-array radar architectures were considered including active-array systems using analog beamforming, which represents the current state-of-the-art for tactically deployed radars [1]. However, the spurious-free dynamic range of today's analog-to-digital converters (ADCs), with typical instantaneous dynamic ranges of 70 dB, limits the performance of active-array radar systems based on analog beamforming. The DBF architecture has the potential to increase system dynamic range by another 30 dB, while also solving many of the performance issues encountered by legacy and current radars. A DBF radar system can provide enhanced S/C ratios, fast adaptive-nulling performance, and more effective time-energy management while lowering costs due to the insertion of available commercial technologies [2].

OBJECTIVES OF THE DAR PROGRAM

The primary objective of the DAR program is to leverage and evaluate commercial technologies for a DBF radar architecture for application to USN radars at L-, S-, and X-band frequencies. The DAR prototype will exploit communications technologies from the wireless and fiber-optic (FO) sectors, and the field-programmable-gate-array (FPGA) and high-speed VME processor markets [3]. To control development costs, the DAR prototype is a 96-element system at L-band with the radar parameters of Table 1, on next page. With the exception of S/C performance, these parameters apply to a single T/R module consisting of microwave and digital portions. As described in the next section, the microwave portion will consist mainly of mixers, filters, amplifiers, and a driver amplifier followed by a cascade of two power-amplifier stages. The digital portion will consist of core technologies, such as an FPGA, bit-serializers and de-serializers, and rows of transmit digital-to-analog converters and receiver ADCs.

An operating frequency at L-band was chosen because of the Navy's need for an L-band volume surveillance radar, and because of the availability and low-cost of commercial products covering this frequency band. The remaining

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Authors' Current Addresses:
B. Cantrell and J. De Graaf, Naval Research Laboratory, Washington, DC 20375, USA; F. Willwerth and G. Meurer, MIT Lincoln Laboratories, Lexington, MA 02420, USA; L. Leibowitz, SFA, Advanced Technology Division, Largo, MD 20774, USA; C. Parris and R. Stapleton, Naval Surface Warfare Center, Dahlgren, VA 22448, USA.

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Table 1. DAR Prototype Radar Parameters

Description	Specification Min	Nominal	Max	Status
Operating Frequency (MHz)	1215		1400	✓
Peak Power (kW)	15	20		Pending
Duty (%)			10	✓
PRF (kHz)	0.3	1	10	✓
Pulse Width (μs)	1		150	✓
Active Elements (#)		100		✓
Instantaneous Bandwidth (kHz)			815	✓
Linear FM		Yes		✓
Base-Clock Phase				
Noise Floor (CW) (dBc/Hz)		-160		✓
S/C Improvement (dB)		85	100	Pending

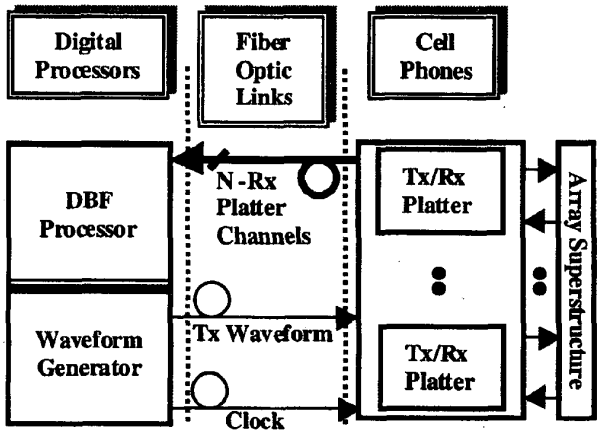


Fig. 1. Basic DAR architecture

objectives are component-performance and demonstration-of-concept related. The component-performance objectives are to evaluate digital-commercial electronics such as FPGAs and bit-serializers and de-serializers and to determine the feasibility in their use in the DAR concept. The last objective, and one that will provide the final test for feasibility, is the demonstration of the DAR concept in the field. There are three focus areas under the DAR concept for demonstration purposes: performance improvement through digitalization on a per-element basis, implementation of DBF (adaptive nulling and rapid main-beam steering), and application of low-cost commercial products and practices.

DAR SYSTEM DESIGN AND TEST RESULTS

Figure 1 shows a simple diagram of the DAR concept. Three subsystems are illustrated to show the basic building blocks of DAR: T/R platter, DBF signal processor, and waveform generator. The DAR prototype leverages a mix of commercially available analog and digital components including high-speed DSPs in the form of FPGAs and digital fiber optic links. Only a few components, such as the power amplifier and the radiating element had to be developed internally.

Figure 2, on next page, shows the DAR system as configured for an experimental prototype. In FY00, the DAR team divided the DAR-prototype development responsibilities in terms of subsystems and interfaces. MIT/LL accepted the responsibility for developing the microwave section including the array superstructure, microwave T/R (MTR) module and integration for a field demonstration. Table 2, on next page, shows the interfaces for Figure 2.

NRL/DC accepted the responsibility for the digital T/R module including FO links, digital receiver design, timing/control implemented in FPGAs, and software development for the T/R-platter controller. NSWC/DD tasks were to design and develop the DBF subsystem, perform test loops, verify adaptive algorithms, and install the final hardware into the prototype.

The T/R platter is a group of eight microwave-digital T/R modules (interface 2). Twelve platters were planned for the prototype, yielding a total of 96 active elements. By way of FO links (interface 3), the T/R platter receives baseband transmit data and control words from a remote T/R-platter controller. The platter controller accepts commands, such as timing gates and waveform parameters, from the radar controller via a reflective memory and scramnet boards (interfaces 5C and 6, respectively). Reflective memory is a ring-based, high-speed networked memory shared among multiple computer systems with no software overhead. From the T/R-platter controller, Q parallel data and I are brought over to the DBF subsystem (interface 4B). For the prototype, processed beam data is recorded and further processed offline. Interface 7 is the

Table 2. DAR Prototype System Interfaces

Interface	Description
1	Array superstructure backend
2	DTR to MTR inside T/R Platter
3A, B & C	Fiber-platter channel, clock and waveform
4A & B	Timing and I/Q data
5A, B & C	FPDP, Number of Beams and reflective memory
6	Ethernet router and cable lines
7	Input ac power port
8	Control input for antenna tuning (impedance)

control line for tuning the element impedance for best match. A detailed discussion of array-element tuning will be covered in a forthcoming MIT/LL report.

Array Antenna and Microwave T/R Module

The array antenna is a square, axially symmetric, planar construction. As shown in Figure 3, the array face is populated with 224 radiating elements. In the prototype, an active T/R module feeds into one radiating element out of the 96 elements allocated for the array. The remaining elements are terminated, thus improving the antenna response of the relatively small array. The elements are circular patches over a dielectric substrate. The patches are shorted at the center and offset-fed. Another characteristic of the circular patches is resonant frequency response, which is modeled as roots of spherical Bessel functions. The patch reflects the harmonics of the radar's output signal to provide improved electromagnetic compatibility.

As shown in Figure 4, on next page, the MTR module employs a two-stage super-heterodyne system and shares filter paths between the exciter and receiver chains. The interface to

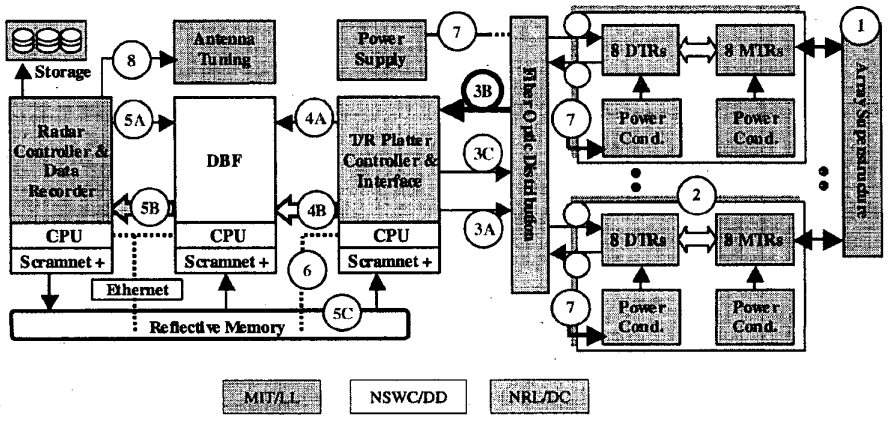


Fig. 2. DAR prototype configuration and team responsibility

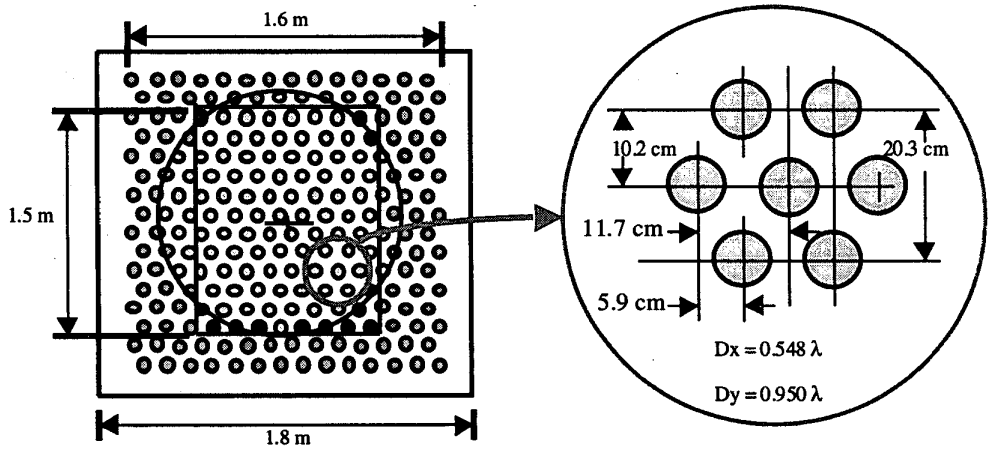


Fig. 3. Array antenna configuration and inter-element spacing diagram

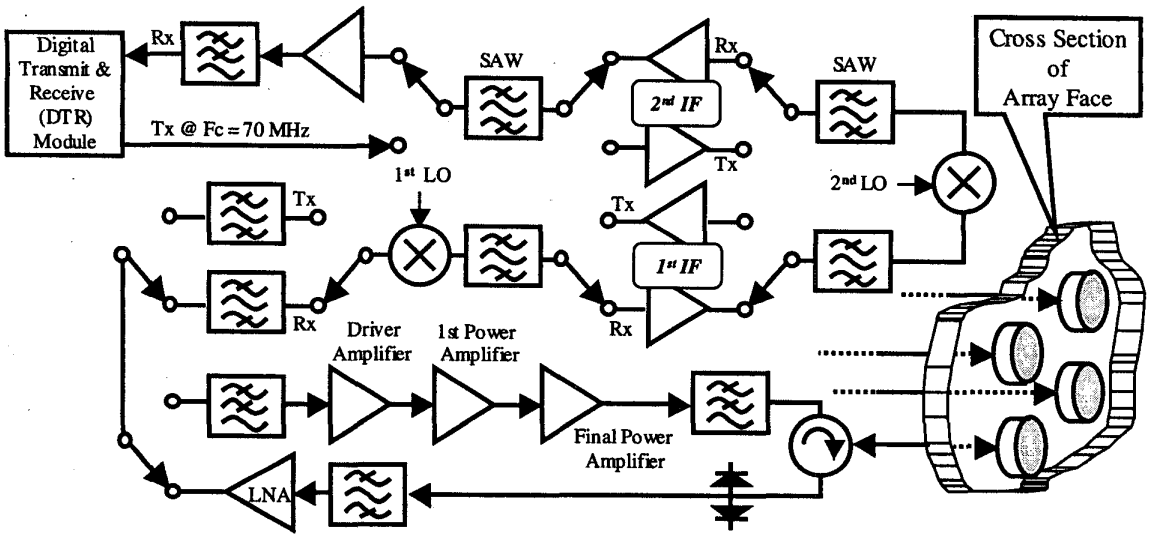


Fig. 4. A single microwave T/R module and circular radiating elements for the array face

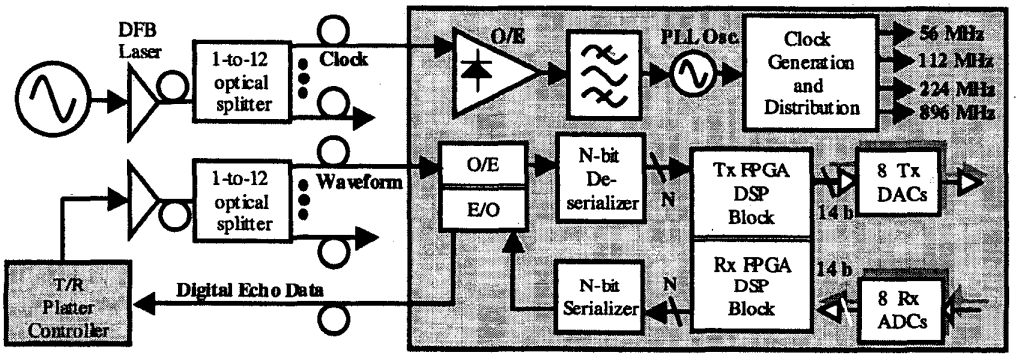


Fig. 5. Digital T/R module (DTR) with respect to a "below-deck" area of waveform/clock optical generation

the T/R module from the digital section is a 70 MHz intermediate frequency (IF) for both transmit and receive. Figure 6A shows the pass-band response of the receiver's IF output stage. The filter response is derived from a SAW filter at the last IF. A SAW filter is necessary to minimize aliasing after the ADC and to reject other spurious products close to the IF. The SAW bandwidth is 1 MHz, which allows 1 MHz chirp waveforms to be digitized by the ADC. As shown in Figure 5, two SAW filters in the second IF of the MTR module are required for improving the rejection of spurs and harmonics.

Digital T/R (DTR) Module and FO Link

The DTR is more complex in terms of how the baseband digital data is routed, processed, and converted to analog and digital signals. In a ship-based installation, the T/R-platter controller (see Figure 2), and the DBF subsystem are installed below deck, which is at least 30 m from the array face, as shown in Figure 5. Transmit data is generated at the T/R-platter controller and converted to a serial bit stream. This data stream is optically converted in single mode at a standard wavelength of 1300 nm (interface 3A). Although not shown in Figure 4, commercial optical tranceivers such as Agilent G-link and Method Electronic products and those of other respective vendors, are being considered for optical-to-electrical (O/E) and electrical-to-optical (E/O) conversions in every DTR module.

The optical-link loss budget includes optical connectors, adaptors from one type of connector to another, other passive components, detector sensitivity, and fiber cable loss, which is very small (< 0.5 dB/Km) for short fiber-cable lengths. To overcome the split loss in a 1-to-12 optical splitter and satisfy the loss budget requires a laser with greater output power than conventional lasers. Two below-deck lasers are required: one for the base clock and the other for the baseband waveform generation. Two distributed feedback (DFB) digital lasers from Lucent Technologies (part number: D2304G) were experimented with to generate higher optical powers in the uplink of digital waveform data and the base clock.

Depending on the type of optical conversion in the T/R platter, an O/E PIN converter in one T/R platter converts the

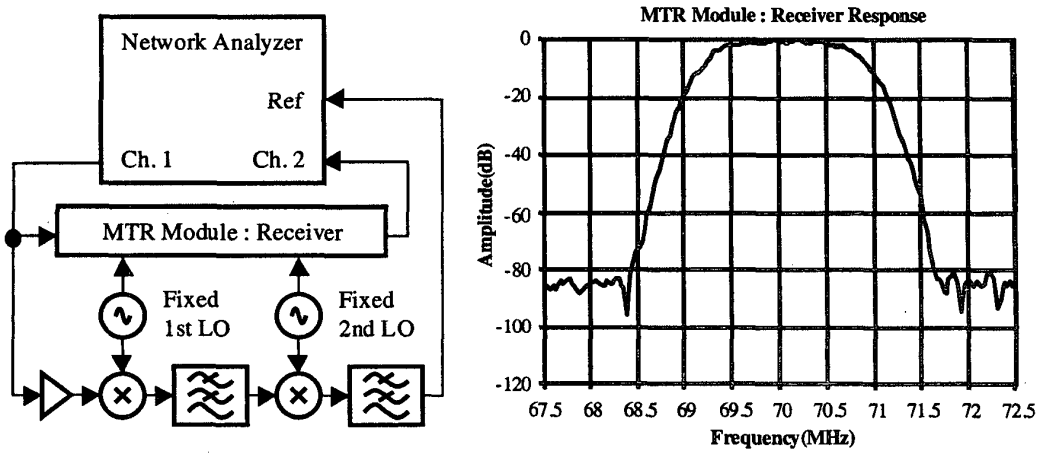


Fig. 6A. Last IF receiver bandwidth characterization

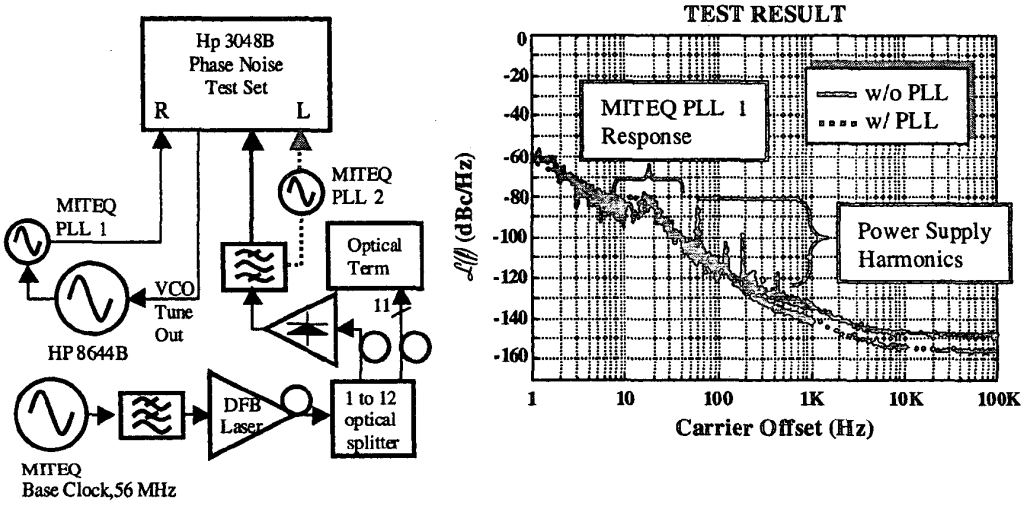
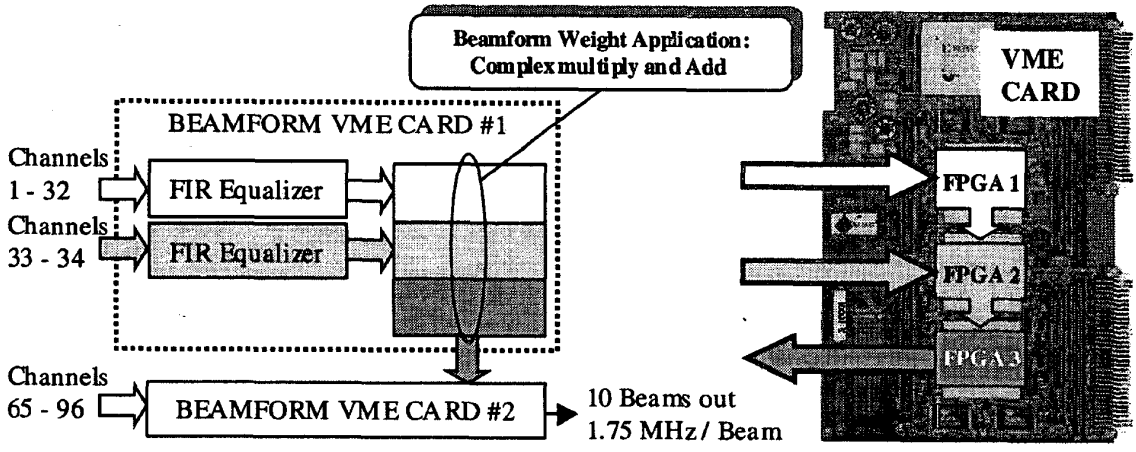


Fig. 6B. Phase-noise comparison of the base clock and FO uplink: with and without PLL oscillator



optical data stream into a PECL-level signal. An Agilent HFBR-53D5 Fabry-Perot laser and PIN diode optical transceiver were initially selected to demonstrate the feasibility of commercial technologies and keep the cost low.

The 56 MHz base clock is generated in an ultra low-noise crystal oscillator (Miteq P/N: XTO-05-56-G-15P). The 56 MHz oscillator is low-pass filtered and optically converted before splitting into 12 equal optical signals. The optically divided signal is then photo-detected by an Agilent HFBR-53D5 optical transceiver in each T/R platter. As shown in Figure 5, the electrical signal, after an O/E conversion, is band-pass filtered and phase locked to a low-noise, phase-lock loop (PLL) oscillator at 56 MHz. The PLL oscillator re-establishes the base clock noise floor, which has been degraded by the E/O-O/E conversions and below-deck DFB laser-noise, to a floor established by the PLL oscillator (Miteq P/N: PLD-56-56-15P-SP) at the same frequency of 56 MHz.

To demonstrate the use of the PLL oscillator, a phase-noise comparison was made between a PLL oscillator at 56 MHz and an E/O-to-O/E optical link with a 1-to-12 optical splitter, as shown in Figure 6B, on previous page. Figure 5 shows the base clock, photo detected and filtered, before being driven into a frequency multiplier. The frequency multiplier generates four fixed frequencies: X2, X4 and X16. The 2nd LO is generated at the X4 port at a fixed frequency of 224 MHz. As predicted, after frequency multiplication by four, the noise floor is raised by 12 dB. At the time this paper was being written, no additional analysis had been performed to determine the noise impact of the 2nd LO on the performance of the microwave TR module.

Not shown in Figure 5, the 1st LO is generated from a serial bit stream that represents a delta-sigma (Δ-Σ encoded sequence. The Δ-Σ sequence was created offline using a MATLAB simulation, called delsig, which is available at the MathWorks web site. The analysis and performance of 1st LO Δ–Σ generation will be covered in a separate report.

FPGA Analysis and Design for a DBF

While digital processing technology based on traditional RISC or DSP technologies is suitable for small DBF implementations, larger scale systems require either custom Application-Specific-Integrated-Circuits (ASICs) or FPGA implementations to meet the real-time data-rate demands. The use of FPGAs gives the advantages of software design with the efficiency of dedicated digital hardware [4]. The DBF employs a COTS-based VME product equipped with two Xilinx Vertix chips: XCV2000E-8. The VME board allows up to four FO I/O channels (Agilent G-Link) and an external clock input per FPGA. The VME board will allow up to four FO I/O channels (Agilent G-Link) and an external clock input. A single board supports the beamforming requirements for eight T/R platters, which means that two cards will be needed for the 96-element test array.

Equalization is required for precise amplitude and phase matching between elements (channels) and dominates the computational load in the DBF subsystem. Data arrives from the T/R platter as eight-channel (one channel per radiating element) multiplexed I and Q. I signals and Q are fed into a 20-tap, 16-bit complex FIR for equalization. If there is no requirement to change the equalizer coefficients in real-time (this is still under investigation), then it is possible to use the distributed arithmetic core by Xilinx, which consumes 229 slices for a single real 16-bit, 20-tap FIR. The configurable logic block (CLB) is a functional element for constructing logic circuits. One Virtex CLB has two vertical slices, which contain two logic cells. A logic cell is the basic building block of the CLB, which includes a function generator with four inputs, carry logic, and a storage element. Approximately 1200 slices for the four real FIRs and additional adders are required to make a complex FIR. The bit-serial implementation requires 16-cycles per sample so required clock speed is only 56 MHz.

A basic parallel-multiplier implementation requires approximately 10,000 slices, which is two-thirds the usable slices on an XCV2000E. To optimize the available resources in the FPGA, the array of complex multipliers in the beamforming weight application will run at double the incoming data rate. Figure 6C, on previous page, shows the basic concept of the DBF subsystem.

SUMMARY

The USN in the 21st century requires a DBF radar with the capability of fully adapting to the operational demands in open and littoral areas. ONR addressed this requirement and sponsored a program to develop a DBF radar prototype for experimental purposes. Three organizations were involved: MIT/LL, NRL/DC and NSWC/DD. Some test results from the DAR program in FY00 were presented and discussed. Future plans for the DAR program are currently being discussed.

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