Development of Cascaded Multilevel Inverter Based Active Power Filter With Reduced Transformers

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Abstract—**Active power filter is a power electronic converter used for improving the quality of supply by eliminating the effect of harmonics due to non-linear loads. This paper recommends a concept for shunt active power filter (SAPF) using a single power source fed to a cascaded multilevel inverter (CMI) with 3-φ transformers. Apart from traditional transformer based topologies, the required number of transformers are substantially reduced, resulting in less space requirement, which leads to low cost and simple control system. The proposed CMI based SAPF has a capacity to compensate for contaminated load with high harmonic and a low power factor. The effective $i_d - i_q$ theory is used to calculate compensation currents. DC link voltage regulator analyzed through delay time and controller gain. The tasks of the controller in the SAPF can perform all necessary actions for correct operation in SAPF. A wide range of computer simulation results demonstrated and validated the results with the prototype experimental setup.**

Index Terms—**Cascaded multilevel inverter, $i_d - i_q$ theory, shunt active power filter, three-phase transformers.**

I. INTRODUCTION

THE power system is perceiving problem because of harmonics. This is because of non-linear loads, namely uninterruptable power supply (UPS) systems, switched mode power supply units (SMPS), variable speed drives, etc. Harmonics not only surge the losses but also introduce unwanted disturbance in the communication system, increase the stresses in voltage and current, etc. This has inspired the introduction of SAPF for improving power quality. It has been demonstrated that the greatest advantages of the active filters are to eliminate harmonics as well as asymmetric current compensation due to the existence of non-linear loads and

unbalanced loads. Owing to the outstanding research in the area of power electronic components used in active filters and forced commutation techniques has been comprehensively studied in the last two years [1]. Nevertheless, there are still some issues for further research and development. One such aspect is power quality. Present work completely devotes to this issue. In general, for SAPF constructions, three major areas are to be considered. First one is the estimation of the compensating currents, secondly power converter topologies, and finally, modulation techniques that track the reference currents.

The present work deals with topology issues. In this domain, several authors have already developed SAPFs by using conventional two-level converters [2], [3], but in recent years multilevel inverter (MLI) topology is a hot topic for researchers. MLI concepts based on using several voltage levels to achieve power conversion [4]. Merits of this particular approach comprise good electromagnetic compatibility, improved power quality, high voltage capability, and less switching losses. H-bridge in series is the first familiarized archetype named as cascaded H-bridge (CHB) multilevel inverter. Later, a different multilevel inverter which employs a group of series capacitors to divide the DC bus voltage is the diode-clamped inverter [5]. Afterward, the capacitor clamped [6] design introduced. In order to clamp the voltage levels, this archetype uses the floating capacitors in place of series capacitors. The P2 multilevel topology introduced after a few years of capacitor clamped [7]. Amongst CHB is superior inverter because of its modularized structure and less components requirement [8]–[10].

Further, series linking of multiple of 1-φ inverters fabricate CHB multilevel inverters [11]. This construction has a capacity to improve the individual low voltage of the individual devices connected in series. Classically, it is required to join several inverters in series to attain the required voltage. Every single inverter module realized as identical circuit design, control management. So, the CHB inverter possesses a high modularity degree [12]–[14]. Thus it is easy to replace the faulty modules quickly. Furthermore, with this advanced control approach, it is very much simple to avoid faulty unit without disturbing the power supply to the load terminals, thereby providing a continuous availability [15], [16]. Several cascaded multilevel inverter topologies have been designed and adopted for several applications [17]–[21].

On the other hand, architectures shown in Fig. 1(a) and (b) are prominent topologies and extensively used for active filters,
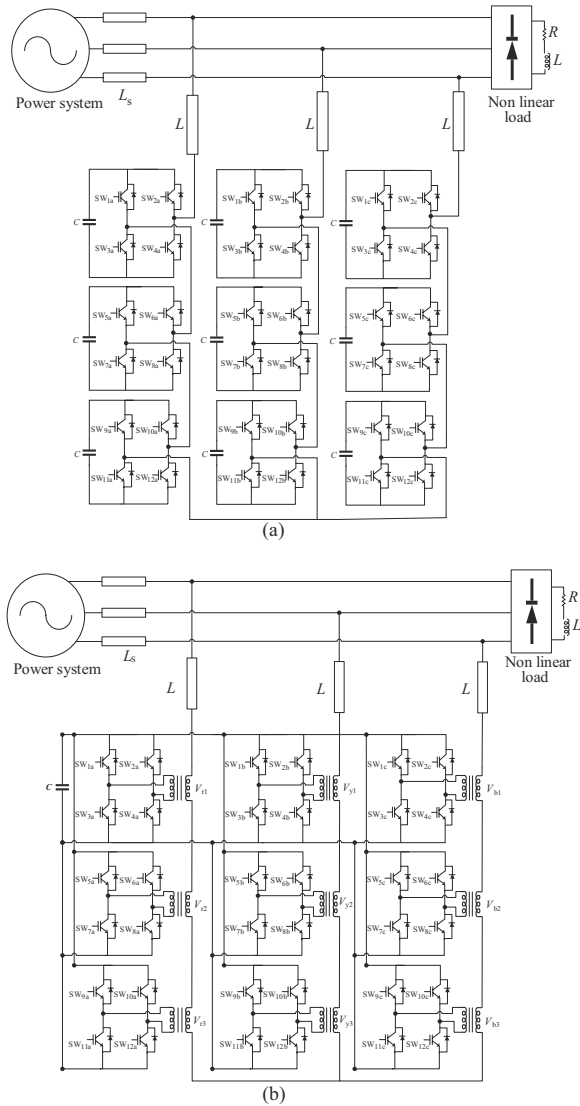
Fig. 1. (a) CMI with separate DC sources interconnected to a power network. (b) CMI with boost type transformers interconnected to a power network.

grid connected systems, flexible alternative systems [22]–[24]. CMI with separate DC-link capacitors interconnected to SAPF shown in Fig. 1(a). It consists of series power conversion cells, the voltage and power level easily scaled. Further, Fig. 1(b) demonstrates the cascaded multilevel inverter with single-phase transformers by using a single DC-link capacitor to SAPF. In the present scenario, these archetypes highly preferred because they efficiently coupled to high-power transmission systems. Further, because of the transformer presence, high-quality waveforms are obtained on the secondary side. Unfortunately, both cascaded multilevel inverters have a particular drawback. One specific drawback for first architecture is the use of isolated voltage sources for each H-bridge module [25]. For other architecture, CMI with boost type, which employs separate transformer for each module increases not only the cost but also the size. In spite of these configurations, we suggested a new topology for CHB inverter uses 3-phase transformers with a single DC power supply. This not only

reduces the size but also increases the reliability of the system. Interesting features of the proposed architecture are: it uses one power source with reduced transformers and most importantly because of 3-phase transformers, the converter produces excellent voltage waveforms and ideal currents.

In this paper, more details of active filter construction with control strategy and proposed CHB multilevel inverter are presented. The proposed configuration is useful for providing thirteen different voltage levels with just six H-bridge cells, and thus drastically reduces switching ripple in compensation currents. The proposed new topology developed in MATLAB/ Simulink. Diode bridge rectifiers and inverters are taken from the power sim block set. Further, a prototype experiment performed to validate the proposed SAPF. Herein, SAPF operation studied by feeding contaminated 3-φ bridge rectifier with inductive load.

To explore the working features of the proposed CMI based SAPF, this paper concentrates on the following aspects:

1) The proposed MLI has the capacity to generate a large number of voltage levels, thereby ensuring excellent voltage and current waveforms.
2) Because of its design and attributes proposed MLI drastically reduces the switch count, which further impacts size, cost, and efficiency.
3) In the proposed configuration, common leg operation with a three-phase transformer arrangement substantially reduces the transformer count when compared with the traditional transformer-based MLI.
4) The control strategy of the proposed active filter is successfully integrated into the system and investigated in detail.
5) To verify the feasibility and effectiveness of the proposed MLI based SAPF, adequate hardware verification are performed in the laboratory.

Further, this paper arranged as follows. Proposed topology and SAPF briefly explained in Section II. System configuration and control strategy were shown in Sections III and IV, respectively. Simulation results demonstrated in Section V. Prototype experimental verification presented in Section VI. Lastly, the conclusions presented in Section VII.

II. PROPOSED TOPOLOGY AND ACTIVE FILTER CONFIGURATION

To demonstrate the conventional active filter topology, consider H-bridge type multilevel inverter employing cascaded transformer shown in Fig. 1(b). The total size of the converter is big due to the series combination of the three 1-φ transformers at the secondary side. The H-bridge connected in parallel to a DC source and thereby increasing the cost of the system. Fig. 2 presents the proposed CMI with low frequency 3-phase transformers. These not only trim down the size of the converter but also reduce the price. Regarding the construction point of view, the DC bus voltage (V_{DC}) is given to the H-bridge module. The output of the H-bridge ($+V_{DC}$, 0, $-V_{DC}$) is given to the primary of the transformer. Later, the voltage across secondary terminals of series connected transformers will boost the level of the output voltage. While investigating Fig. 2,
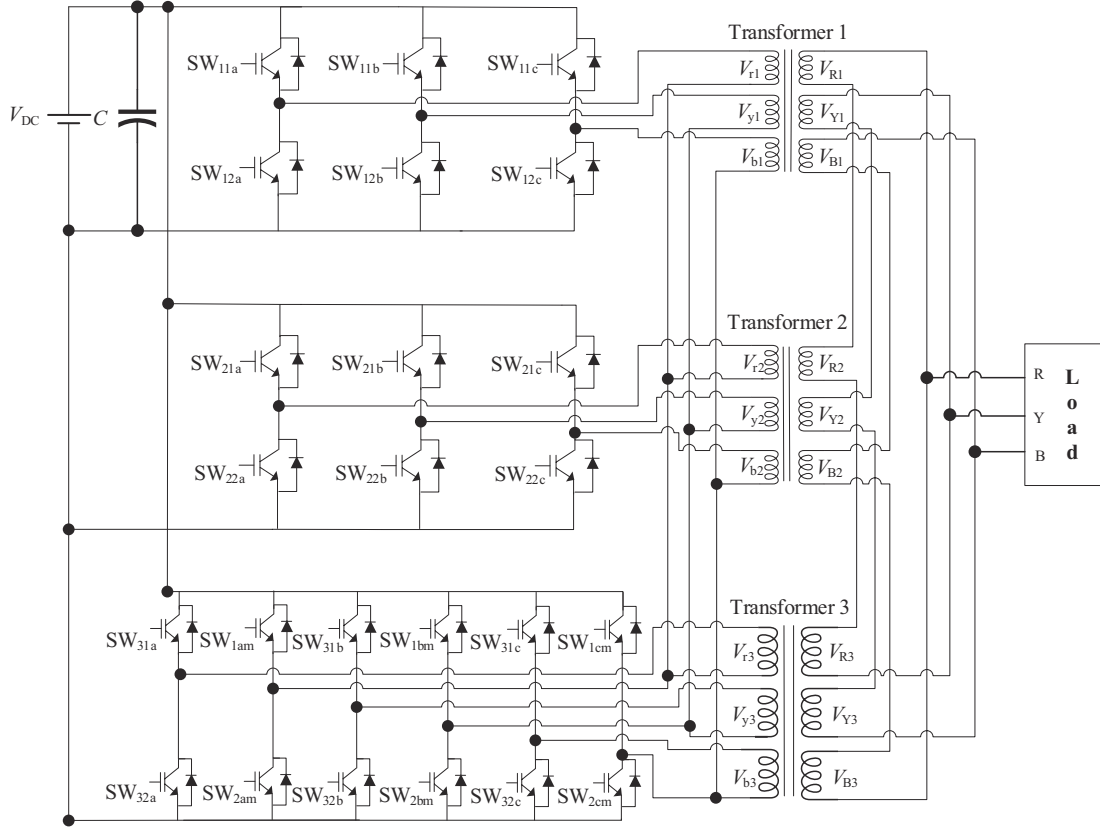
Fig. 2. Proposed multilevel inverter employing 3-phase transformer.

the third harmonic component from the supply eliminated by using a delta connection.

Additionally, the proposed version demonstrates the 3-φ reduced transformer based arch type. On observing, standard power modules utilize for extending the structure, while the common leg module arranged for generating suitable voltage levels. For example, to generate a V_{rl} (voltage at phase 'r' of transformer one) switches in the first module of leg one, and switches in common module of leg one operated. A similar operation extends for module two in combination with the common module. The generated the quasi square voltage across each primary of the transformer is shown in Fig. 3. The secondary terminals of all transformers are connected in series to generate phase voltage. Therefore, each phase of the multilevel inverter can be defined independently. So, each phase represented as an isolated multilevel inverter in cascaded form. The following equations describe the relationship between primary and secondary voltages of the 3-φ transformer.

$$V_{RK} = \frac{2V_{rk} - V_{yk} - V_{bk}}{N} \qquad (1)$$

$$V_{YK} = \frac{-V_{rk} + 2V_{yk} - V_{bk}}{N} \qquad (2)$$

$$V_{BK} = \frac{-V_{rk} - V_{yk} + 2V_{bk}}{N} \qquad (3)$$

Where N is the transformation ratio (n_2/n_1) between secondary

and primary, the summation of individual phase voltages will be zero for balanced input.

$$V_{RK} + V_{YK} + V_{BK} = 0 \qquad (4)$$

$$\begin{bmatrix} V_{RK} \\ V_{YK} \\ V_{BK} \end{bmatrix} = N \begin{bmatrix} V_{rk} \\ V_{yk} \\ V_{bk} \end{bmatrix} \qquad (5)$$

From (5) each output phase voltage calculated from the product of the input voltage matrix and transformation ratio N. But, (5) is not satisfied for unbalanced conditions. The balanced output voltage condition occurs when V_{rk}, V_{yk} and V_{bk} are all equal to V_{DC}. Therefore, (1)–(3) satisfies the unbalanced conditions. The primary flux of phase 'r' will influence phase 'y' and phase 'b' and represented by –1. The proposed multilevel inverter is shown in Fig. 2. All the secondary terminals of the transformers are connected in a series fashion. So, the output voltage is the summation of the individual voltages of the transformers. Therefore, the summation summarized as

$$[V_{RS} \ V_{YS} \ V_{BS}] = \left[\sum_{i=1}^{k} V_{Ri} \ \sum_{i=1}^{k} V_{Yi} \ \sum_{i=1}^{k} V_{Bi} \right]. \qquad (6)$$

Where V_{RS}, V_{YS} and V_{BS} represent a summation of secondary voltages. Thus, line voltages V_{RY}, V_{YB} and V_{BR} are given by
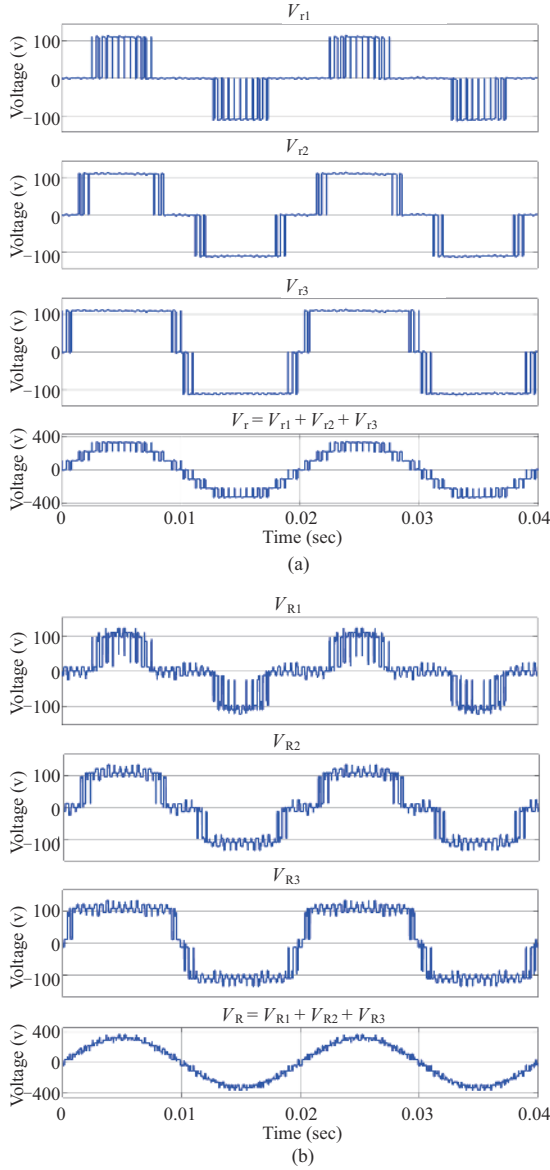
Fig. 3. Details of simulation when modulation index is 1.0. (a) Voltage across the primary of the first winding in each 3-φ transformer (V_{r1}, V_{r2} and V_{r3}). (b) Voltage across the secondary of the first winding in each 3-φ transformer (V_{R1}, V_{R2} and V_{R3}).

$$\begin{bmatrix} V_{RY} \\ V_{YB} \\ V_{BR} \end{bmatrix} = \begin{bmatrix} V_{RS} \\ V_{YS} \\ V_{BS} \end{bmatrix} = \begin{bmatrix} V_{R1} + V_{R2} + \ldots\ldots + V_{RK} \\ V_{Y1} + V_{Y2} + \ldots\ldots + V_{YK} \\ V_{B1} + V_{B2} + \ldots\ldots + V_{BK} \end{bmatrix}. \quad (7)$$

Validate the proposed structure, simulation results along with the experimental verifications are incorporated. Fig. 3 portraits primary and secondary voltages of the transformer by considering the modulation index as one. By observing the primary and secondary voltage waveforms, the individual input voltages are symmetrical quasi square voltages results in seven levels at the primary side of the transformer. The secondary connected in delta fashion, which provides thirteen level output voltage for load.

TABLE I
Components Comparison

System components	Conventional MLI	Proposed CMLI
Switches	6 ($q-1$)	3 ($q+3$)/2
Main diodes	6 ($q-1$)	3 ($q+3$)/2
Clamping diodes	0	0
DC-bus capacitor	1	1
Balancing capacitors	0	0
Input DC source	1	1
1-φ transformers	3 ($q-1$)/2	0
3-φ transformers	0	($q-1$)/4

Further to emphasize this new concept the comparative approach is carried out between conventional CMI with single phase transformers and proposed MLI with three-phase transformer. The number of levels (q) possible in a proposed multilevel inverter is $4m + 5$, where m ranges from 0 to ∞ and the number of switches denoted with $3(q + 3)/2$. To figure out some of the advantages, consider Table I which provides the information regarding components requirements in conventional and proposed configurations. The proposed architecture uses ($q-1$)/4 transformers required for the same number of output levels. Whereas $3(q-1)/2$ transformers are required in the conventional structure.

To comprehend a 13 level inverter is considered for comparison. In fact 18 number of 1-φ transformers are required to get 13 output voltage levels in a conventional arrangement, whereas, only 3 three-phase transformers needed in the proposed system. Further comparison in switches, the proposed system requires only 24 switches when compared with 72 switches in the conventional system, which means that the switch count reduced to one third. Therefore, the space requirement, size, and cost of the system come down. Besides this issue, the voltage rating of the switch fixed by the number of switches connected in series. The voltage and current ratings of all the switches are equal. The conventional inverter uses a circulating switch pattern to keep the equal ratio in the switch utilization. Finally, the reduced number of switches makes the proposed system is cost effective when compared with the conventional active filters.

However, the proposed architecture is quite suitable for a grid connected system. In this issue, transformer output depends upon accumulated voltages which synthesized with respective input voltages. Therefore, there is no additional transformer required for galvanic isolation. The motto of the paper is to build an SAPF with proposed configuration. Thus further sections completely deal with an SAPF constructions with a proposed archetype.

III. System Configuration

The proposed CMI construction is presented as an active power filter for harmonic compensation, and its construction
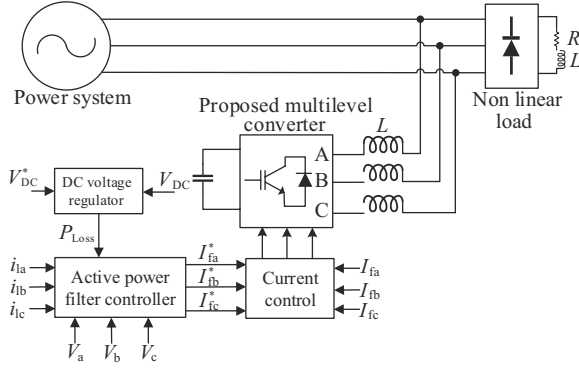
Fig. 4. General Structure of power network.

presented in Fig. 4. The structure designed with a 50 Hz supply. Shunt active power filter is placed at the point of common coupling (PCC) in parallel with the power network. Therefore, CMI acts like a power source, which is proficient in obstructing the current harmonics resulted from the contaminating loads. The proposed model was developed based on instantaneous active and reactive currents component strategy. It is explained concisely in the next section. For compensation achievement, SAPF construction is more significant. The precise compensation and the controller must realize the given requirements: i) managing and providing the harmonics currents caused by the load, ii) controlling the reactive power with fundamental frequency components, iii) maintaining continuous DC voltage across the energy storage element.

The power and control investigation can be verified by assuming that the inverter feds a sinusoidal voltage source corresponding to the connected load [26] herein, SAPF controller controls the reactive power as well as harmonic reduction caused by non-linear loads. Thereby, filter performance is analyzed to generate compensation currents. Additionally, CMI is not capable of long term distribution of active power.

The line impedance which connects to two power source formed by the geometrical relation (under steady state). The correlated expressions for the load current given as:

$$i_{Load}(t) = \sum_{n=1}^{\infty} \left[I_{Load.a.n} \times \sin\left(n\omega t + \theta_{Load.a.n}\right) \right] \quad (8)$$

The offered load current data has been divided into three different components, which are a total harmonic component at various frequencies, active component and reactive component at the base frequency i.e.,

$$\begin{aligned} i_{Load}(t) = &\left[I_{Load.a.1} \cos\theta_{Load.a.1} \times \sin(\omega t) \right] \\ &+ \left[I_{Load.a.1} \sin\theta_{Load.a.1} \times \cos(\omega t) \right] \\ &+ \sum_{n=2}^{\infty} \left[I_{Load.a.n} \times \sin\left(n\omega t + \theta_{Load.a.n}\right) \right]. \end{aligned} \quad (9)$$

$$i_{Load}(t) = \left[I_{Load.a.active}(t) + I_{Load.a.reactive}(t) + I_{Load.a.harmonic}(t) \right] \quad (10)$$

Injecting (compensation) currents that active power filter should generate is

$$I_{compensation}(t) = -I_{Load.a.reactive}(t) + I_{Load.a.harmonic}(t) \quad (11)$$

Consequently, the filter must achieve this compensation through finite control arrangements. In the next section, the extractions of injecting currents presented.

IV. OVERALL SYSTEM CONTROL

A. Reference Current Generation

In the present paper i_d–i_q control strategy used to generate compensation currents [26]. This compensation system illustrated in Fig. 5. The control i_d and i_q used to generate reference currents. The dq load current attained from (12). The stationary and rotating reference frame relations obtained with two stage transformations. The voltage vector is in the stationary reference frame, and the current vector is in a rotating reference frame. The parameter $d\theta/dt$ is not constant, and it keeps on vary. The key reason to vary is the transformation angle θ, as θ is sensitive to all unbalanced voltages and harmonics. Corresponding mathematical equations presented in (12), (13). Further, in the present control strategy θ is calculated directly by utilizing main voltages, and this is one of the remarkable merits. Thus adequate expression for reference currents obtained with (14).

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{1}{\sqrt{V_\alpha^2 + V_\beta^2}} \begin{bmatrix} V_\alpha & V_\beta \\ -V_\beta & V_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (12)$$

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}, \theta = \tan^{-1}\left(v_\alpha/v_\beta\right) \quad (13)$$

$$\begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix} = \frac{1}{\sqrt{V_\alpha^2 + V_\beta^2}} \begin{bmatrix} V_\alpha & -V_\beta \\ V_\beta & V_\alpha \end{bmatrix} \begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} \quad (14)$$

Moreover, this control method allows functioning like frequency independent, thereby synchronizing circuits like PLL are eliminated [27]. Thus control approach evades synchronizing problems under different supply conditions (unbalanced and distorted conditions). Consequently, the cut-off frequency of CMI inverter and i_d–i_q approach makes to function with large frequency operating limit. Control diagram specifies that, currents obtained from park transformation are load currents of i_d and i_q are sent by the high pass filter (HPF) to nullify the DC components in the contaminated load. Herein butterworth filter is used to minimize the DC components. But, the similar performance of a high pass filter obtained by using a low pass filter with the difference of input signal and filter one. In fact influence on transient response depends on filter choice. Although high pass filter functions extremely well but the transient response is poor. However, high pass filter influence minimized with an above mentioned arrangement. Further, in
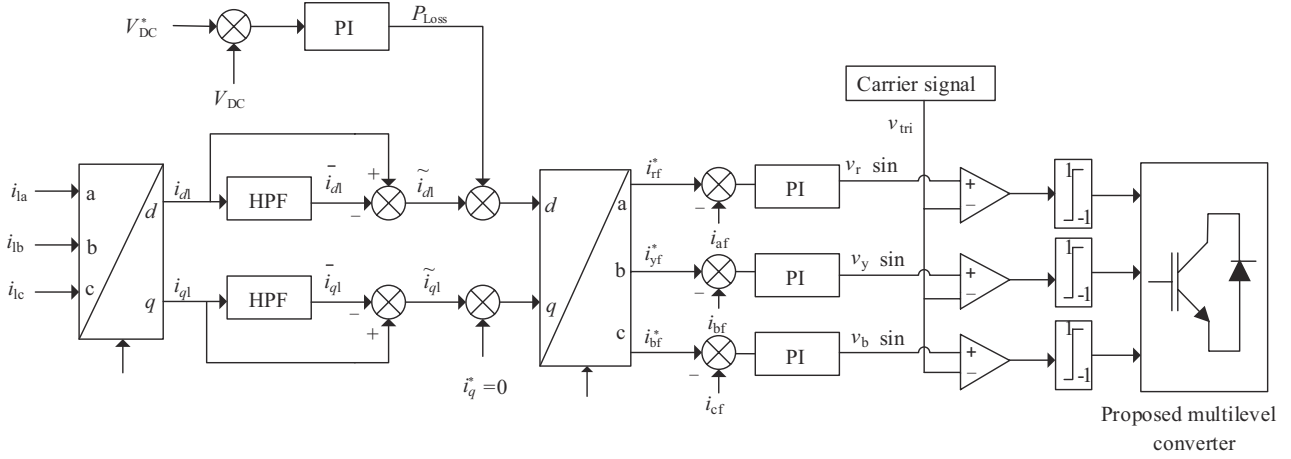
Fig. 5. Control diagram of proposed shunt active power filter.

the present control algorithm, one half of the main frequency with an adequate phase shift is used in the butterworth filter in order to obtained high transient response.

B. Harmonic Current Regulator

The obtained reference currents are sent to the current regulator. The current regulator controls the compensator by giving command signals. These command signals are generated by the PI current controller. It is suitable for non-sinusoidal currents. Variable switching pattern changes the switching frequency as well as phase interaction accordingly. A pulse width modulation (PWM) technique is used to avoid this undesirable phenomenon. It provides zero steady state error for dominant frequencies. The harmonic currents will be tracked by the current controller. The current controller is simple in structure and it saves the computational time as well. The current control approach clearly illustrated in Fig. 6. It converts the command current signal into a corresponding command voltages and then applied to a voltage source in PWM cycles. The appropriate range assigned by normalizing the commanded voltages to the corresponding DC voltage.

C. Multilevel Voltage Source Modulation

The i_d–i_q method compared with the PQ theory is given in [28]. The multilevel inverter uses two level ramp-comparison control method with level-shifted multi-carrier PWM [29]. Here, thirteen levels achieved by comparing the given carrier waveforms with a sinusoidal reference wave. The generation of command signals is modulating V_{ref} which compared with the carrier signals V_{car} of frequency f_s with a fixed amplitude shown in Fig. 6. The process of generating the pulses for a multilevel inverter follows the logical combination of command signals. The sequence of switching is given in the following section.

when,

SW_{11a} and SW_{2am} are on, leading to $V_{r1} = + V_{DC}$,
SW_{11a} and SW_{1am} are on, leading to $V_{r1} = 0$, and
SW_{12a} and SW_{1am} are on, leading to $V_{r1} = -V_{DC}$.

From the given sequence, the voltage levels for H-bridge is $V_{DC}, 0, -V_{DC}$. The same process is repeated for other H-bridges
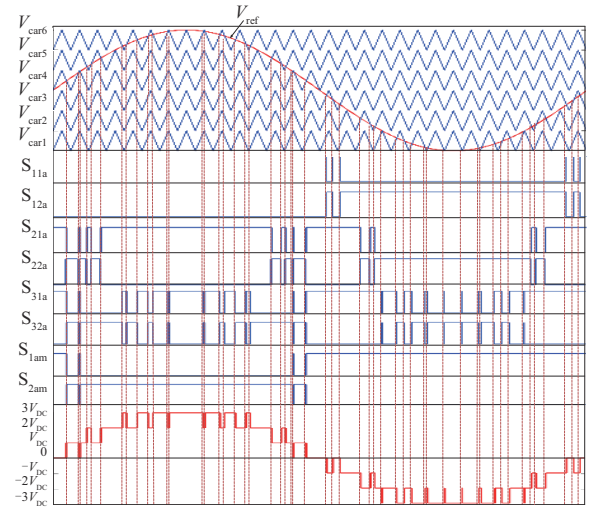

Fig. 6. Switching pattern of a proposed multilevel inverter.

in a multilevel inverter with a level shift in a carrier wave by the different offset voltages. The net output voltage is the sum of all three voltage waveforms. The proposed CMI uses level shifted modulation. There are several advantages with level shifted modulation over phase shifted PWM like. Simple configuration, it produces the lowest total harmonic distortion (THD) of the output voltage. All the given advantages result in low switching losses. As the THD profile is low, voltage and current are sinusoidal nature, which further results in improved efficiency when compared to former topologies.

D. DC Voltage Controller

The DC reference voltage (V_{DC}^*) and DC link voltage (V_{DC}) are given to the PI controller. The input will be the difference between V_{DC} and V_{DC}^*. The real power from the PV system directly linked with the capacitor voltage. Therefore, it is customary to maintain the DC capacitor voltage at a constant value. Real power is not required to maintain the DC voltage constant. But a small amount of power is utilized in converter switching. The real power needs to control for the successful operation of the active power filter. Power flow can
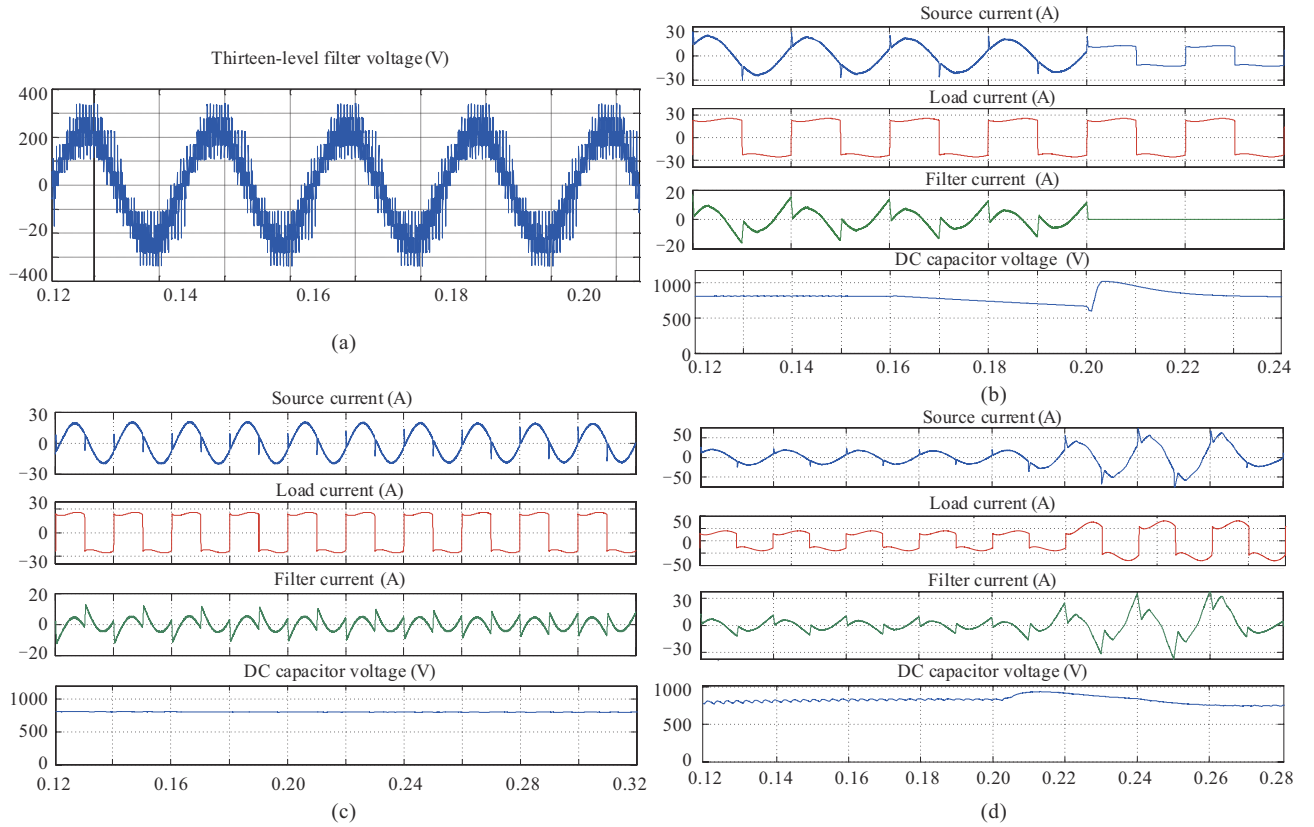
Fig. 7. (a) Simulation results of thirteen-level filter voltage for phase a. (b) Details of simulation results for with and without SAPF. (c) Steady state operation of the proposed SAPF. (d) Dynamic response of proposed SAPF with step change in load.

be controlled smoothly by controlling the positive sequence currents of active and reactive power. The positive sequence of first harmonic active current (i_{d+}) controls the active power and a positive sequence of first harmonic reactive current (i_{q+}) controls the reactive power. Finally, this voltage controller maintains constant DC power and controls the reactive power to reduce the harmonic distortion caused by the non-linear load.

E. Proportional-Integral (PI) Controller Design Aspects

Voltage control is very much simpler in the proposed topology. A PI controller is used to control the DC voltage. The difference between reference DC voltage and DC link voltage is given to the PI controller. Capacitor voltage for step input for different values of integration coefficient (k_i) of the PI controller by keeping the proportional constant (k_p) at 0.75. From the step response, it noticed that the overshoot increases as k_i increases, whereas there is a decrement in rising time. The noise increased as proportional constant k_p increases, results in degradation of reference current extraction. Even though there is an improvement in reference current for increased values of k_i, it increases the oscillations. Further, it may generate large transients in the capacitor voltage. Finally, it may lead to trip the protection circuit. The value of the k_p considered as 0.75 and the value of k_i considered as 1. Voltage ripple will decrease as capacitance increases and is independent of the integrator

coefficient.

V. SIMULATION RESULTS

The proposed SAPF based on CMI topology is implemented in Simulink and diode bridge rectifier, and inverters are built from the powersim block set. The Simulink results verified with a prototype experimental setup. The complete analysis is given based on the experimental observations to avoid theoretical calculation.

The simulation is carried out for non-linear load under steady state and transient conditions. Thirteen-level of filter output voltage is shown in Fig. 7(a) when connected to the power network. Various performance curves with and without a filter is shown in Fig. 7(b). Source current waveform is sinusoidal when the filter is activated. Source current is affected by the load current when it operated without a filter. Filter current provides the compensation current, results in sinusoidal source current. There is a deviation in the capacitor voltage when the filter is deactivated. Fig. 7(c) shows the various performance curves with filter under steady state condition. It is showing that the injecting filter current at PCC maintains sinusoidal source current. To observe the dynamic performance of the system, the load is changed suddenly. The dynamic response curves are shown in Fig. 7(d). Fig. 8 gives the percentage of THD with and without SAPF.
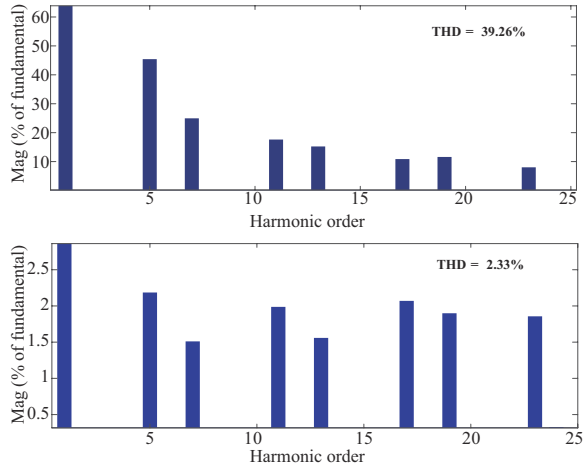
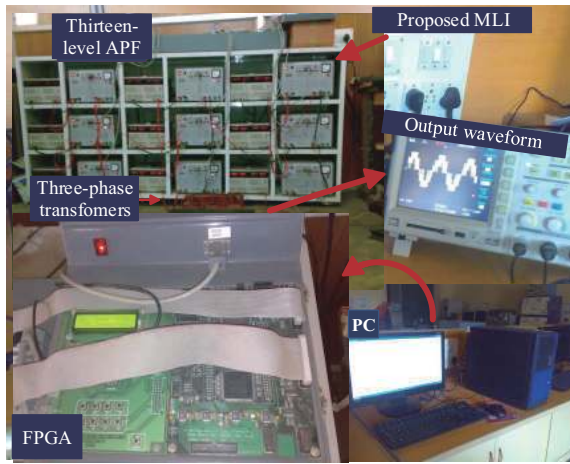Fig. 8. FFT analysis of source current before and after the proposed SAPF.

Fig. 9. Prototype set up for proposed thirteen-level SAPF.

From results, it has observed that the filter effectively eliminates the harmonic component from source current under these dynamical conditions. So, the proposed methodology effectively improves the quality of power. Further, to validate the simulated results, adequate experimentation is done with a prototype setup. In depth assessment of prototype setup and results are reported in the next section.

VI. EXPERIMENTAL RESULTS

The field programmable gate array (FPGA) controller used for experimentation. The proposed circuit topology realized with code composer. Fig. 9 indicates a 5-kVA proposed thirteen-level SAPF construction using 3-phase transformers. The supply currents, supply voltages, load currents and compensation currents measured with Hall Effect current and voltage transducers. Complete details of the prototype experimental setup furnished in Table II.

Experimental verifications provided to figure out some of the advantages of the proposed topology. Fig. 10 demonstrates the performance of conventional CMI with 3-phase transformers. From observing intensely, thirteen-level performances are achieved at modulation index one by using the same number

TABLE II
HARDWARE DETAILS

Items	Specification and features
kilovolt ampere rating	5 kVA
Supply voltage	400 V
Supply frequency	50 Hz
Source inductor	1.5 mH
Transformers	EI lamination (3EA) 1:1 ratio
FPGA	PWM signals generate device
Translator	Voltage translator SN74LVCC3245A
Line-to-line voltage	13-level, 400 V
Current sensor	LTS 25-NP 25 A
Voltage sensor	LV 25-NP 1200 V
DC link capacitor	2200 μF
Switching frequency	2 KHz
Non linear load	$R = 20\ \Omega$, $L = 100$ mH
DC voltage control	$k_p = 0.75$, $k_i = 1$

of H-bridge cells. Further, The modulation index changed from 0.1 to 1. The number of voltage levels varies from five-level to thirteen-level is shown in Fig. 10. It shows the capacity of the converter. In other terms, proposed topology is capable of produce twice output voltage levels with the same number of H-bridge cells. It is obvious, as the number of levels increases harmonic content drastically reduces. But an important point to notice herein is that secondary side transformers connected in delta fashion, this helps in nullifying third harmonics as well as multiple harmonics in the output voltage.

Further, FPGA compares the measured capacitor voltage and reference voltage to generate reference active filter currents. Fig. 11(a) shows the performance curves are given with and without a filter. All the experimental results almost resemble the simulated results. An isolation transformer provides an output voltage of the inverter terminal as 13 levels. The DC capacitor voltage is adjusted to 800 V to produce a nominal voltage under the steady state condition at the terminals of the inverter and the value of source voltage set to 115 V. The performance of SAPF observed at balanced condition. Fig. 11(b) shows the various experimental results with SAPF under balanced condition. SAPF successfully generates the compensation currents to improve the quality of source current.

Further, it has observed that the supply current is in phase with source voltage without harmonic component, results in improving the power factor. A step change in load introduced to observe the dynamical behavior of the proposed topology. Fig. 11(c) provides the information of DC voltage across the capacitor, filter current, load current and source current under the dynamical state. The performance curves prove that the SAPF successfully compensates for the effect of load harmonics on source current. Fig. 12 gives the percentage of THD with and without SAPF. The proposed SAPF has confirmed excellent performance. During the steady state and transient condition, given FFT spectrum reveals that the successful elimination of lower order harmonics successfully
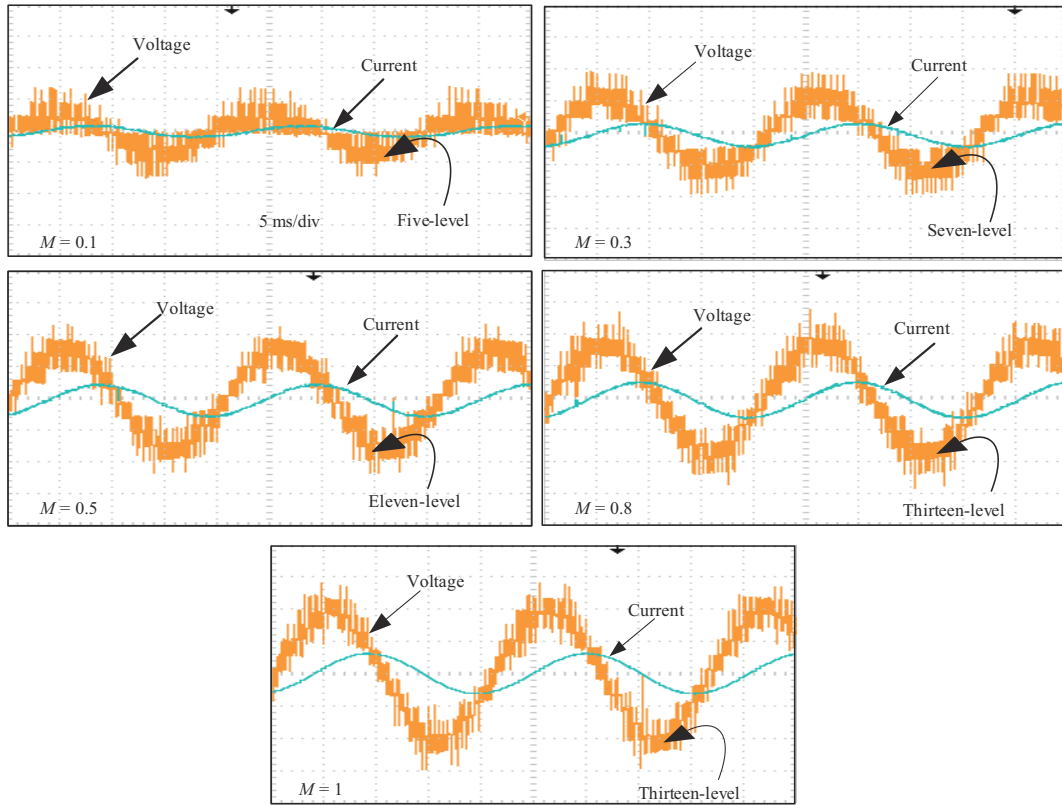
Fig. 10. Results of the proposed multilevel inverter voltage and current waveforms for different modulation index (M).
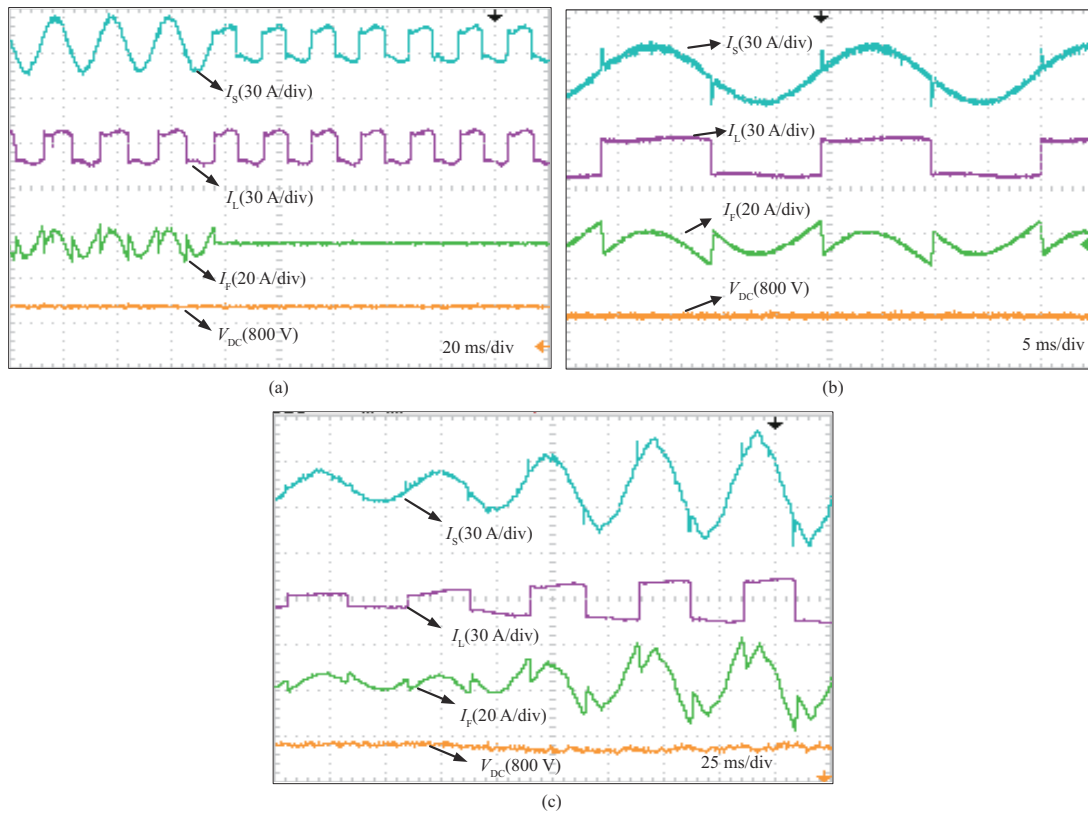

Fig. 11. (a) Experimental waveforms for with and without proposed SAPF, (b) experimental steady state response of the proposed SAPF and (c) experimental dynamic response of the proposed SAPF with step change in load.
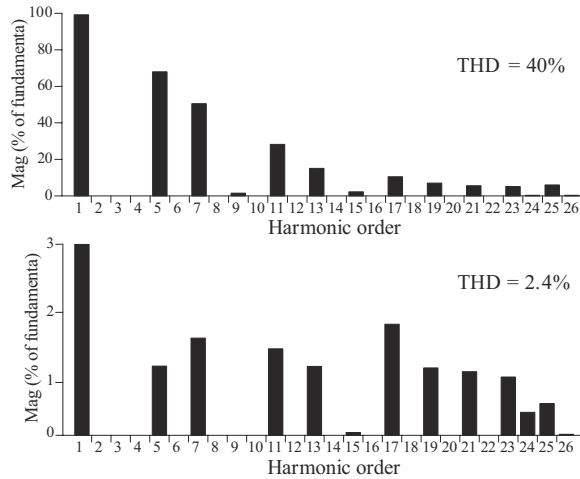
Fig. 12. FFT spectrum of source current before and after the proposed SAPF.

TABLE III
Cost Comparison of Proposed With Conventional

Components	Series	Price ($)	C	P
IGBT	RGPR30NS40HR	1.55	111.6	37.2
Main diodes	DPG30C400PB	1.4	100.8	33.6
Gate drivers	IR2110SPBF	1.97	70.92	23.64
DC-bus capacitor	B43701	65.99	65.99	65.99
1-φ transformers	SP1000MQMJ	153.18	2757.24	-
3-φ transformers	SBK2KVA	380.79	-	1142.37
Total	-	-	3106.55	1302.80

eliminated. Moreover, the given system possesses many other advantages such as simple configuration and easy control scheme as there is only one storage element. Further, the size of the system is reduced because of the three-phase transformer when compared with the conventional system. The component specifications and their corresponding cost are incorporated in Table III. It is manifest from the comparison result that the proposed MLI is highly cost effective.

VII. Conclusion

This article presents a new CMI topology for SAPF. The proposed CMI reduces the number of transformers required to perform the same task by the conventional strategies. Thereby, the size and cost of the equipment reduced. Switching losses also reduced due to low switching frequency, results in a reduction in EMI problems. Additionally, there is no ambiguity in controlling the system since there is only one storage device. The $i_d−i_q$ theory used to generate the reference current signals. The angle 'θ' can be calculated from the main voltages. Therefore it is frequency independent system. It eliminates the problem of synchronization. The DC voltage also maintained at a constant level. The proposed topology for SAPF improves the quality of power by terminating the harmonics caused by the non-linear loads. The proposed method is applies to balanced and unbalanced conditions. The different conditions are considered and simulated in MATLAB. The obtained simulated results verified with the experimental setup. Further, the experimental results conclude that the proposed system is accurate and cost effective.

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