Development of Enhancement Mode AlGaN/GaN MOS-HEMTs using Localized Gate-Foot Oxidation

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***Abstract* — A new method for realising enhancement mode AlGaN/GaN devices using a localized gate-foot oxidation is described. Thermal oxidation of the AlGaN barrier layer converts the top surface/part of this layer into aluminium and gallium oxides, which serve as a good gate dielectric and improve the gate leakage current by several orders of magnitude compared to a Schottky gate. The oxidation process leaves a thinner AlGaN barrier which can result in normally off operation. Without special precaution, however, the oxidation of the AlGaN barrier is not uniform from the top but occurs at higher rates at the defect/dislocation sites. This makes it impossible to control the barrier thickness and so rendering the barrier useless. To avoid the problem of non-uniform oxidation, a thin layer of Aluminum is first deposited on the barrier layer and oxidized to form Al_2O_3 on top. This additional oxide layer seems to ensure uniform oxidation of the AlGaN barrier layer underneath on subsequent further oxidation. Preliminary results of the fabricated 2µm × 100µm AlGaN/GaN MOS-HEMTs with a partially oxidized barrier layer showed a maximum drain current of 660 mA/mm at high gate bias of 3V before current compression sets in.**

I. INTRODUCTION

Wide band-gap III-Nitride semiconductor materials possess many superior material properties than conventional Si, GaAs or any other III-V compounds. The major advantages of the nitride-based devices which make them extremely capable for high power and high frequency applications are high electron mobility and saturation velocity, high breakdown field, high sheet concentrations at heterojunctions and low thermal impedance when grown accordingly on suitable substrates like Si, 4H-SiC or bulk AlN [1]. III-nitrides also possess better chemical and thermal stability even for temperatures as high as 1000^{O}C. They also find very useful applications in the field of power electronics as they allow for high power switching with sub micro- and nano-second switching times. Presently, GaN-based devices for these applications are depletion mode devices.

Enhancement mode GaN-based HEMTs, on the other hand, are in high demand in the market for high power switching purposes because they are normally-off devices and as such fail safe. They are also attracting interest because their use of a single-polarity voltage supply simplifies power amplifier circuits. One of the most common ways of achieving E-mode operation is by barrier thinning of the gate-foot [2], [3] or by flourine ion implantation [4]. These methods are neither reliable nor stable since for recess gate technology, reproducibility is an issue as it is very hard to control the etch depth and hence the threshold voltage of the devices varies across a sample/wafer. For ion implantation, the implanted fluorine ions makes the devices very unstable and also degrades the drain breakdown voltage of the devices.

Based on the dry oxidation technique originally developed by Hiroyuki Masato et al [5] for device isolation in AlGaN/GaN devices, we are developing a new process, which involves the oxidation of the gate region in dry oxygen at 800^{O}C. This technique oxidizes the semiconductor and converts it into a mixture of highly crystalline aluminum and gallium oxide [6]. Preliminary results suggest the approach can deliver high performance E-mode devices.

A very similar technique was recently reported for InAlN/GaN MOS-HEMTs [7]. In Ref.[7], the barrier is Indium Aluminium Nitride (InAlN). This layer (InAlN) seems to oxidise uniformly without any special precaution. In our case, the topmost layer is AlGaN which without special precaution as described in this paper does not oxidise uniformly.

II. CONCEPT & EXPERIMENTS

The AlGaN/GaN MOS-HEMT structure used in this study was grown using Molecular Beam Epitaxy (MBE) on sapphire substrate (Al_2O_3) with a Ga-face (0001) orientation. The epitaxial layer consists of (from top) a 2 nm GaN cap layer, an undoped 20 nm $Al_{0.25}Ga_{0.75}N$ layer followed by a 3µm undoped GaN channel layer, which is grown on Sapphire substrate with a very thin (2nm) AlN buffer in between. Initial Hall measurements show a 2DEG concentration of $1.3x10^{13}$ cm^{-2} and a mobility of ~1700 cm^2/V.s. Selective oxidation of the AlGaN

layer underneath the gate-foot could be employed for the effective thinning of this barrier layer and thereby achieving E-Mode operation by locally reducing/eliminating the 2DEG carrier concentration. The mixture of the aluminum and gallium oxide created also serves as a good high-k gate dielectric, which helps in reducing the gate leakage.

Several researchers have been working on the growth and electrical properties of thermally grown oxide on (Al)GaN material at different temperatures in order to create a good gate dielectric. For AlGaN, the oxidation rate at the dislocation sites appears to be much higher and hence the oxides are formed throughout the barrier rather than uniformly from the top [8]. If one attempted to make MOS-HEMTs this way, the device performance is very poor as a result [9].

In this paper a new technique is presented, which can be used to achieve uniform oxidation of the AlGaN barrier layer from the top and prevent the preferential oxidation at the dislocation sites. This method involves the evaporation of a thin film of Aluminum over the barrier layer prior to oxidation. Details of the fabrication steps are given below.

A. Device Processing

Initially, the AlGaN barrier layer was oxidised directly without any special precautions. Fabrication steps for the proof-of-concept are detailed below and also illustrated in Fig.1.

1. Deposition of 150 nm Silicon Nitride (SiN) all over the sample using Inductive Coupled Plasma (ICP)
2. Gate alignment using optical lithography. Gate foot defined in SiN for eventual oxidation with SiN as a mask
3. Dry etching of SiN with SF_6 gas (RIE) using the photoresist as an etch mask
4. Oxidation of the barrier in an RTA in O_2 environment at 800^oC for a desired time span in order to reduce the effective barrier thickness accordingly.
5. Etching of SiN using RIE with SF_6 to define Ohmic contact areas
6. Alignment of Ohmic contacts followed by deposition of a metal stack of Ti (30nm)/Al (180nm)/Ni (40nm)/Au (100nm). This is then annealed at 800^oC for 30 sec in N_2 environment.
7. Deposition of Field Plate over the gate foot, Ni (50nm)/ Au (150nm).

B. Growth & Analysis of the Oxide

In order to evaluate how the AlGaN barrier oxidises, two samples were directly oxidized, i.e. without the thin Al layer, one for 5 mins and the other for 10 mins at 800^oC. Cross- sectional TEM analysis of both the samples was carried out and TEM pictures are shown in Fig. 2a. These results show that the oxidation was not uniform from the top but rather throughout the barrier layer (assumed to be along the dislocation/defect sites) as shown in the TEM picture. The oxidation rate within the barrier seems to be at a much faster rate. Fig. 2b shows the oxygen mapping in the oxidized barrier confirming the non-uniform oxidation.

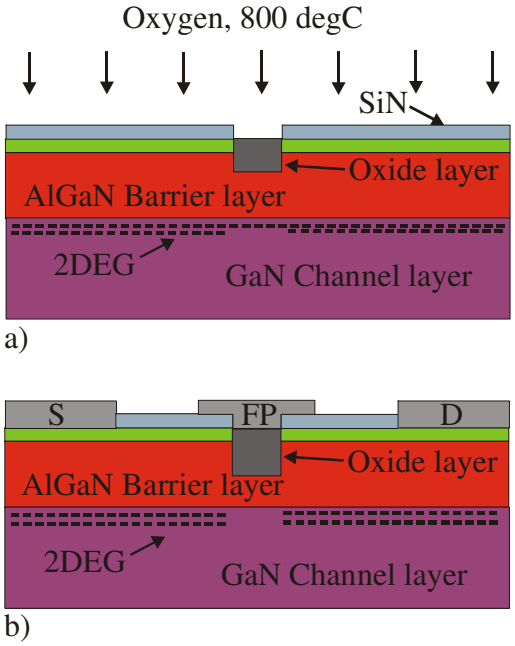

Fig.1: Concept and process flow for AlGaN/GaN MOS-HEMTs.

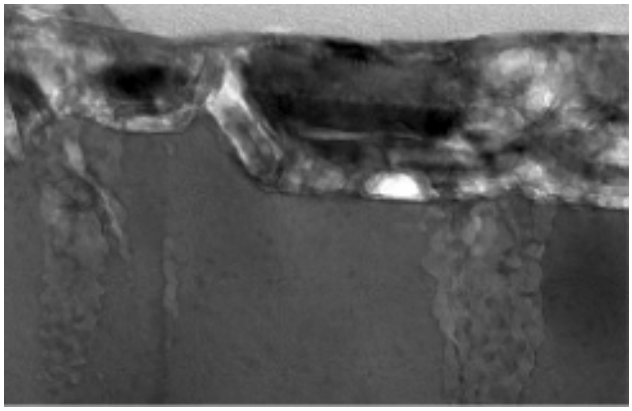

Fig. 2a: Cross-sectional TEM analysis showing oxidation takes place not only from the top of the barrier layer, but also within the barrier at the dislocation sites.

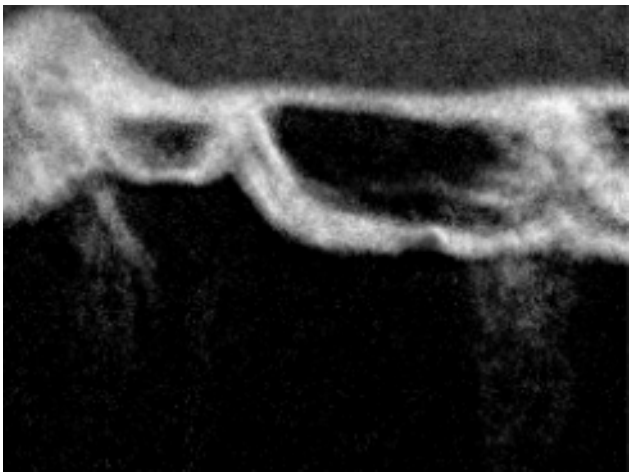

Fig. 2b: Cross-sectional TEM analysis showing oxygen mapping.

C. Modified oxidation approach

The TEM analysis proved that direct oxidation of the barrier layer could not be used to fabricate devices because of the non-uniformity of the formed oxide which practically renders the barrier useless. To achieve uniform oxidation of the AlGaN barrier layer a very thin layer of Aluminium (~2-5nm) was deposited on the gate-foot before oxidation of the samples. The Al layer was first annealed at 800C in N_2 environment for 30~60 sec. The samples were then oxidized for 2.5mins at 800^{O}C along with the thin annealed layer of Aluminium on top. S-TEM analysis was performed on the samples, results of which are shown in Fig. 3.

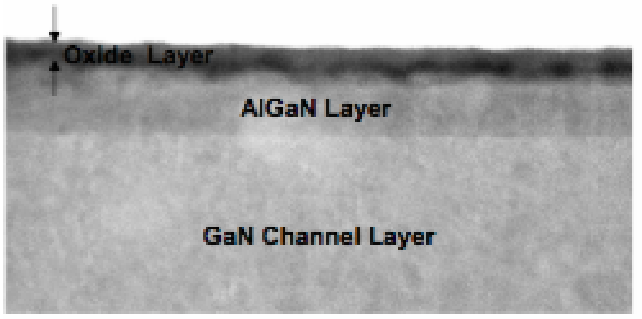

Fig. 3: Cross-sectional S-TEM analysis showing the uniformity in the oxide growth.

The micrograph in Fig.3 shows that depositing a thin Aluminium layer on top significantly improves the quality and the uniformity of the oxidation. During the oxidation process, the Al is oxidised first forming Al_2O_3 which acts as a protective layer for the barrier layer underneath. On further oxidation, the oxide grows uniformly underneath the initial Al_2O_3 layer consuming the barrier AlGaN layer which thins uniformly. The rate of oxidation was extracted from the cross-section of the S-TEM picture (Fig.3) and shows a uniform growth rate of 2 nm/min of the semiconductor itself with a total oxide thickness of around 9nm, which consists of the initial 4 nm from the Al and the rest from the AlGaN barrier layer. After 2.5 mins of oxidation 17nm of the barrier was still found intact, which corresponds to consumption of 5 nm of the barrier layer (including 2nm GaN cap layer).

III. RESULTS AND ANALYSIS

In order to assess the electrical properties of the samples before and after oxidation, simplified HEMT devices of gate length 2µm and width 100µm were fabricated with two-step lithography (ohmics and gate) with and without oxidation. I-V characteristics for the Schottky gate devices are shown in Fig. 4, while those for the MOS device with 6.5 min oxidation time is shown in Fig. 5. The transconductance for the devices with different oxidation times are shown in Fig.6. It is clear that for the devices with the thinned (partly oxidised) barrier layer, the transconductance remains high (i.e. no current compression) for gate voltages as high as 4V. Fig.6 also shows that the threshold voltage has shifted from -5.1V for the Schottky gate device to -3V for the MOS device after 6.5 mins of thermal oxidation. These results indicate that the device is starting to exhibit E-mode operation.

CV measurements (not shown) show no hysteresis between the forward and reverse sweeps indicating the good quality of the grown oxide. Current work is focused on further thinning the barrier though oxidation until normally-off E-mode operation is achieved.

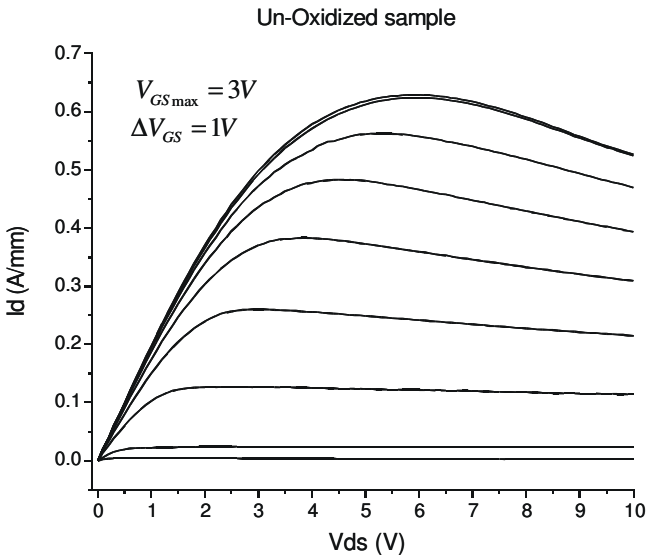

Fig. 4: I-V Characteristics of a Schottky gate AlGaN/GaN HEMT.

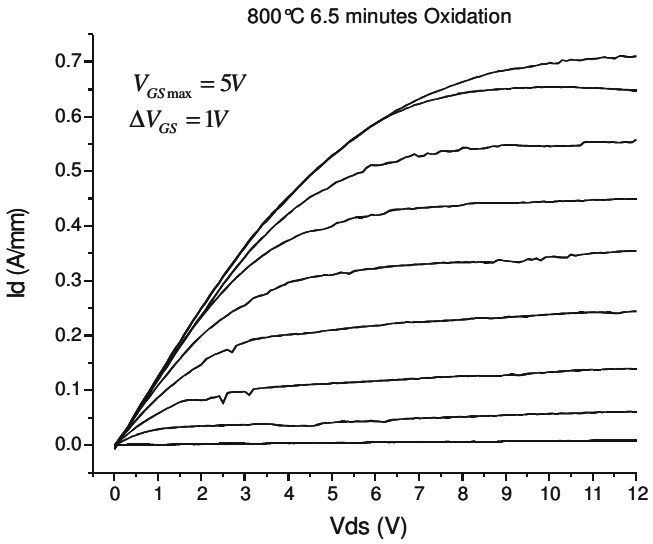

Fig. 5: I-V Characteristics of the AlGaN/GaN MOS-HEMT device after 6.5 mins of thermal oxidation.

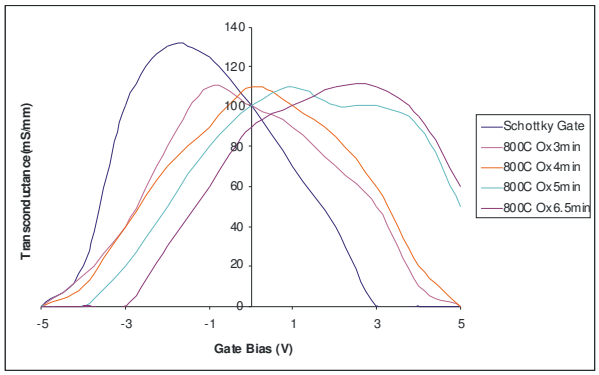

Fig. 6: Transconductance characteristics of the Schottky gate and the MOS devices with 3,4, 5 and 6.5 mins oxidation of the barrier underneath the gate foot. No current compression up to 4V gate voltage is noticeable and the threshold voltage is less negative with higher oxidation times indicating that the device is starting to exhibit E-mode operation.

IV. CONCLUSION

A simple method for realizing enhancement mode AlGaN/GaN MOS-HEMTs by using thermal oxidation of the AlGaN barrier has been described. Preliminary results based on the drain characteristics and the transconductance comparison indicates that this may be a feasible method for achieving high performance E-mode devices. Since both the AlGaN/GaN-based E-mode devices and the conventional D-mode AlGaN/GaN devices can be made on the same wafer, an E/D device technology for realisation of GaN-based logic circuits is potentially available.

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