AIP Review of Scientific Instruments

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Citation: Rev. Sci. Instrum. **68**, 3566 (1997); doi: 10.1063/1.1148324
View online: http://dx.doi.org/10.1063/1.1148324
View Table of Contents: http://rsi.aip.org/resource/1/RSINAK/v68/i9
Published by the American Institute of Physics.

Development of infrared focal plane arrays for space

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(Received 10 October 1996; accepted for publication 16 June 1997)

Space astronomy requires large-area cryogenic infrared focal plane arrays (FPAs) with high quantum efficiency, extremely low dark current, low power dissipation, and background limited noise performance. To meet these requirements, especially at temperatures of 5–15 K, Santa Barbara Research Center designed and fabricated a new multiplexer, CRC-744. The FPAs made by bonding InSb detector arrays to CRC-744 multiplexers were evaluated at the University of Rochester. The best array achieved the read noise of 5 e^- with 12 s integration and 7 e^- with 200 s integration with Fowler-64 sampling at 15 K, the average dark current of $<0.2\ e^-/\mathrm{s}$ at both 15 and 29 K, and the average quantum efficiency of 87% at both 15 and 29 K. The 10%–90% rise time was 4 μs driving a 600 pF external load. The power dissipation was 0.3–0.4 mW when running flat-out (100% duty cycle). The full well capacity was 10^5 e^- (230 mV) with 400 mV of applied bias. The above test results demonstrate that the FPAs meet background-limited space experiment requirements. The CRC-744 multiplexer works well down to at least 5 K (the lowest temperature of our tests). © *1997 American Institute of Physics.* [S0034-6748(97)02709-3]

I. INTRODUCTION

Cryogenic space telescopes such as the Space Infrared Telescope Facility (SIRTF) require large-area focal plane arrays (FPAs) with high sensitivity. Of course, the detector material must exhibit high quantum efficiency (QE), and ultralow dark current—in fact, the dark current must be negligible with respect to the zodiacal background photocurrent. In addition, the FPAs must be background-limited for SIRTF application. This implies that the read noise must be much less than that given by fluctuations in the number of background photons detected. This latter constraint places large demands on readout arrays to simultaneously provide low noise and high responsivity at low power dissipation.[1,2] Santa Barbara Research Center (SBRC) has developed a low-noise 256×256 pixel Si readout, the CRC-744, designed for low temperature (~5–15 K) operation. In the application discussed here, an InSb (1–5.5 μm) detector array is bump-bonded to the CRC-744 multiplexer (mux) to form the FPA, as contracted by the SIRTF Infrared Array Camera (IRAC) team. The CRC-744 will also be used with Si:As impurity band conduction (IBC) arrays for IRAC, and could be used with visible fine guidance sensors (FGS).

The unit cell employs a switched source-follower-per-detector (SFD) design wherein signals are multiplexed onto four outputs while row and column scanners can flexibly address small block portions of the array to conserve power. The data for this article are from readouts developed under contract to the IRAC team, which have been fabricated using an optimized cryo-complementary metal-oxide semiconductor (cryo-CMOS) process developed at Hughes (formerly HTC) specifically for low temperature. This process is currently available at the Hughes Microelectronics Division. Since previous generation readouts employed by SBRC had been developed for higher temperatures (e.g., the popular CRC-463, which exhibits fairly good noise characteristics at temperatures ~30 K used in the SBRC commercial astronomy array program, and for previous SIRTF developmental arrays), our program goal was to achieve superior noise performance at 5–15 K. As discussed in detail below, we have achieved impressive read noise (5 e^-), as well as excellent quantum efficiency and dark current for these InSb FPAs. Staring FPAs designed for astronomy have made impressive progress in the decade. Figure 1 illustrates the improvement in read noise (at various temperatures) for SBRC astronomy FPAs.

II. DESCRIPTION OF THE InSb FPAS

A. The InSb arrays

The detectors are 256×256 element, back-illuminated photovoltaic indium antimony (InSb) arrays constructed of Firebird undoped ($\sim 10^{14}\ \mathrm{cm}^{-3}$) and low doped ($\sim 2\times 10^{14}\ \mathrm{cm}^{-3}$) material. The elements are spaced on 30 μm centers in both dimensions of the two-dimensional array, and the optically active area of each element is $\sim(30\ \mu\mathrm{m})^2$, that is, the fill factor is nearly 100%. Each array has an antireflection coating applied to the light-incident surface to improve quantum efficiency. Low temperature response uniformity has been enhanced by tight control of the detector thickness with a goal of $7\pm 1\ \mu$m.

B. CRC-744 readout description

The Si readout is connected to a detector array by indium bump contacts on 30 μm centers to create a focal plane array (FPA). Figure 2 illustrates the 256×256 amplifiers for integrating detector current. Each unit cell contains a source follower which allows the array to be read out nondestructively, that is, the voltage can be sampled without losing the integrated signal. Every fourth column is multiplexed to one of four outputs. There is a fast scanner which multiplexes the

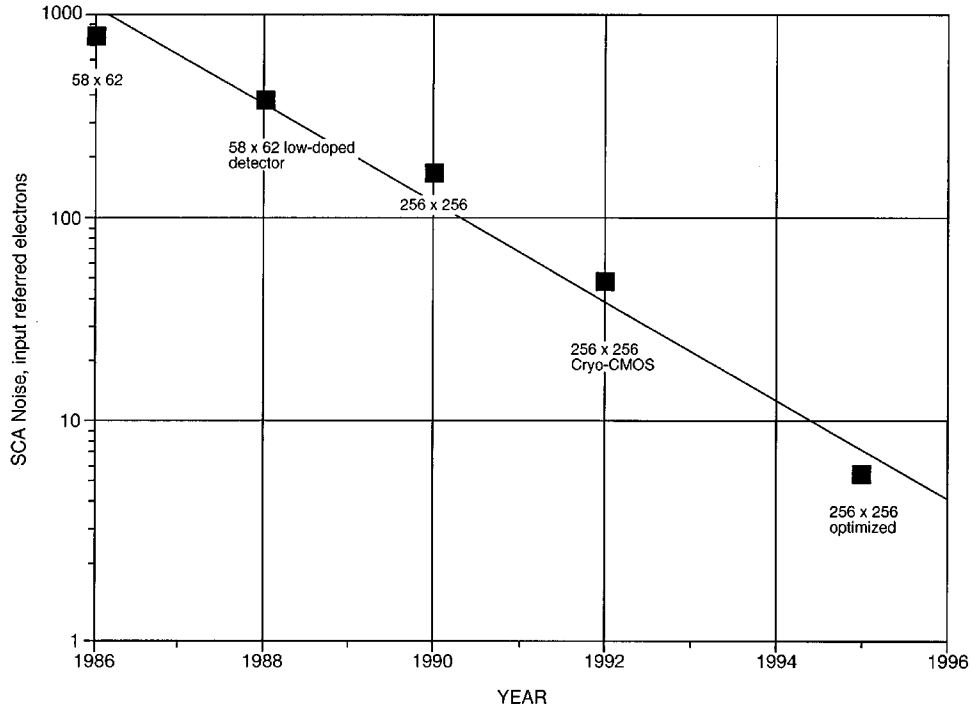

FIG. 1. Read noise for SBRC astronomy SCAs over the last decade.

signal from the columns and a slow scanner that enables the rows. There are eight clocks and ten biases required for the operation of the FPA.

There are two features built into the architecture of this device. The first feature is the nondestructive read, which is necessary for multiple sampling, as required for low read noise.[3–5] The second feature is the flexibility of the scanners. The design of the scanners allows for the capability of accessing data for the full array as well as a subarray, simply by adjusting the clocking pattern. It is possible to burst to the desired row or column, read that portion, and then either burst again to the end or terminate the scan and reset the shift registers. The development of the CRC-744 built upon the success of the CRC-463 readout, which is also a SFD readout.[6,7]

Major changes incorporated into the present readout in both the processing and design were made to reduce noise at the desired low temperature. Changes in fabrication included both starting material and processing steps. Since freeze-out at these low temperatures is a well known cause of increased read noise (as in Fig. 2 of Ref. 7 when $T<25$ K), it was important to address all the possible improvements needed to mitigate this phenomenon. In addition to theoretical analysis, actual lot splits which varied both the starting material and the processing were made to confirm the hypotheses: the final SIRTF design readout was chosen from these lot splits. The splits were distributed to give both good yield for the most optimal process and to also confirm the mechanisms for performance enhancement.

The most significant design changes made were in the

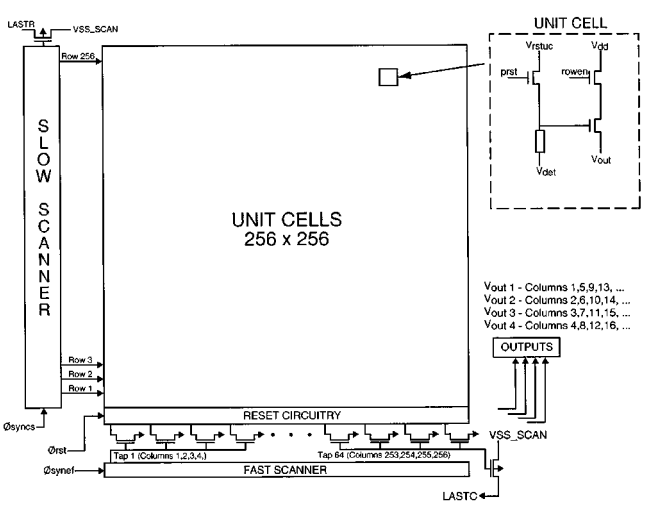

FIG. 2. CRC-744 readout.

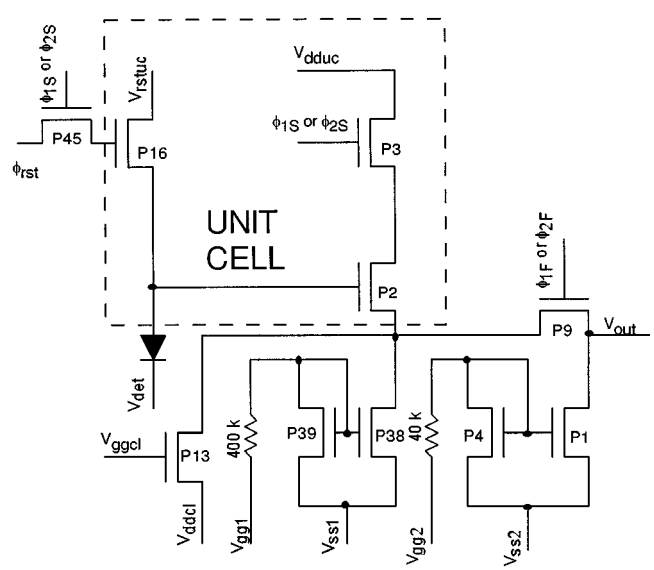

FIG. 3. CRC-744 unit cell.

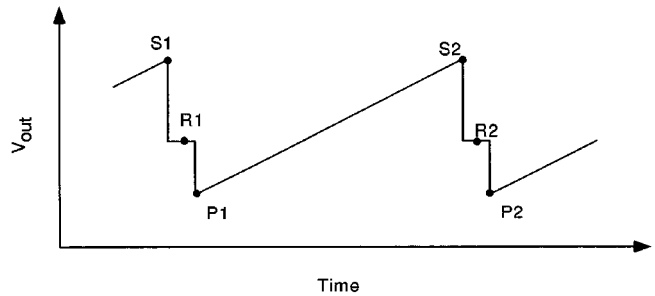

FIG. 4. Schematic showing the output from one pixel vs time and the correlated triple sampling (SRP) mode. S, R, and P refer to the signal, reset, and pedestal levels. In this mode, four levels ($P1$, $R1$, $S2$, and $R2$) are sampled and the combination $(S2-R2)-(P1-R1)$ is recorded, where $P1$ and $R1$ refer to the pedestal and reset levels in the beginning frame and $S2$ and $R2$ refer to the signal and reset levels in the end frame. However, since 256 unit cells in each row of CRC-744 are reset together, it is only possible to perform true correlated triple sampling on the first four unit cells in each row.

unit cell itself (see Fig. 3). The configuration was from a four transistor architecture (as in the CRC-644 and CRC-463 multiplexers) to a three transistor architecture (as in the SBRC Aladdin 1024×1024 readout, SBRC-084). With this design, the unit cells are reset by row. This minimizes the time necessary to reset the whole array (about 256×15 μs), which is advantageous for (''Fowler'') or sampling up the ramp (SUR) nondestructive multiple sampling.[3,8] However, it is not possible to perform correlated double or triple sampling (see Fig. 4) with this architecture in the same way as with the CRC-463. A new program was written to clock the CRC-744 multiplexers (muxes) in Fowler sampling mode. However, as discussed in Sec. III, we used the CRC-463 clock program to make noise measurements in correlated triple sampling mode. A further modification was the inclusion of a clamp circuit (V_{ggcl} and V_{ddcl} in Fig. 3). This reduces the clock feed-through to the detector integrating node.

III. EVALUATION OF MUX LOT SPLITS

Four CRC-744 muxes were tested, one from each of the low temperature optimized splits (Lawrence 2 μm process, Lawrence 3 μm process, standard cryo-CMOS process, and TRW 2 μm process). The tested muxes are listed in Table I. There was a fifth split, optimized for operation at $T\sim 30$ K, which has not been tested.

TABLE II. Clock settings.

Clocks	Active (V)	Inactive (V)
ϕ_{rst}	−5.5	−3.0
$\phi_{\mathrm{sync}S}$	−7.0	−1.0
ϕ_{1S}	−7.0	−1.0
ϕ_{2S}	−7.0	−1.0
$\phi_{\mathrm{sync}F}$	−4.0	−1.0
ϕ_{1F}	−4.0	−1.0
ϕ_{2F}	−4.0	−1.0
ϕ_{ggcl}	−5.0	−1.0

The first activity was to determine the clock patterns, clock voltages, and bias voltages to employ for best performance. The initial voltages and currents utilized came from the engineering design (see Tables II and Tables III). There were two areas of special concern. First, it was necessary to determine whether to use the current source per frame $P1$, or the current source per column $P38$ (see Fig. 3), to supply current to the unit cell amplifiers and second, it was necessary to determine how large the current should be. The design specifies each $P38$, which uses the current from V_{gg1} as the reference current and provides 1 μA; and $P1$, which uses the current from V_{gg2} as the reference current and provides 1 or possibly 10 μA. In turn, the current from V_{gg1} should be 4 μA and the current from V_{gg2} should be 4 or possibly 40 μA. A 400 kΩ resistor was used with V_{gg1} and a 40 kΩ resistor was used with V_{gg2}. Initial operation of the first mux at room temperature indicated better uniformity from row to row using $P1$ rather than $P38$. However later, when operating at $T\sim 6$ K, we observed a significant anomaly, namely that the signal level in the correlated triple sampling mode was 0.3 V higher than the pedestal level, with no illumination of the mux. These two levels should be approximately equal. It was found that turning V_{gg2} off (0 V) and V_{gg1} on (−3 V) cured this problem, and also gave a much more uniform Reset level. We concluded that the current source per column $P38$ gave superior performance. All the tests reported here used this current source. In addition, V_{dduc}, V_{ddout}, and ϕ_{rst} were also changed from −3.0, −1.0, and −2.0/−4.5 V to −3.5, −1.2, and −3.0/−5.5 V, respectively, to improve dynamic range. Later in the FPA tests, when the gate protection Zener diode was replaced by a 1 MΩ resistor, V_{gg1} was adjusted to give a reasonable wave

TABLE I. Test summary of CRC-744 bare muxes.

	Lawrence 2 μm	Lawrence 3 μm	Cryo-Std. CMOS	TRW 2 μm
Wafer No.	17	20	08	14
R-P charge dump (V) (output referred)	0.28	0.32	0.32	0.30
Time constant (μs) (rising, 5%–70%)	2.4	2.4	2.4	2.4
Time constant (μs) (falling, 70%–5%)	0.7	0.6	0.7	0.6
dc gain	0.827	0.873	0.863	0.827
Dynamic range of V_{rstuc} (V)	−3.85 to −2.75	−3.75 to −2.75	−3.95 to −2.95	−3.9 to −2.9
Current of V_{gg1} (μA)	⋯	4.2	4.0	⋯
Current V_{gg2} (μA)	0	0	0	0

TABLE III. Bias setting.

Biases	Volt	I_{park} (μA)[a]	I_{flat} (μA)[a]
V_{gg1}	-4.2[b]		
V_{gg2}	0.0		
V_{dduc}	-3.5		-105
V_{ssS}	-1.0		
V_{ssF}	-1.0		
V_{ddcl}	-1.9	-105	
V_{ddout}	-1.2	-260	-270
V_{ss1}, V_{ss2}	-1.0	105	105
V_{rstuc}	-3.5		
V_{det}	$V_{rstuc}+V_{bias}$[c]		
V_{sub}	0.0		

[a]Only currents more than 20 μA are noted.
[b]To provide -3.0 V at the chip carrier.
[c]V_{bias} is the applied back bias voltage across the photodiodes. For bare muxes. $V_{bias}=0$ V. For CRC744-40716, $V_{bias}=400$ mV.

form and dynamic range at the output, while maintaining low power dissipation. The unit cell current employed was about 0.4 μA. (In Table III, the V_{dduc} current when running flat out is the sum of the unit cell current from 256 unit cells.) This is considerably lower than the 1 μA employed for the bare mux tests. (In Table I, the V_{gg1} current is four times the unit cell current.) This may explain the improved stability observed with the FPAs compared with the bare muxes.

The next significant problem was resetting in the Fowler sampling mode: in this mode, the array is reset and the average of n pedestal levels are subtracted from the average of n signal levels in the same integration ramp. The technique initially used was to hold the reset clock on while clocking through all the rows, then turning it off. However, it was found that the Fowler pedestal and signal levels were significantly different from those seen in the correlated triple sampling mode, which cannot be correct. It was found that proper resetting in the Fowler sampling mode required selecting a row, then turning the reset clock on (for 15 μs), then turning it off, then selecting the next row. With this clocking, the Fowler pedestal and signal levels were quite comparable to those seen with correlated triple sampling. If one studies the schematic for the unit cell in Fig. 3, it makes sense that just holding the reset clock ON while enabling succeeding rows is not a good idea, since this could leave the reset field-effect transistor (FET) of each unit cell in an ON state. After resetting, we want this FET to be in the OFF state, to allow the integrating node to debias from dark current and photocurrent.

The tests concentrated on the Fowler sampling mode. As shown in Figs. 5(c) and 5(d), this mode can lead to significantly reduced noise. All previous muxes we have tested showed poor performance in Fowler sampling mode at temperatures below about 23 K.[7] We also measured noise in the correlated triple sampling mode [signal-reset-pedestal (SRP) mode in our software] to compare with previous measurements of the CRC-590 and 644 muxes and also to evaluate this mode at low temperatures, in case the Fowler sampling mode proved to be unstable as it had for the CRC-590 and 644 muxes. Finally, the reset mode (R-G in our software) was also tested to check out the noise of the FETs with the unit cell gate (the gate of $P2$ in Fig. 3) held at the reset voltage V_{rstuc}. In Fowler and correlated triple sampling modes, we are sensitive to noise with that gate floating (the reset FET turned off).

For correlated triple sampling (Fig. 4) and R-G modes, our old clock program for the CRC-463, 590, and 644 was used. This would not be correct for actual array operation, since each unit cell is being reset 64 times, and only the first four pixels in each row have the correct integration time. However, we believe this to be a reasonable expedient when there is no signal or dark current, and we are just measuring the noise. When checking for response to visible light in the SRP mode, only the first four pixels of each row showed a large response.

The procedure employed was to cool to $\sim$5.5 K. Then the steps followed were:

(1) operate the mux and confirm reasonable operation;
(2) check the last row and last column diagnostic lines to verify correct operation of the shift registers;
(3) measure the gain by measuring the output voltage as a function of the reset voltage (V_{rstuc});
(4) shine optical light on the array and verify reasonable response (positive signals were seen);
(5) take data with 6 s integration times as the Dewar warms up (liquid helium runs out).

Two frames of data each in the SRP, R-G, Fowler-1, Fowler-8, and Fowler-32 were acquired (Fowler-n refers to Fowler sampling with n pairs of samples). Successive frames in the same mode were subtracted and a 25×25 region near the center of the array was analyzed. After correcting for the $\sqrt{2}$ factor for the two data frames, the rms noise in this region gives the pixel read noise. The average difference between the two frames, which should be close to zero, was examined in order to investigate instability, commonly seen in Fowler sampling mode at the lower temperatures. The bias frames (short integration dark current frames) were also studied. Bias frames should be zero for Fowler mode; nonzero values indicate some instability. The SRP bias frame should also be close to zero. The R-G bias frame includes an arbitrary dc offset. It is examined to look for any drastic shifts in the operating point of the FETs, for example, caused by freeze-out.

The 25×25 region examined was positioned near array center. For Lawrence 2 μm material and TRW 2 μm material, it was centered at (row,column)=(128,128). For the other two muxes it was centered at (row,column)=(100,100) to avoid a bad pixel. The conversion from measured ADUs to voltage (referred to the input) was based on the measured dc gain, our gain of 20 preamplifiers, and the fact that 10-V for our analog digital converters (ADCs) gives 32 768 analog digital units (ADUs). The conversion to electrons was based on the estimated node capacitance (without detectors) of 27.7 fF from the engineering design. Figure 5 shows the noise measurement results. Figure 6 illustrates the instability test results for Fowler mode with 32 sample pairs.

From our bare mux data, Lawrence 2 μm material appeared to be superior. Above 18 K, Fowler sampling modes appear well-behaved and the noise with 32 pairs of samples

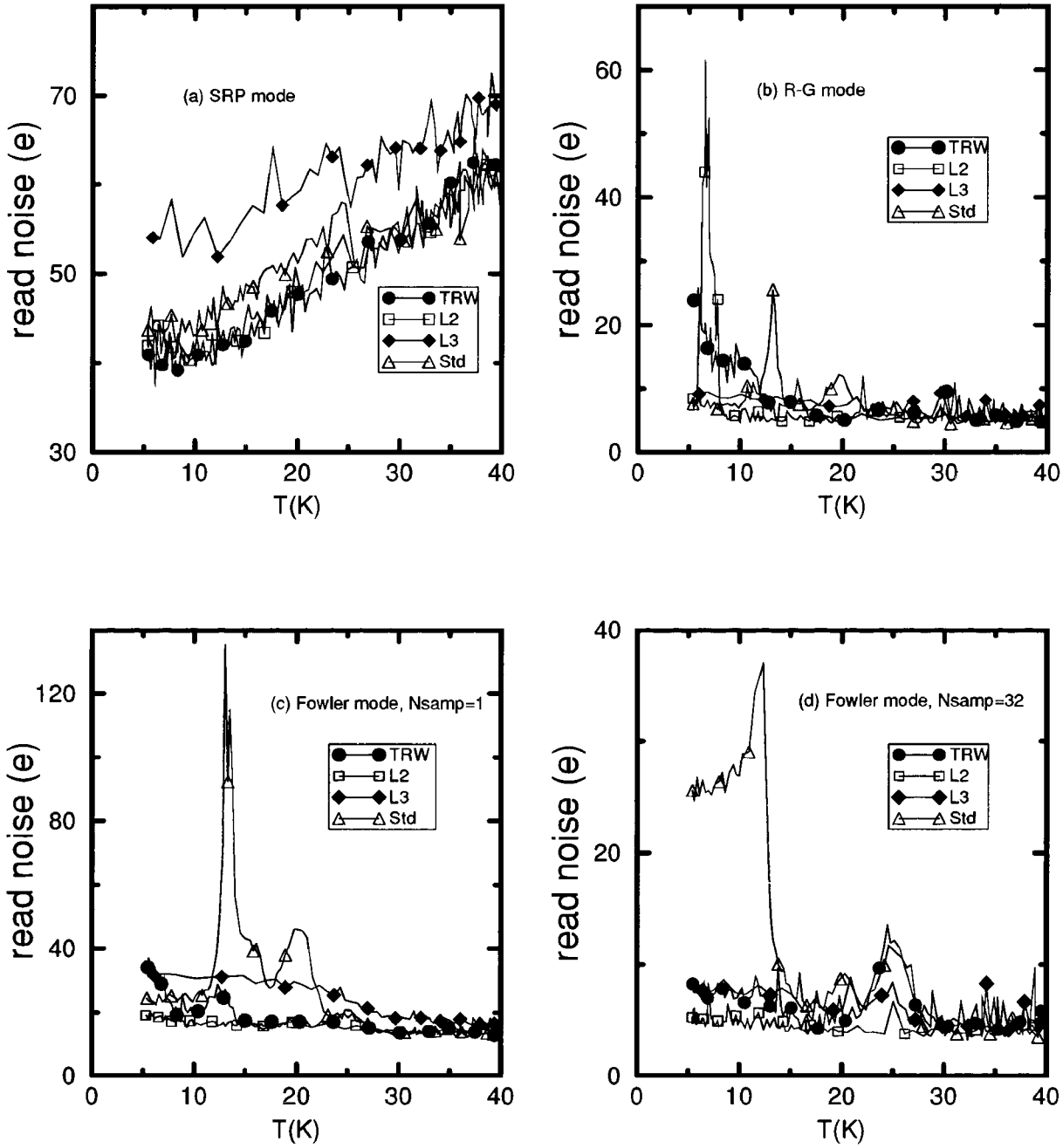

FIG. 5. Read noise vs temperature in SRP mode, R-G mode, and Fowler mode with one sample pair and Fowler mode with 32 sample pairs for Lawrence 2 μm, Lawrence 3 μm, standard cryo-CMOS, and TRW 2 μm muxes.

is about 4 e^- or 27 μV. Below 18 K, there was some instability in the Fowler modes. Lawrence 3 μm material was the next best, although it has somewhat higher noise and more instability in the SRP mode. Lawrence 2 μm and Lawrence 3 μm materials originate from the same manufacturer, differing only in epitaxial thickness. Standard cryo-CMOS material was well behaved in the SRP mode, but shows substantial instability in the Fowler mode. We compared its performance to CRC-590 and 644 muxes we have tested earlier (also standard cryo-CMOS) and they are roughly comparable. TRW 2 μm material performed well in the SRP mode. It was reasonably good above 15 K in Fowler modes, but showed an annoying noise peak at 25 K. Below 15 K, the instability in the Fowler mode was a little larger than for the Lawrence materials.

IV. FPA TESTS

SBRC indium bump-bonded low doped (1.7–2.0 $\times 10^{14}$ cm^{-3}) and undoped ($\sim 1.0\times 10^{14}$ cm^{-3}) Firebird InSb to CRC744 muxes formed from Lawrence 2 μm and Lawrence 3 μm materials. The best six FPAs using CRC-744 muxes and InSb detectors have been tested at the University of Rochester. Tests of noise, mux stability, and QE were made as the Dewar warmed up from 5 to 50 K, after exhaustion of the LHe supply exactly as described for the bare mux tests. For noise and mux stability tests, the detector

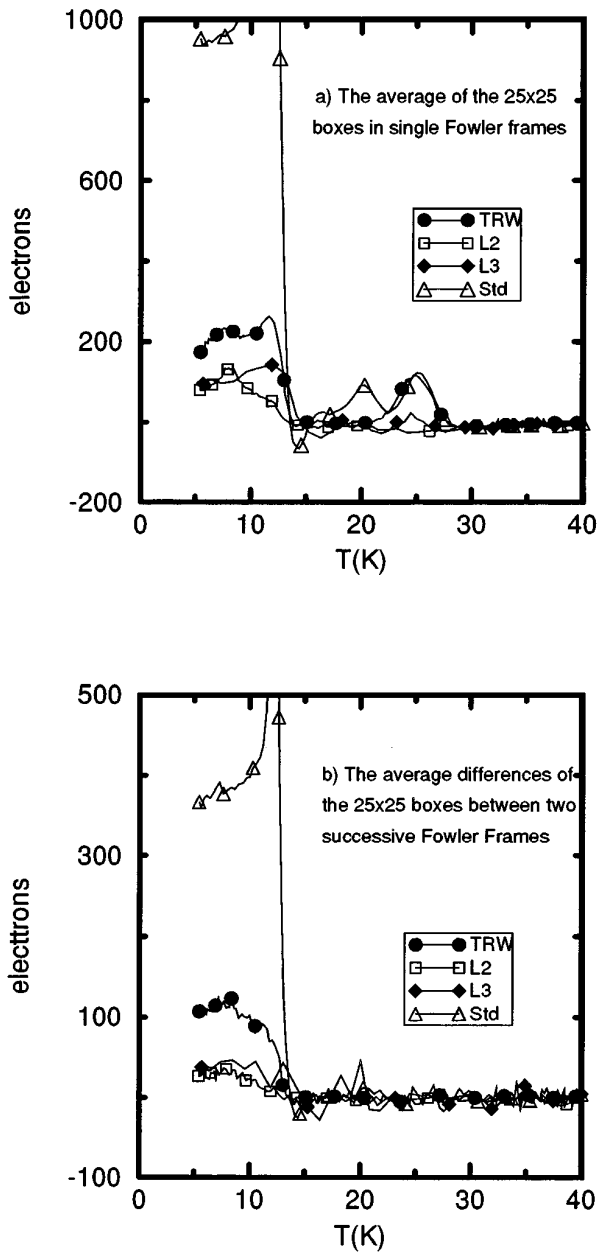

FIG. 6. Instability in Fowler mode with 32 sample pairs.

viewed our cold dark slide. For the QE tests, data were taken through a 3.3 μm filter viewing the laboratory. It took about 30 min for the arrays to warm up from 10 to 20 K during which time 12 data sets were acquired. More detailed and accurate tests of read noise, QE, and dark current were made with the temperature stabilized around 14.5 and 28.5 K. The operating voltages and currents for the arrays are presented in Tables II and III.

The FPA performance was more stable than that of the bare muxes. They showed smaller differences between two successive frames in the same mode and smaller Fowler ''bias'' frame values than the bare muxes. Most of the FPAs showed low noise, small dark current, and high QE. The FPAs made from Lawrence 2 μm muxes had hundreds of e^- of dark charge in the dark images, which caused unexplained nonlinearity in dark current versus integration time curves. In addition, some FPAs made from Lawrence 2 μm muxes

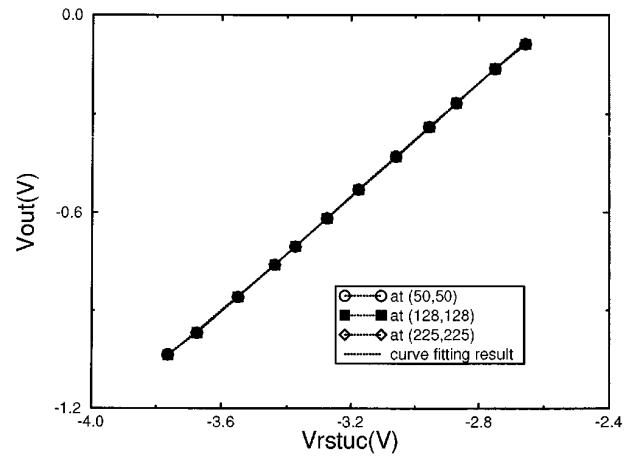

FIG. 7. The reset voltage measured at the output amplifiers vs the reset voltage applied to the integrating node at 14.5 K for FPA CRC 744-40716.

showed a quite wide distribution of zero bias points, which required operation at very high applied detector bias (800 and 1250 mV). Therefore, the FPAs made from Lawrence 3 μm muxes were judged to give better overall performance.

Among all the FPAs, CRC744-40716, which has a Lawrence 3 μm mux bonded to a Firebird low doped InSb array, exhibits the best overall performance. Its best read noise of 5 e^- was obtained using the Fowler sampling mode with 64 sample pairs at 15 K. The dark current images for this array were reasonably uniform and there were only a few hot pixels. At both 14.5 and 28.5 K, the 3σ upper limit to the dark current was $<0.2\ e^-$/s/pixel. The average quantum efficiency in the whole array is 87% at both 14.5 and 28.5 K. The central part of the array has somewhat lower quantum efficiency (78% at 14.5 K and 82% at 28.5 K) and it decreases when the temperature is reduced. This behavior is anomalous, and is under current investigation. The power dissipation and load driving capability at 14.5 K was also measured for this array.

The following discussions will concentrate on CRC744-40716.

A. Calibration

The dc gain of the multiplexer was determined from the slope of the reset level measured at the output amplifiers versus the reset voltage applied to the integrating node (see Fig. 7). At both 14.5 and 28.5 K, it was 0.87 throughout the whole array.

To calibrate our voltages to the charge collected on the integrating node, the noise^2 versus signal method was used. The read noise in Fowler mode with one sample pair and the signal were measured in three 25×25 pixel boxes. The slope of the noise^2 versus signal gives the system gain in ADU/e^-. This information, in conjunction with the dc gain measurement (which gives the conversion ADU/V), determines the total capacitance of the integrating node.

The noise^2 versus signal curve was measured at both 14.5 and 28.5 K. Figure 8 shows the data obtained at 14.5 K. The capacitances calculated within three 25×25 boxes centered at (column,row)$=(x,y)=(50,50)$, (128,128), and (225,225) are summarized in Table IV. Since the capacitance

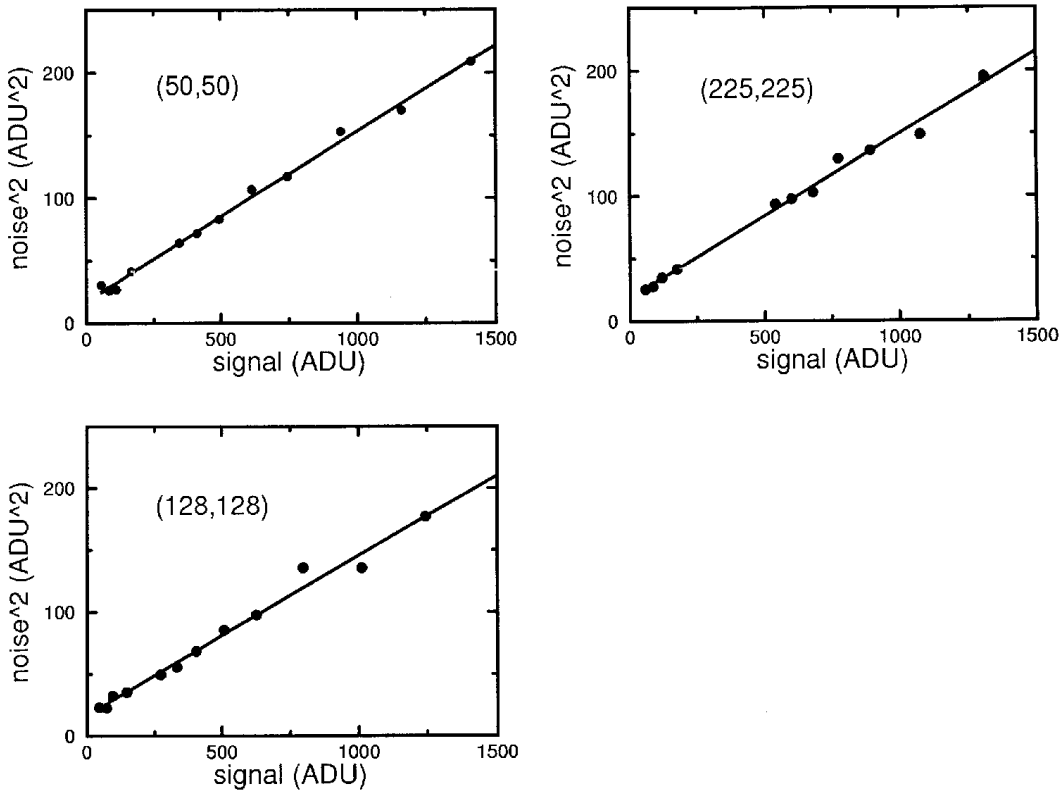

FIG. 8. Read noise squared vs signal at 14.5 K and three (x,y) positions on FPA CRC744-40716. The slope of the straight line fit is converted to unit cell capacitance and e^-/ADU in Table IV.

is a function of the bias voltage, when the signal increases the noise^2 versus signal curve deviates from a straight line. Thus, only the data points with signal <1500 ADU were used for curve fitting.

The capacitance does not change much between the two temperatures except in the box at (50,50) which includes some early forward biased pixels at 28.5 K. Therefore, the capacitances at 14.5 K were used in the calculations for both temperatures and an average capacitance of 0.069 pF was used for the whole array.

It is appropriate to use the capacitance obtained above to calculate the dark current or the read noise, since the signal is usually small for those measurements. However, for the QE measurement with a signal of about 3500–4000 ADUs, the change in capacitance caused by the detector discharge has to be considered.

The array is inherently nonlinear because the nodal capacitance increases as the InSb diodes discharge toward zero bias. We calibrate this effect by observing the signal, the change of the voltage across a detector caused by a constant light source, as a function of integration time t. For a constant discharge current, the signal is proportional to t and $1/C$, where C is the nodal capacitance. When normalized to its maximum value at zero signal, it gives C_0/C as a function of signal as shown in Fig. 9, where C_0 is the nodal capacitance at zero signal. It is evident that C_0/C is not a constant, which indicates the nonlinearity. The abrupt drop above 12 000 ADU in C_0/C results from detector saturation. We fit this curve before saturation to a straight line and use the curve-fitting results to determine the capacitance used for the QE calculation. The small signal capacitance quoted earlier was obtained by fitting the data with signals of 0–1500 ADUs (Fig. 8). The capacitance of 7.6 e^-/ADU obtained by the above fitting is good for the signal level around 600 ADUs. At 4000 ADUs, the approximate signal in the QE flat field, the capacitance is estimated to be 8.0 e^-/ADU.

B. Zero bias point and well depth

To obtain the zero bias voltage the array was exposed to a low level photon flux until it was saturated. The level of the photon flux was kept low in order to minimize the influence of the additional forward bias, caused by the photon flux, on the accuracy of the test results. A K filter ($\lambda_0 = 2.23\ \mu$m) and room illumination of the array were used for this purpose. The time to saturate was about 60 s at 14.6 K and about 40 s at 28.5 K. The amount of signal collected with low level

TABLE IV. Capacitance (pF) at 400 mV applied bias.

T (K)	(50,50)	(128,128)	(225,225)	Average
14.5	0.067 (7.3e^-/ADU)	0.071 (7.7e^-/ADU)	0.070 (7.6e^-/ADU)	0.069 (7.6e^-/ADU)
28.5	0.050 (5.5e^-/ADU)	0.074 (8.1e^-/ADU)	0.069 (7.6e^-/ADU)	⋯

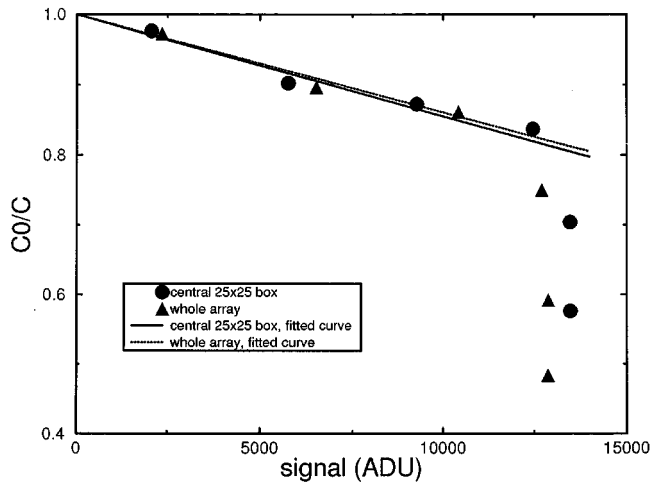

FIG. 9. Measurements of FPA CRC744-40716 nonlinearity: C_0/C vs signal level, C is the nodal capacitance as a function of signal and C_0 is the nodal capacitance at zero signal.

saturation is the well depth. The zero bias point is simply the well depth subtracted from the applied bias.

The well-depth data under 400 mV applied bias at 14.6 and 28.5 K are summarized in Table V. Well depth decreases as temperature increases. The average zero bias point of the whole array is a little higher than that of the central box.

C. Quantum efficiency

Figures 10 through 13 show flat-field images and QE histograms at 14.5 and 28.5 K, and the data are summarized in Table VI. The data were taken at an applied bias of 400 mV, a 0.172 s integration time, and using a 3.256 μm broadband filter ($\Delta\lambda = 0.220$ μm). The optical area was assumed to be $(30\ \mu\text{m})^2$ (i.e., 100% fill factor). The flat field images are fairly uniform across the whole array. However, some ''tree-rings'' (intrinsic to the InSb array) can be seen and the central part has lower quantum efficiency. The average quantum efficiency at 14.5 K is 87% for the whole array and 78% in the central 25×25 box (see Table VI). The average quantum efficiency at 28.5 K is 87% for the whole array and 82% in the central 25×25 box. Figure 14 shows the quantum efficiency versus temperature for the central 25×25 box and the whole array.

D. Dark current

Images of the cold dark slide at different integration times were taken in the Fowler mode with 32 sample pairs at 14.5 and 28.5 K. Dark signal data obtained from a 25×25 box at the center of the array, in which there are no hot pixels, are presented in Table VII. No Fowler bias has been subtracted.

By fitting the data in Table VII to straight lines, the slope is found to be $0.01 \pm 0.04\ e^-/\text{s}$ at 14.7 K and $0.08 \pm 0.04\ e^-/\text{s}$ at 28.5 K. Taking the mean slopes plus three times their standard deviations as the upper limits to the dark current, the dark current is $<0.2\ e^-/\text{s}$ for both temperatures. Figures 15–18 show the images and histograms of the differences of dark signals with integration times of 400 and 10 s at 14.7 and 28.5 K. It can be seen that the images are quite

TABLE V. Well depth (W.D.) and zero bias point (Z.B.P.) at 400 mV applied bias.

	T (K)	W.D. (ADU)	W.D. (e^-)	W.D. (V)	Z.B.P. (V)
Whole array	14.6	1.29×10^4	1.03×10^5	0.23	0.17
25×25 Central box	14.6	1.35×10^4	1.08×10^5	0.24	0.16
Whole array	28.5	1.0×10^4	8.0×10^4	0.18	0.22
25×25 Central box	28.5	1.1×10^4	8.8×10^4	0.19	0.21

TABLE VI. Quantum efficiency (%) at 400 mV bias.

	Whole array	25×25 box at (128,128)
$T = 14.6$ K	87	78
$T = 28.5$ K	87	82

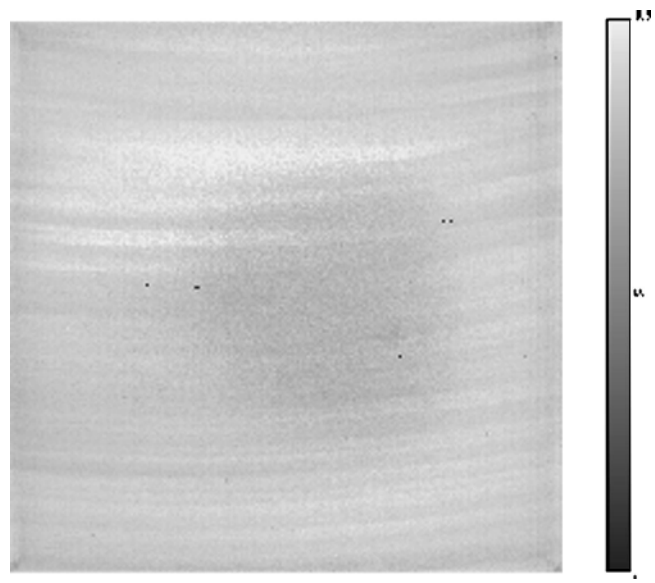

FIG. 10. QE (%) at 14.6 K for FPA CRC744-40716.

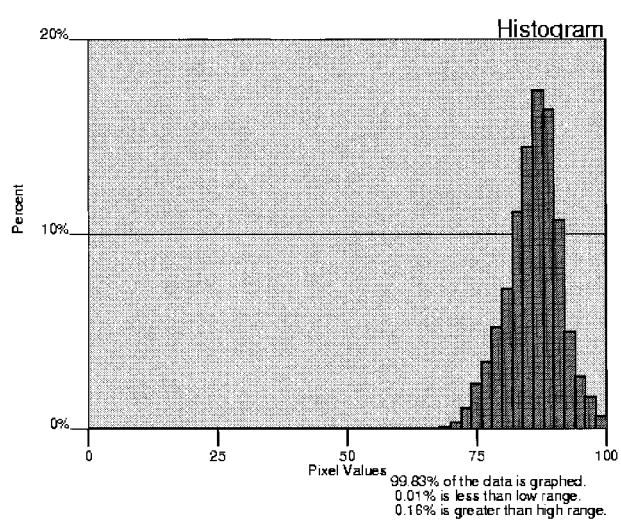

FIG. 11. QE (%) histogram at 14.6 K for FPA CRC744-40716. All pixels are included.

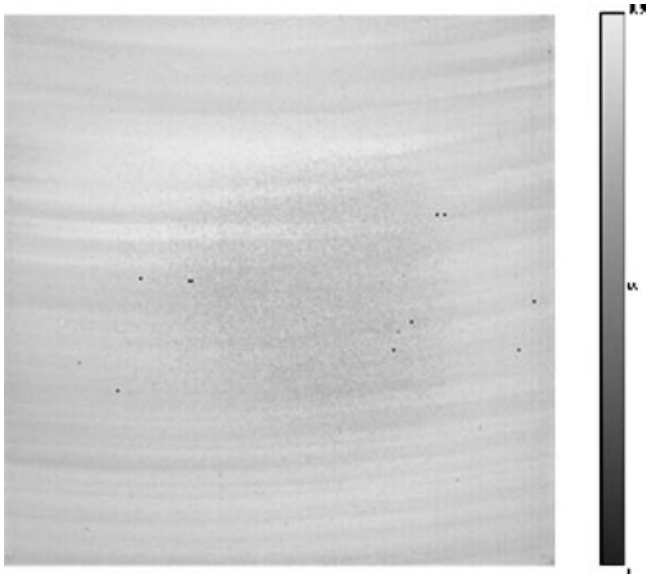

FIG. 12. QE (%) at 28.5 K for FPA CRC744-40716.

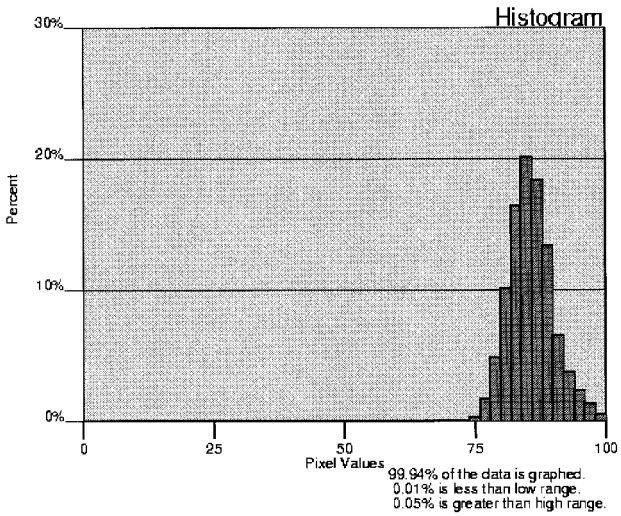

FIG. 13. QE (%) histogram at 28.5 K for FPA CRC744-40716. All pixels are included.

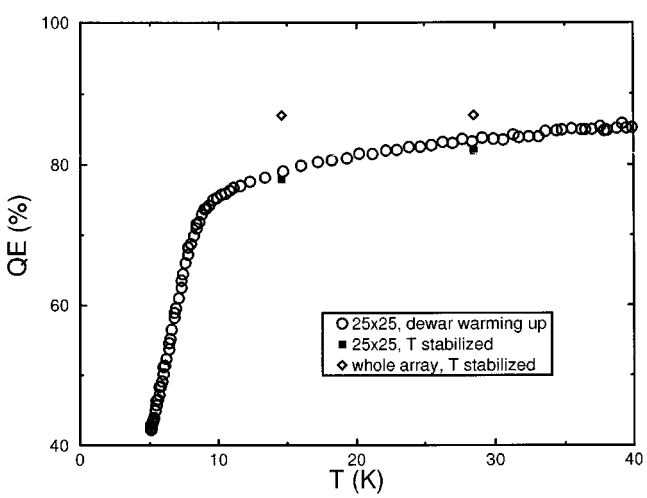

FIG. 14. QE of the central 25×25 box of FPA CRC744-40716 as the Dewar warmed up and when the fanout board was stabilized at 14.6 and 28.5 K. Also included are the average QE for the whole array when the fanout board was stabilized at 14.6 and 28.5 K.

TABLE VII. Dark signal (e^-) vs integration time (s) at 400 mV bias.

Integration time (s)	Dark signal at 14.7 K (e^-)	Dark signal at 28.5 K (e^-)
10	6.2± 7.3	9.2± 9.2
50	−15.4± 8.5	−12.3±10.8
100	8.5± 9.2	−4.6±11.6
200	0.8±10.0	13.9±13.1
400	3.9±13.1	30.8±14.6

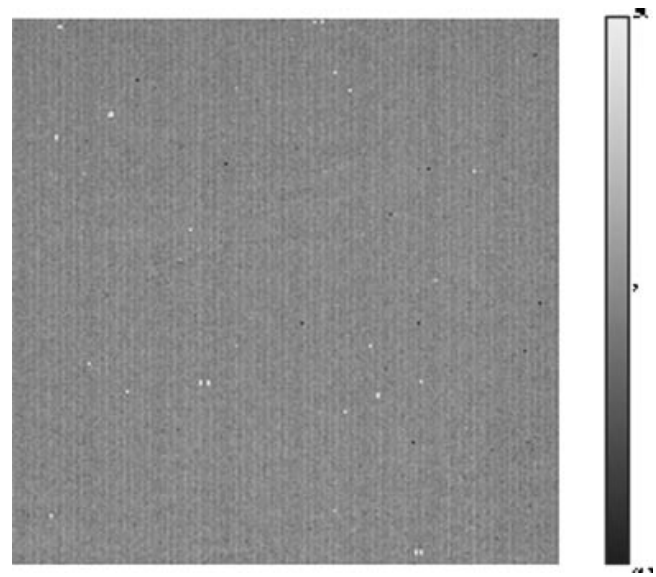

FIG. 15. Difference of dark images of FPA CRC744-40716 with 400 and 10 s integration times at 14.7 K (Unit: e^-).

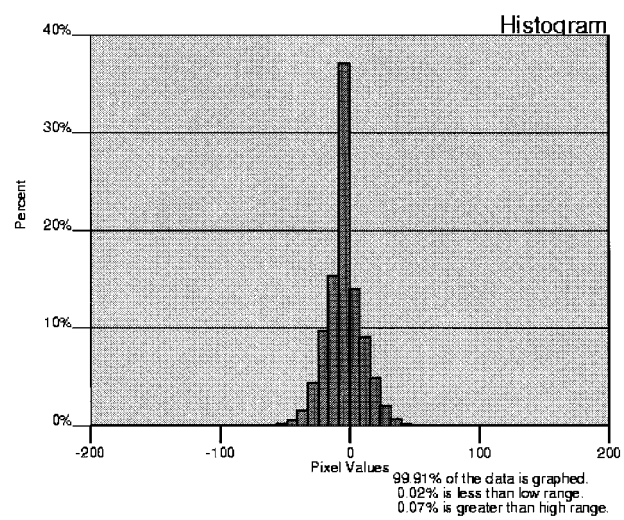

FIG. 16. Histogram of Fig. 15 (Unit: e^-). All pixels are included.

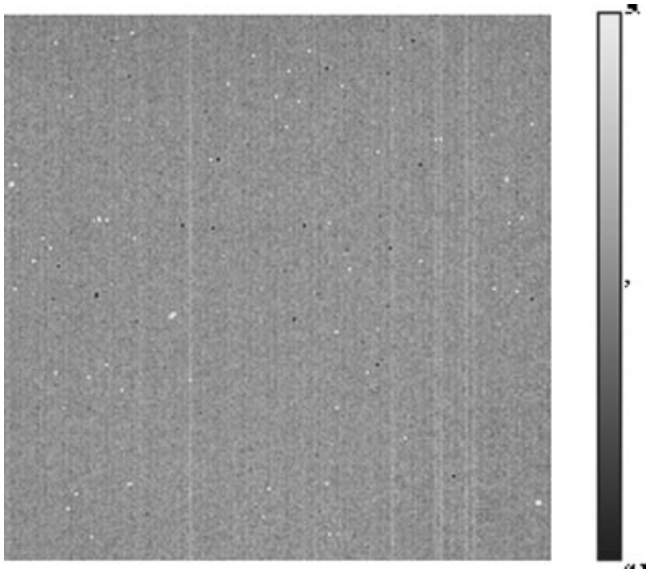

FIG. 17. Difference of dark images of FPA CRC744-40716 with 400 and 10 s integration times at 28.5 K (Unit: e^-).

uniform throughout the whole array and there are only a few hot pixels (the pixels with large dark current). The actual hot pixels are fewer than the large current pixels which can be seen in Figs. 15–18. Some large current pixels in Figs. 15–18 were caused by the remnant radiation from our Dewar which had been used in a proton radiation test five months ago. The 28.5 K histogram indicates that a real dark charge of $\sim 20\, e^-$ may be present; which would correspond to a dark current of $0.05\, e^-/\mathrm{s}$.

E. Noise

The read noise data were taken at 14.5 and 28.5 K with integration times of 6 s for 1–32 pairs of Fowler samples, 12 s for 64 pairs, and also 200 s for 1–32 pairs. Figure 19 shows the noise versus number of Fowler pairs at 14.5 K. The noise improves with increasing numbers of Fowler pairs up to the maximum of 64 pairs. This was true at 14.5 K as well as 28.5 K. Table VIII lists the noise obtained for 32 sample pairs

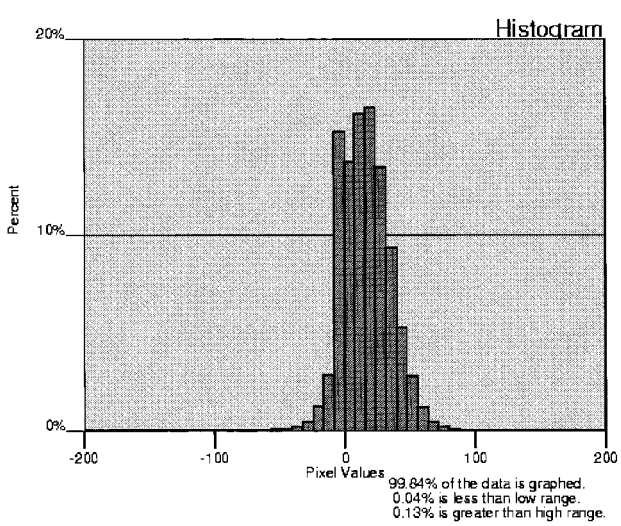

FIG. 18. Histogram of Fig. 17 (Unit: e^-). All pixels are included.

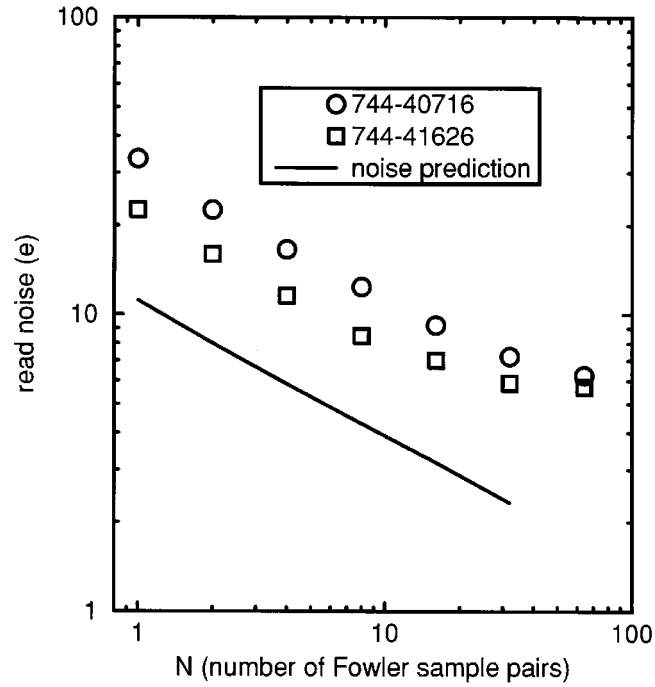

FIG. 19. Read noise of FPA CRC744-40716 and CRC744-41626 vs number of Fowler sample pairs N at 14.5 K. The modeling result described in the text is also plotted as the solid line. The 41626 FPA employs a 2 μm Lawrence mux.

with 6 s of integration time, 64 sample pairs with 12 s of integration time, and 32 sample pairs with 200 s of integration time at 14.6 and 28.5 K. At 200 s of integration time, the noise was about 50% larger than at 6 s. The 200 s performance is noticeably better at 14.6 K than at 28.5 K.

Figure 20 shows read noise in 6 s integration time with 1, 8, 32, and 64 Fowler sample pairs versus temperature. The data shown were obtained from a 25×25 box at the center of the array. From 5 to 40 K, the noise with 8 and 32-sample pairs increases very gradually as the temperature rises. It can be seen in Table VIII that the noise in the central 25×25 box for 32 Fowler sampling pairs and 6 s of integration time stabilized at temperatures of 14.6 and 28.5 K is about 1 e^-

TABLE VIII. Noise (e^-) at 14.5 K and 28.5 K, Fowler sampling.[a]

$N_{\mathrm{samp}}=32$, integration time=6 s	$(x,y)=(50,50)$	$(x,y)=(128,128)$	$(x,y)=(225,225)$
$T=14.6$ K	7.2(6.4[b])	6.9(6.2[b])	7.3(6.7[b])
$T=28.5$ K	7.5	7.7	8.4
$N_{\mathrm{samp}}=64$, integration time=12 s			
$T=14.6$ K	6.7(5.3[b])	5.8(5.2[b])	6.6(5.6[b])
$T=28.5$ K	6.9	7.3	7.9
$N_{\mathrm{samp}}=32$, integration time=200 s			
$T=14.6$ K	9.2	9.4	10.3
$T=28.5$ K	12.7	14.2	14.3

[a]Statistical uncertainty: $\pm 2\%$.
[b]After fixing a small problem in our preamp board.

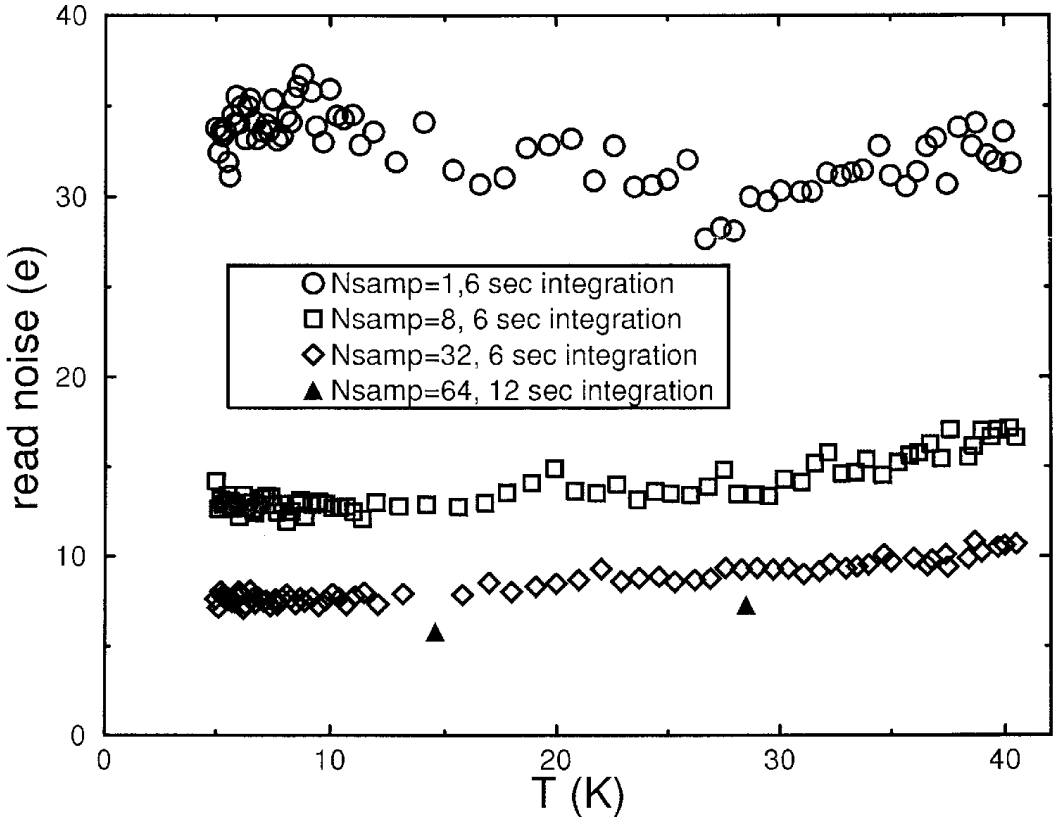

FIG. 20. Read noise in a 25×25 box at the center (128,128) of FPA CRC744-40716 vs temperature. The curves for $N_{\mathrm{samp}}=1,8,32$ were obtained in the Dewar warming up process and the statistical uncertainty in each point is $\pm 0.04\sigma$. The two $N_{\mathrm{samp}}=64$ data points were obtained when the dewar was stabilized at 14.6 and 28.5 K and the statistical uncertainty in each point is $\pm 0.02\sigma$.

smaller than those displayed in Fig. 20 for similar conditions. Two factors may cause this difference:

(1) The data in Table VIII were acquired when temperature was stabilized, whereas the data in Fig. 20 were obtained as the Dewar warmed up.
(2) When acquiring the data in Table VIII, after a parameter, e.g., the number of samples was changed, the same measurements were performed four times, and the average was obtained. However, when acquiring the data in Fig. 20, Fowler mode noise measurements with different numbers of samples were interspersed with SRP and R-G mode noise measurements, and Fowler mode QE measurement. It is a less stabilized situation and could contribute to a small increment in read noise.

Recently, after fixing a small problem in our pre-amp board, we achieved 5 e^- of read noise for CRC744-40716 with 12 s integration time and 7 e^- for CRC744-41626 with 200 s integration time at 15 K with 64 sample pairs.

The FPA read noise of the Fowler sampling mode[3,4] should be dominated by the voltage noise of V_n of the source follower metal-oxide-semiconductor field-effect transistor (MOSFET) in the unit cell. This can be calculated from

$$\delta n = C_v \sqrt{\int_0^\infty \frac{V_n^2}{\Delta f} \frac{2[1-\cos(2\pi f \tau_{\mathrm{int}})]}{1+(f/f_0)^2} \frac{\sin^2(N\pi f \tau)}{N^2 \sin^2(\pi f \tau)}\, df},$$

where δn is the read noise in electrons, C_v is the integrating node capacitance in e^-/V, $V_n^2/\Delta f$ is the power spectral density of the source follower FET, N is the number of Fowler sample pairs, f_0 is the 3 dB cutoff frequency of the bandwidth-limiting RC filter, τ_{int} is the integration time, and τ is the time between two successive sample pairs. From measurements on various FETs using the same processing employed for the CRC744, the FET noise power spectral density $V_n^2/\Delta f$ can be estimated. Scaling to the size of the unit cell FETs at a temperature 14.5 K this becomes

$$\frac{V_n^2}{\Delta f} = \left(1.5\times 10^{-16} + \frac{5.1\times 10^{-12}}{(f/\mathrm{Hz})^{0.77}}\right)(\mathrm{V}^2/\mathrm{Hz}),$$

with $f_0 = 1\ \mathrm{MHz}/2\pi$ of the RC filter preceding our A/D converters. The second term, the flicker noise, is much more important than the first term, the white, or thermal, noise. This noise prediction at 14.5 K is plotted in Fig. 19 in comparison to the measured read noise from two CRC744 InSb FPAs.

F. Power dissipation

The power dissipation at 400 mV bias and around 14.5 K was measured with the FPA running in the following four different readout modes: flat-out with output amplifiers on, flat-out with output amplifiers off, park-mode with output amplifiers on, and park-mode with output amplifiers off. The measurements are described as follows: fanout temperatures were measured at ''power off,'' in which all voltages to all pins were set to zero, and in each of the above readout

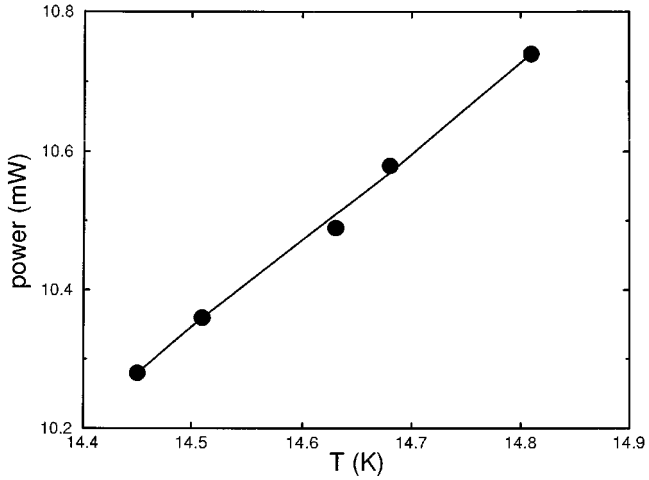

FIG. 21. Fanout temperature vs heating power. The straight line has a slope of 1.28 mW/K.

modes. In order to convert fanout temperature to power dissipation, fanout temperature versus heating power of a 1 kΩ resistor (heater or auxiliary heater) was measured in the power off mode. The difference in the power required to heat the fanout board to the temperatures measured in one of the four readout modes, and the heating power to keep the fanout board at the power off temperature, was taken as the corresponding power dissipation for that mode. The flat-out mode was realized by running the array with one Fowler sample pair, 10 μs clamp-to-sample time, and 172 ms integration time to reach 100% duty cycle. For the park-mode, the array ''parked'' between two frames. V_{ddout} was set to either -1.2 V or 0 V in order to turn the output amplifiers on or off.

There are 19.1 MΩ resistors protecting the lines leading to the gates of 744-40716 and two others to the unused pins for V_{guard}. The power dissipated by these resistors is about 117 μW when the arrays are parked between readouts and 156 μW when the arrays are running flat-out. In the power off mode, there is no power dissipation from 1 MΩ protective resistors. There is also some power dissipated in our 400 kΩ V_{gg1} resistor on the order of $\sim 6\ \mu$W.

Figure 21 shows the fanout temperature versus heating power. From these data the temperature to heat-load conversion factor is 1.28 mW/K. Table IX shows the power dissipation using different readout modes. When measuring the

TABLE IX. Power dissipation of CRC744 near 15 K.

1.28 mW/K Readout mode	Amplifier status	P.D. (mW)[a]	Net P.D. (mW)[b]	Net P.D. (mW)[c]
Park-mode	on	0.34	0.22	0.24
Park-mode	off	0.17	0.05	0.10
Flat-out	on	0.47	0.31	0.40
Flat-out	off	0.32	0.16	0.21

[a]Measured power dissipation, including the power dissipated by the 1 MΩ protective resistors.
[b]Measured power dissipation, minus the power dissipated by the 1 MΩ protective resistors.
[c]Calculated power dissipation, with current and voltage drop data, excluding the power dissipated by the 1 MΩ resistors.

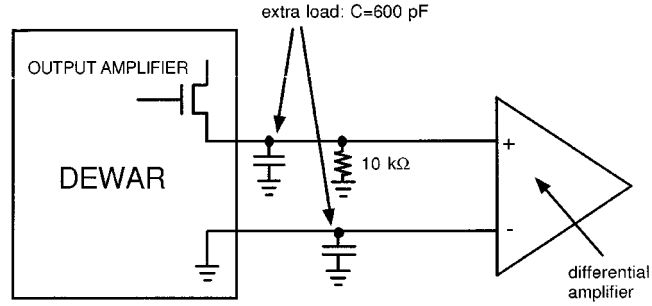

FIG. 22. Load driving measurements. Extra load: a 600 pF capacitor. Cable load: ~40 pF.

temperature of different modes, a heater voltage of 3.206 V was applied to keep the fanout board temperature ~14.5 K. Approximately 1 h was required to reach thermal equilibrium upon a change of mode. (The thermal time constant was measured to be about 17 min).

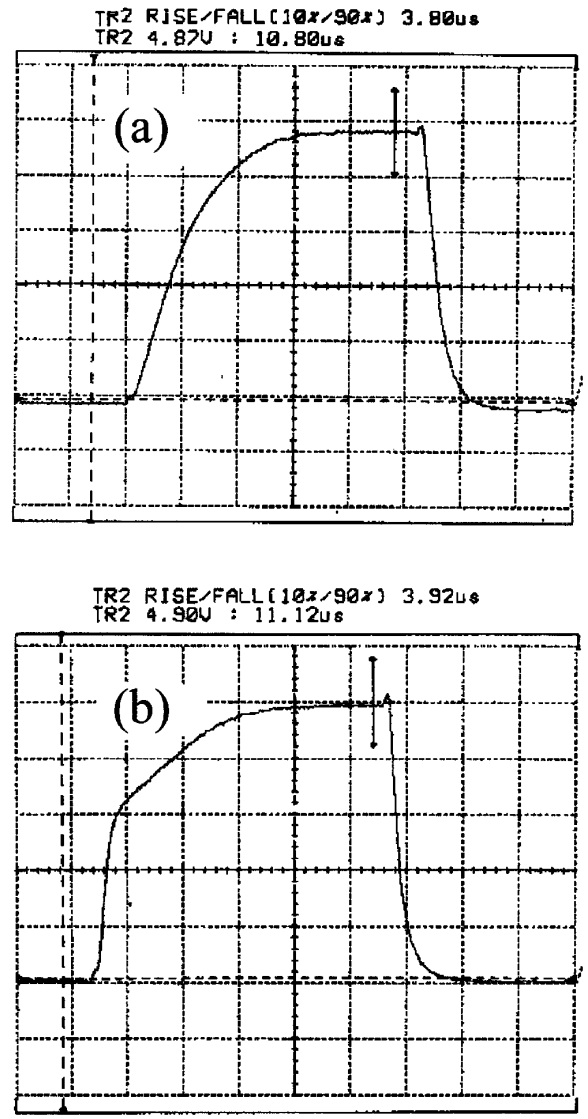

FIG. 23. The influence of a 600 pF capacitor on the wave form ($g\times 20$, horizontal: 2μs/div), vertical: 1(V/div): (a) with a 600 pF load, 10%–90% rise time: 3.9 μs, 90%–10% fall time: 1.2 μs; (b) without a 600 pF load, 10%–90% rise time: 4.1 μs, 90%–10% fall time: 0.9 μs. The test was on FPA CRC744-40716.

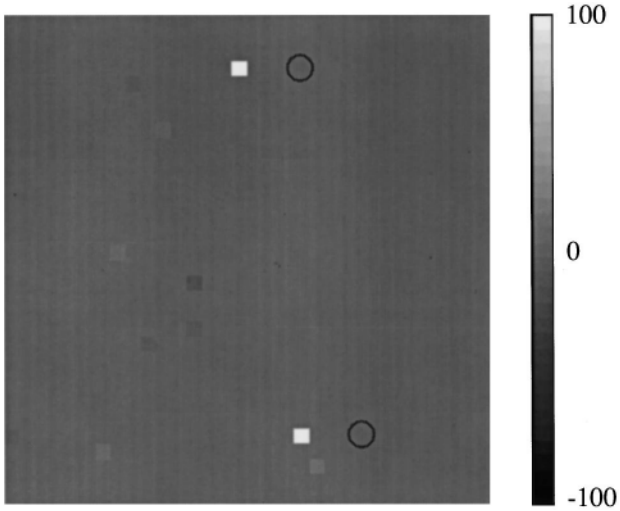

FIG. 24. No cross talk was found in the channel with a 600 pF load. The circle indicates the position of a cross talk pixel, four columns to the right of a hot pixel. (Unit: ADU).

From Table IX, it can be seen that the output amplifiers dissipate 0.15 mW running flat-out and 0.17 mW in park-mode. The whole array dissipates 0.31 mW running flat-out and 0.22 mW in park-mode.

The power dissipation can also be estimated by measuring the voltages and the currents drawn by different bias pins which are listed in Table II. Table II lists the voltages and the currents of those pins with current larger than 20 μA.

The four output amplifiers draw 260 μA in park-mode and 270 μA running flat-out. This current entered the mux from the sources of the four output amplifiers and came out through $V_{dd\mathrm{out}}$. Since $V_{dd\mathrm{out}} = -1.2$ V and the source of each output amplifier had a 10 kΩ resister to the ground, the voltage drop on the mux was 0.55 V for the park mode and 0.525 V when running flat-out. Thus the output amplifiers dissipate 0.14 mW in both modes.

V_{ssl} drew 105 μA in both modes. This current came from $V_{d\mathrm{duc}}$ when it ran flat-out and from $V_{d\mathrm{del}}$ when it was in the park-mode. The voltage drop is 2.5 V in flat-out mode and 0.9 V in park-mode. Therefore the power dissipation is 0.26 mW running flat-out and 0.10 mW in park-mode.

The last column of Table IX summarized the power dissipation calculated with the current and the voltage drop. Considering the uncertainty of the measurements, the power dissipation calculated from the currents and voltage drops are consistent with the measured values.

G. Load driving

In the IRAC SIRTF experiment, we expect to drive 600 pF lines. The load driving measurements were performed by adding a 600 pF capacitor to each input of two of the four channels as shown in Fig. 22. The original cable load was 40 pF.

The rise and the fall times were obtained by looking at some isolated ''hot'' pixels which were saturated by large dark current. The 600 pF load changes wave forms as shown in Fig. 23, although 10%–90% rise time (about 4 μs) does not change much. The 90%–10% fall time increased from 0.9 to 1.2 μs by introducing the 600 pF load. The noise for the channels with and without the 600 pF capacitors stayed about the same ($\sim 8.4\, e^-$) at $T = 14.6$ K with 20 s integration time and 32 Fowler sample pairs. Looking at the pixels four columns away from the hot pixels, which are the pixels addressed immediately after the hot pixels, no cross talk was found as shown in Fig. 24: the output of the pixel four columns away is $<0.3\%$ of the output of the hot pixel.

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