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Research Article

Development of Low-Noise Small-Area 24 GHz CMOS Radar Sensor

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We present a low-noise small-area 24 GHz CMOS radar sensor for automotive collision avoidance. This sensor is based on direct-conversion pulsed-radar architecture. The proposed circuit is implemented using TSMC 0.13 μm RF (radio frequency) CMOS ($f_T/f_{\max}$ = 120/140 GHz) technology, and it is powered by a 1.5 V supply. This circuit uses transmission lines to reduce total chip size instead of real bulky inductors for input and output impedance matching. The layout techniques for RF are used to reduce parasitic capacitance at the band of 24 GHz. The proposed sensor has low cost and low power dissipation since it is realized using CMOS process. The proposed sensor showed the lowest noise figure of 2.9 dB and the highest conversion gain of 40.2 dB as compared to recently reported research results. It also showed small chip size of 0.56 mm^2, low power dissipation of 39.5 mW, and wide operating temperature range of −40 to +125°C.

1. Introduction

The rapid evolution of wireless communications has resulted in a strong motivation toward building high performance SoC (System-on-a-Chip) in silicon. Particularly CMOS-based circuit is realizing its low cost and high level of integration. Thanks to these advantages, the growing demand for larger bandwidth also pursues CMOS-based circuits to move toward higher frequencies [1–4]. Recent works have shown these circuits as a promising technology for building high performance RF (radio frequency) circuits for applications above 20 GHz [5–8]. These systems for applications of above 20 GHz contain wireless sensor networks, various portable products, automotive collision avoidance radars, wireless local networks, LMDS (local multipoint distribution service), RTIS (Real Time Traffic Information System), and other ISM band applications. Most of all, automotive collision avoidance radar using 24 GHz band offers safety functions such as precrash sensing and collision. Most of the well-known car companies and suppliers are already working on the development of the next generation vehicle known as ASV (Advanced Safety Vehicle). The radar-based ACC (autonomous cruise control) at 77 GHz first introduced from Mercedes-Benz in 1999 is widely available in many high and mid class automotive models. In the last 15 years, silicon-based 24 GHz short-range automotive radars have been investigated by both industry and academia [5, 6]. Therefore, next generation radars may well be required to support 24 GHz band for compatibility and lower overall cost [5–9].

In this paper, we propose a low-noise and small-area 24 GHz receiver for the automotive radar. The proposed circuit is fabricated using TSMC 0.13 μm RF CMOS ($f_T/f_{\max}$ = 120/140 GHz) technology. The circuit is powered by a 1.5 V supply. It is designed using a direct-conversion scheme to simplify overall system complexity. Especially to reduce total chip size instead of real bulky inductors, transmission lines are used. We used the unique layout technique for 24 GHz RF band to reduce parasitic capacitance.

2. Radar Sensor Principle

Thanks to the higher positioning accuracy and its narrow bandwidth, frequency-modulated continuous wave (FMCW)

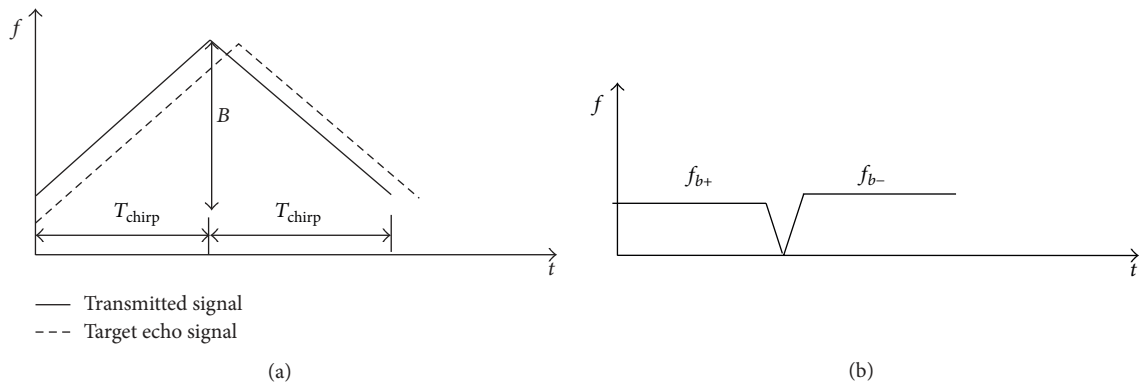

Figure 1: FMCW radar principle.

radar based on positioning techniques is often used in automotive radar systems [5]. The FMCW signal is a classical and well-known waveform for many different radar applications [7]. Generally the system bandwidth is described by B and the chirp duration is named T_{chirp} for up chirp and down chirp as shown in Figure 1(a). When the signal is transmitted, the radar echo signal is directly downconverted by the instantaneous carrier frequencies, f_{b+} and f_{b-}. These are the beat frequencies of up chirp and down chirp, respectively, as shown in Figure 1(b) [7].

For these cases related equations are expressed as (1) [7]. Consider

$$f_{b+} = \frac{2RB}{cT_{chirp}} - f_d$$
$$f_{b-} = \frac{2RB}{cT_{chirp}} + f_d \quad (1)$$
$$f_d = \frac{2v}{\lambda},$$

where R is the target range, c is the speed of light, f_d is the Doppler frequency produced by moving target, and λ is the wavelength of the carrier frequency. From (1), we can obtain the target range R and the radial velocity v by the following equations:

$$R = \frac{(f_{b+} + f_{b-})\, cT_{chirp}}{4B}$$
$$v = \frac{(f_{b+} - f_{b-})\, cT_{chirp}}{4}\lambda. \quad (2)$$

If there is another radar operation with the same modulation scheme and the same frequency band, mutual interference will occur.

3. The Proposed Radar Sensor

3.1. The Proposed Radar Sensor. The proposed sensor is based on the direct-conversion pulsed-radar architecture shown in Figure 2. The radar senses RF pulses at a rate determined by the *prf* (pulse repetition frequency). The presence of an object is detected in R_x by correlating the reflected pulse with a delayed version of the transmitted pulse. To detect targets over a wide range of 0.1 to 50 m, it is necessary to have a widely tunable delay between pulse transmission and sensor correlation. Most of all, to obtain longer range and higher range resolution, it is necessary to incorporate variable *prf* and pulse width [8]. To meet these requirements, the CMOS baseband pulse generator shown in Figure 2 can generate pulses with widths ranging from 100 ps to 1 ns (*pw*[5:0]), with a variable *prf* of 1 MHz to 1 GHz (*prf*[12:0]). The delay of R_x trigger can be tuned from 1 ns to 0.2 μs (*delay*[12:0]), corresponding to the 0.1 to 50 m radar range. 50 m might be sufficient for speed below 100 km/h. The *prf* generation circuit is clocked by the 100 MHz reference input of the synthesizer. The 1 GHz clock required for R_x trigger generation is derived from a divider output in the PLL. To input the control bits of the pulse generator, an on-chip JTAG TAP interface is used.

3.2. Each Block Design of the Proposed Radar Sensor

3.2.1. Low-Noise Amplifier. Figure 3 shows a 24 GHz two-stage cascode LNA (Low-Noise Amplifier) with inductive degeneration. It is fabricated using TSMC 0.13 μm mixed-signal/RF CMOS process (f_T/f_{max} = 120/140 GHz). The outputs of the second stage are combined into LC filter, so they allow sharing of the downconversion chain of the band. Although only one path is active at a time, an interferer from the other input can desensitize the broadband mixer. This circuit uses transmission lines of L_{T1}~L_{T10} to reduce total chip size instead of real bulky inductors for input and output impedance matching. It has fully symmetrical differential structure to improve linearity of amplifier and to reduce RF noise and unnecessary ripple variations. Series transmission lines of L_{T8} and L_{T10} are inserted to increase voltage gain, and parasitic capacitance from drain nodes of M_5 and M_6 are minimized by using oscillation effect. C_1 (or C_2), L_{T1} (or L_{T2}), and L_{T3} (or L_{T5}) are used to make input impedance matching at the first stage. Values of C_3, C_4, L_{T4}, L_{T6}, and

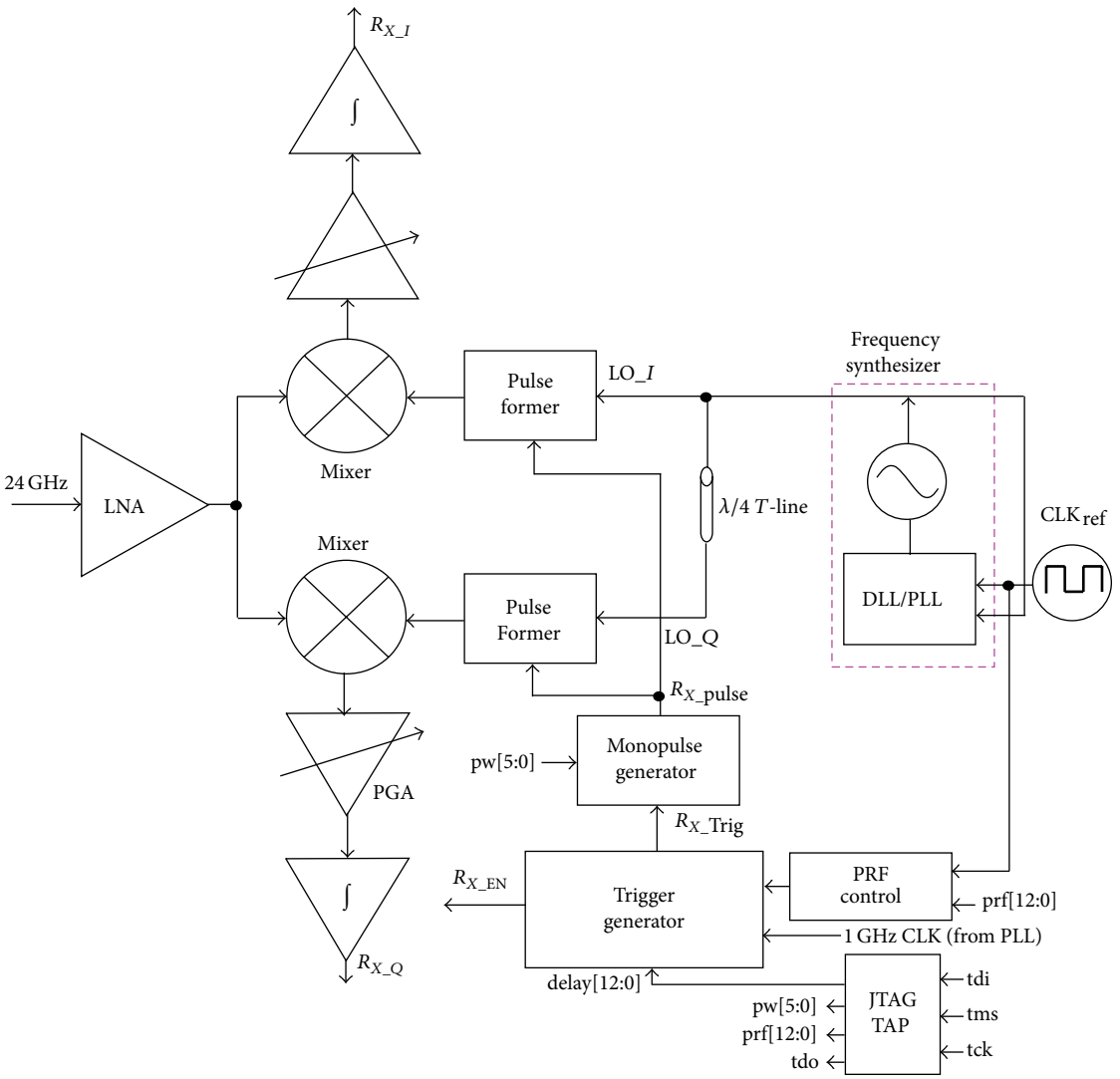

Figure 2: The proposed direct-conversion sensor.

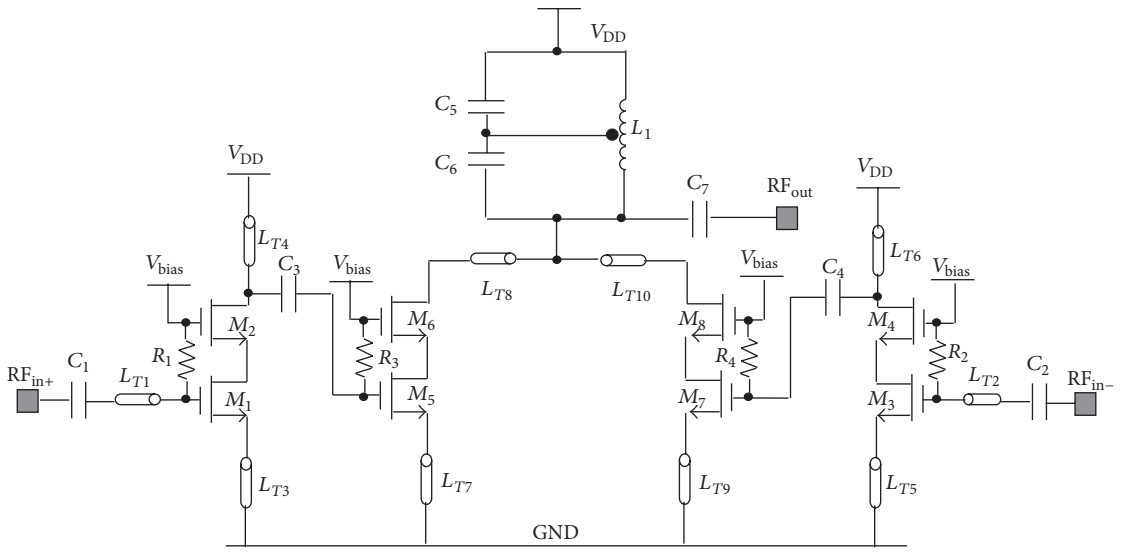

Figure 3: Low-noise amplifier for 24 GHz radar sensor.

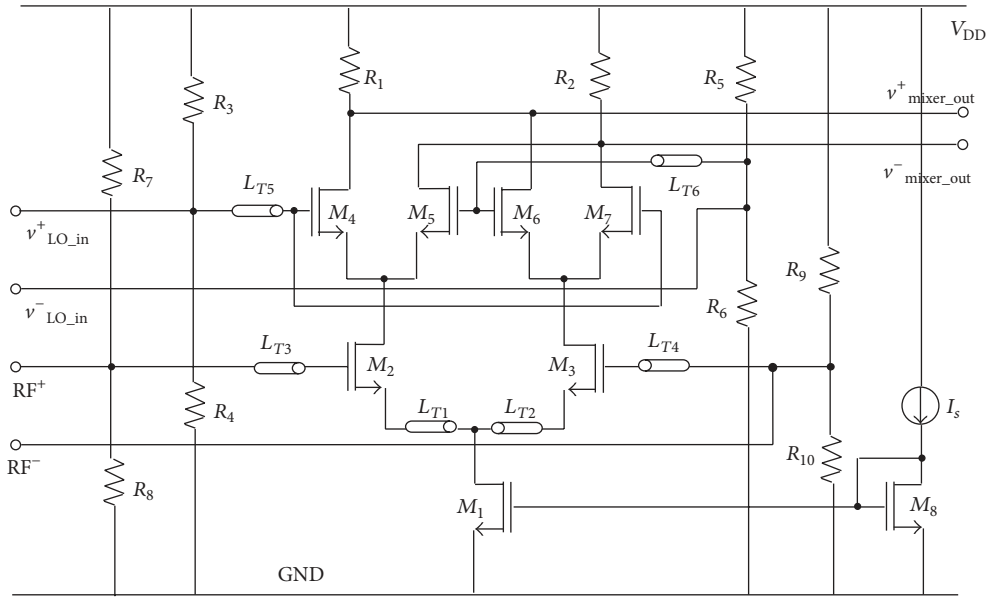

Figure 4: Gilbert-cell downconversion mixer.

L_{T7} are optimized to make input impedance matching at the second stage. L_{T4} and L_{T6} are inserted to supply stable dc in drain regions of M_2 and M_4.

The input impedance expressed in (3) is derived using RF small signal equivalent circuit:

$$Z_{\text{in(LNA)}} \approx \frac{g_{m1}T_3}{C_{gs1}} + j\left[\omega\left(T_1 + T_3\right) - \frac{1}{\omega C_{gs1}}\right], \quad (3)$$

where C_{gs1} is gate-to-source capacitance of transistor M_1 and its value is $C_{gs1} = 2WLC_{ox}/3 + WC_{gso}$.

Equation (4) is voltage gain derived using RF small signal equivalent circuit at the first stage, and C_3 (or C_4) is utilized to control voltage gain:

$$G_{\text{LNA}} = \frac{T_4 C_{gs1}\left(T_1 + T_3\right)}{T_3\left[C_{gs1}\left(T_1 + T_3\right) - C_3 T_4\right]}. \quad (4)$$

Considering only the drain current noise, the NF (noise figure) of the neutralized LNA can be shown as

$$F_1 = 1 + \frac{\left(Y_s^2 + \omega^2 C_{g1}^2\right)\gamma g_{d01} R_s}{g_{m1}^2}, \quad (5)$$

where Y_s is the source admittance, R_s is the source resistance, ω is the operating angular frequency, C_{g1} is the gate capacitance, γ is the technology-dependent excess noise parameter, and g_{d01} is the drain-source (channel) conductance at zero drain-source voltage.

In a cascade LNA, the extra common-gate transistor contributes additional noise, resulting in an overall NF of

$$F_2 = F_1 + \frac{\omega^2\left(C_{g1} + C_{g5}\right)^2\left(Y_s^2 + \omega^2 C_{g1}^2\right)\gamma g_{d05} R_s}{g_{m1}^2 g_{m5}^2}, \quad (6)$$

where C_{g5}, g_{m5}, and g_{d05} are the corresponding parameters of the cascade transistor.

3.2.2. Downconversion Mixer. The core of the mixer shown in Figure 4 is a double-balanced Gilbert-type mixer. It has also fully symmetrical differential structure to improve linearity of circuit and to reduce RF noise and unnecessary ripple variations. The RF input applies at the gates of M_2 and M_3 which are used as transconductance amplifiers. The linearity of these amplifiers is improved by using source degeneration transmission lines L_{T1} and L_{T2}, which also adjust the input impedance seen looking at the gates of M_2 and M_3 to improve the impedance matching at the LNA-mixer interface. M_2 and M_3 are biased at 2 mA dc current.

The chopping function is accomplished by the mixing cells of M_4 to M_7, and 1.2 V peak-to-peak differential LO (local oscillator) signal is applied. Cascode amplifiers following the differential mixing cells are used to drive the 50 Ω loads. The input matching is accomplished by L_{T5} and L_{T6}.

3.2.3. Voltage-Controlled Oscillator. Figure 5 shows 24 GHz VCO (voltage-controlled oscillator). The proposed circuit is powered by a 1.5 V supply. This circuit has basic scheme of the switched resonator, and it contains CMOS LC tuning circuit to use a 24 GHz frequency band. It has also fully symmetrical scheme to improve linearity of the circuit and to reduce RF noise and unnecessary ripple variations. The switching transistors (M_4 and M_5) are designed to operate near the boundary of current-limited and voltage-limited region to reduce power dissipation. In particular, the switched resonator contains the active inductor consisting of transistors (M_{1a}, M_{2a}, M_{1b}, and M_{2b}) and current sources (I_{s1} and I_{s2}) instead of real spiral inductor to reduce total chip size and power dissipation. This VCO also contains self-biasing

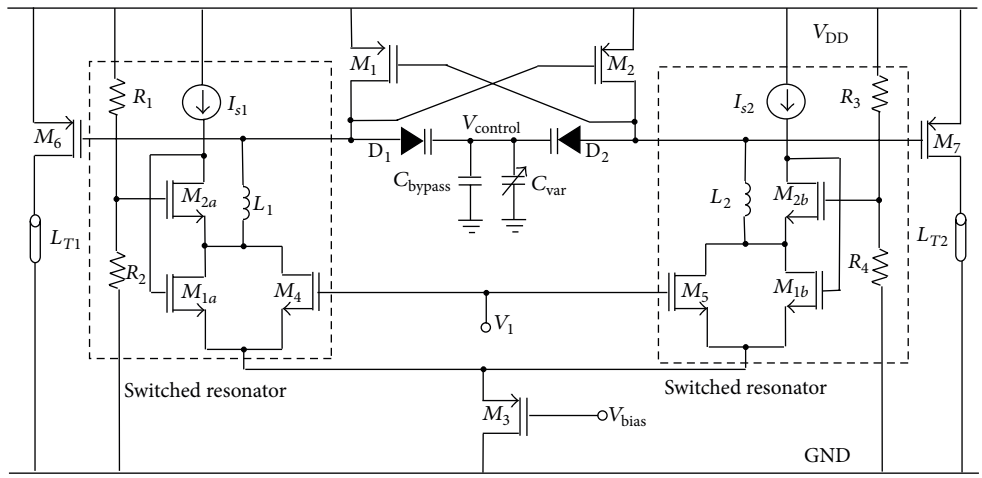

Figure 5: Voltage-controlled oscillator.

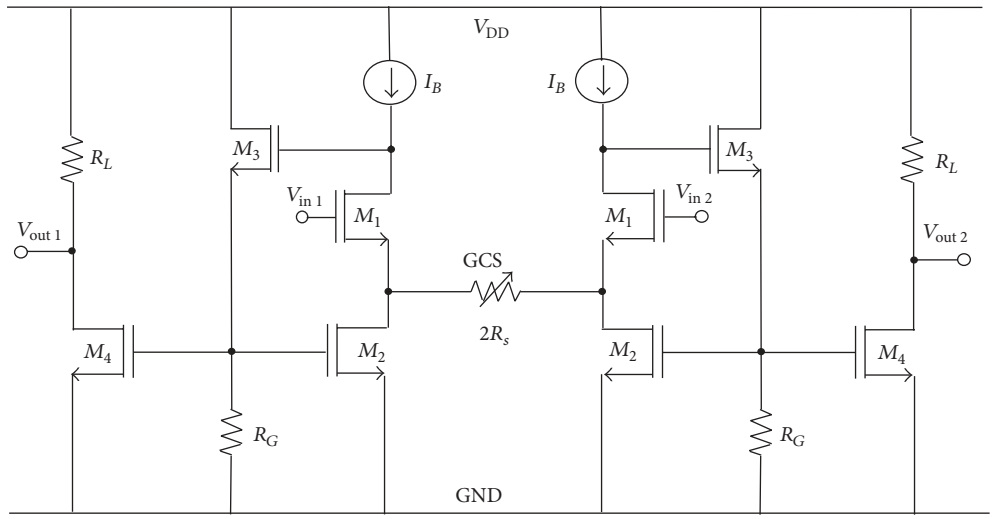

Figure 6: Programmable gain amplifier.

control circuits (R_1~R_4). The notch filtering technique is applied to reduce phase noise from transistor M_3 for tail current supply.

3.2.4. PGA (Programmable Gain Amplifier). Choosing the method to control a gain is essential at PGA design. The proposed PGA with source degeneration resistor is shown in Figure 6. It has fully symmetrical structure at differential mode, and sources of transistors M_1~M_2 have an opposite voltages when two inputs with opposite phases are inserted into the circuit. The amplifier gain can be selected by using a ratio of degeneration or a load resistor. Both sides of the symmetrical structure have the same value with direct current at the source node, and then the gain is adjustable by changing the degeneration resistor R_s with GCS (Gain Control Stage). To get higher gain, the value of the total degeneration resistor must be lower, and thus it leads to the increment of gain errors. Therefore, to obtain a more accurate and higher gain, the proposed PGA includes gm-boosted source-degenerated differential pair and an additional amplifier stage. Small signal gain of differential mode is expressed by

$$A_{\mathrm{dm}} = \frac{g_{m4} g_{m1} r_{01} \left(r_{04} // R_L\right)}{g_{m1} g_{m2} r_{01} \left(r_{02} // R_s\right) + g_{m2} \left(r_{02} // R_s\right) + 1 + 1/g_{m3} \left(r_{03} // R_G\right)}, \quad (7)$$

where r_0 is output resistance.

3.2.5. Switched-Capacitor Integrator. The proposed SC (switched-capacitor) integrator contains some basic building blocks such as operational transconductance amplifier, capacitors, switches, and nonoverlapping clocks as shown in Figure 7. The integrator is implemented in a fully differential configuration to minimize nonidealities such as PSRR, device matching, and noise coupling. The input is sampled during phase 1 (ϕ_1 and ϕ_{1d}). During phase 2, the charge

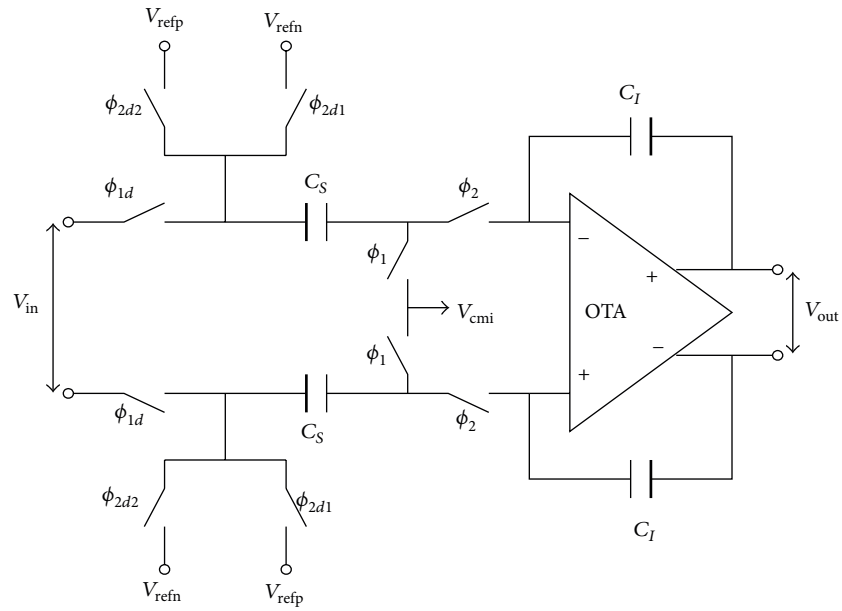

Figure 7: Fully differential switched-capacitor integrator.

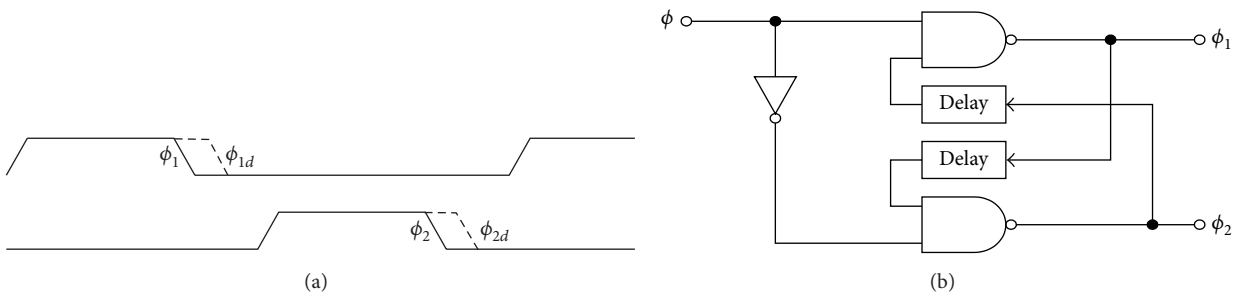

Figure 8: Nonoverlapping clocks: (a) clock signals and (b) possible circuit implementation of nonoverlapping clocks from a single clock.

is transferred from the sampling capacitor, C_S, to the integrating capacitor, C_I. At the same time, depending on the output value, the appropriate DAC reference level is applied by closing either labeled switch ϕ_{2d1} or ϕ_{2d2}. The integrator employs the bottom-plate sampling technique to minimize signal-dependent charge-injection. This is achieved through delayed clocks of ϕ_1, ϕ_{1d}, and ϕ_{2d}. When switch ϕ_1 is first turned off, the charge-injection from those switches remains, to a first order, independent of the input signal. Because one of the plates is now floating, turn-off switch ϕ_{1d} shortly does not introduce charge-injection errors.

At least one pair of nonoverlapping clocks is essential in SC circuits. These clocks determine when charge transfers occurs and they must be nonoverlapping to reduce inadvertent charge lost. As seen in Figure 8, the nonoverlapping clocks refer to two logic signals running at the same frequency.

3.2.6. Layout Issues. The circuits are designed and fabricated using TSMC 0.13 μm mixed-signal/RF CMOS process (f_T/f_{max} = 120/140 GHz). This process offers six metal layers with two top layers of 0.8 μm thick copper. This radar sensor uses transmission lines to reduce total chip size instead of real bulky inductors, and the only inductors (L_1 and L_2) in VCO shown in Figure 5 are spirals. Shield pads are employed at both RF and IF ports. Grounded metal1 underneath the pads prevents loss of the signal power and noise generation associated with the substrate resistance. Ground rings are placed around each transistor at minimum distance to reduce the substrate loss. To minimize parasitic capacitance all transistors are designed by folded structure [4, 16–19]. Separated V_{DD} are assigned to the LNA, mixer, VCO, PGA, integrator, and bias circuits. Large on-chip bypass capacitors are placed between each V_{DD} and ground.

Table 1 summarizes each component area for transmission lines of radar sensor. This sensor uses transmission lines to reduce total die size instead of real bulky inductors. The LNA and mixer showed small size of approximately 58% and 67% as compared to conventional circuits, respectively. The size of the core cell is only 0.75 × 0.50 mm^2, and the size of chip is 0.80 × 0.70 mm^2 including a large area occupied by the wide ground rings and pads.

The die photograph is shown in Figure 9. The size of the core cell is 0.75 × 0.50 mm^2, and the size of chip is 0.80 ×

Table 1: Comparison of each component area of radar sensor.

	Proposed circuit		Conventional circuit	
	Transmission lines	Area ($W \times L$) (μm $\times$ μm)	Inductors	Area ($W \times L$) (μm $\times$ μm)
LNA	L_{T1} (= L_{T2})	20 × 150	L_1 (= L_2)	70 × 70
	L_{T3} (= L_{T5} = L_{T7} = L_{T9})	30 × 150	L_3 (= L_5 = L_7 = L_9)	80 × 80
	L_{T8} (= L_{T10})	10 × 150	L_8 (= L_{10})	50 × 50
	Total TL area	180 × 150	Total inductor area	140 × 140+ 160 × 160+ 100 × 100
	Total LNA area	200 × 180	Total LNA area	250 × 250
Mixer	L_{T1} (= L_{T2})	10 × 150	L_1 (= L_2)	50 × 50
	L_{T3} (= L_{T4})	20 × 150	L_3 (= L_4)	70 × 70
	L_{T5} (= L_{T6})	30 × 150	L_5 (= L_6)	100 × 100
	Total TL area	120 × 150	Total inductor area	100 × 100+ 140 × 140+ 200 × 200
	Total mixer area	180 × 180	Total mixer area	220 × 220
VCO	L_{T1} (= L_{T2})	20 × 150	L_1 (= L_2)	70 × 70
	L_1 (= L_2)	70 × 70	L_3 (= L_4)	80 × 80
	Total TL area	110 × 150	Total inductor area	150 × 150
	Total VCO area	160 × 160	Total LNA area	180 × 180
PGA + integrator	Total area	12 × 12	Total area	13 × 13
Die	Total area	800 × 700	Total area	1,500 × 1,500

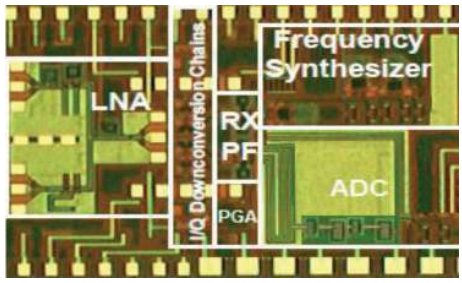

Figure 9: Die photograph.

0.70 mm^2 including a large area occupied by the wide ground rings and pads.

4. Experiment Results and Discussion

The input and output pads are laid out in GSG configuration with a pitch of 150 μm to do wafer level testing for LNA and each block using a probe station with network analyzer. The measurements for LNA have been used here which represent 2-port measurements. The measurements are based on a separate LNA test chip. The power of −20 dBm is applied from the synthesized sources at both port 1 and port 2. We applied the attenuators of 0 dB at both port 1 and port 2. The measured S-Parameter was translated into voltage gain and input impedance.

The radar sensor is tested by probing the input, output, and LO ports. The input, output, and power supply pads are laid out in GPG (ground-power-ground) and GSG (ground-signal-ground) configurations with a pitch of 50 μm to perform packaged level testing. The power and ground pads are wire-bonded to the testing board. The S-Parameters at the RF and IF ports are measured using an HP 8722D vector network analyzer, and the spectrum is obtained using HP 8593A spectrum analyzer.

4.1. Low-Noise Amplifier. Figure 10 shows the input impedance, voltage gain, and noise figure of the LNA for the frequency range of 23~26 GHz. Measurement is obtained using S-Parameter results, and calculation is extracted using (4) to (6) and high-frequency small signal equivalent model. Ideal input impedance of the amplifier must have 45~50 Ω at the operation frequency. As can be seen in Figure 10, the proposed LNA showed very close results for external equipment measurement as well as the calculation. This LNA also showed good impedance matching with input impedance of 46 Ω, high voltage gain of approximately 39 dB, and low-noise figure of 2.86 dB at the operation frequency of 24 GHz.

Table 2 lists comparison results for two different measurement techniques of input impedance (Z_{in}), voltage gain (G_{LNA}), *NF* (noise figure), input return loss (RL_{in}), and output signal-to-noise ratio (SNR_{out}). Vector network analyzer measures the transmission and reflection characteristics of devices and networks by applying a known swept signal

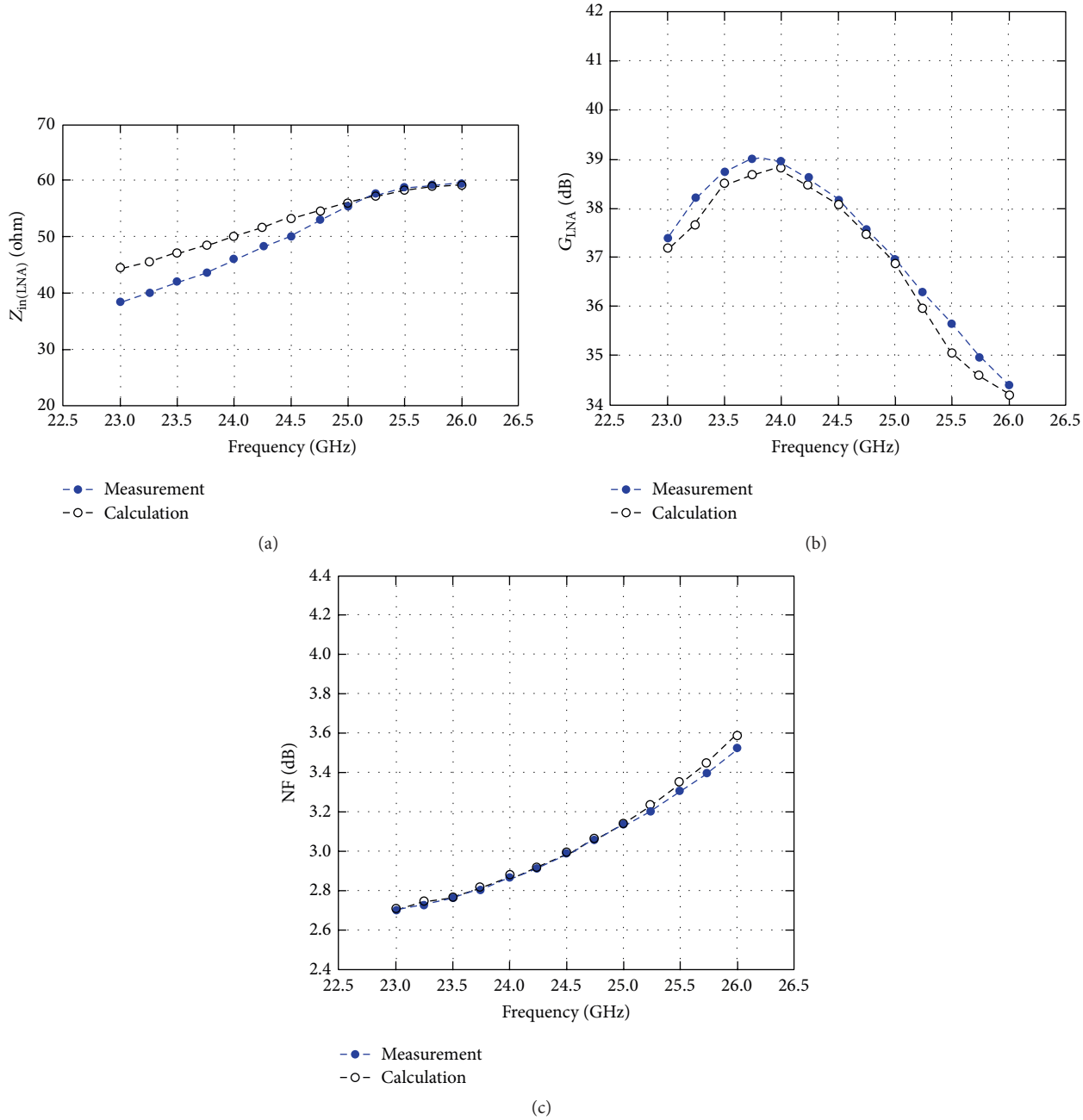

Figure 10: Performance results as a function of frequency: (a) input impedance, (b) voltage gain, and (c) noise figure.

from a synthesized source. Device reflection parameters such as reflection coefficient, return loss, VSWR, and complex impedance and transmission parameters such as insertion loss and gain can be measured using the instrumentation. For a good input matching, the LNA must have input impedance of approximate 50 Ω. As can be seen in Table 2, the proposed LNA showed very close results in input impedance, gain, noise figure, input return loss, and output signal-to-noise ratio as compared to the calculation. These results verify that the proposed LNA shows very low overall error of less than 5% for important parameters at the operation frequency range of 23.0~25.5 GHz.

4.2. Downconversion Mixer. Figure 11(a) shows the conversion gain of the downconversion mixer at the output. Figure 11(b) shows the noise figure of the downconversion mixer for the frequency range of 22.5 GHz to 25.5 GHz. To provide high conversion gain at the operation frequency, we optimized W/L of M_2 and M_3, and we also inserted transmission lines T_3 and T_2 as shown in Figure 4. Noise figure measurement is obtained using S-Parameter results, and calculation is extracted using high-frequency small signal equivalent model. As can be expressed in Figure 11, the proposed mixer showed very close results for external equipment measurement as well as the calculation. This

Table 2: Comparison results for two different measurements.

Test		Frequency [GHz]					
		23.0	23.5	24.0	24.5	25.0	25.5
Measurement	Z_{in} [Ω]	38.5	42.2	46.0	50.1	55.2	59.4
	G_{LNA} [dB]	37.4	38.8	39.0	38.2	36.9	35.6
	NF [dB]	2.70	2.76	2.86	3.00	3.12	3.31
	RL_{in} [dB]	−17.7	−13.8	−13.7	−19.4	−26.1	−22.8
	SNR_{out} [dB]	97.2	96.8	95.6	97.8	99.1	101.1
Calculation	Z_{in} [Ω]	44.3	47.2	50.2	53.5	56.2	58.1
	G_{LNA} [dB]	37.2	38.5	38.9	38.1	36.8	35.0
	NF [dB]	2.71	2.77	2.87	3.01	3.13	3.35
	RL_{in} [dB]	−17.7	−13.8	−13.9	−19.5	−25.9	−24.5
	SNR_{out} [dB]	96.8	95.6	95.5	96.7	98.8	99.9

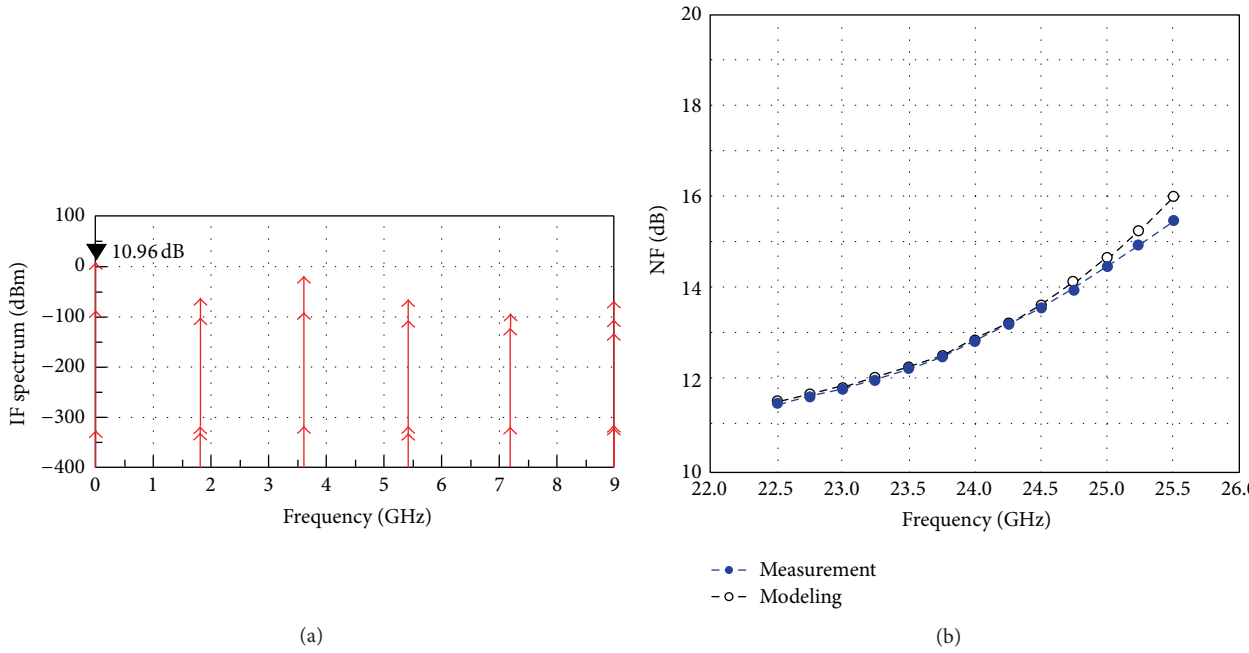

Figure 11: Performance of mixer: (a) conversion gain and (b) noise figure.

mixer also showed excellent noise figure of 12.9 dB at the operation frequency of 24 GHz. The proposed circuit showed the highest conversion gain of 10.96 dB, IIP3 of 7.6 dBm, and FoM (figure of merit) of 14.1 dB and the smallest power consumption of 4.1 mW and die size of $0.1 \times 0.1\,mm^2$ as compared to recently reported research results. It also showed input return loss of −43.6 dB and LO-RF isolation of −49.2 dB as compared to conventional research results, respectively.

4.3. Voltage-Controlled Oscillator. The tuning voltage characteristics, transient voltage, Fourier spectrum, and phase noise of the voltage-controlled oscillator are shown in Figure 12. The result of Figure 12(b) is closely related to phase noise. As shown in Figure 12(b), the proposed oscillator showed almost undistorted waveform at the operation frequency of 24 GHz. This result verifies that the proposed circuit shows very low phase noise. Several important parameters were also measured for the proposed oscillator. The oscillator showed measurement result of approximately 9% at the 24 GHz for the FTR (frequency tuning range) and phase noise of approximately −96 dBc/Hz at the 1 MHz offset. The VCO also showed low power dissipation of 5.5 mW and very small die area of $0.0425\,mm^2$ at the operation frequency as compared to conventional research results.

4.4. PGA (Programmable Gain Amplifier). Figure 13 shows transient voltage for the proposed PGA. It is designed by providing gains of 40 dB and 60 dB. The results show average values from 10 times' experiments and time variations within less than 2%. These values are measured after 40 nanoseconds' settling time of the PGA to ensure steady-state value. As shown in Figure 13, the proposed PGA showed acceptable values of 40 dB and 60 dB.

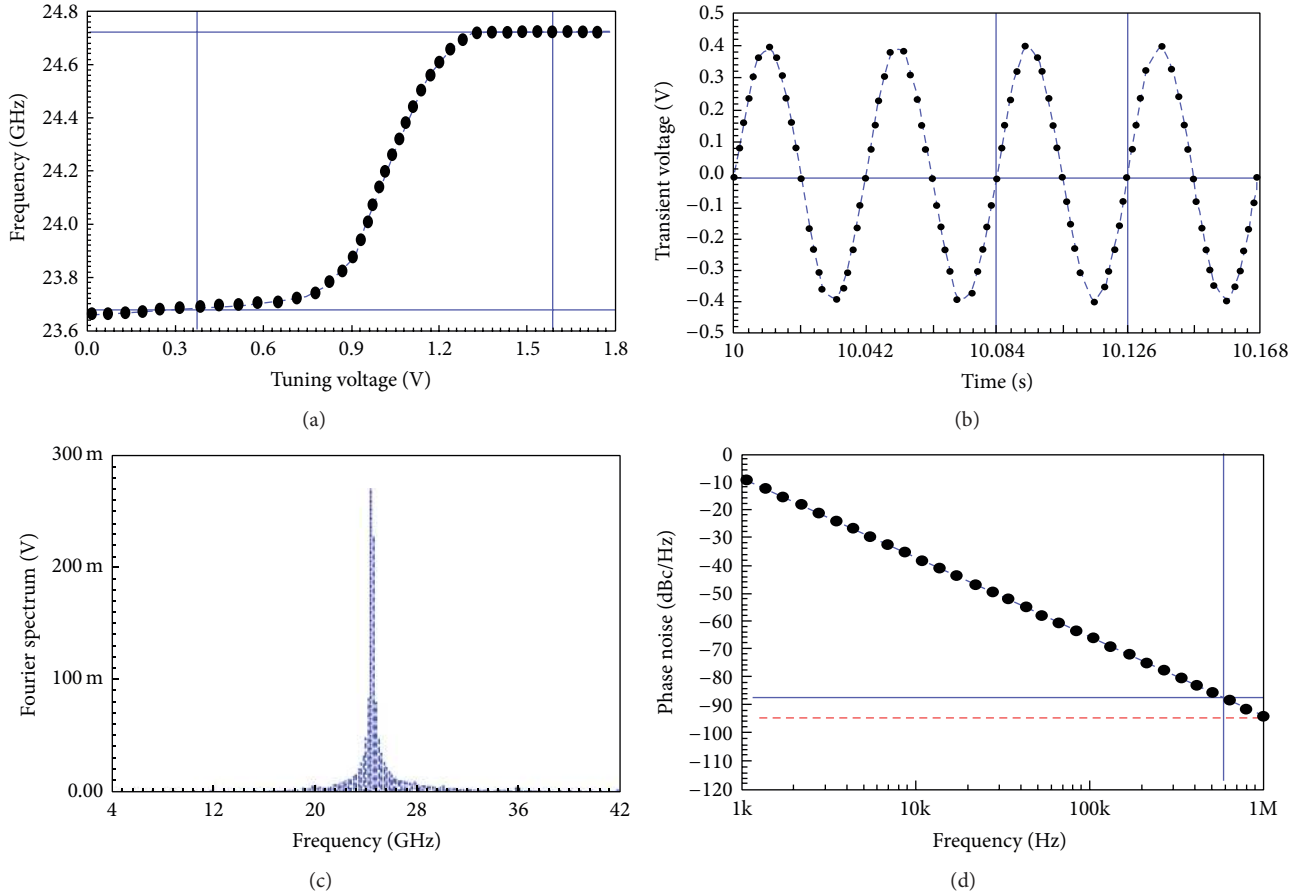

Figure 12: Performance of VCO: (a) tuning voltage characteristics, (b) transient voltage, (c) Fourier spectrum, and (d) phase noise.

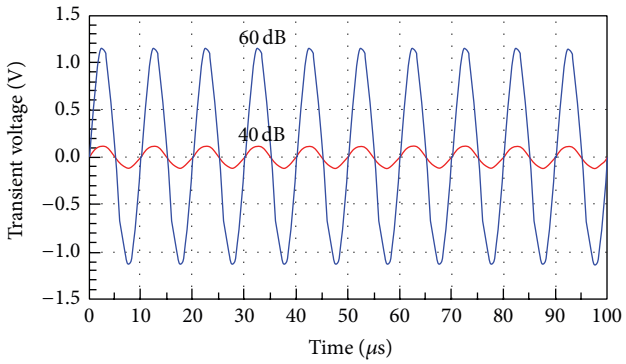

Figure 13: Transient voltage of PGA.

4.5. Radar Sensor. The sensor chip performance is measured using a coaxial setup for 24 GHz. In addition to circuit breakouts, in situ probing is also enabled using pads that are absorbed as part of the design. The measured pulse width at the input is chosen for full bandwidth of 7 GHz operation, and the PLL output frequency is set at the center frequency of the 24 GHz band. The 24 GHz output is directly measured on a sampling oscillator. The spectrum corresponding to pulse width of about 300 ps for the 24 GHz pulse is readily measured.

The complete measured performance comparison of the sensor is summarized in Table 3. The receiver correlation function is determined by varying the delay R_x trigger in the pulse generator. Due to the sensor mask constraints at 24 GHz, multiple pulses need to be integrated to raise the signal above the noise floor. This is demonstrated in measurement results of Table 3, which shows the integrator output after coherent integration of 200 pulses for each delay setting. A 1 ns pulse is generated, corresponding to a 12 cm range resolution, and the delay is varied in 100 ps steps, corresponding to 2 cm range accuracy. From this comparison, it can be seen that the proposed CMOS receiver compares the state-of-the-art realizations and also achieves the lowest noise figure of 2.9 dB reported so far among the K-band CMOS realizations. The proposed radar sensor showed the very low-noise figure of 2.9 dB and the highest conversion gain of approximately 40 dB as compared to recently reported research results as shown in Table 3. This sensor also showed very small chip area of 0.8×0.7 mm^2, low power dissipation of 39.5 mW, and wide operating temperature range of −40 to +125°C.

5. Conclusion

This paper presented low-noise small-area 24 GHz CMOS radar sensor based on direct-conversion pulsed-radar architecture. The proposed sensor was fabricated using TSMC

Table 3: Performance comparison of 24 GHz radar sensor.

Performance	This work	[10]	[11]	[12]*	[13]*	[14]	[15]
Conversion gain (dB)	**40.2**	16.5	35	27.5	16	31.5	37.7
DSB noise figure (dB)	**2.9**	5.3	4.5	7.7	5	6.7	5.8
Input return loss (S_{11}) (dB)	−24.34	NA	<−10	−21	NA	−16	<−14.5
Output return loss (S_{22}) (dB)	−26.28	NA	<−15	−10	NA	NA	<−15
LO-to-RF leakage (dB)	−40.48	<−45	<−70	NA	−44	NA	<−30
LO-to-IF leakage (dB)	−38.24	<−45	<−38	NA	−34.6	NA	<−23
Input $P_{1\,dB}$ (dBm)	−30.2	−26	−33.2	−23	−24.6	−24	−20.8
Technology (μm)	0.13 CMOS	0.13 CMOS	0.18 BiCMOS	0.18 CMOS	0.13 CMOS	0.065 CMOS	0.18 CMOS
Size (mm × mm)	**0.8 × 0.7**	1.4 × 0.5	3.9 × 1.9	0.4 × 0.5	0.86 × 0.59	1.6 × 1.2	3.0 × 1.0
Power dissipation (mW)	39.5	18	107.5	64.5	22.2	78	131
Operating temperature (°C)	−40~125	—	—	—	−40~125	—	—

*LNA + mixer.

0.13 μm RF CMOS technology. To reduce total chip area, transmission lines instead of real bulky inductors were used. The layout techniques for RF were used to reduce parasitic capacitance at the frequency range of 22~26 GHz. The proposed circuit showed the very low-noise figure of 2.9 dB and the highest conversion gain of approximately 40 dB as compared to recently reported research results. This sensor also showed very small chip area of 0.56 mm^2 and low power dissipation of 39.5 mW. The results were compared in measurement of operating temperature range from −40 to +125°C for practical use in real cars.

Competing Interests

The authors declare that they have no competing interests.

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