Development of Single-Transistor-Control LDO Based on Flipped Voltage Follower for SoC

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***Abstract*—The design issues of a single-transistor-control (STC) low-drop-out (LDO) based on flipped voltage follower is discussed in this paper, in particular the feedback stability at different conditions of output capacitors, equivalent series resistances (ESRs) and load current. Based on the analysis, an STC LDO was implemented in a standard 0.35-μm CMOS technology. It is proven experimentally that the LDO provides stable voltage regulation at a variety of output-capacitor/ESR conditions and is also stable in no output capacitor condition. The preset output voltage, minimum unregulated input voltage, maximum output current at a dropout voltage of 200 mV, ground current and active chip area are 1 V, 1.2 V, 50 mA, 95 μA, and 140 μm $\times$ 320 μm, respectively. The full-load transient response in the no output capacitor case is faster than a micro second and is about 300 ns.**

***Index Terms*—Flipped voltage follower (FVF), low drop out (LDO), loop gain and power management.**

I. Introduction

POWER management is a timely and essential research area, enabling advancement of system-on-chip (SoC) technology. The development of high-performance integrated voltage regulators, in terms of accuracy, power efficiency, response time, silicon area, and off-chip component free feature, is undoubtedly vital to the success of SoC. To enable these requirements, a low drop out (LDO) with single-transistor control (STC) based on the flipped voltage follower (FVF) [1]–[3], with emphasis on the circuit theory for successful implementation, is presented in this paper [4].

It is well known that generic LDO structure suffers from unavoidable tradeoffs between the accuracy and feedback stability [5], [6]. A high loop gain, which results in improved steady-state regulation, degrades close-loop stability, so that different methodologies such as an advanced pole–zero cancellation scheme in [5], a load-dependent reference voltage concept in [6], pole-splitting schemes in [7]–[10], were proposed. Recently, a super source follower [11], in form of FVF [1]–[3], has been applied to the designs of a buffer [12] and a power stage [13] in LDO. The main advantage of the FVF is the reduced output impedance due to shunt feedback connection [11], which is the key for obtaining good regulation and achieving frequency compensation. However, there are, in fact, many design issues have to be studied when using the FVF as a power stage. The studies in [1]–[3] do not focus on LDO design, and the application of the FVF in [12] is not for the power stage. In addition to the impedance control in [13], loop stability is undoubtedly a key issue needed to be analyzed in detail, especially when using different combinations of output capacitor and ESR values [14], [15] or when operating in the no output-capacitor (no-capacitor) condition [7], [8].

With regard to the above considerations, this paper intends to provide a detailed study on the stability of an LDO based on the FVF for different capacitors, equivalent series resistances (ESRs) and load conditions. No-capacitor condition for SoC applications is one of the topics that will be discussed in this paper.

The organization of this paper is as follows: Section II will introduce the STC-LDO structure and discuss the voltage regulation based on its local series-shunt feedback [11]. Section III will study the stability of the STC-LDO. The stability of the cases with the presence of an off-chip capacitor and no capacitor will be analyzed. Section IV will cover the load transient response and design requirements for fast response. Experimental results will be included in Section V.

II. Structure and Working Principle of STC-LDO

The complete structure of a STC-LDO, including the required control-voltage generator, is shown in Fig. 1. In particular, the STC-LDO is mainly composed of M_P (the power pMOSFET to deliver load current from the supply to the output), M_C (the control transistor) and a current source $I_{\rm BIAS}$. The parasitic resistances and capacitances are included in the analysis in Section III. There is an off-chip capacitor $C_{\rm OUT}$ with ESR of R_E. $I_{\rm OUT}$ models the loading circuit.

The source terminal of M_C is the sensing terminal of the common-gate amplifier M_C. When $V_{\rm OUT}$ varies, M_C provides an error voltage at its drain to control the gate voltage of M_P. This mechanism controls the amount of drain current delivered by M_P to regulate $V_{\rm OUT}$. The control voltage $V_{\rm CTRL}$ is to provide the preset $V_{\rm OUT}$, according to the relationship

$$V_{\rm OUT} = V_{\rm CTRL} + V_{\rm SGC} \tag{1}$$

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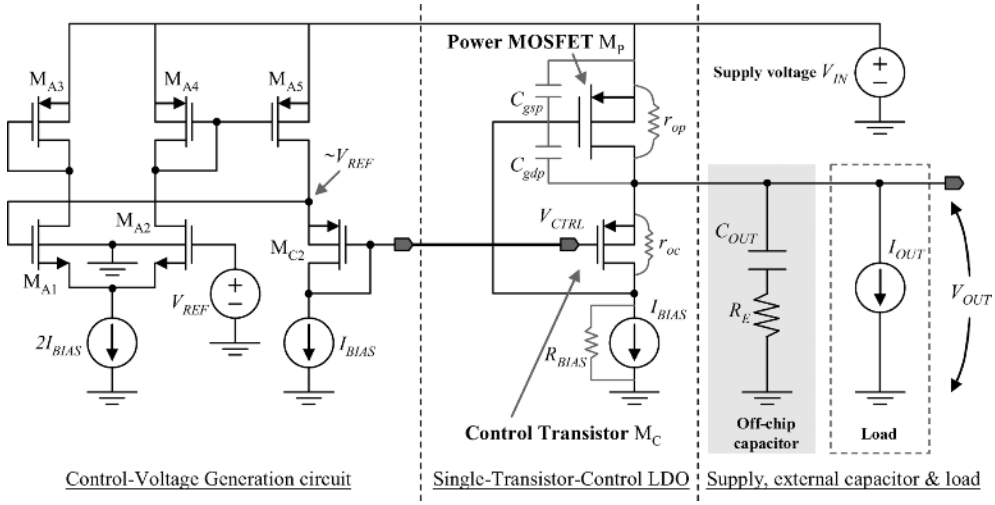


Fig. 1. Proposed STC LDO with the control-voltage generation circuit.

where $V_{\rm SGC}$ is the source–gate voltage of M_C. $V_{\rm SGC}$ is a constant and is independent of $I_{\rm OUT}$ since it is biased constantly by $I_{\rm BIAS}$.

It is obvious from (1) that $V_{\rm OUT}$ cannot be controlled independently of temperature and process variations due to $V_{\rm SGC}$. Therefore, a control-voltage generator is designed in Fig. 1 to overcome this problem.

The control-voltage generator is basically a simple amplifier in unity-gain configuration, except an additional transistor M_{C2} in diode connection biased by $I_{\rm BIAS}$ (same bias level of M_C) is inserted at the output stage. By providing a low tempco reference voltage $V_{\rm REF}$ (e.g., bandgap voltage reference) at the input of the unity-gain buffer, this $V_{\rm REF}$ will be re-generated at the output of the buffer. Thus, $V_{\rm CTRL}$ is given by

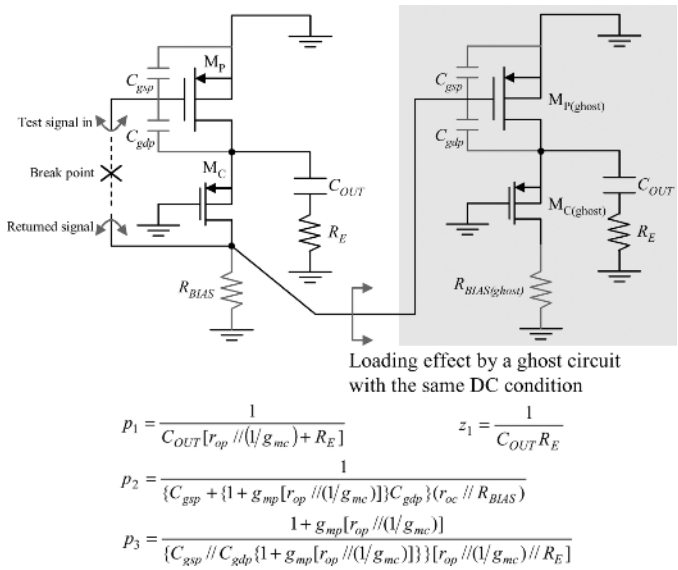
$$V_{\rm CTRL} = V_{\rm REF} - V_{\rm SGC2} \tag{2}$$

where $V_{\rm SGC2}$ is the source–gate voltage of M_{C2}. Since $V_{\rm SGC2} = V_{\rm SGC}$ (M_C and M_{C2} are of the same size and of the same bias condition), the following relationship is achieved:

$$V_{\rm OUT} = V_{\rm REF}. \tag{3}$$

Scalable $V_{\rm REF}$ could provide an adjustable $V_{\rm OUT}$ accordingly [11]. The channel length of M_C and M_{C2} are suggested to be long such that channel modulation effect due to different V_{SD} can be minimized. A decoupling capacitor is suggested to be connected between the voltage node $V_{\rm CTRL}$ and the ground for eliminating voltage spikes at $V_{\rm OUT}$ through charge re-distribution of C_{gd} of M_C during the fast transient response for achieving better dynamics accuracy. In addition, the suggested decoupling capacitor helps to lessen noise injection to the STC-LDO.

This STC-LDO is simpler than the one reported in [13]. It can be easily observed that the structure in [13] is suitable for wide supply-voltage range. However, LDO is designed for voltage regulation at a small dropout voltage (even at the maximum $I_{\rm OUT}$) for maximizing the power-conversion efficiency. Therefore, the typical application of the LDO is to provide a regulated



$$p_1 = \frac{1}{C_{OUT}[r_{op} /\!/ (1/g_{mc}) + R_E]} \qquad z_1 = \frac{1}{C_{OUT} R_E}$$

$$p_2 = \frac{1}{\{C_{gsp} + \{1 + g_{mp}[r_{op} /\!/ (1/g_{mc})]\} C_{gdp}\}(r_{oc} /\!/ R_{BIAS})}$$

$$p_3 = \frac{1 + g_{mp}[r_{op} /\!/ (1/g_{mc})]}{\{C_{gsp} /\!/ C_{gdp}\{1 + g_{mp}[r_{op} /\!/ (1/g_{mc})]\}\}[r_{op} /\!/ (1/g_{mc}) /\!/ R_E]}$$

Fig. 2. Loop gain analysis by including loading effect.

voltage from a close-to-output supply voltage or as a post-regulator. The STC-LDO is well-suited for these applications, due to its extremely simple structure. The regulation range of the STC-LDO is given by

$$V_{\rm IN} < V_{\rm OUT} + V_{\rm SGP} - V_{\rm SDC(sat)} \tag{4}$$

where $V_{\rm SDC(sat)}$ is the saturation voltage of M_C. From (4), the regulation range counting from $V_{\rm OUT}$ is about one $V_{\rm SGP}$, which is generally sufficient for the aforementioned applications.

The mechanism of voltage regulation is explained here. Supposing $V_{\rm OUT}$ is lower than the preset value, $V_{\rm SGC}$ will be enforced to be reduced such that the gate voltage of M_P decreases due to the non-inverting voltage gain of a common-gate amplifier. The increase of $V_{\rm SGP}$ causes more drain current to be sourced to the load, as well as to the output capacitor. $V_{\rm OUT}$ therefore increases. Similarly, when $V_{\rm OUT}$ is higher than the preset value, $V_{\rm SGP}$ is reduced and M_P delivers less drain current

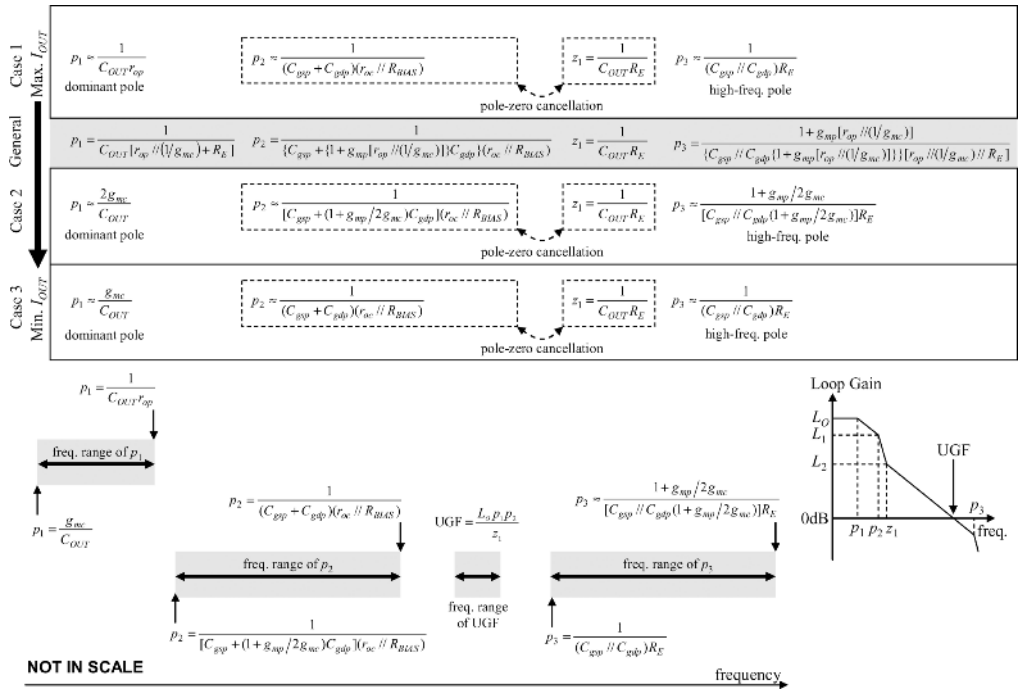


Fig. 3. Pole–zero analysis of the loop-gain transfer function of the STC-LDO with an off-chip capacitor with R_E not large.

to cause a decrease of $V_{\rm OUT}$. This continuous feedback results in the voltage regulation of STC-LDO at the preset voltage defined by $V_{\rm REF}$.

The line and load regulations of a LDO are given by [5], [7]

$$\text{Load regulation} = \frac{\Delta V_{\rm OUT}}{\Delta I_{\rm OUT}} = \frac{R_O}{1 + A_{\rm EA} G_m R_O} \approx \frac{1}{A_{\rm EA} G_m} \tag{5}$$

$$\text{Line regulation} = \frac{\Delta V_{\rm OUT}}{\Delta V_{\rm IN}} = \frac{G_m R_O}{1 + A_{\rm EA} G_m R_O} \approx \frac{1}{A_{\rm EA}} \tag{6}$$

where $A_{\rm EA}$ is the voltage gain of the error amplifier in LDO; G_m and R_O are the transconductance and open-loop output resistance of the power pMOSFET. R_O in STC-LDO is reduced by $1/g_{mc}$. In general, $G_m R_O > 1$ for low-to-moderate $I_{\rm OUT}$. The approximations in both (5) and (6) are valid. This shows that the STC-LDO behaves similar to the conventional LDO. When $I_{\rm OUT}$ is high, R_O will be dominated by $r_{\rm op}$ but not $1/g_{mc}$. However, although $G_m R_O$ may not be greater one and the approximations in (5) and (6) are no longer valid, both load and line regulations of the STC-LDO are just same as those of the conventional LDO. Therefore, the key to improve both load and line regulations is to develop a high-gain error amplifier, while unaffecting the closed-loop stability.

III. Stability of STC-LDO

The previously-stated voltage-regulation mechanism relies much the stability of the built-in local negative feedback of the STC-LDO. In this section, two cases will be studied. The first case is the STC-LDO with an off-chip capacitor. Different combinations of the loading condition and capacitor/ESR will be studied. The second case is the no-capacitor condition.

A. Presence of Off-Chip Capacitor

Fig. 2 shows the equivalent small-signal circuit of the STC-LDO. Loop-gain analysis is done by breaking the feedback loop at the gate of M_P. The loading effect due by M_P is included by a "ghost" circuit.

The transistor sizes of $M_{P(\rm ghost)}$ and $M_{C(\rm ghost)}$ are exactly equal to those of M_P and M_C, respectively. Moreover, the dc bias of $M_{P(\rm ghost)}$ and $M_{C(\rm ghost)}$ are same as that of M_P and M_C as well. From the analysis, it is found that there are three left-half-plane (LHP) poles [shown in (7a)–(7c), at the bottom of the next page], and one LHP zero as follows.

$$z_1 = \frac{1}{C_{\rm OUT} R_E}. \tag{7d}$$

The poles are $I_{\rm OUT}$-dependent, since different $I_{\rm OUT}$ vary $g_{mp} (\propto \sqrt{I_{\rm OUT}})$ and $r_{\rm op} (\propto 1/I_{\rm OUT})$. In particular, $r_{\rm op}$ may be smaller or larger than $1/g_{mc}$ and R_E in different $I_{\rm OUT}$. Moreover, from (7b), Miller effect happens to C_{gdp} such that p_2 is pushed to a lower frequency. Fig. 3 summaries the relationship of the poles and zero in different $I_{\rm OUT}$. It is highlighted that this analysis is for R_E not large. The boundary of this definition relates to $r_{\rm op}$. For example, when M_P operates in the saturation region in low $I_{\rm OUT}$ condition, $r_{\rm op}$ is definitely larger than R_E. When M_P is in the dropout region, $r_{\rm op}$ is reduced. The worst case is when the M_P operates in the linear region, and $r_{\rm op}$ can be simply found by $V_{\rm SDP}/I_{\rm SDP}$. Therefore, when the dropout voltage is 200 mV and $I_{\rm OUT} = 50$ mA, $r_{\rm op}$ is 4Ω. Based on this study, $r_{\rm op}$ is generally larger than R_E, which is about 100 mΩ for capacitance in micro-Farad up to a few ohms for capacitance in nanofarad. In general, a large R_E is not preferred since this introduces large voltage spikes in the transient response [16].

The study is considered when the $I_{\rm OUT}$ decreases from the maximum to zero (i.e., $I_{\rm BIAS}$). The equations in (7a) to (7c) are modified at different $I_{\rm OUT}$. There are three possible cases:

1) Case 1: $I_{\rm OUT}$ = maximum or high: When $I_{\rm OUT}$ is very large, $r_{\rm op}$ is much smaller than $1/g_{mc}$ but is larger than R_E. Therefore, p_1 is dominated by $r_{\rm op}$, and the Miller effect at p_2 is negligible. From Fig. 3, p_2 is cancelled by z_1 within one decade of frequency. p_1 becomes the dominant pole. Since p_3 is a function of C_{gsp}, C_{gdp} and R_E, p_3 is located at a frequency higher than the unity-gain frequency (UGF) of the loop gain. Thus, the loop gain basically has a single pole, and it is absolutely stable [11].

2) Case 2: $I_{\rm OUT}$ = moderate: When $I_{\rm OUT}$ is lower and is at a level such that $r_{\rm op} = 1/g_{mc}$, (7a)–(7c) are reduced to the forms in Fig. 3. p_1 becomes a constant. The change of $I_{\rm OUT}$, in principle, does not affect p_1. The Miller effect to p_2 is also not significant due to the small g_{mp}, but p_2 is located at a relatively lower frequency than that in Case 1. Similar to Case 1, p_3 is at a high frequency. Thus, z_1 is designed to cancel p_2 within one decade of frequency. p_1 is the dominant pole, and p_3 is higher than UGF. The feedback loop is stable.

3) Case 3: $I_{\rm OUT} = 0$: When $I_{\rm OUT} = 0$, the drain current of M_P is equal to $I_{\rm BIAS}$ (see Fig. 1). $r_{\rm op}$ is much larger than $1/g_{mc}$, and g_{mp} is close to g_{mc} (as M_P is in deep subthreshold region) such that Miller effect is not significant. Similar to Case 2, the change of $I_{\rm OUT}$, in principle, does not affect p_1. However, p_2 moves to a relatively higher frequency than that in Case 2. This illustrates p_2 is bounded due to the STC-LDO structure. As a result, the design of z_1 by R_E is much easier than typical LDO, since the range of p_2 is bounded. The only requirement of R_E is that z_1 should be designed within the range of p_2 (shown in Fig. 3) to achieve the best cancellation of p_2 for the stability of the STC-LDO.

From the discussion, it is found that p_1 is load-independent in principle when $I_{\rm OUT}$ is reduced. The loop bandwidth at the moderate-to-zero load conditions is much better than the conventional LDO [17]. In addition, p_2 is bounded so that the requirement of R_E is not as harsh as in the conventional LDO design.

In case of a large ESR such that $R_E \ll r_{\rm op}$ and $1/g_{mc}$ in any $I_{\rm OUT}$ condition, it is trivial from (7a) and (7d) that p_1 is exactly equal z_1 for perfectly pole–zero cancellation, i.e.,

$$p_1 = z_1 = \frac{1}{C_{\rm OUT} R_E}. \tag{8}$$

Both p_2 and p_3 are independent of $C_{\rm OUT}$. p_2 will be the dominant pole, and p_3 is always at a frequency higher than UGF. It

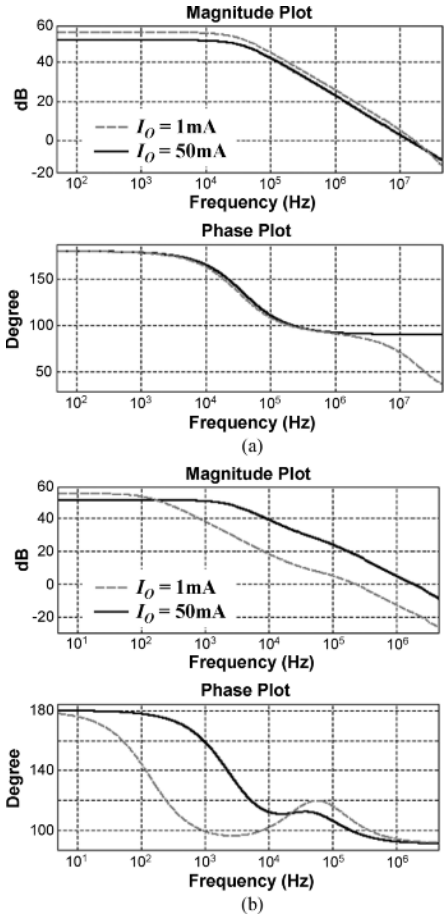


Fig. 4. Simulated loop gain (a) no output capacitor (b) $C_{\rm OUT} = 4.7\ \mu$F and $R_E = 1\ \Omega$.

can be proven by comparing the effective capacitance and the effective resistance of both p_2 and p_3. As a result, the stability of STC-LDO is achieved when R_E is very large.

It is noted that the UGF of Case 1, 2, and 3 can be found by the magnitude plot in Fig. 3 using gain-bandwidth product. Therefore, $L_O p_1 = L_1 p_2$, $L_1 p_2^2 = L_2 z_1^2$ and $L_2 z_1 = \text{UGF}$, the expression of $\text{UGF} = L_O p_1 p_2 / z_1$ can be obtained. The UGF is obviously not a constant since L_O, p_1 and p_2 are load-dependent.

B. No-Output Capacitor

When there is no off-chip capacitor, there is just a parasitic capacitance due by the routing to the load circuit. As a result, it is reasonable to claim $C_{\rm OUT} \to 0$ and $R_E = 0$. p_1 in (7a) locates to a very high frequency when $C_{\rm OUT} \to 0$

$$p_1 = \frac{1}{C_{\rm OUT}\left[r_{\rm op}//(1/g_{mc}) + R_E\right]} \tag{7a}$$

$$p_2 = \frac{1}{\left\{C_{gsp} + \left\{1 + g_{mp}\left[r_{\rm op}//(1/g_{mc})\right]\right\} C_{gdp}\right\}\left(r_{oc}//R_{\rm BIAS}\right)} \tag{7b}$$

$$p_3 = \frac{1 + g_{mp}\left[r_{\rm op}//(1/g_{mc})\right]}{\left\{C_{gsp}//C_{gdp}\left\{1 + g_{mp}\left[r_{\rm op}//(1/g_{mc})\right]\right\}\right\}\left[r_{\rm op}//(1/g_{mc})//R_E\right]} \tag{7c}$$

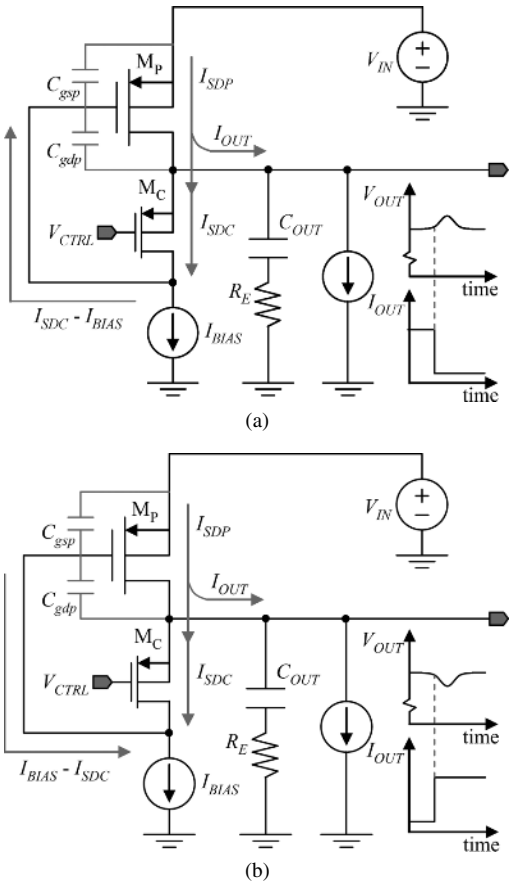


Fig. 5. Analysis of the load transient response. (a) Step-down load. (b) Step-up load.

and z_1 in (7d) vanishes. By re-written p_2 into $p_{1(nc)}$, p_3 into $p_{2(nc)}$ and p_1 into $p_{3(nc)}$, the remaining two poles are given by (9a)–(9c), at the bottom of the page. From (9a) and (9b), it is obviously that $p_{2(nc)}$ locates at a much higher frequency than $p_{1(nc)}$ at different $I_{\rm OUT}$. Moreover, when the STC-LDO is used to power-up a local, on-chip circuit block individually, the equivalent load capacitance from the small circuit block is not much. It is just about ∼20 pF at most. Assuming $g_{mc} = 400$ μA/V and $r_{\rm op}$ is larger than $1/g_{mc}$ (the worst case), the corresponding position of $p_{3(nc)}$ is about 3 MHz and is typically higher than the UGF of the loop bandwidth of the STC-LDO when $C_{\rm OUT} = 20$ pF. Therefore, STC-LDO is absolutely stable in no-capacitor condition. Moreover, p_1 is a function of the small parasitic capacitances. The loop response in no-capacitor condition is fast.

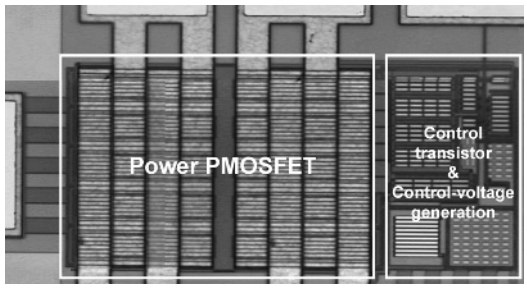


Fig. 6. Micrograph of the STC-LDO.

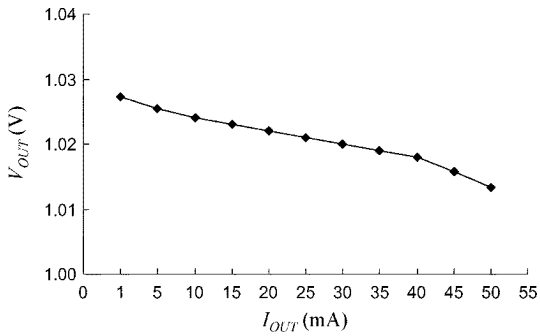


Fig. 7. Measured load regulation of STC-LDO at $V_{\rm IN} = 1.2$ V.

The proposed LDO in Fig. 1 have been simulated using the BSim3v3 models of a 0.35-μm CMOS process, provided by Austria Mikro System (AMS) Group, Austria. Fig. 4 shows the loop-gain simulations with and without the output capacitor. From the simulation, the proposed LDO has phase margin of more than 60° when $I_{\rm OUT} = 1$ mA and $I_{\rm OUT} = 50$ mA.

IV. Transient Response of STC-LDO

The load transient response of STC-LDO can be studied by Fig. 5. The cases of step-down load and step-up load are analyzed in this section. A design condition of the control transistor will be derived after the analysis.

1) Case 1: Step-Down Load [Refer to Fig. 5(a)]: When $I_{\rm OUT}$ decreases rapidly, the drain current of M_P, $I_{\rm SDP}$, cannot stop instantaneously. The output capacitor is over-charged and the capacitor voltage exceeds the preset $V_{\rm OUT}$. The $V_{\rm SGC}$ is thus increased, and this causes a larger $I_{\rm SDC}$ happened. There is an excess current of amount of $I_{\rm SDC} - I_{\rm BIAS}$ to charge the gate capacitance of M_P for increasing the gate voltage such that M_P will deliver less current to the load. The overshoot is then settled.

$$p_{1(nc)} = \frac{1}{\{C_{gsp} + \{1 + g_{mp}\,[r_{\rm op}//(1/g_{mc})]\}\,C_{gdp}\}\,(r_{oc}//R_{\rm BIAS})} \tag{9a}$$

$$p_{2(nc)} = \frac{1 + g_{mp}\,[r_{\rm op}//(1/g_{mc})]}{\{C_{gsp}//C_{gdp}\,\{1 + g_{mp}\,[r_{\rm op}//(1/g_{mc})]\}\}\,[r_{\rm op}//(1/g_{mc})//R_E]} \tag{9b}$$

$$p_{3(nc)} = \frac{1}{C_{\rm OUT}\,[r_{\rm op}//(1/g_{mc})]} \tag{9c}$$

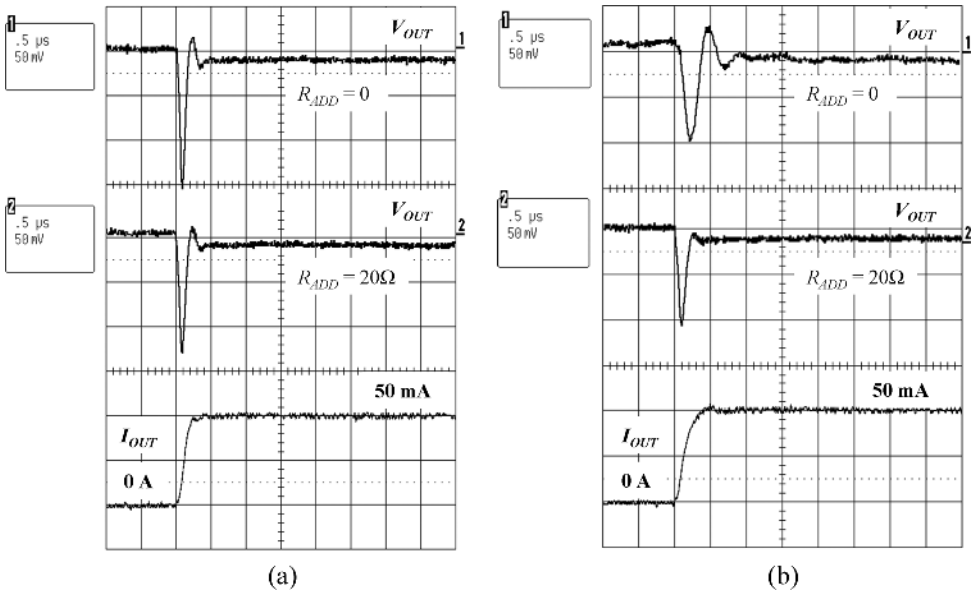


Fig. 8. Measured load transient responses an off-chip capacitor of 1 and 47 nF, where R_{ADD} is the added series resistance. (a) $C_{\mathrm{OUT}} = 1$ nF and $R_E \approx 4.4\ \Omega$. (b) $C_{\mathrm{OUT}} = 47$ nF and $R_E \approx 2.2\ \Omega$.

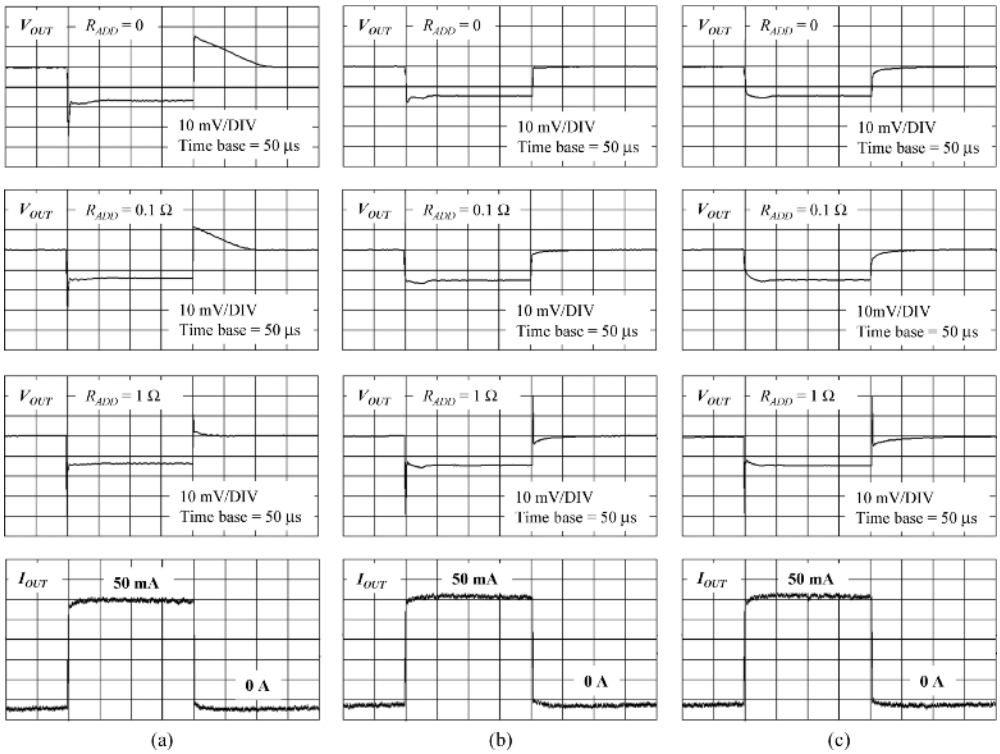


Fig. 9. Measured load transient responses with an off-chip capacitor of 1, 4.7, and 10 μF, where R_{ADD} is the added series resistance (full view). (a) $C_{\mathrm{OUT}} = 1\,\mu$F and $R_E \approx 16$ mΩ. (b) $C_{\mathrm{OUT}} = 4.7\ \mu$F and $R_E \approx 32$ mΩ. (c) $C_{\mathrm{OUT}} = 10\ \mu$F and $R_E \approx 32$ mΩ.

2) Case 2: Step-Up Load [Refer to Fig. 5(b)]: Similarly, when I_{OUT} suddenly increases, I_{SDP} is not sufficient to supply the load. The output capacitor discharges and delivers current to the load. This causes drop of V_{OUT}. This drop causes the reduction of V_{SGC}, and then I_{SDC} is reduced. The discharging current of the gate capacitance of M_P is $I_{\mathrm{BIAS}} - I_{\mathrm{SDC}}$. Once the V_{SGP} increases, more drain current from M_P will supply the load and charge C_{OUT} back to the preset voltage.

From the case study, it reveals that I_{SDC} should be large for step-down load, while it should be small or even zero for step-up load. It is preferred that I_{SDC} is sensitive to ΔV_{SGC}. The design condition of M_C for higher sensibility to ΔV_{SGC} can be found by

$$I_{\mathrm{SDC}} + \Delta I_{\mathrm{SDC}} = \frac{\mu_p C_{\mathrm{OX}}}{2}\left(\frac{W}{L}\right)(V_{\mathrm{SGC}} + \Delta V_{\mathrm{SGC}} - V_{\mathrm{TH}})^2 \tag{10}$$

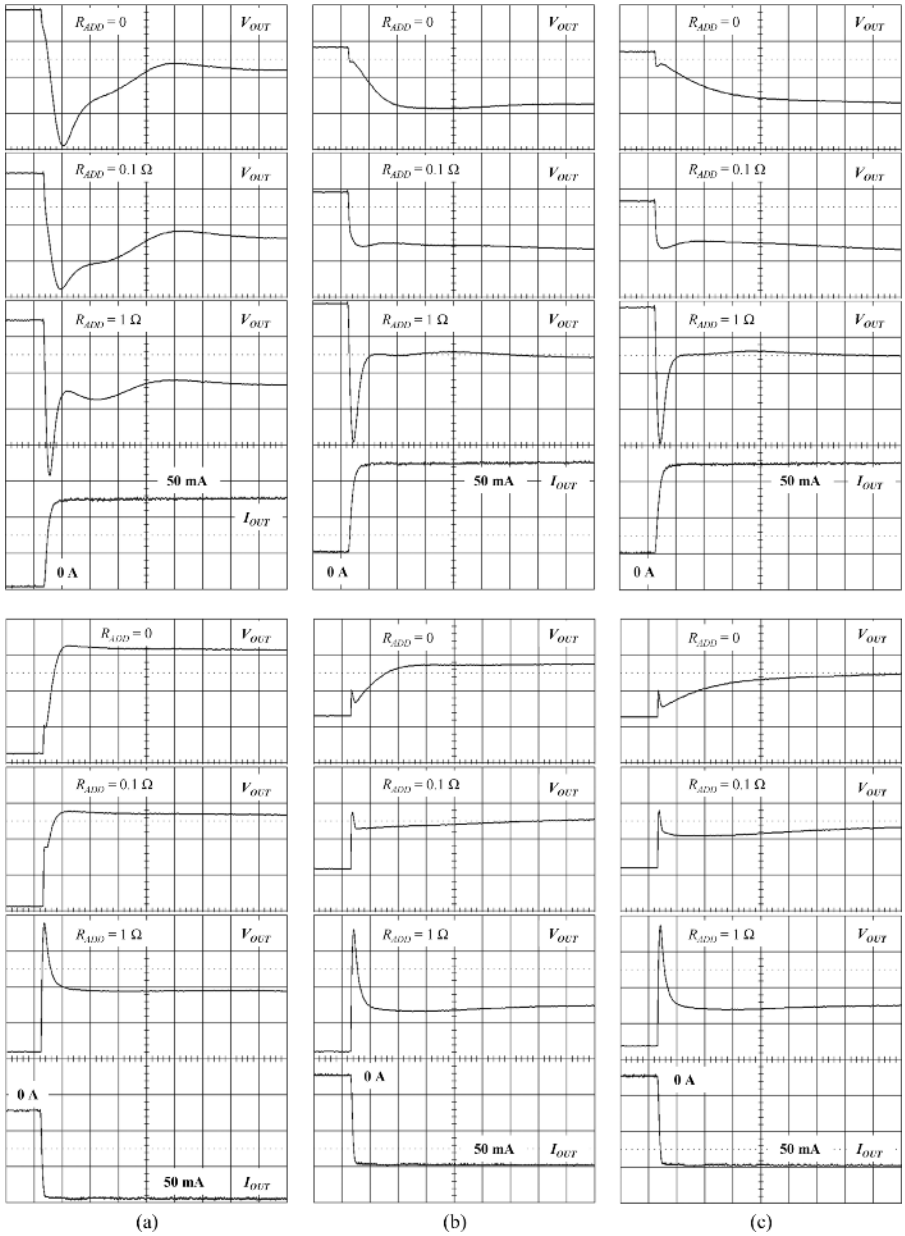


Fig. 10. Measured load transient responses with an off-chip capacitor of 1, 4. , and 10 μF, where $R_{\rm ADD}$ is the added series resistance (zoom-in view, $\rm time\,base = 1\ \mu s$ and $V_{\rm OUT}$ displays at 10 mV/DIV). (a) $C_{\rm OUT} = 1\ \mu$F and $R_E \approx 16\ \rm m\Omega$. (b) $C_{\rm OUT} = 4.7\ \mu$F and $R_E \approx 32\ \rm m\Omega$; (c) $C_{\rm OUT} = 10\ \mu$F and $R_E \approx 32\ \rm m\Omega$.

where (W/L) is the aspect ratio of M_C. The variables in equation in (10) are extracted to

$$\Delta I_{\rm SDC} = \left[\mu_p C_{\rm OX}\left(\frac{W}{L}\right)(V_{\rm SGC} - V_{\rm TH})\right]\Delta V_{\rm SGC} + \frac{\mu_p C_{\rm OX}}{2}\left(\frac{W}{L}\right)\Delta V_{\rm SGC}^2. \quad (11)$$

From (11), it is found that the first term refers to the expected response such that a positive $\Delta V_{\rm SGC}$ results in a positive $\Delta I_{\rm SDC}$, and vice versa. However, the $\Delta V_{\rm SGC}^2$ term helps the positive $\Delta V_{\rm SGC}$ (step-down load case) but discourages the case with a negative $\Delta V_{\rm SGC}$ (step-up load case). Therefore, when both step-up and step-down cases are needed to improve, a larger overdrive voltage is preferred, while a small W/L of M_C is suggested.

V. Experimental Results

The LDO regulator shown in Fig. 1 has been implemented in AMS 0.35-μm CMOS process. The chip micrograph is shown in Fig. 6. The chip area without testing pads is $140\ \mu\rm m \times 320\ \mu m$. The regulator is designed to provide a load current of 0–50 mA with an output voltage of 1 V from a 1.2- to 1.5-V supply. The dropout voltage is about 200 mV at the maximum $I_{\rm OUT}$ (the worst case). The ground current is 95 μA.

The measured line and load regulations at $V_{\rm IN} = 1.2$ V are 18 mV/V and 280 $\mu \rm V/mA$, respectively. Fig. 7 shows the load regulation of the STC-LDO at $V_{\rm IN} = 1.2$ V.

The measured load transient responses are shown in Figs. 8, 9 and 10. In Fig. 8, smaller-value capacitors (1 nF and 47 nF) are used. Their measured ESRs are larger, as predicted and are about 4.4 Ω (for $C_{\rm OUT} = 1$ nF) and 2.2 Ω (for $C_{\rm OUT} = 47$ nF),

TABLE I
SUMMARY OF EXISTING LDO STRUCTURES

Ref.	Power Transistor	Features	Technology	I_Q	V_{IN}	$I_{OUT(max)}$	Line Reg.	Load Reg.
[18]	NMOS	Charge-pumped gate drive for low dropout, cap-free.	0.8-μm BiCMOS	N/A	4 V	5 mA	49 mV/V	22 mV/7 mA
[21]			BiCMOS	0.55 mA	1.7 – 5.5V	150 mA	0.01%/V	0.002%/mA
[19]	DMOS	Zero V_{TH} device for low dropout., cap-free.	DMOS	1 mA	N/A	500 mA	N/A	N/A
[20]	PMOS	Adaptively-biased buffer for fast transient response and high efficiency.	2-μm CMOS	23 μA	≥ 1 V	50 mA	4 mV/3.8 V	19 mV/50 mA
[5]		Advanced frequency compensation scheme for loop stability. Cap-free in [7] and [8].	2-μm CMOS	N/A	N/A	50 mA	N/A	12 mV/100 mA
[7]			0.6-μm CMOS	38 μA	1.5 – 4.5 V	100 mA	0.25% in total	
[8]			0.35-μm CMOS	N/A	1.2 – 3.3 V	100 mA	344 μV/V	388 μV/mA
[9]			0.5-μm CMOS	25 μA	3.3 V	160 mA	N/A	0.2 V/160 mA
[10]			0.35-μm CMOS	53 μA	2 – 5 V	150 mA	0.143%/V	92.8 ppm/mA
[13]		Simple LDO structure. Cap-free in this paper.	90-nm CMOS	6 mA	1.2 V	100 mA	N/A	N/A
This work			0.35-μm CMOS	95 μA	1.2 – 1.5 V	50 mA	18 mV/V	280 μV/mA

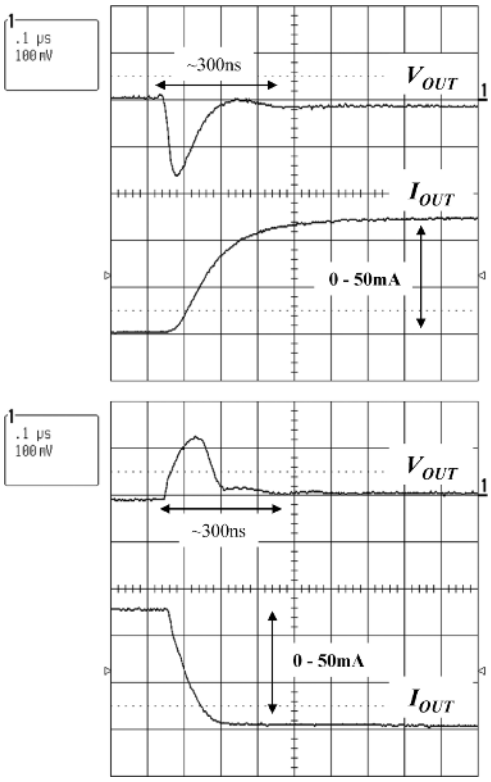


Fig. 11. Measured load transient response of the STC-LDO in no-capacitor condition.

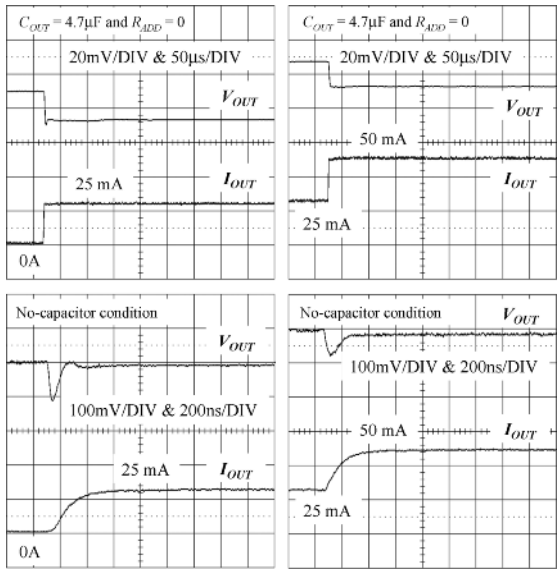


Fig. 12. More results of the load transient responses for the case with $C_{\rm OUT} = 4.7\ \mu$F and the no-capacitor condition.

respectively. It is obvious that the STC-LDO is stable in both cases. The settling time is as fast as $< 1\ \mu$s. In Fig. 9 (Fig. 10 is the zoomed-in views), low-ESR capacitors are used for the measurement. $C_{\rm OUT} = 1\ \mu$F, 4.7 μF and 10 μF with $R_E = 16$ mΩ to 32 mΩ. In these measurement, $I_{\rm OUT}$ changes between 0 and 50 mA in about 500 ns. An added resistor $R_{\rm ADD}$ is connected in series with the off-chip capacitor to test the effects of the additional ESR with increment of decades. From Fig. 8, it is obvious that the STC-LDO is stable for those cases. The larger voltage spike when $I_{\rm OUT} = 0 \rightarrow 50$ mA and 50 mA $\rightarrow 0$ is introduced by the transient current flowing into the larger $R_{\rm ADD}$. Therefore, when the STC-LDO is stable, it is no reason to add $R_{\rm ADD}$.

For the no-capacitor case, a load transient response has been measured and is shown in Fig. 11. The measurement probe capacitance is about 20 pF, and $p_{3(nc)}$ is therefore higher than 1 MHz, which is the estimated UGF of the loop bandwidth of the STC-LDO. From the result, the STC-LDO is again proven stable and responds fast to settle $V_{\rm OUT}$ in about 300 ns. As a remark, there is no minimum load current requirement for the STC-LDO to be stable in the no-capacitor condition [7], [8].

More measurement results are included in Fig. 12 to prove the LDO is stable when the loading current changes from 0 to a moderate value and then to the maximum value. Two cases are specially tested: $C_{\rm OUT} = 4.7\ \mu$F and the no-capacitor condition. From the measurement waveforms, it is obviously that the LDO is stable.

VI. Conclusion

In this paper, the LDO regulator based on the FVF to reduce the output impedance has been described. The impacts of the structure have been examined. It has been discussed that the STC-LDO structure provides much better LDO stability than the conventional LDO. In particular,

1) The loop bandwidth at low load current is independent of the load current. It has wider bandwidth than the conventional LDO.
2) The requirement of the ESR of the output capacitor is relatively easier to achieve, comparing the conventional LDO. It is due to the fact that the load-dependent range of the second non-dominant pole is bounded.
3) The STC-LDO is absolutely stable for an output capacitor with a small or large ESR.
4) In addition, it is also absolutely stable in the no-capacitor condition. The loop bandwidth is wide as well for faster transient response.

Moreover, the load transient response has been investigated. A design condition to improve the sensitivity of the control transistor has been derived. Experimental results have proven the analysis and the stated arguments.

Finally, Table I summarizes the existing LDO structures using MOS technology, their features and the specifications. From this table, it reveals the recently developed approaches of LDOs, focusing on the improving the stability and transient response, as well as the most recent work–simpler LDO structure, which is the contribution of this paper.

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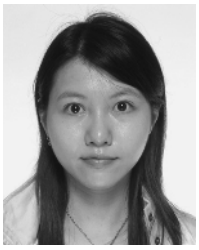

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