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Development of SOI pixel process technology

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ABSTRACT

A silicon-on-insulator (SOI) process for pixelated radiation detectors is developed. It is based on a 0.2 μm CMOS fully depleted (FD-)SOI technology. The SOI wafer is composed of a thick, high-resistivity substrate for the sensing part and a thin Si layer for CMOS circuits. Two types of pixel detectors, one integration-type and the other counting-type, are developed and tested. We confirmed good sensitivity for light, charged particles and X-rays for these detectors.

For further improvement on the performance of the pixel detector, we have introduced a new process technique called buried p-well (BPW) to suppress back gate effect. We are also developing vertical (3D) integration technology to achieve much higher density.

1. Introduction

A silicon-on-insulator (SOI) technology is a very attractive method to get high-speed and low-power LSI circuit. With its unique structure of two different Si layers in a single wafer, researchers developing imaging devices have long expected to realize high-performance monolithic pixel detectors via the SOI technology. However, thus far, development of SOI radiation image sensor has been mostly limited to laboratory scale [1].

We have been developing an SOI pixel process based on OKI Semiconductor Co. Ltd. 0.2 μm CMOS fully depleted (FD-)SOI process [2]. The SOI wafer is composed of a thick, high-resistivity substrate (sensor part) and a thin low-resistivity Si layer (CMOS circuitry) sandwiching a buried oxide (BOX) layer. After removing the top Si and the BOX layer in the region of the sensing nodes, p or n dopant is implanted to the substrate. Then contact vias and metal connections from the p–n junction to the transistors are created (see Fig. 1) [3–5]. This detector has many good features for applications in high-energy experiments, astrophysics, material analysis, medical imaging and so on.

- There is no mechanical bump bonding, so obstacles which cause multiple scattering are eliminated and smaller pixel size is possible.
- Parasitic capacitances of sensing nodes are very small (~10 fF), so large conversion gain and low noise are possible.
- Full CMOS circuitry can be implemented in the pixel.

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- The cross-section of single event effects caused by radiation is very small. A latch-up mechanism, which destroys conventional bulk CMOS LSI, is absent.
- Unlike conventional CMOS process, there is no leakage path to bulk. Thus SOI transistors are shown to work over a very large temperature range from 4 to 600 K.
- The technology is based on industry standards, so further progress and lower cost are foreseeable.

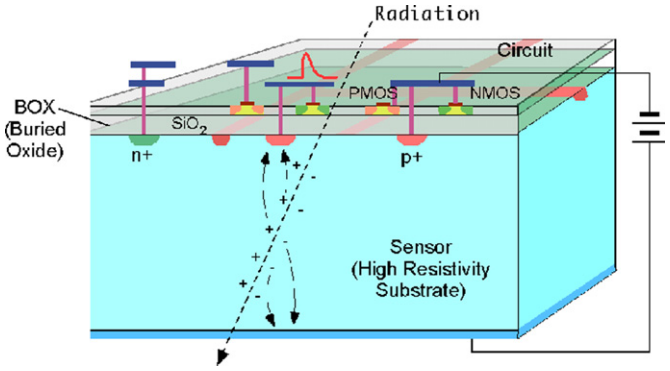

Fig. 1. Cross-sectional view of the SOI pixel detector.

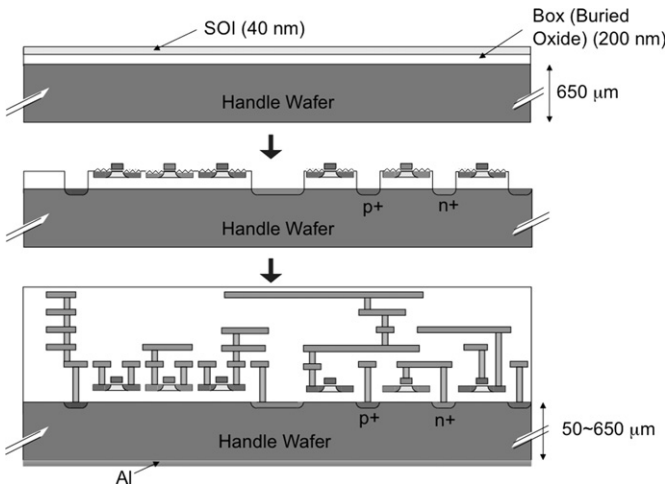

Fig. 2. Simplified SOI pixel process flow.

Table 1
SOI pixel process specifications.

Process	0.2 μm Low-leakage fully depleted SOI CMOS, 1 Poly, 4 metal layers, MIM cap., DMOS option core (I/O) voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, Top Si: Cz, ~18 Ω-cm, *p*-type, ~40 nm thick Buried oxide: 200 nm thick Handle wafer: Cz *n*-type 700 Ω-cm, 725 μm thick
Backside	Thinned to 260 μm and sputtered with Al (200 nm).
Transistors	Normal and low threshold transistors are available for both core and IO transistors. Three types of structures (body-floating, source-tie and body-tie) are available.
Optional process	Buried p-well formation Vertical integration with μ-bumps.

- Emerging vertical (3D) integration techniques are a natural extension of the SOI technology, so a much higher integration density is possible.

In Section 2, we describe the details of the process. The R&D effort on vertical integration is shown in Section 3. In Section 4, some of the test results of the SOI pixel detectors we have developed are shown.

2. SOI pixel process

In Fig. 2, a simplified procedure for the fabrication of the SOI pixel is shown. First, conventional SOI processes are performed to

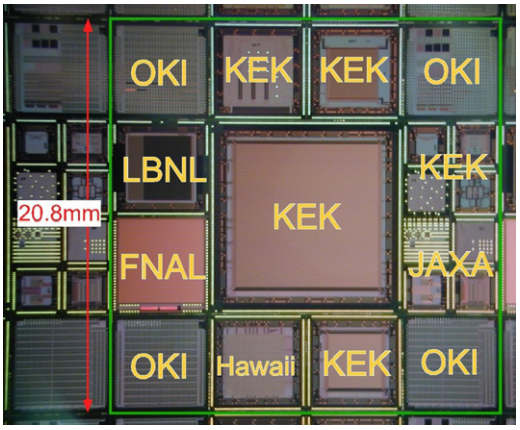

Fig. 3. A photograph of a wafer processed in 2008. The mask size used is 20.8 × 20.8 mm. In addition to Japanese laboratories and universities, US institutions also contributed designs.

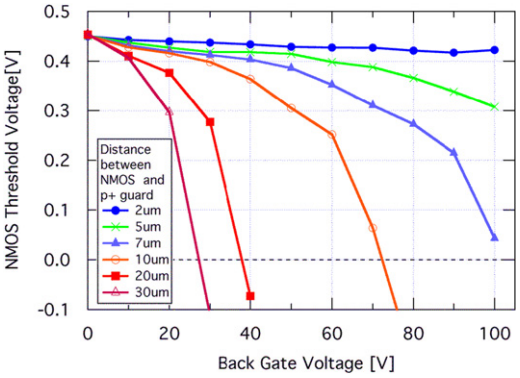

Fig. 4. Simulation results of NMOS transistor threshold voltage shift by the back gate voltage. By creating guard ring around the transistor at the distance shown, the shift can be reduced.

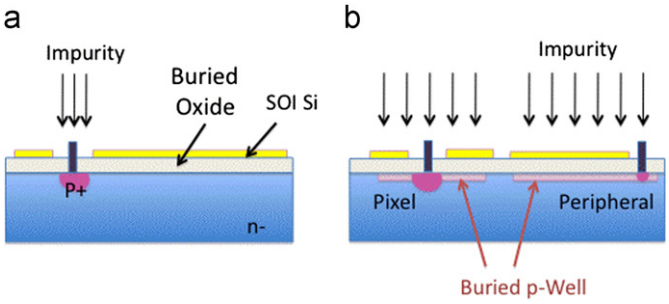

Fig. 5. (a) Normal implantation method to create p–n junction in the substrate and (b) buried p-well implantation method. By fixing the BPW potential under peripheral circuit, the back gate effect is completely suppressed. In the pixel area, BPW may be used to extend sensor area.

form transistors. Then the BOX layer is opened to implant p+ and n+ dopant to the handle wafer. After the implantation, annealing and contact via formation through the BOX are done. Then, conventional backend processes are followed.

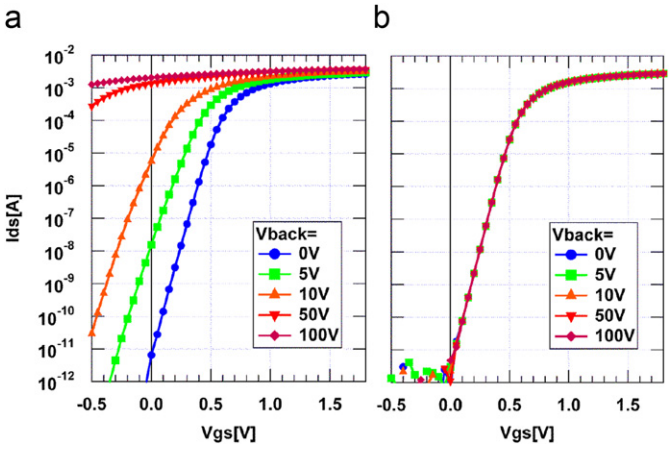

Fig. 6. Backside voltage dependence of an NMOS Id–Vgs curve (a) without BPW and (b) with BPW connected to 0 V.

The main specifications of the process are summarized in Table 1. The process has two kinds of transistors: core and I/O transistors. There are three types of transistor structures: body-floating, body-tied and source-tied. Metal–insulator–metal (MIM) capacitors, depletion MOS (DMOS) transistors, lateral diodes and several kinds of resistors are also available.

To reduce the development cost, several chip designs are put on a mask. We submitted two runs in year 2009. In each run, we

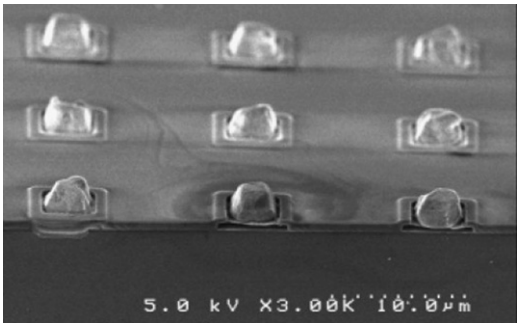

Fig. 8. Photograph of the µ-bumps created on the SOI pixel.

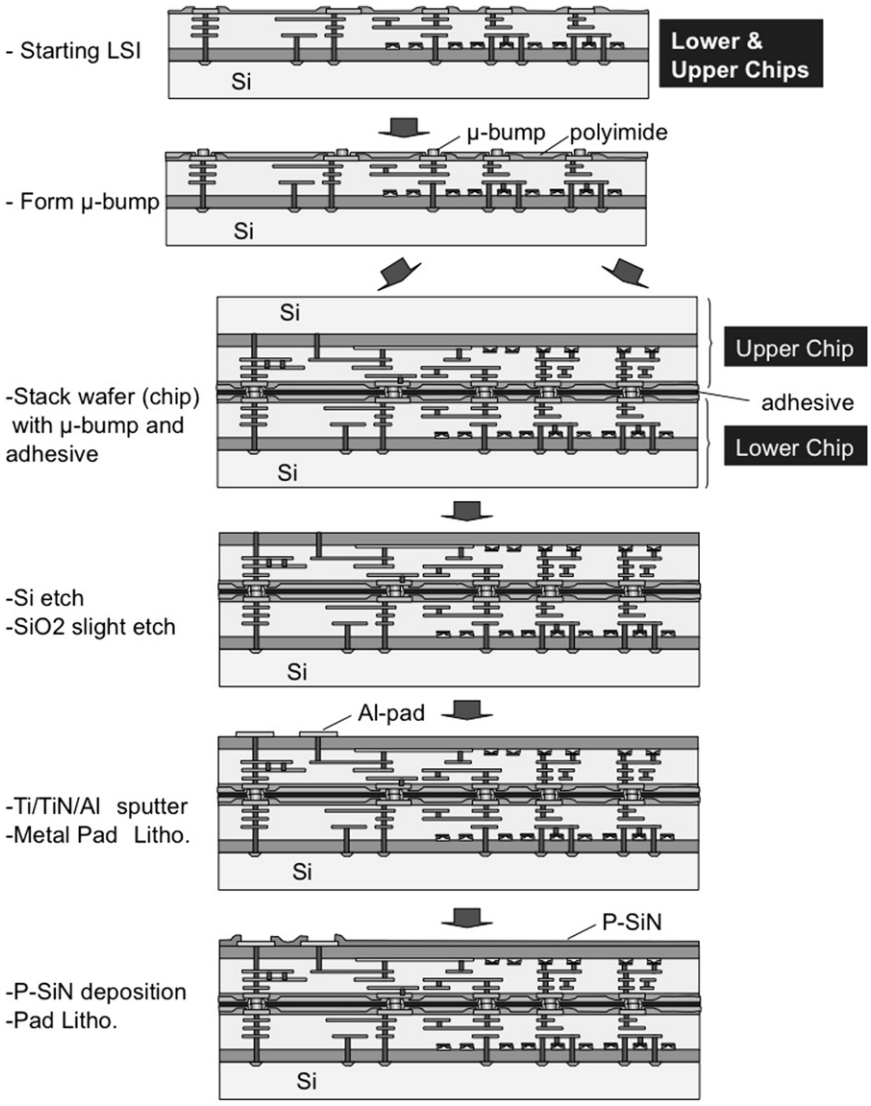

Fig. 7. Process flow of the µ-bump bonding.

included about 16 designs from our collaborators [6–8]. A photograph of a wafer from the recent run is shown in Fig. 3.

2.1. Back gate effect

One of the major difficulties in creating a sensor from the SOI wafer substrate is the back gate effect. Since the area under the transistor acts as a back gate, its potential affects the threshold voltage and the leakage current of the transistor.

The back gate effect is small compared to the front gate since the front gate oxide (~4 nm) is much thinner compared with that of the buried oxide (~200 nm). However the required backside bias voltage is very high (>100 V) since sensor construction usually requires a thick depletion layer. So the back gate effect cannot be neglected.

One method to reduce the back gate effect is the creation of a guard ring around the transistors. By keeping the distance between the transistors and the guard ring less than 10 μm or so, the threshold voltage shift can be reduced to an acceptable level (Fig. 4). However this method needs additional area and decreases the integration density, so this is not a desirable solution in most of the cases.

To avoid the area penalty, we developed Buried p-well (BPW) process (Fig. 5). We implant p-type dopant through the top Si layer and create a buried p-well (BPW) region under the BOX. This BPW region will help to stabilize the underside potential of the transistors. The doping level of the BPW is about 3 orders of magnitude lower than that of the p+ sensor node and drain/source region, so it does not affect the transistor characteristics. In addition, the implantation energy is controlled so that the peak density will be located under the BOX region.

Fig. 6 shows Ids–Vgs curve of an NMOS transistor when the back gate voltage is applied. The Ids–Vgs characteristics, especially on NMOS, change dramatically when the back gate voltage is applied. However, by introducing the BPW and connecting it to a fixed voltage, this effect is completely suppressed.

The suppression of the back gate effect is also confirmed in existing pixel chips. Signal charge increases by increasing the detector voltage, but in the absence of a BPW layer the output signal will decrease if the detector voltage exceeds 15 V or so. With the addition of the BPW layer, the same kind of pixel chip works for more than 100 V detector voltage without problem.

The BPW process also introduces many attractive features for the pixel application: it reduces electric field gradients at a critical point, so that break down voltage increases. Furthermore, we can create large sensing nodes without removing the top Si layer.

2.2. Radiation hardness

Since the active Si layer is very thin (~40 nm), radiation generated charge is also small. Thus the Single Event Effect (SEE) cross-section of the SOI chip is normally small compared with that of the conventional CMOS circuit.

As for the Total Ionizing Damage (TID), the SOI chip is not necessarily radiation hard since it has relatively thick buried oxide (BOX) of ~200 nm, so radiation generated holes will tend to be trapped. The transistor threshold voltage shifts a few hundreds of mV after a dose of one hundred krad (Si). This becomes worse when we apply the backside voltage.

In this aspect, the reduction of BOX electric field by using the BPW layer helps to increase radiation hardness, since it increases recombination probability of generated electron–hole pairs in the BOX. Further studies to reduce the effect of hole trap in the BOX are also ongoing.

3. Vertical integration

Since the performance improvements by shrinking the process technology are approaching the limit, vertical (3D) integration technologies are emerging in the semiconductor industry. In addition to higher circuit density, in 3D technology, signal propagation time can be shortened, so that higher performance and lower power can be realized.

Vertical integration is especially desirable in pixel applications, since it can enhance pixel functions without increasing pixel size. The SOI technology is well suited for vertical integration.

We have designed a test chip applying vertical integration. We used μ-bump technology of ZyCube Co. Ltd. [9]. Minimum pitch of the bump is 5 μm. The bonding process is shown in Fig. 7. The test chip, which includes 13 μm pitch pixels and several test elements, is fabricated in OKI Semiconductor and then bonded at ZyCube. Photograph of the μ-bumps and the cross-section of the bonding is shown in Figs. 8 and 9. Detailed tests are under preparation.

4. Results of pixel detectors

We are mainly developing two kinds of pixel detectors. One is an integration-type pixel called INTPIX, and the other is a counting-type pixel called CNTPIX. There are also many other designs by MPW users.

4.1. Integration-type pixel

The basic schematic of the integration-type pixel (INTPIX) is shown in Fig. 10. INTPIX2 and 3 chips are 5 × 5 mm in size having

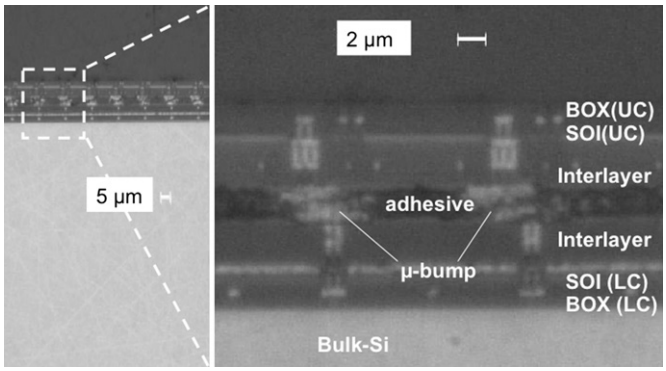

Fig. 9. Cross-sectional view of the μ-bump bonding after stacking.

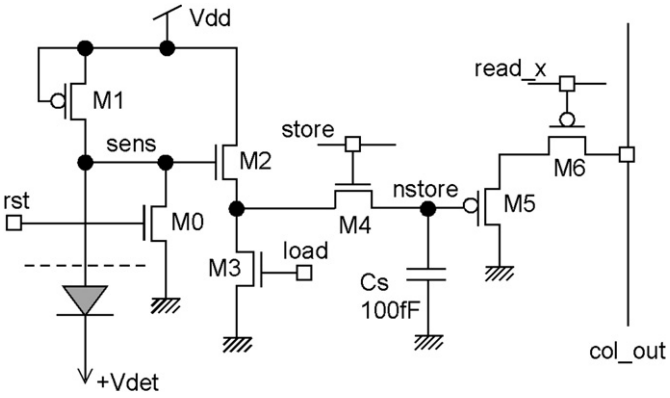

Fig. 10. Schematic of the integration type pixel (INTPIX).

128×128 pixels each 20 μm square. Reverse bias voltage is applied from the bottom surface or top n+HV ring. Leakage current and break down voltage of the INTPIX3 are shown in Fig. 11. The leakage current is about 10 nA at 100 V bias voltage, and the break down voltage is about 160 V.

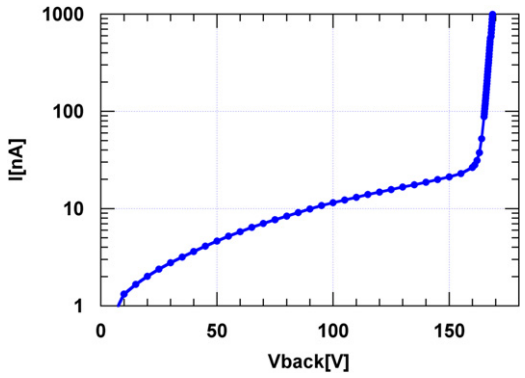

Fig. 11. Sensor leak current and break down voltage (INTPIX3, 5×5 mm^2 chip, measured at 5 °C).

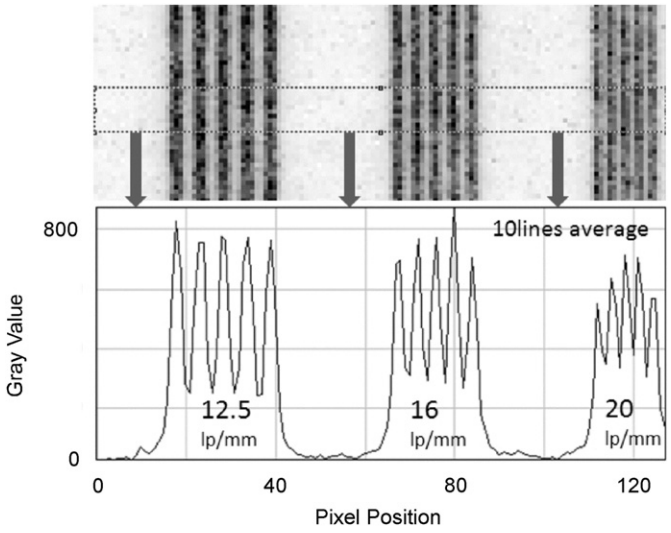

Fig. 12. X-ray image taken with the integration type pixel (INTPIX2).

Fig. 12 shows a test chart image taken by the INTPIX2 with ~8 keV X-rays. It indicates 20 lines/mm are resolved well. The present INTPIX has a window area, in which there are no metal or transistors, allowing illumination from the topside to ease testing. It may be possible to shrink the pixel size to less than 10 μm squares.

4.2. Counting-type pixel

A pixel circuit of the counting-type pixel (CNTPIX) is shown in Fig. 13. The preamplifier circuit is based on that proposed by Krummenacher [10] which contains leakage current compensation circuitry. After the low and high threshold discriminator, the input signal is processed in a 16-bit counter.

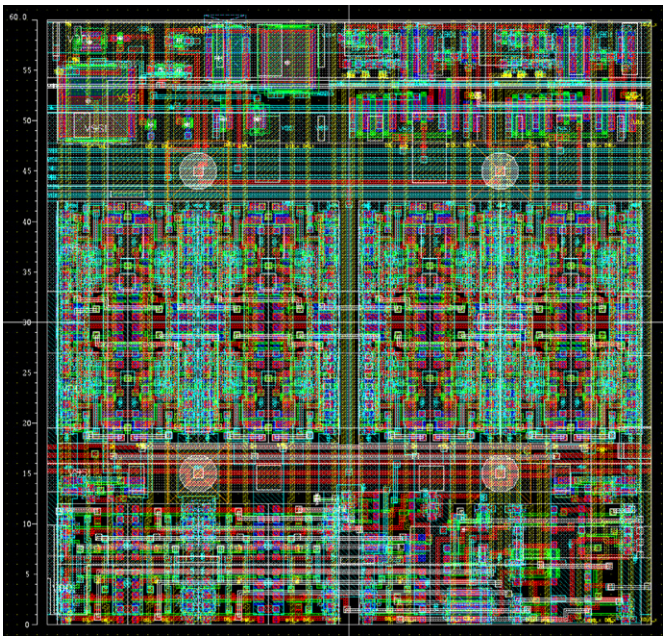

Fig. 14. Layout of a pixel in the CNTPIX2 chip. The size of a pixel is 60×60 μm, and each pixel contains about 600 transistors.

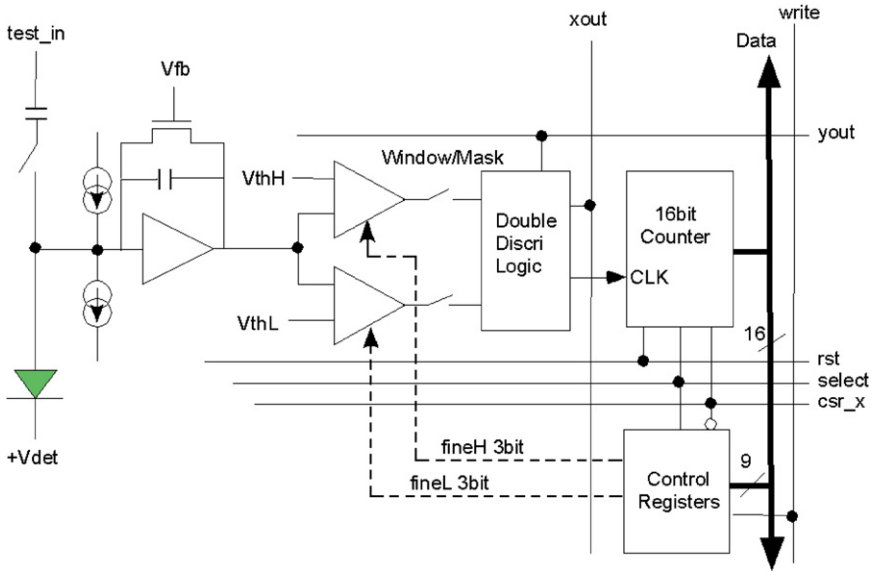

Fig. 13. Circuit of the CNTPIX2 pixel.

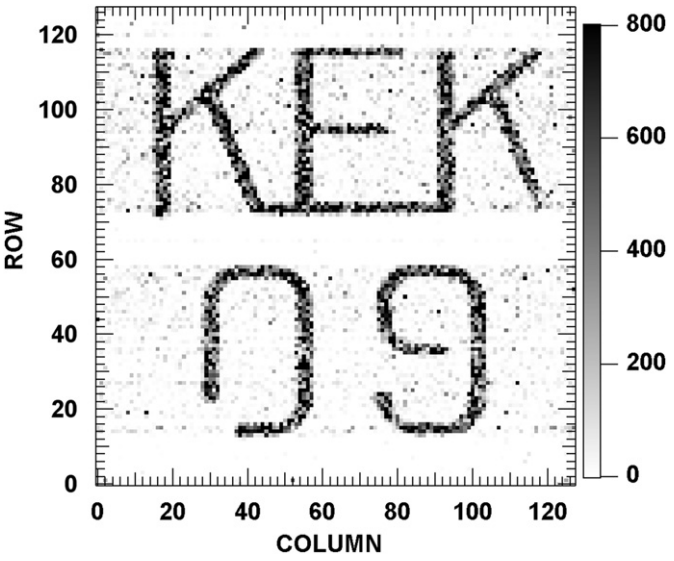

Fig. 15. X-ray image taken with the CNTPIX2. X-ray generator with Cu target was used.

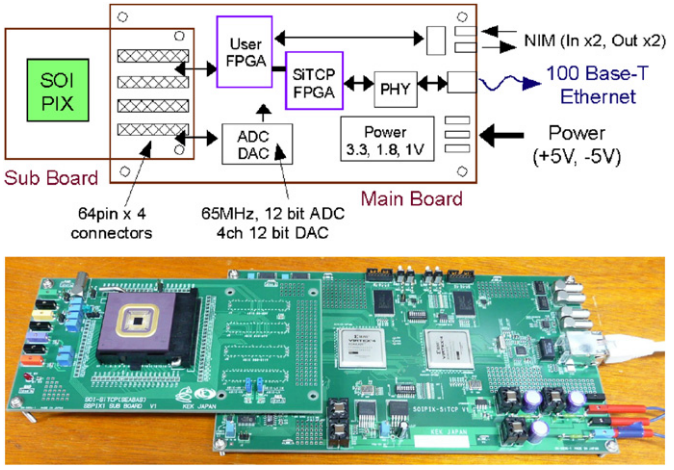

Fig. 16. (top) Block diagram of the SEABAS board. (bottom) Photograph of the SEABAS board and its sub-board.

The layout of the CNTPIX2 is shown in Fig. 14. The size of a pixel is about 60 μm square, and there are 128 × 128 pixels in a 10 mm square chip.

A metal plate image taken with 8 keV X-ray is shown in Fig. 15.

4.3. Test system

We have developed a test board called SEABAS (SOI Evaluation Board with SiTCP[11]). It has two FPGA chips, one is for pixel control signals and the other handles TCP/IP protocol to communicate with PC via Ethernet. Each pixel chip is mounted on a sub-board and connected to the SEABAS board through four 64-pins connectors. The block diagram and photograph of the SEABAS main/sub board is shown in Fig. 16.

The SEABAS board also has 65 MHz 12 bit ADC, a four channel 12 bit DAC, and NIM I/O ports for easy testing.

5. Summary

We have developed a SOI pixel process based on a commercial 0.2 μm FD-SOI process. We have demonstrated basic performance of the SOI integration-type and counting-type pixel detectors.

A new implantation process which creates buried p-well (BPW) under the BOX is introduced. We confirmed the BPW suppress the back gate effect very efficiently. The BPW process also gives us the possibility to increase break down voltage and radiation hardness.

We are also developing 3D integration technology by using the μ-bump bonding technique. The μ-bump pitch is only 5 μm, so we can increase the functionality of a pixel without increasing the pixel size.

We also developed an easy-to-use test board.

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