Development of the scalable readout system for micro-pattern gas detectors and other applications

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Development of the scalable readout system for micro-pattern gas detectors and other applications

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ABSTRACT: Developed within RD51 Collaboration for the Development of Micro-Pattern Gas Detectors Technologies, the Scalable Readout System (SRS) is intended as a general purpose multi-channel readout solution for a wide range of detector types and detector complexities. The scalable architecture, achieved using multi-Gbps point-to-point links with no buses involved, allows the user to tailor the system size to his needs. The modular topology enables the integration of different front-end ASICs, giving the user the possibility to use the most appropriate front-end for his purpose or to build a heterogeneous experimental apparatus which integrates different front-ends into the same DAQ system. Current applications include LHC upgrade activities, geophysics or homeland security applications as well as detector R&D. The system architecture, development and running experience will be presented, together with future prospects, ATCA implementation options and application possibilities.

KEYWORDS: Electronic detector readout concepts (gas, liquid); Data acquisition circuits; Modular electronics; Data acquisition concepts

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1 Introduction

Established in 2008, the RD51 Collaboration [1] brings together more than 80 institutions worldwide in a collective effort to sustain the development of the Micro-Pattern Gas Detector (MPGD) technologies and increase their impact in the scientific research. Parallel to the development of new detectors, the community recognized the need for new developments in the field of associated readout electronics. A dedicated working group was formed within the collaboration and mandated to establish a "Portable Multichannel Readout system for Multi Pattern Gas Detectors" and to develop a discharge protection strategy to protect the electronics when used for Gas detectors like MicroMegas or GEMs. In 2009, the Scalable Readout System (SRS) was proposed featuring a scalable architecture and a general-purpose chip link interface, allowing the user to choose from a variety of front-end chips on hybrids with integrated spark protection circuitry.

First prototype SRS systems were introduced in fall 2010 and were successfully used for cosmic tomography using GEM detectors and for R&D work of the ATLAS MicroMega stations at the CERN's SPS. Following this encouraging experience, first small SRS systems with channel counts in the order of 16,000 channels were deployed for the MPGD community and also detector teams with solid state detectors are preparing for using SRS with appropriate readouts chips.

In the following section a brief overview of the SRS system will be given, while section 3 will go into more detail about the development of the individual SRS components. Finally section 4 will briefly cover the current and future applications of the system, as well as the planned upgrade of the system to an industrial standard like ATCA.

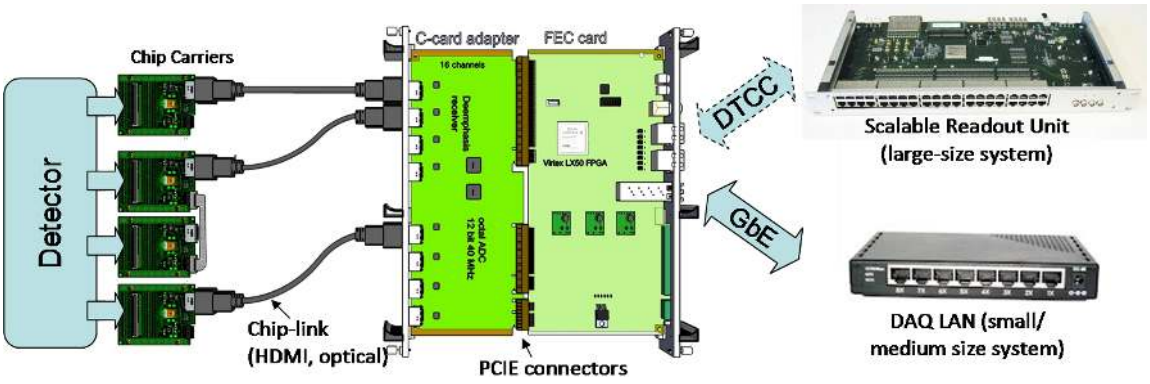

Figure 1. Overview of the SRS DAQ unit.

2 The SRS architecture

2.1 Overview

Figure 1 shows a schematic view of the SRS DAQ unit, which is the base of the entire system. This DAQ unit is split in three parts. In the front-end of the system, close to the detector, a front-end hybrid carries the front-end ASIC together with all necessary supporting circuits (discharge protection, power regulators, etc.). On the other end of the DAQ unit there is a FPGA-based card called Front-End Card (FEC), which contains most complex circuits of the DAQ unit (programmable logic, memory, high-speed communication). Between the two ends of the DAQ unit there is a specific "chip-link" cable and an Adapter Board, which plugs in to the FEC board using edge-mount PCI-E type connectors.

With this modular scheme, the Adapter Board can be tailored to the particular front-end ASIC and/or with the particular application, giving the user the freedom of choice for the front-end circuit which is most suitable for his detector and application. The back-end board (the FEC card) remains fixed for all applications while the adapter board can be exchanged if the application requirements call for a different front-end, channel density, etc. Since most of the high-cost components (FPGAs, memory, high-speed devices) sit in the FEC board and the rest of the back-end system, which is identical for all users and applications, the users can share a higher volume production for these boards, thus reducing the cost. In practice, as it will be seen in the following sections, also the Adapter Boards can have a multiple use, integrating different front-end circuits with sufficiently similar interface.

2.2 Scalability concept

The SRS system design uses a bivalent scalability concept. On one hand side, the user can expand the system in the application dimension, exploiting the possibility to use different front-ends as briefly described in the previous section. On the other hand side, SRS employs a star topology (see figure 2) with point-to-point connections between all components of the system, which enables the user to increase the number of DAQ cells when moving to a larger area detector, for instance, avoiding the inherent bandwidth and reliability issues with more traditional DAQ busses.

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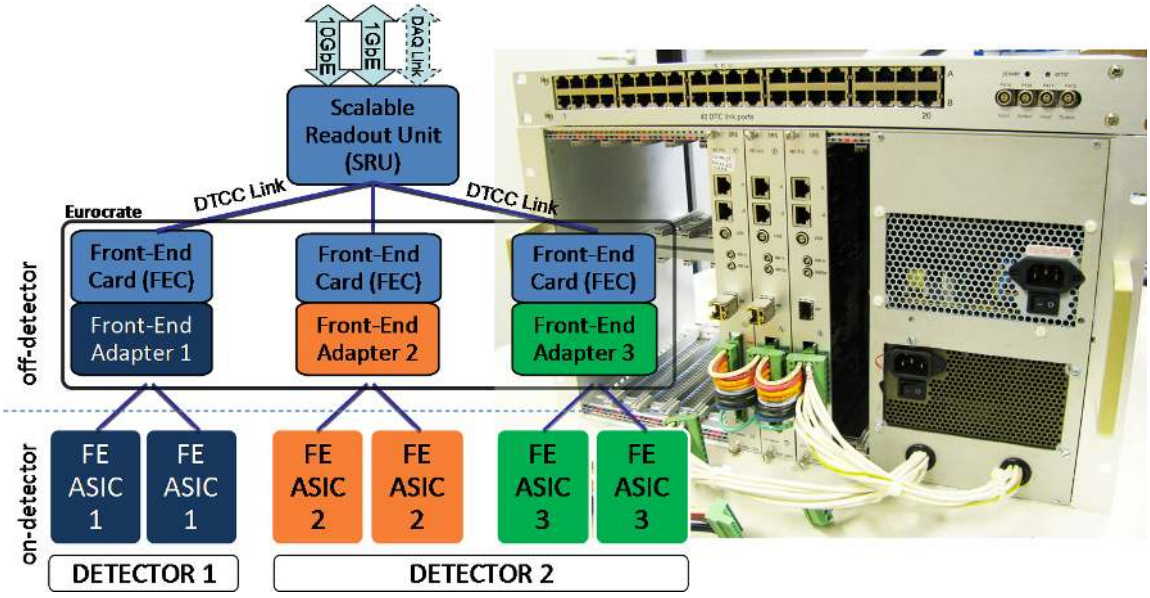

Figure 2. Architecture of the SRS system.

A standard 6U Eurocrate can host the FEC and Adapter cards, each being accessed from the opposite sides. A number of boards can be placed in parallel in the same crate expanding the number of detector channels which are readout. As it will be seen in the following sections, in most practical cases each SRS DAQ unit can readout 2,048 detector channels, leading to more than 16,000 channels per crate, for an 8-board crate system.

For a small or medium-size system, the FEC card(s) can be connected to the DAQ cluster via Gigabit Ethernet for data transfer and slow-control operations. The SFP technology used accepts either optical or copper Ethernet plugs which are commercially available. If more boards are used, a commercial network switch can merge the DAQ data streams to one or more DAQ PCs.

In these two cases the clock and trigger are sent using legacy NIM circuitry or from LVDS sources. If a more complex system is envisaged, a higher level component is supplied, namely the Scalable Readout Unit (SRU) (see figure 2). In this case the FEC board uses the second type of DAQ port to connect to the SRU which bundles together data transfer, clock & trigger information and slow-control channel over inexpensive CAT6/7 cable (DTCC Link). Up to 40 FEC cards can be connected to the same SRU, boosting the number of detector channels to more than 80,000 channels. The SRU offers additional programmable logic resources and buffering memory for event building and data reduction, providing 10 Gb Ethernet interface to the DAQ farm, or generic SFP+ interfaces that can be used with application-specific protocols.

Regarding the trigger specifications, the SRS concept does not take assumptions about any specific architecture. Fast trigger connections are provided in both directions, giving the possibility to transport trigger primitives from the detector and implement both trigger-driven or trigger-less (data driven) readout schemes.

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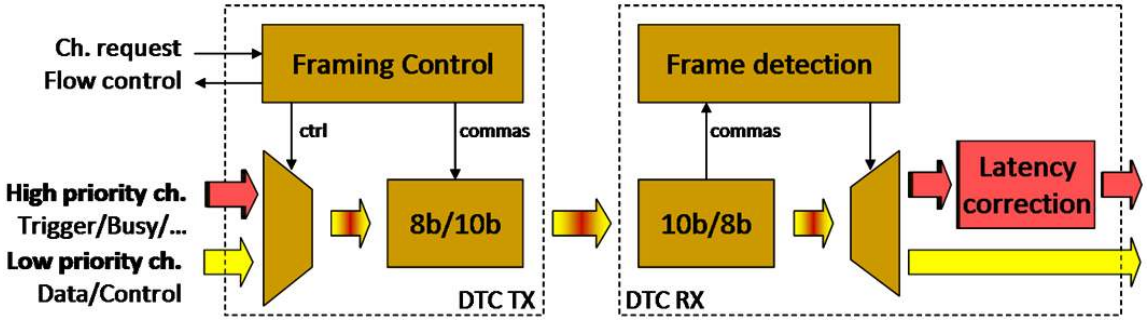

Figure 3. Overview of the DTCC link protocol.

2.3 Serial transport of data, trigger, clock and control information

2.3.1 Chip link

Depending on the application, the length of the connection between the front-end hybrid and the back-end electronics (the "chip-link") can extend to tens of meters or more. In this respect, an optical link between the two would maximise the range of this connection. On the other hand, the use of optical technology would lead to an increased complexity of the front-end hybrid which is only beneficial for a larger scale experiment, where the detector environment is not suitable for the backend-electronics (radiation, magnetic field, etc.). For this reason, in the first implementation, the SRS system uses HDMI cables for this link, taking advantage of their electrical performance, availability and low cost. The HDMI cable integrates four high-speed links specified for multi-gigabit transfer rates, and a low speed serial interface (I^2C) [2]. This is sufficient for clock, trigger and serial data transport (either analog or digital), in addition to a slow-control channel. The same cable can also supply power to the front-end hybrid, eliminating the need of an additional low voltage power supply on the detectors side.

2.3.2 DTCC (Data, Trigger, Clock and Control) link

The DTCC link hosts all digital communications between the FEC cards and the SRU board for large SRS systems. The link uses LVDS signaling over shielded CAT6/7 cables, taking advantage of the high IO density and speed of modern FPGAs. The bidirectional serial link is designed to transport DAQ data, timing information (clock and trigger) and slow-control.

The link is offering two types of channels with low and high priority (figure 3). The two channels are time multiplexed using the out-of-band signaling provided by the 8b/10b encoding, with the exception that the high-priority channel can interrupt any ongoing data transmission, which is later resumed after completion of the high-priority transmission. In this way, the high-priority channel provides fixed latency necessary for the timing information (trigger, busy, etc.). The same protocol is applied to both uplink and downlink directions, giving the possibility to transport trigger primitives or timing signals generated in the front-end towards the DAQ system or to a separate Trigger System.

Current implementation offers 640 Mbps for data transport over a few meters, and fast-channel latency of 9 clock cycles (225 ns at 40 MHz system clock). With further optimization the data bandwidth should exceed 1 Gbps. An initial iterative training phase realizes phase alignment between

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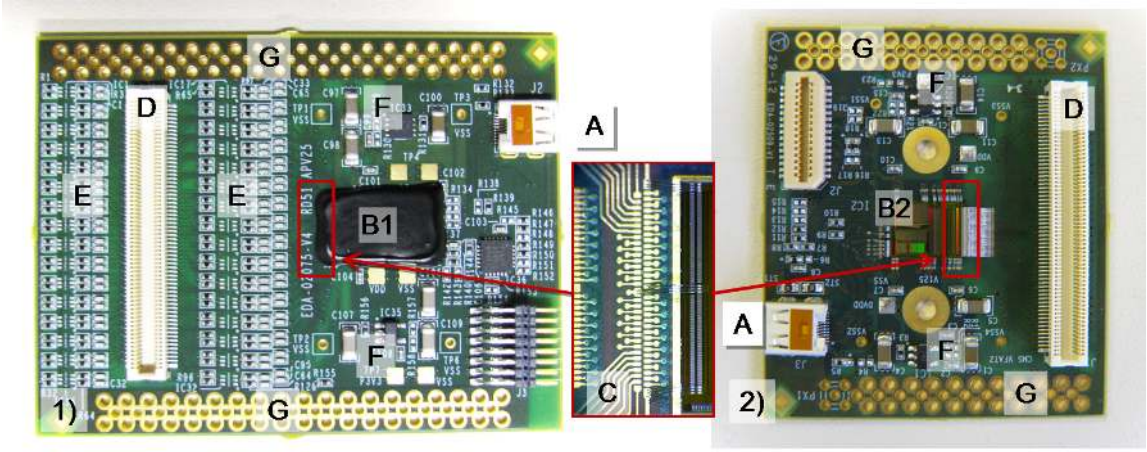

Figure 4. Front-end hybrids: 1) APV25, 2) VFAT2; A — Micro-HDMI connectors (Type-D); B1 — APV25 ASIC with top-globbing protection; B2 — VFAT2 ASIC wire-bonded; C — detail of the microvias used for the high-density wire-bond region; D — RD51 detector connectors (Panasonic); E — spark protection circuitry; F — power regulators; G — via array for the low-ohmic ground connectors.

the two remote devices. More details on the DTCC link realization will be presented in a separate paper.

3 SRS components

3.1 Front-end hybrids

As briefly described earlier, the purpose of the front-end hybrid is to host the front-end ASIC and the associated circuitry. It is physically located directly on the detector in order to minimize the stray capacitance at the input of the front-end chip. The presence of the discharge protection as close as possible to the detector readout electrodes allows a better control and containment of the discharge, mitigating also against the spreading of the destructive discharge effects to the rest of the system.[1] The design of the hybrid tries to minimize the electrical interface between the hybrid and the rest of the DAQ system. This reduces the complexity of the overall system, leading to a higher integration density and also allowing the use of longer cables between the hybrid and the back-end system.

The first hybrid offered to the community is based on the APV25 [3] analog front-end chip (figure 4.1). The chip was designed for silicon tracking detectors in CMS, but it has also been used over the years by the gaseous detectors community, representing a great tool for detector development. The 128 input channels of the chip are AC coupled to the detector and protected against discharge by a commercial fast ESD diode with low stray capacitance (NUP4114).

[1] This aspect is very important especially when the system is used with larger area experimental gaseous detectors, where the discharge behaviour is not well controlled. In practice, in absence of proper discharge protection, we observed discharge-correlated effects also in the backend part of the system (digital upsets or, rarely, physical damage of the input circuitry of the Adapter Card). These effects were attributed to high current transients generated by the discharge which can travel across the chip-link cable if they are not effectively returned to ground at the front-end side, by proper discharge protection and low-ohmic ground connection between the front-end hybrid and the detector.

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The ground connection to the chamber is realized using one or more pairs of low-ohmic low-profile RF coaxial connector from Samtec. The connectors can be placed anywhere on the sides of the hybrid using the dedicated via array, allowing some degree of flexibility in the design of the corresponding grounding of the detector readout structure. In addition to the good ground connection for signal return, the connector assures a short return path for any discharge that is clamped by the protection diodes.

The chip is wire-bonded on the hybrid and protected by top-globbing, a process readily available in industry. One major challenge of the hybrid design was to realize the high-density wire-bond region corresponding to the input connections of the chip. After a number of iterations, the best solution from the point of view of manufacturability was the use of micro-vias, which allows the PCB bonding pads to be staggered on four rows. In this way the wire-bonds are parallel to each other, significantly increasing the yield of this process. This method avoids the use of more expensive pitch adapters.

A second hybrid which is now prototyped is based on the VFAT2 [4] chip. The chip comes in two flavours, one with integrated discharge protection and one without. For this reason there are two hybrids planned. Figure 4.2 shows the hybrid version which does not have external discharge protection.

Both hybrids use HDMI cable as electrical interface, integrating a low-profile micro-HDMI connector. In the case of the APV25 chip, the cable carries two serial analog streams as data readout. Two hybrids can be connected in a master-slave configuration on the same cable, using a low-pitch 16-lead flat cable between them.

In the VFAT2 case which offers a binary readout, the cable transports LVDS logic signals. In addition to the data and control signals the HDMI cable provides power to the hybrid. Since the front-end needs 2.5 V power supply which is regulated by local LDOs, the voltage level supplied via the HDMI cable was initially set to 3.3 V. Later, it was observed that the drop-out voltage on the HDMI cable, especially when using longer cables, can be too high for the correct operation of the LDOs. In fact, the HDMI specifications require only 50 mA as maximum supply current through the cable [2] and the hybrids use several times more. Finally, the 3.3 V supplied by the adapter boards was replaced by 5 V for correct operation of the hybrids.

A few new hybrids are now designed or planned throughout the community integrating the Beetle chip [5], Timepix [6] or MicroROC [7]. Of particular interest is also the new VMM1 chip [8] and its future versions which are designed at BNL for the ATLAS Muon Upgrade Project.

3.2 Adapter cards

An ADC-based Adapter Board was developed to be paired with the APV25 hybrid and the planned Beetle hybrid (figure 5). The board integrates 16 12-bit pipeline-ADC channels featuring up to 65 MSPS conversion rate using two octal ADCs from Texas Instruments, together with the complete slow-control and timing services for the analog hybrids. A specific challenge of the board design was to compensate for the loss of bandwidth due to long cables. An equalization filter was embedded into the front-end circuitry of the board, which provides 4 steps of equalization levels for cable length up to 30 meters. Figure 5E and 5F shows the signals before and after equalization for a cable length of 15 m. In practice, since the cables can have any length up to 30 meters the 4

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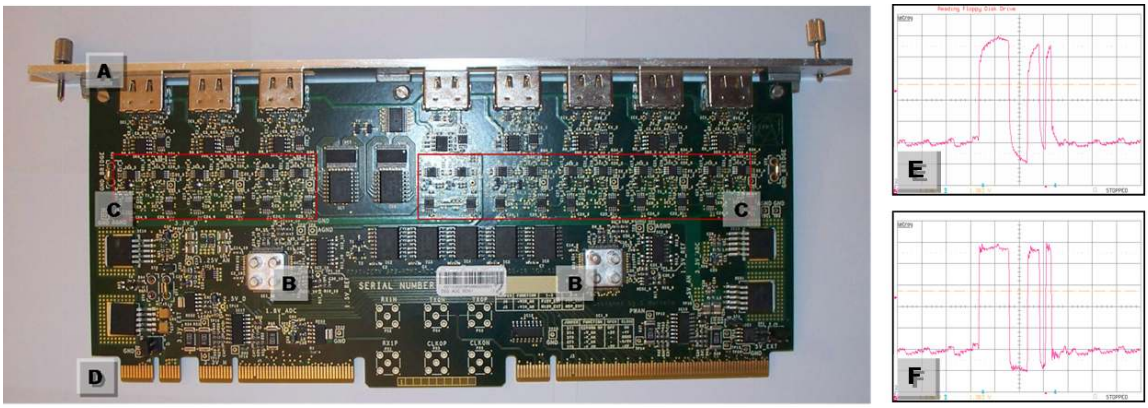

Figure 5. ADC Adapter card. A — Front panel with 8 HDMI connectors; B — two 8-channel 12-bit ADCs; C — analog equalization circuitry for long cables; D — PCIe finger connectors; E — signal shape after 15 m of HDMI cable; F — recovered signals after the equalization filter.

equalization steps do not always provide a fully adapted compensation. Additional compensation can be applied on the digital stream, either offline or online in the FPGA firmware.

Overall, the specific noise figure of the ADC Adapter Card is below 300 μVrms (0.63 ADC bins) at 40 MSPS. The total power consumption is around 9 W, or 4.5 mW per detector channel when fully equipped with 16 APV25 hybrids. The hybrids add in average another 4.6 mW per detector channel to this figure.

Another digital HDMI Adapter Board is now being prototyped for the VFAT2 hybrid or other digital chips. The board features four LVDS lines per HDMI channel, integrating digital buffers with equalization and pre-emphasis option. The four lines can be configured as 2 inputs and 2 outputs (the default VFAT2 mode), or all inputs or outputs. An additional LVDS input channel is provided as an option for each HDMI port by making use of the new featured Ethernet channel in the HDMI 1.4 specifications [2].

Both Adapter Boards presented can be used as general purpose analog or digital readout, without the use of the SRS front-end hybrids. Other adapter boards were developed by the user community for the readout of signals coming from SiPM detectors [11] or the novel VMM1 front-end prototype [8].

3.3 The FEC card

The FEC card contains most of the high-complexity components of the SRS DAQ cell. It carries out all operations required for the control of the front-end and data acquisition. The board is based around a Virtex 5 Xilinx FPGA, integrating a 2 Gbit DDR2 memory chip, one SFP connector for Gigabit Ethernet communication, general purpose NIM and LVDS interfaces and two LVDS DTCC ports. On the front-end side, the FEC board interfaces with various Adapter Boards via edge-mounted PCIe connectors. Regular IOs of the FPGA are routed to this interface, with no compliance with the PCIe signal mapping. Part of the FPGA resources are reserved for an application-specific firmware core which is linked to the application and the particular adapter board and front-end used. More details about the board can be found in [9].

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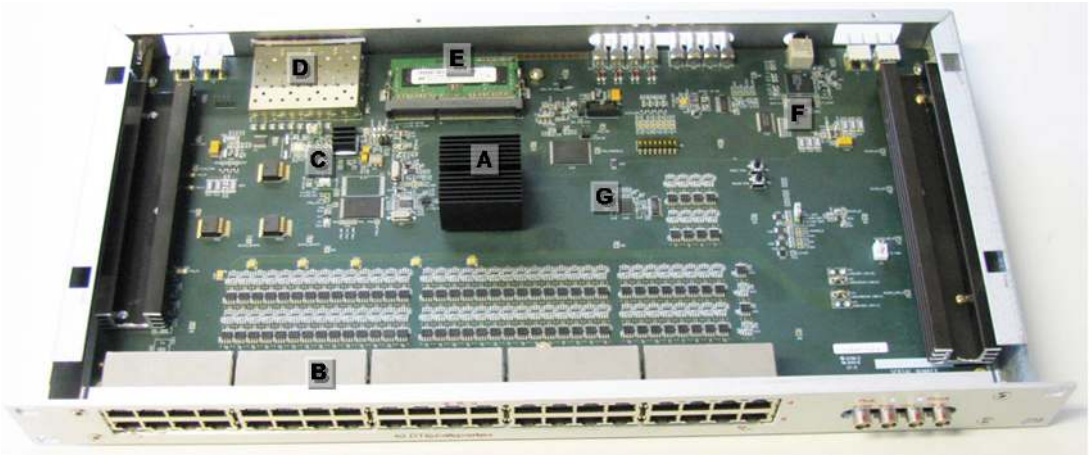

Figure 6. The Scalable Readout Unit (SRU) board: A — Xilinx Virtex 6 FPGA; B — front panel with 40 DTCC connectors (RJ45); C — 10 Gbps Ethernet Phy chip; D — quad SFP+ connector assembly (one 10 GbE and 3 lower speed (< 5 Gbps)); E — DDR3 SO-DIMM socket; F — TTCrx chip; G — jitter-cleaner PLL.

3.4 The Scalable Readout Unit (SRU)

For large systems, the complexity and cost of the Gigabit Ethernet infrastructure required to readout all SRS DAQ cells can grow considerably, due to the high amount of aggregated bandwidth and contention ratio. To alleviate this, a high level board is used called the Scalable Readout Unit (SRU) which can be connected downstream to up to 40 FEC boards using the DTCC protocol described in section 2.3.2. The SRU board offers in addition programmable-logic and memory resources that allow for event building and data buffering.

The board integrates one PHY chip for 10 Gb Ethernet data transfer over a SFP+ connector. Three other SFP+ ports are directly connected to the FPGA's high speed serial transceivers for general purpose serial data transport up to 5 Gbps. In addition, the board integrates the TTCrx [10] chip used in the LHC environment for transport of timing information. A DDR3 SO-DIMM socket accepts memory modules up to 4 GByte.

The board is designed to work under LHC conditions of magnetic field and in regions of lower radiation. The design uses only linear regulators without any magnetic materials. Moreover it offers the possibility of remote programming of the on-board firmware flash memory via Ethernet. The native Virtex6 option of continuous readback and error correction of configuration data [12] is now under evaluation.

4 Current applications and planned ATCA-SRS implementation

Since the fall of 2009 when the SRS was introduced, the readout system progressively gained momentum in the MPGD community. Medium-sized systems are currently involved in muon tomography experiments with GEM detectors in Florida [13], or in Micromegas R&D work within the Muon ATLAS MicroMegas Activity (MAMMA) at CERN. Contributors from the beginning to the SRS project, Polytechnic University of Valencia is currently using a medium-size system in the recent detector prototype for the NEXT experiment (Neutrino Experiment with a Xenon

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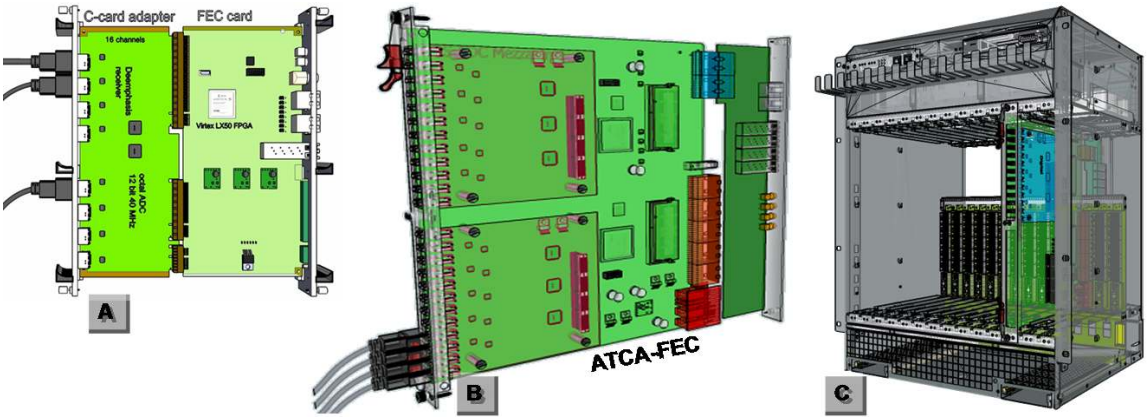

Figure 7. ATCA-SRS project overview. A — classical SRS DAQ unit; B — ATCA-FEC blade with mezzanine Adapter Boards and RTM module; C — ATCA-SRS crate.

TPC) [14]. A number of smaller systems are in use for detector R&D work for Micromegas technology throughout the MAMMA community or in a geophysical muon-tomography application in the T2DM2 project at LSBB (France). Other RD51 groups are using the system for Thick-GEM detector characterization or ILC-TPC R&D [6].

While migrating to full-scale experiment size, some of the above applications have increasingly higher requirements in terms of integration density, data bandwidth and robustness. For this reason, the RD51 community involved in the development of the SRS system is planning to translate the current implementation into an industrial standard. The AdvancedTCA standard [15] is more likely to provide a more robust platform and the required technical capabilities for large-scale applications like the NEXT experiment [14], the proposed ATLAS New-Small Wheel upgrade or the large-area geophysical application proposed by the T2DM2 project. Figure 7 depicts the planned ATCA-SRS system which is currently under design with the help of an industrial partner with specific experience. The FEC card will be replaced by a custom ATCA blade which integrates the capability of two FEC cards on the same board, while the adapter boards will be replaced by mezzanine cards. A custom ATCA-SRU blade will take the role of the classical Scalable Readout Unit. Taking advantage of the high-speed ATCA backplane options and latest FPGA families, the speed of the DTCC links can be increased up to 10 Gbps, increasing the overall throughput and also reducing the latency of the DTCC fast-channel for the transport trigger and timing information. With the current SRS front-ends the ATCA-SRS system is capable of integrating more than 65,000 detector channels per crate, about 4 times more than the classical implementation. The new system keeps the same scalability capability, allowing the integration of novel front-end ASICs based on the Versatile Link interface or with custom high-speed optical or copper interfaces.

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