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Special Issue

Development of Thin-film $Cu(In,Ga)Se_2$ and CdTe Solar Cells

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$Cu(In,Ga)Se_2$ and CdTe heterojunction solar cells grown on rigid (glass) or flexible foil substrates require p-type absorber layers of optimum optoelectronic properties and n-type wide-bandgap partner layers to form the p–n junction. Transparent conducting oxide and specific metal layers are used for front and back electrical contacts. Efficiencies of solar cells depend on various deposition methods as they control the optoelectronic properties of the layers and interfaces. Certain treatments, such as addition of Na in $Cu(In,Ga)Se_2$ and $CdCl_2$ treatment of CdTe have a direct influence on the electronic properties of the absorber layers and efficiency of solar cells. Processes for the development of superstrate and substrate solar cells are reviewed.
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KEY WORDS: solar cells; CdTe; $Cu(In,Ga)Se_2$; thin-films; photovoltaics; solar energy

INTRODUCTION

Polycrystalline thin-film solar cells such as $CuInSe_2$ (CIS), $Cu(In,Ga)Se_2$ (CIGS) and CdTe compound semiconductors are important for terrestrial applications because of their high efficiency, long-term stable performance and potential for low-cost production. Because of the high absorption coefficient ($\sim 10^5\,cm^{-1}$) a thin layer of $\sim 2\,\mu m$ is sufficient to absorb the useful part of the spectrum. Highest record efficiencies of 19·2% for CIGS[1] and 16·5% for CdTe[2] have been achieved. Many groups across the world have developed CIGS solar cells with efficiencies in the range of 15–19%, depending on different growth procedures. Glass is the most commonly used substrate, but recently some effort has been made to develop flexible solar cells on polyimide and metal foils. Highest efficiencies of 12·8% and 17·6% have been reported for CIGS cells on polyimide[3] and metal foils,[4] respectively. Similarly, CdTe solar cells in the efficiency range of 10–16%, depending on the deposition process, have been developed on glass substrates, while flexible cells with efficiency of 7·8% on metal,[5] and 11% on polyimide[6] have been achieved. Currently, these polycrystalline compound semiconductors solar cells are attracting considerable interest for space applications, because proton and electron irradiation tests of CIGS and CdTe solar cells have proven that their stability against particle irradiation is superior to Si or III–V solar cells.[7] Moreover, lightweight and flexible solar cells can yield a high specific

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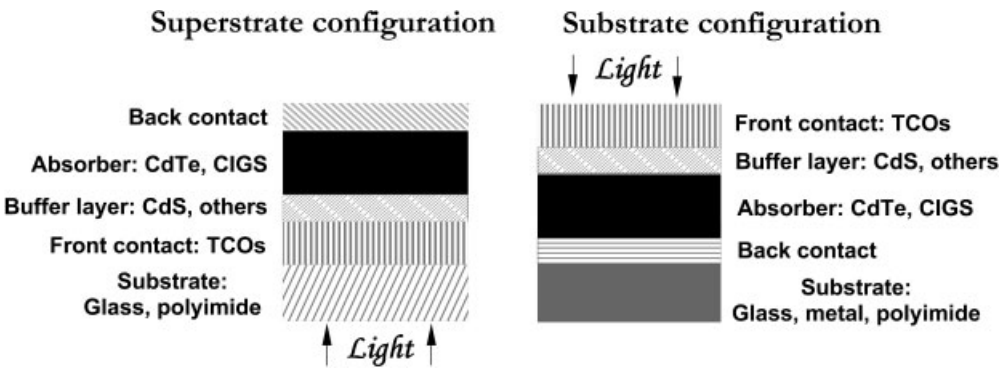

Figure 1. Schematic cross-section of 'superstrate' and 'substrate' configurations for CdTe and CIGS solar cells

power (W/kg) and open numerous possibilities for a variety of applications. As shown in Figure 1, thin-film solar cells based on CdTe or chalcopyrite absorbers can be grown in 'superstrate' or 'substrate' configurations. The superstrate configuration facilitates low-cost encapsulation of solar modules. This configuration is also important for the development of high-efficiency tandem solar cells, effectively utilizing the complete solar spectrum for photovoltaic power conversion.

There are several chalcopyrite compounds with optical and electrical properties suitable for photovoltaic conversion, but this review article is focused on the CIGS compound because of space limitation, and for the same reason many important papers and reviews are not mentioned in the references. Module manufacturing technologies have matured in recent years and several companies are involved in industrial or pilot-scale production of solar modules. However, module related issues are not covered in this review article. The emphasis is placed on various aspects of solar cell development and most of the efficiencies reported are related to small-area cells($\leq$1 cm^2).

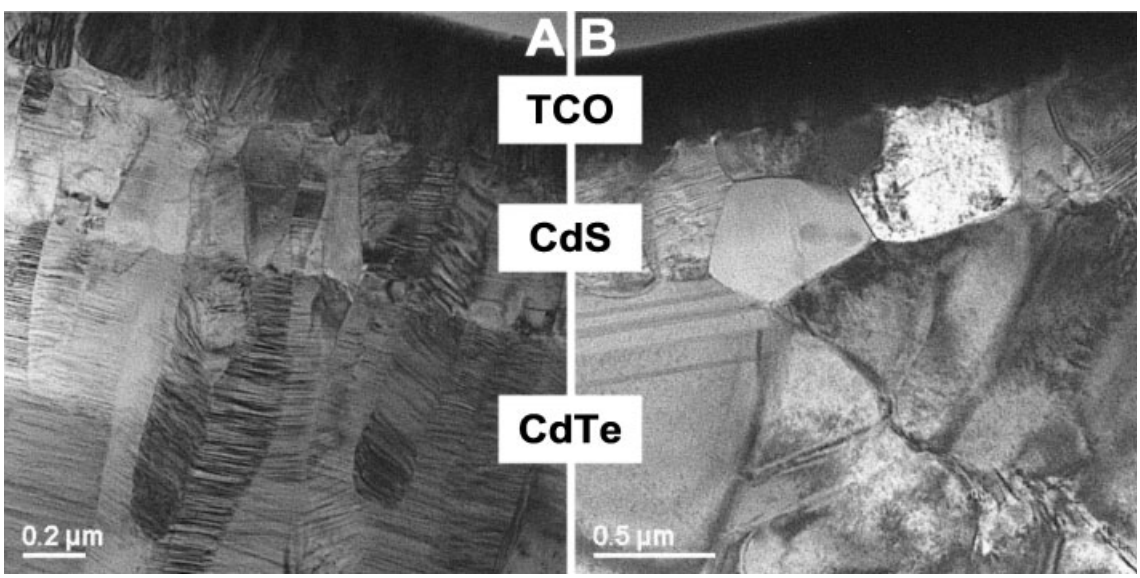

Figure 2. (a) TEM micrograph of the cross-section of a CdTe/CdS cell after deposition—both the columnar grain structure and the high density of twins on {111} plains in the CdTe and {0001} plains in the CdS layer are visible; (b) a sample area after $CdCl_2$ treatment—both, the CdTe and the CdS layers are characterized by grain growth (note the different scale bars), recovery and recrystallization; the CdTe/CdS interface exhibits grain coarsening[166]

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CELL CONFIGURATION

CIGS solar cells

Generally, CIGS solar cells are grown in a substrate configuration (see Figure 1). This configuration gives the highest efficiency owing to favorable process conditions and material compatibility but requires an additional encapsulation layer and/or glass to protect the cell surface. This cover glass, in contrast, is not required for the cells grown in the superstrate configuration. CIS-based superstrate solar cells were investigated by Duchemin *et al*.[8] using spray pyrolysis deposition, but efficiencies did not exceed 5%. The main reason for this low efficiency in CdS/CIGS superstrate cells is the undesirable interdiffusion of Cd into CIS (or CIGS) during the elevated temperatures required for absorber deposition on CdS buffer layers.[9]

To overcome this problem of interdiffusion more stable buffer materials and low-temperature deposition processes such as electrodeposition (ED), low-substrate temperature co-evaporation and screen printing were investigated. Nakada *et al*.[10] achieved a breakthrough by replacing CdS with undoped ZnO and co-evaporating Na_xSe during CIGS deposition. With the additional introduction of composition grading in absorber layer, 12·8% efficiency cells were developed.[10]

This co-evaporation of Na_xSe for incorporation of sodium in CIGS is essential for high-efficiency cells, as the ZnO front contact acts as diffusion barrier for Na from the glass substrate and leads to a low net carrier density in CIGS and cells with low open-circuit voltage V_{OC} and fill factor.[11] Investigations of the interface between the ZnO buffer layer and CIGS revealed the presence of a thin layer of Ga_2O_3 which acts as barrier against photocurrent transport.[10,12,13] However, Na-free superstrate solar cells with efficiencies of up to 11·2% have been obtained, but a strong light-soaking treatment was necessary.[14] The fundamental reasons for light-soaking-induced improvements in cell efficiency are not yet investigated.

CdTe solar cells

The CdTe solar cells can be grown in both substrate and superstrate configurations (see Figure 1), but the highest efficiency is achieved in the superstrate configuration. The CdTe/CdS layers for superstrate cells are grown on transparent conducting oxide (TCO)-coated glass substrates. The glass substrate can be a low-cost soda-lime glass for growth process temperatures below 550°C, or alkali-free glass for high-temperature processes (550–600°C). Various kinds of back contacts can be applied, as they do not have to withstand the high temperature of successive layer deposition. Cells in superstrate configuration have given the highest efficiency[2] of up to 16·5%.

For substrate configuration (see Figure 1), CdTe is deposited on metal foils or metal-covered glass substrates. The main advantage of the substrate configuration is that the substrate does not have to be transparent, which allows a variety of foils (e.g., molybdenum, stainless steel or polyamide) as a substrate for the development of flexible cells.[15] The highest efficiency obtained in the substrate configuration is 10·3% on a Mo/Cu-coated glass substrate,[16] while flexible cells of 7·8% efficiency on molybdenum foils have been realized.[5] However, the stability of the back contact remains a limiting factor in the substrate configuration. Recently, with a novel lift-off process, 11% efficiency cells in superstrate and 7·7% efficiency cells in substrate configuration have been developed on flexible polyimide films.[6,17] By reversing the order of deposition and subsequent lift-off to reconfigure the substrate configuration, the issue of back contact stability at high temperature—encountered during cell processing—is avoided.[6]

FRONT CONTACT

CIGS solar cells

During the early days of CIS and CIGS substrate cell development a bilayer of undoped and doped CdS served as a buffer and front contact, respectively.[18,19] High conductivity in doped CdS was achieved either by controlling the density of donor type defects or by extrinsic doping with Al or In.[18,19] Spectral absorption loss in the conducting CdS layer was reduced by increasing the bandgap, alloying with ZnS or later replacing it with TCOs

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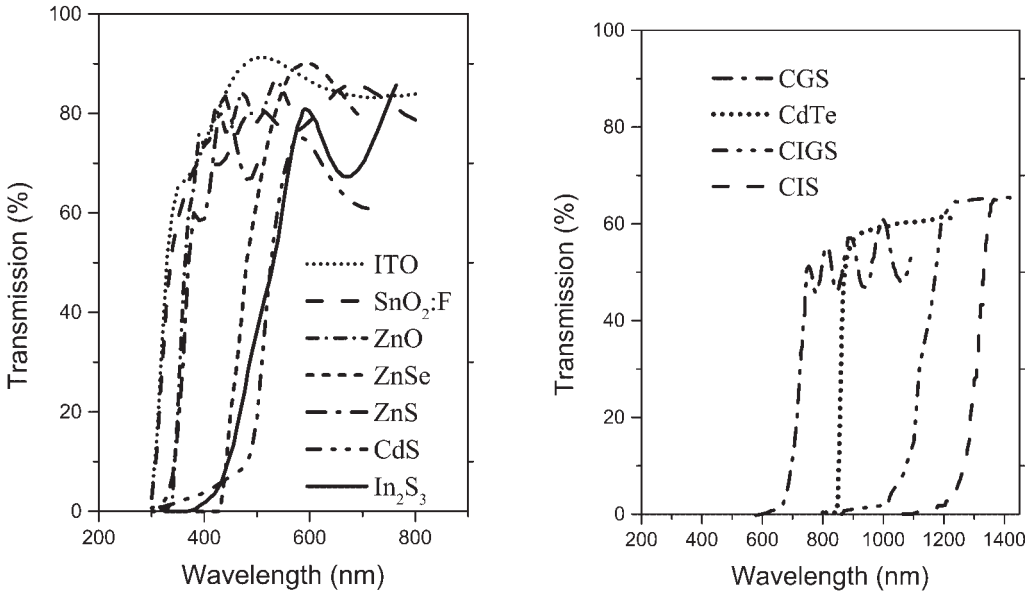

Figure 3. Optical transmission of different front contacts and buffer layers (left) and of different absorber layers (right)

with bandgaps of above 3 eV.[18] Transmission spectra of various TCOs and buffers are shown in Figure 3. Today, CIGS solar cells employ either In_2SnO_3 (ITO) or, more frequently, RF-sputtered Al-doped ZnO. A combination of an intrinsic and a doped ZnO layer is commonly used, although this double layer yields consistently higher efficiencies, the beneficial effect of intrinsic ZnO is still under discussion.[20] Doping of the conducting ZnO layer is achieved by group III elements, particularly with aluminum.[21] However investigations show boron to be a feasible alternative, as it yields a high mobility of charge carriers[22] and a higher transmission in the long-wavelength spectral region, giving rise to higher currents.[23] For high-efficiency cells the TCO deposition temperature should be lower than 150°C in order to avoid the detrimental interdiffusion across CdS/CIGS interface.

CdTe solar cells

A highly transparent and conducting TCO layer with an electron affinity below 4·5 eV is required to form an ohmic contact and a good band alignment with the CdS. If the electron affinity of the TCO is higher than that of CdS, a blocking Schottky contact is formed.

The most commonly used TCOs for CdTe solar cells are F-doped SnO_x [SnO_x:F (FTO)] or ITO (see their transmission spectra in Figure 3). They are often used in combination with a thin intrinsic SnO_x layer between the TCO and the CdS window layer maintaining a high voltage by preventing possible shunts through pinholes in the CdS.[24] Intrinsic (high-resistivity) TCO facilitates the use of a thinner CdS layer for reducing photon absorption losses for wavelengths smaller than 500 nm.

The Al doped ZnO, commonly used in CIGS cells, yields a high series resistance in CdTe cells, resulting in low efficiency.[25] However, recently 14% efficiency cells have been developed on ZnO:Al with a sputtering method.[26] The CdS deposition and post-deposition annealing of the cell can change the properties of the TCO layer and the CdS/TCO interface characteristics. ITO front contacts are often sensitive to annealing treatment, an increase of the electron affinity from around 4 to 5 eV, caused by oxidation or a post-deposition treatment, results in a blocking contact.[27,28] By doping ITO with F, N. Romeo *et al*. (private communication) were able to increase the stability of the front contact.

Best results have been achieved with a RF-sputtered stack of highly conductive Cd_2SnO_4 and resistive Zn_2SnO_4 buffer layers,[2] each with a thickness of 200 nm. The Cd_2SnO_4 excels in conductivity and

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bandgap, allowing for a higher current and fill factor in solar cells. Similarly the high conductivity and transmission of $CdIn_2O_4$ layers have been obtained by a co-sputtering method.[29,30] A drawback of the stannates is their high deposition temperature, above 600°C, which does not allow the use of low-cost soda-lime glass substrates.

BUFFER LAYERS

CIGS solar cells

Semiconductor compounds with *n*-type conductivity and bandgaps between 2·0 and 3·6 eV have been applied as buffer for CIGS solar cells. However, CdS remains the most widely investigated buffer layer, as it has continuously yielded high-efficiency cells. CdS for high-efficiency CIGS cells is generally grown by a chemical bath deposition (CBD), which is a low-cost, large-area process. However, incompatibility with in-line vacuum-based production methods is a matter of concern. Physical vapor deposition (PVD)-grown CdS layers yield lower-efficiency cells, as thin layers grown by PVD do not show uniform coverage of CIGS and are ineffective in chemically engineering the interface properties. For a comprehensive review on CBD-deposited CdS see Ortega-Borges and Lincot[31] and Hodes.[32]

The recent trend in buffer layers is to substitute CdS with 'Cd-free' wide-bandgap semiconductors and to replace the CBD technique with in-line-compatible processes. The first approach has been to omit CdS and form a direct junction between CIGS and ZnO, but the plasma (ions) during ZnO deposition by RF sputtering can damage the CIGS surface and enhance interface recombination. Possible solutions include ZnO deposited by metal organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD) or a novel technique, called ion layer gas reaction.[33–35]

As an alternative to CdS, various materials show promising results. These include layers of CBD-ZnS,[36] MOCVD-ZnSe,[37] ALD-ZnSe,[38] CBD-ZnSe,[39] PVD-$ZnIn_2Se_4$,[40] co-sputtered $Zn_{1-x}Mg_xO$[41] and ALD-In_2S_3.[42,43] All of these Cd-free buffer layers have demonstrated efficiencies well above 11% with a record efficiency[36] for CBD-ZnS of 18·1%. However, Zn-based compounds tend to form a blocking barrier due to the band alignment with CIGS.[44] Using layers of less than 50 nm thickness, the barrier can be crossed by tunneling of charge carriers, but this poses high requirements on the quality of the deposition process and the CIGS surface to obtain a uniform coverage. The band offset can be reduced as well, if impurities such as hydroxides that can be present in a CBD are incorporated in the CIGS/buffer layer interface.[45]

CdTe solar cells

Due to the limited dopability and high absorption coefficient of CdTe, high-efficiency homojunction devices are not attractive. Heterojunction structure with *n*-CdS and *p*-CdTe is most commonly used for high-efficiency cells. Like CdTe, CdS grows under most deposition conditions in a stable stoichiometric phase, α-CdS, which has the hexagonal wurtzite structure. Under high-pressure growth conditions or in thin films, CdS may be found in the cubic, metastable zincblende structure.[46] Layers of *n*-conducting CdS are easily grown by various deposition methods including CBD as well as PVD. CBD yields the highest efficiency devices, owing to its inherent ability to form very thin (5–50 nm), but continuous layers, that allow a high transmission through the window layer for low-wavelength photons.

High-vacuum evaporation (HVE)-grown CdS films exhibit[47] sub-micrometer-sized, columnar grains that grow with preferred $[2\overline{1}\overline{1}0]$ orientation parallel to the substrate (Figure 2a). Recently, attempts have been made to enhance the crystal quality of CdS by the incorporation of O or $CdCl_2$ as flux agent and post-deposition treatments in air and Ar. Impurities can compensate the doping in CdS and act as carrier traps, turning the CdS into a transport barrier modulated by light. This mechanism has already been investigated for CIGS cells,[48] and adapted models have been developed for CdTe cells.[49] Hence, not only the direct influence of the front contact, but its indirect influence on the electrical properties of the CdS by interdiffusion of impurities across the TCO/CdS interface should be considered in terms of cell stability.

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MATERIAL PROPERTIES OF THE ABSORBERS

CIGS

I–III–VI_2 semiconductors, such as CIS or CIGS are often simply referred to as chalcopyrites because of their crystal structure. These materials are easily prepared in a wide range of compositions and the corresponding phase diagrams are well investigated.[50–52] For the preparation of solar cells only slightly Cu-deficient compositions of *p*-type conductivity are suited.[53,54] Depending on the [Ga]/[In + Ga] ratio, the bandgap of CIGS can be varied continuously between 1·04 and 1·68 eV, (Figure 3). The current high-efficiency devices are prepared with bandgaps in the range 1·20–1·25 eV, this corresponds to a [Ga]/[In + Ga] ratio between 25 and 30%.

CdTe

The CdTe phase diagram is characterized by a congruently melting intermediate phase,[55] α-CdTe, which forms at 50 at% Te. It has a cubic zincblende (sphalerite) structure. Under pressure or in thin films, two other phases of cubic or hexagonal structure can form.[46,56] The deviation from stoichiometric composition is negligible, the width of the stability region of the stoichiometric phase above 400°C is 10^{-6} at.%. The high liquidus temperature results from a strong ionic binding between Cd and Te atoms. These features make CdTe as a robust material suitable for high-deposition-rate industrial processes.

While the CdS/CdTe interface suffers from a 10% lattice mismatch that produces misfit dislocations,[57] CdTe absorber layers can be separated in two groups, depending on the substrate temperature used during the CdTe growth. For low-temperature processes (e.g., HVE) CdTe grows epitaxially on the CdS grains, with the {111} planes of CdTe being parallel to the {0001} planes of CdS. The CdS grain size is conserved across the interface and determines the lateral grain diameter of CdTe, which remains unchanged throughout the absorber layer. The high density of microtwins on {111} planes, seen in Figure 2(a) as black stripes, is the result of low substrate temperatures during deposition, combined with a low stacking fault energy in CdTe. The CdTe layers grown by high-temperature (∼550°C) close-space sublimation (CSS) processes have grain sizes equivalent to the CdS grain size at the interface, but develop into much larger grains of several micrometers in diameter towards the CdTe top surface. The density of microtwins is smaller, compared with low-temperature-grown CdTe and an orientational relationship between the CdS and the CdTe layers is less apparent.

When grown under Cd rich conditions, as-grown CdTe is intrinsic or *n*-conducting due to the Fermi level being pinned near the midgap by the compensating donor defect Cd_i^{2+}. In the Te-rich limit CdTe is intrinsic or slightly *p*-conducting since the Fermi energy is pinned closer to the valence band maximum. The reliable enhancement of *n*- and *p*-conductivity by doping remains a difficult and long-standing problem.[58] Limitations for *n*-doping are the self-compensation by intrinsic defects such as Cd vacancies, and *p*-doping suffers from the lack of available dopants with both high solubility and shallow acceptor levels.[59] Moreover, most of the doping atoms have a high mobility and a tendency to segregation in CdTe films. Typical doping concentration in polycrystalline CdTe is of the order of 10^{15} cm^{-3} for a high-efficiency device.

ABSORBER GROWTH

CIGS layers

Co-evaporation processes

The most successful technique for deposition of CIGS absorber layers for highest-efficiency cells is the simultaneous evaporation of the constituent elements from multiple sources in single or sequential processes where Se is offered in excess during the whole deposition process. While a variation of the In to Ga ratio during the deposition process leads to only minor changes in the growth kinetics, variation of the Cu content strongly affects the film growth. Thus, different co-evaporation growth procedures are classified by their Cu evaporation profile. In spite of the variations in the Cu flux, in most cases a homogeneous Cu distribution throughout the finished absorber layer is established, which should be Cu poor for high-efficiency cells.

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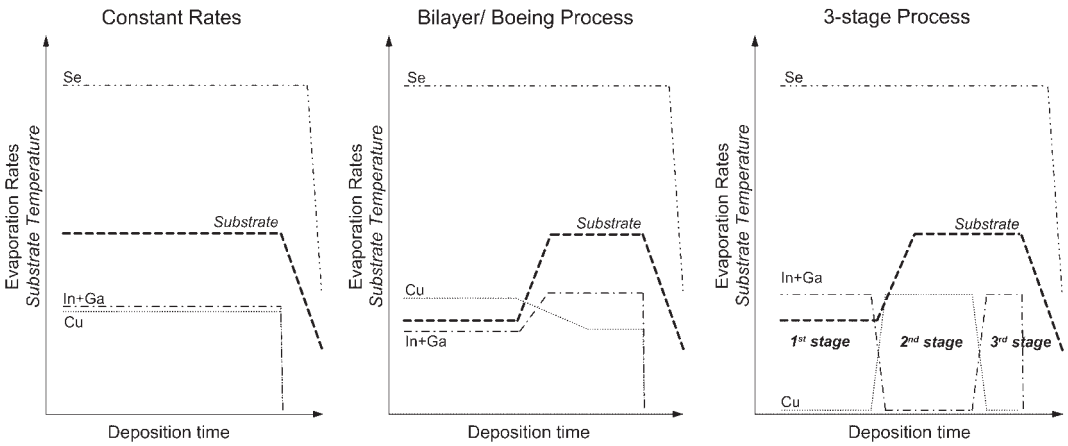

Figure 4. Schematic illustration of different co-evaporation recipes

The use of a bilayer process (also called the 'Boeing process') (Figure 4) originates from the work of Mickelsen and Chen.[60] This bilayer process yields larger grain sizes compared to the constant rate (single-stage) process. This is attributed to the formation of a Cu_xSe phase during the Cu-rich first stage, that improves the mobility of group III atoms during growth.[61–63] An 'inverse' two-stage process starts with a precursor layer that is more Cu-poor than the finished film.[64,65] The so-called three-stage process, introduced by NREL,[66] is obtained by starting the deposition with an $(In,Ga)_xSe_y$ precursor, followed by the co-deposition of Cu and Se until Cu-rich overall composition is reached, and finally the overall Cu concentration is readjusted by subsequent deposition of In, Ga and Se.[66] This method leads, up to now, to the most efficient solar cells. CIGS films prepared by the three-stage process exhibit a smooth surface, which reduces the junction area and thereby is expected to reduce the number of defects at the junction.[66] This smoother surface facilitates the uniform conformal deposition of a thin buffer layer and prevents ion damage in CIGS during sputter deposition of ZnO/ZnO:Al.

Variation of the In/Ga flux ratio during the deposition allows the fabrication of graded bandgap absorbers. An increasing Ga/In concentration ratio towards the back of the absorber results in an increased conduction band minimum and therewith enhanced back-surface field, which increases V_{OC} and fill factor. This concept is being applied to reduce the indium concentration and the thickness of the absorber layer. The optimum grading is determined by a trade-off between enhanced open-circuit voltage and lower current density because of reduced electron–hole pair generation due to a reduced absorption of low-energy photons.

Selenization of precursor materials

The interest in sequential processes is sparked by its suitability for large-area film deposition with good control of the composition and film thickness. Such processes consist of the deposition of a precursor material, followed by thermal annealing in controlled reactive or inert atmosphere for optimum compound formation via the chalcogenization reaction (Figure 5).

Among possible precursor materials, metallic and metal selenide layers are the most investigated. Alloyed or stacked metal layers are commonly deposited by thermal evaporation,[67] sputtering[68] or electrodeposition.[69,70] The DC-magnetron sputtering technique is well established for the production of large-area solar modules up to $60\times120\,cm^2$ yielding maximum efficiencies of 13% on $30\times30\,cm^2$ modules.[71,72] Adhesion problems due to the high volume expansion during the selenization of metallic precursors can be reduced by using metal selenide precursors which additionally reduce interdiffusion of In and Ga.[73,74] A maximum cell efficiency of 17·5% after annealing has been achieved with an In–Ga–Se/Cu–Se bilayer evaporated on a heated substrate.[75]

By far the most common chalcogenization reactants are vapors of selenium[76] and selenium hydride,[68,70] sometimes combined with sulfur or sulfur hydride.[72] Hydrides are generally diluted in argon or nitrogen, but remain problematic because of their high toxicity. In a recent investigation, diethylselenide was proposed as a

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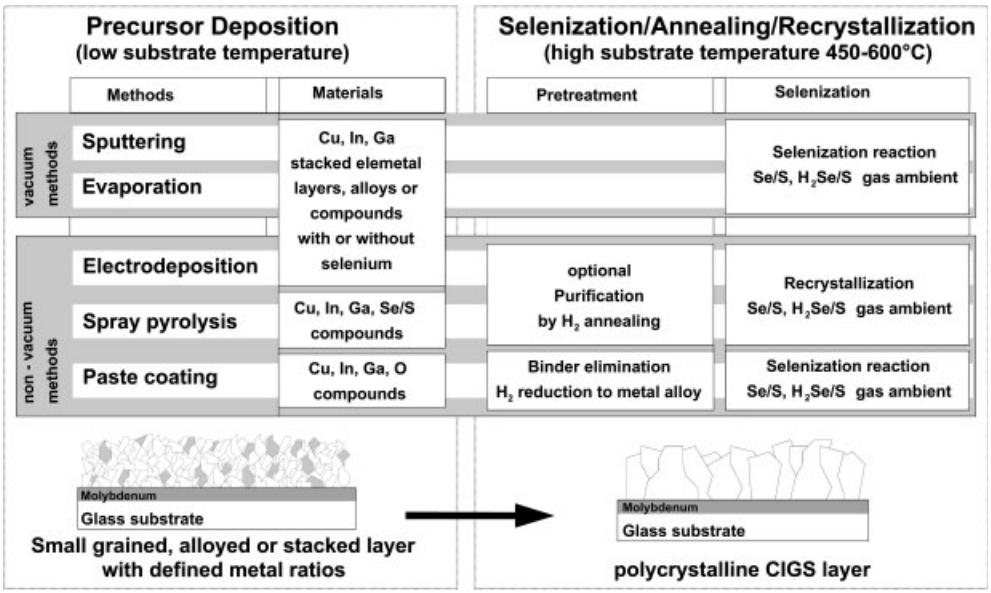

Figure 5. Schematic of the various processes for selenization of precursor materials

substitute for the toxic hydrogen selenide.[77] Chemical reaction enthalpy calculations for Se and hydride vapors predict a more efficient conversion by elemental vapors,[78] but reaction analysis indicates that the rate of selenium incorporation into the film is the same,[79] and qualitatively a higher degree of reaction control is reported for hydride reactions.[80] Annealing at high temperature in inert Ar atmosphere was identified to promote interdiffusion of In and Ga in segregated CIS and CGS phases, resulting in a homogeneous CIGS phase.[68] In industrial production, the processing time is a key factor for low-cost manufacturing and has led to the development of rapid thermal processes.[81] Fast heating rates are reported to inhibit binary compound formation and de-wetting of amorphous Se layers from layered elemental stacks. The use of toxic hydride chalcogen sources is not required, but a Se or S vapor atmosphere improves film uniformity.[82,83] Selenization of compound metal oxide precursor materials replaces O by Se.[84,85] The long selenization times required, owing to the stability of the In_2O_3 and Ga_2O_3 phases, are a drawback of oxide precursors and can only be overcome by a prior chemical reduction to the metallic state using hydrogen gas at high temperature.

A recent innovative approach utilizes the stability of the oxides to produce nanosized precursor particles.[86,87] They are mixed in an ink suspension, which allows low-cost, large-area deposition by doctor blading, screen-printing or spraying, and results in solar cell efficiencies of over 13%. Such non-vacuum deposition of precursors allows a very efficient material utilization of almost 100% of the non-abundant metals indium and gallium.

Alternative CIGS growth processes

The CIS compound can be formed directly by electrodeposition from a chemical bath,[88] but the as-deposited layers do not yield efficient devices. Therefore, annealing, typically done at 400°C in an Se atmosphere,[89] is required to increase the grain size, form a proper stoichiometric compound, improve the electrical properties and finally obtain efficiencies of up to 8·8%. Another approach[90] uses additional vacuum deposition of In, Ga and Se at high temperatures, to yield efficiencies as high as 15·4%. In spray pyrolysis, metal salts with a chalcogen reactant are sprayed on a heated substrate to form a CIS layer. However a subsequent heat treatment in a reducing atmosphere is still required to improve crystallinity and purity.[91] MOCVD has recently been investigated[92] for the deposition of CGS layers as part of a tandem structure, but the growth rate and cell efficiency are rather low.

Sodium incorporation in CIGS

As early as 1993 the importance of sodium 'contamination' in CIGS absorber layers was realized by Hedström *et al*.[93] Since then, the effects of Na have been investigated by numerous groups and different mechanisms have

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been proposed, but no comprehensive interpretation of the structural and electronic effects of Na has been achieved up to now.

Most commonly, Na is introduced into CIGS by diffusion from a soda-lime glass substrate during the absorber deposition. The diffusion of Na through the Mo back contact appears to be primarily determined by Mo oxide phases, present at grain boundaries.[94,95] However, the Na concentration inside the CIGS is relatively independent of the Mo deposition conditions.[95,96] Since soda-lime glass is not a reliable source of Na for the manufacturing of solar cells and modules, alternative methods are used to incorporate sodium in CIGS grown on soda-lime glass covered with barrier layers (Al_2O_3, Si_3N_4, etc.). These buffer layers inhibit sodium diffusion from the glass substrate. CIGS on flexible substrates (metal and polyimide foils) also need controlled incorporation of sodium. Various methods have been used for reliable Na incorporation of sodium in CIGS (Figure 6). The methods include the co-evaporation or the deposition of a thin precursor of a Na compound such as NaF, Na_2Se or Na_2S. The effects of other alkali metal salts (e.g., KF, CsF, LiF) have been investigated.[97,98] The observed effects of the KF and LiF precursors were similar to those of NaF, but less pronounced, while the CsF precursor had only a minor influence on the CIGS properties. Generally, Na in CIGS improves the cell efficiency by increasing the V_{OC} and fill factor.[97,99,100] The optimum Na dose is often considered to be equal to the amount diffusing from a soda-lime glass substrate, resulting in a typical Na concentration of approximately 0·1 at.%.

While some groups[101,102] have reported an increase of the grain size in CIGS films containing Na, others did not support these observations.[103–106] A decreasing grain size was observed for several Na incorporation methods in a direct comparison.[107] The CIS compound formation in rapid-thermal-processed layers was found to be delayed in the presence of Na, resulting in CIS growth at a higher mean temperature, which serves as an explanation for the observed increase in grain size.[108] The main portion of sodium in CIGS films was shown to reside on grain boundaries and surfaces.[109] In several reports,[99,101] a change in texture of CIGS films towards (112) orientation has been attributed to Na and supported by theoretical considerations for the case of high Na concentrations,[110] but remains disputed, owing to contrary results.[100,104,106,107] Higher doses of Na are shown to lead to small grain sizes and porous films and to be detrimental to the cell performance.[104,105]

The most obvious electronic effect of Na incorporation into CIGS films is a decrease in resistivity by up to two orders of magnitude.[111–113] An increase in carrier concentration of typically one order of magnitude is often associated with a lower number of compensating donors.[104,114,115] Various models have been proposed to explain the effects of Na on the electronic and structural properties of layers and influence on solar cells.[97,110,116–118]

CdTe layers

CdTe thin films have been succesfully grown by a variety of vacuum and non-vacuum deposition methods. Generally, CdTe growth methods such as CSS or close-spaced vapor transport with deposition temperature above 500°C are classified as high-temperature processes, while methods such as electrodeposition, HVE and sputtering with deposition temperature below 450°C are classified as low-temperature processes.

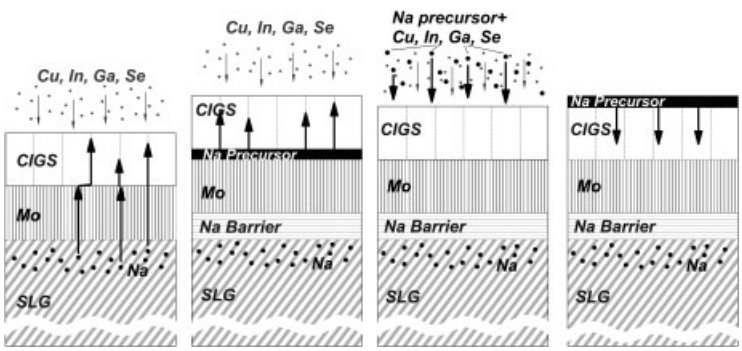

Figure 6. Schematics of different Na incorporation methods into the CIGS absorber

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Layers deposited by high-temperature processes exhibit large grain size of up to 10 μm owing to the enhanced mobility of atoms at the growth surface. Investigation of the morphology shows that $CdCl_2$ treatment does not increase the grain size,[119] but reduces the structural defects and affects the grain boundaries, resulting in a higher effective acceptor concentration.

In low-temperature-deposited CdTe, the grain size is about 0·1–0·5 μm and grain growth is enhanced by a post-deposition annealing or $CdCl_2$ treatment. However, even after recrystallization, these layers have lower crystalline quality than those deposited at high temperature. The mobility of Cd and Te atoms during growth may also be increased by supplying high-energy electrons or ions, created by RF sputtering, to the growth surface.[120] Efficiencies of high-temperature-processed cells reach 16·5% on alkali-free glass substrates, and 14·4% for low-temperature-deposited cells on soda-lime glass substrates. Comprehensive reviews of CdTe solar cell technology are available.[121,122]

The $CdCl_2$ treatment of CdTe

Independent of the growth process, as-deposited CdTe cells exhibit poor electrical performance after growth. However, special annealing treatments significantly improve the cell efficiency, in some cases the increment is up to three times the initial value. Therefore, it has become common routine[123,124] that CdTe/CdS stacks are subjected to heat treatments under Cl-containing ambient at temperatures between 350 and 600°C. Furthermore, the presence of oxygen during annealing is beneficial.[125] This annealing procedure in Cl–O ambient is called '$CdCl_2$ treatment' or 'junction activation.' Both for low- and high-temperature grown cells the effect is an improvement of the structural quality of the layers and of the electronic characteristics. An increase in grain size by a factor of 5–20 in low-temperature grown CdTe has been observed (see Figure 2b). In high-temperature grown cells little or no grain growth is observed, except for the region close to the CdS/CdTe interface, where the small CdS grain size has caused the formation of small CdTe grains during the early stage of the deposition.[126] The overall density of stacking faults and misfit dislocations is reduced by recovery.

The CdTe-$CdCl_2$ phase diagram predicts only sub-at.% solubility of Cl in CdTe at temperatures below 525°C, hence it is not surprising, that Cl is assumed to diffuse into the CdTe layer preferentially along grain boundaries.[127,128] The mechanism by which Cl promotes structural changes in CdTe and CdS is most likely a formation of CdO and $TeCl_2$ at the grain boundaries.[129] An increase in the mobility of Cd and Te atoms results, and recrystallization starts from the CdTe surface, leading to the mentioned loss of texture in low-temperature CdTe.[119, 130] Owing to their better structural quality after deposition, high-temperature films show only little crystallographic changes during $CdCl_2$ treatment.[119,131] After annealing, Cl, Te and O segregation is found along the CdS/CdTe interface and at CdS grain boundaries, due to the low solubility of Cl in both CdTe and CdS, but are absent in case of annealing without oxygen (Terheggen *et al*., unpublished data). While the electrical relevance of the segregation is unclear, their presence corroborates the formation of $TeCl_2$ and CdO. A similar reaction leads to the recrystallization of CdS and promotes the diffusion of S into CdTe.[131]

The formation of a $CdS_x Te_{1-x}$ layer at the interface results, with x not exceeding 0·06 in accordance with the CdTe/CdS phase diagrams, though layers of higher S content may grow under non-equilibrium conditions.[132,133] The diffusion of S decreases the thickness of the CdS film and can eventually lead to the formation of shunts across the CdS/CdTe junction. Therefore, a thermal treatment of the CdS layer prior to CdTe deposition is frequently employed. The $CdS_x Te_{1-x}$ layer reduces the lattice mismatch between CdS and CdTe, but the importance of a lattice-mismatch reduction, especially in films that show no or little orientational relationship after annealing between the CdS and CdTe layer, is probably small. More important are the electrical changes induced by Cl, O and S. An overall increase of the shallow-acceptor concentration leading to enhanced *p*-doping after annealing with Cl and O was observed.[134,135] In particular, the grain boundary regions become more *p*-doped, owing to preferred grain boundary diffusion and segregation of Cl and O, and an increased photo-carrier collection efficiency is measured.[136–138] A decrease in interface states after the $CdCl_2$ treatment is commonly reported, that changes the mechanism of current transport from tunneling/interface recombination to junction recombination in case of CSS deposition.[136,139] Whether this is due to S diffusion or Cl incorporation is unclear. The diffusion of S may shift the *p–n* junction away from the metallurgical interface into the CdTe absorber and decrease the CdTe band gap.[140–143]

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BACK CONTACT

CIGS

Various metal contacts to *p*-type CIS were examined by Matson *et al.*[144] concluding that only Au and Ni ensure an ohmic contact. Recently, Orgassa *et al.*[145] fabricated CIGS solar cells with different back-contact materials, emphasizing the role of the back contact as an optical reflector. Early results by Russell *et al.*[146] suggested that Mo back contacts for CIS form a Schottky-type barrier. But recently, a work of Shafarman *et al.*[147] who analyzed the Mo/CIS interface separately from the cell, shows the contact to be ohmic. Nowadays, Mo growth by sputtering or e-beam evaporation is the most commonly used back contact for CIGS solar cells.

Its influence on the ohmic contact behaviour at the CIGS/Mo interface makes $MoSe_2$ formation an important issue. Fundamental work by Raud and Nicolet[148] on Mo/Se, Mo/In and Mo/Cu diffusion couples showed Se to react with Mo, forming $MoSe_2$ in very small amounts after annealing at 600°C. Jones *et al.*[149] investigated the interface properties of d.c.-sputtered Mo on CIS layers, deposited by co-evaporation, and concluded that $MoSe_2$ does not form below 500°C and it might be an artefact of the sputtering process. Similar results have been obtained by Schmid *et al.*[150] They detected Mo–O and Mo–O–Se compounds, while selenizing the Mo-coated substrate prior to the CIS deposition at 600°C. They concluded that there should be a Schottky-type barrier at the CIS-Mo/MoO_2 interface.

Wada *et al.*[151] reported the formation of a $MoSe_2$ layer at the Mo/CIGS interface during the second stage of the three-stage process, yet only under (In,Ga)-rich growth and for substrate temperatures higher than 550°C. They found Na to enhance the formation of $MoSe_2$ (see also Section 6·2). $MoSe_2$ layers were confirmed also in $CuGaSe_2$-based solar cells by Würz *et al.*[152] Contrary to the above results, Ballif *et al.*[153] could not detect any intermediate compound within the Mo/CIGS interface.

In conclusion, results reported on the existence and formation of a $MoSe_2$ layer at the Mo/CIGS interface remain ambiguous. Though, it should be considered that this ambiguity may be due to the large differences in layer growth procedures and characterization techniques.

CdTe

To form an ohmic contact on *p*-CdTe, metals with a work function greater than 5·7 eV are required. Such metals are not available and the formation of a Schottky barrier at the back contact would be unavoidable. To overcome this problem a heavily *p*-doped CdTe surface is created by chemical etching and a buffer layer of high carrier concentration is often applied.[154] Subsequent post-deposition annealing diffuses some buffer material into CdTe where it changes the band edges and interface states. The contact barrier is lowered, resulting in a quasi-ohmic contact.

Commonly used buffer layer/metallization combinations are Cu/Au,[154,155] Cu/graphite[156] or graphite pastes doped with Hg and Cu,[2] ZnTe doped with Cu[157–159] and Au or Ni metallization, Cu/Mo.[160] Alternatively, Cu-free back contacts such as Ni:P, ZnTe,[161] Au[162] or Sb_2Te_3/Ni[163] contacts have also been investigated.

Metallization layers based on Cu, Au, Al or Ni are known for their high diffusivity in CdTe layers with a tendency for these elements to accumulate at the CdS/CdTe or CdS/TCO interface.[161,164] This diffusion from the back contact can not be sufficiently controlled, and usually causes degradation in the cell performance. However, a PVD-deposited Sb buffer layer with Mo metallization has yielded high efficiency and low degradation in long-term performance.[163] Best cell stabilities have been achieved with RF-sputtered Sb_2Te_3 buffer layer with Mo metallization as introduced by N. Romeo *et al.*[165] Further, with Sb_2Te_3 deposited by PVD and ED, the positive influence on the solar cell stability has been reconfirmed.[163,164] Long-term stability data for different buffer layer/metallization combinations obtained by light-soaking at elevated temperatures are shown in Figure 7.

In some cases, the degradation is reported to recover partly, especially under reverse bias, indicating the electromigration of ionized Cu atoms. While Cu-based back contacts form barriers smaller than 0·25 eV with the CdTe layer, barrier heights reported[125,164] for proven long-term stable devices are in the range of 0·35–0·5 eV. Despite the higher initial efficiency the detrimental effect of Cu-based back contacts on the long-term stability suggest that Cu should be avoided for commercial modules.

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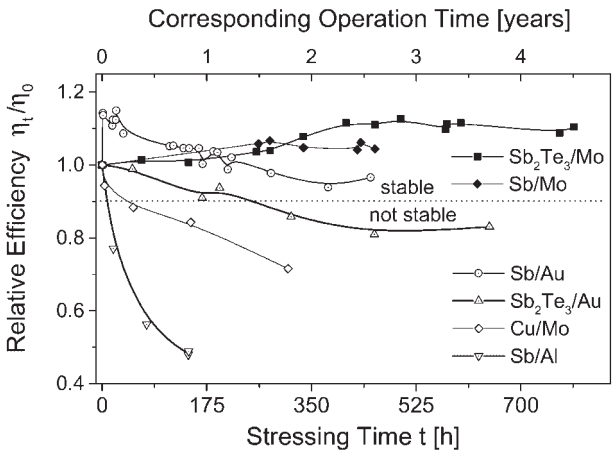

Figure 7. Stability of CdTe cells with different back contacts on comparable absorbers. Cells with Cu-based contacts show fast degradation while cells with Sb_2Te_3/Mo are stable[164]

SUMMARY AND OUTLOOK

Remarkable progress has been made in the development of high-efficiency CIGS and CdTe solar cells. However, each component of the solar cell structure and its manufacturing requires further investigation to simplify the processing, improve the performance and to develop the next generation of still more efficient and lower-cost solar cells. While sophisticated deposition processes, e.g. to grow graded-bandgap absorber layers with optimum composition profiles and reduced bulk defect density, have the potential to further increase the cell efficiency, non-vacuum deposition methods are becoming attractive for low-cost manufacturing. However, CIGS cell efficiencies of the latter methods are still lower because it is difficult to add an optimum concentration of Ga with the desired concentration profile. Further increase in cell efficiency and development of a non-toxic and safer selenization process will boost the prospects of these methods.

Improvements in the properties of the buffer layers, of the TCOs and of their deposition processes are necessary since they influence the interface recombination, and even the bulk electronic properties in the case of strong diffusion. Alternative buffer layers with wide bandgaps are needed to reduce the optical losses and, for a better band alignment in substrate and superstrate solar cells, the compatibility of their deposition process with in-line processing is desirable.

TCO front contacts may have direct impact on the interface barrier properties of heterojunctions. The application of novel TCOs has shown promising potential to increase the cell efficiency and viability of tandem solar cells. The next generation of solar cells, monolithic tandem cells, with envisioned 25% efficiency will require high-efficiency cells with wide-bandgap (1·7 eV) absorbers, transparent front and back contacts and intermediate tunneling junctions.

Molybdenum is generally accepted as a suitable back contact for CIGS substrate cells, but for superstrate cells the back contact has not been sufficiently investigated. Especially, the relevance of $MoSe_2$ is not clear. The application and optical optimization of alternative back contacts can help to reduce the thickness of absorber layers. Back-contacting for high-efficiency CdTe solar cells requires a chemical etching process, which is not suitable for industrial production. Therefore, efforts should be directed towards the development of 'dry processes' that are compatible with in-line vacuum deposition systems. Sodium incorporation in CIGS and chlorine or $CdCl_2$ treatment of CdTe solar cells are important for high efficiency, but the process controllability and the understanding of physical mechanisms need improvement. Common to both technologies is the need to develop robust and low temperature ($<400°C$) deposition processes for high-efficiency cells and modules. Preferably the substrates should be flexible metals or polyimide foils to facilitate roll-to-roll manufacturing and to extend the range of applications from the terrestrial to the space market.

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