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Developments of SOI monolithic pixel detectors

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ABSTRACT

A monolithic pixel detector with 0.2 μm silicon-on-insulator (SOI) CMOS technology has been developed. It has both a thick high-resistivity sensor layer and thin LSI circuit layer on a single chip. Integration-type and counting-type pixel detectors are fabricated and tested with light and X-rays. The process is open to many researchers through Multi Project Wafer (MPW) runs operated by KEK. Further improvements of the fabrication technologies are also under investigation by using a buried p-well and 3D integration technologies.

1. Introduction

A monolithic pixel detector, in which both semiconductor sensors and readout electronics are fabricated on the same wafer has many attractive features for applications in high-energy experiments, astrophysics, material analysis, medical imaging and so on. We have realized such a detector by using a SOI (silicon-on-insulator) technology which bonds wafer of thick, high-resistivity Si and thin low-resistivity Si together (see Fig. 1) [1,2].

Some of the SOI pixel detector features are

- No mechanical bump bonding, so obstacles which will cause multiple scattering are minimized and smaller pixel size is possible.
- Parasitic capacitances of sensing nodes are very small (~10 fF), so large conversion gain and low noise is possible.
- Full CMOS circuitry can be implemented.
- Cross-section of single event effects is very small.
- The technology is based on industry standards, so further progress and low cost is envisaged.
- SOI transistors are shown to work over a very large temperature range from 4 to 600 K.

2. SOI pixel process and MPW run

We have developed a 0.2 μm SOI pixel process in collaboration with OKI Semiconductor Co. Ltd. The basic technology for fabricating the pixel detector is OKI's fully-depleted 0.2 μm CMOS SOI process [3]. Additional processing steps to create substrate implants and contacts between the implant nodes to the circuitry were established. Main specifications of the process are summarized in Table 1.

To reduce development cost of a design, we have been organizing MPW (Multi Project Wafer) runs. Two MPW runs were completed and one run is being processed now. In each run, we have about 16 designs from our collaborators [4–6]. Photograph of the last MPW run wafer is shown in Fig. 2.

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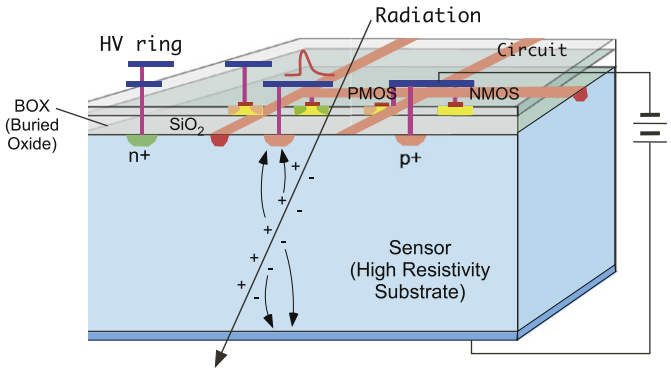

Fig. 1. Cross sectional view of a SOI pixel detector.

Table 1
SOI pixel process specification.

Process	0.2 μm low-leakage fully-depleted SOI CMOS, 1 Poly, 4 metal layers, MIM Cap., DMOS options, Core (I/O) voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, Top Si: Cz ~ 18 Ω–cm, p-type, 40 nm thick. Buried Oxide: 200 nm thick, Handle wafer: Cz ~ 700 Ω–cm, n-type, 725 μm thick
Backside	Thinned to 260 μm, and sputtered with Al (200 nm).

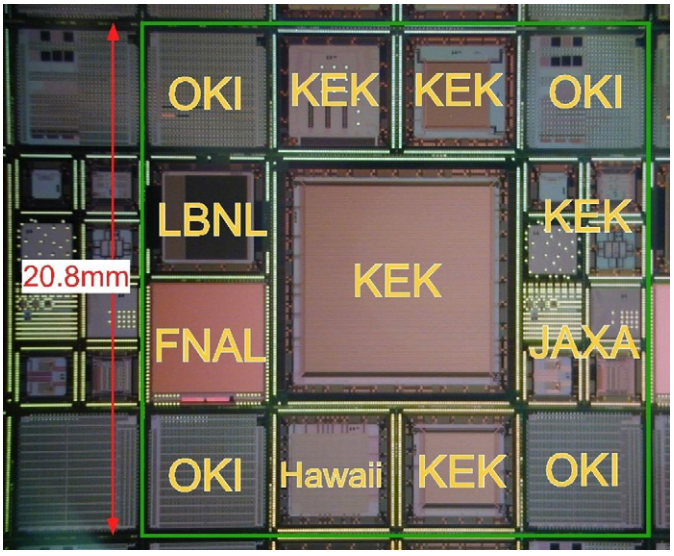

Fig. 2. Photograph of a Multi Project Wafer processed in 2008. In addition to Japanese laboratories and universities, there are designs from US institutions.

3. Pixel detectors

We are developing two kinds of pixel detectors. One is an integration-type pixel called INTPIX2, and the other is a counting-type pixel called CNTPIX2. In these detectors, reverse bias voltage is applied from the bottom surface or top n+ HV ring. Breakdown voltage is observed between 50 and 230 V depending on the pixel layout. Leakage current is less than 0.1 pA/μm^2.

3.1. Integration-type pixel

A schematic of the INTPIX2 is shown in Fig. 3. Chip size is 5 mm by 5 mm and has 128 × 128 pixels each 20 μm square. Fig. 4 shows a test chart image taken by the INTPIX2 with 8 keV X-rays. It indicates 20 lines/mm is well resolved. Each pixel has a window to illuminate light from topside to ease testing. It is possible to shrink the pixel size to less than 10 μm square.

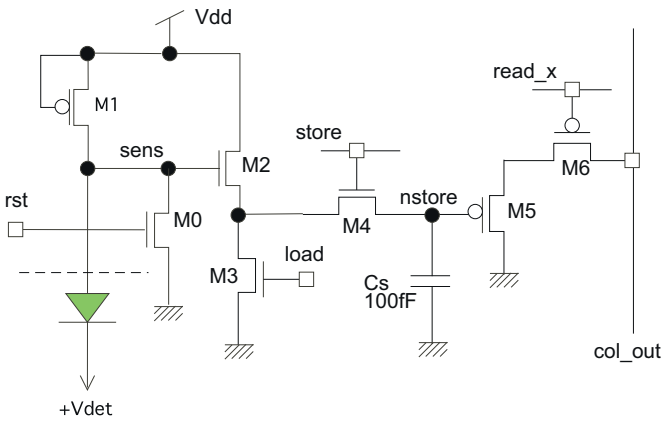

Fig. 3. Schematic of the integration type pixel (INTPIX2).

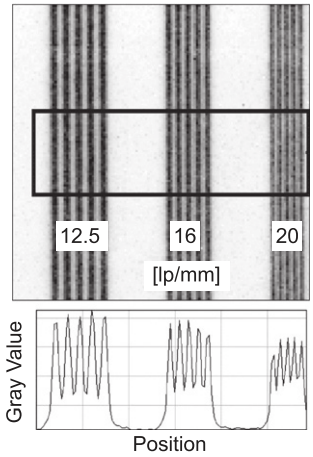

Fig. 4. X-ray image taken with the integration type pixel. The results are shown for three space resolution patterns from 12.5 to 20 lp/mm.

3.2. Counting-type pixel

A pixel circuit of the CNTPIX2 is shown in Fig. 5. The preamplifier circuit is same type proposed by Krummenacher [7] which contains leakage current compensation circuitry. After the low and high threshold discriminator, the input signal is counted in a 16-bit counter. Layout of the CNTPIX2 is shown in Fig. 6. There are 128 x 128 pixels in a 10.2 mm square chip. A metal plate image taken with 8 keV X-ray is shown in Fig. 7 and the operation was confirmed. We also see some crosstalk within a pixel and inefficiencies, so detailed study is continuing.

4. On-going R&D

Since the sensor nodes and circuits are placed very close together in the SOI pixel detector, there will be some interference between them. One of the newly developed techniques is buried p-well creation in the substrate. We implant p-type dopant through the top Si layer and create a buried p-well (BPW) region under the BOX. This BPW region will help to fix the underside potential of the transistors and reduce the so called back gate effect. The doping level of the BPW is about 3 orders lower than that of the p+ sensor node and drain/source region, so it does not affect the transistor characteristics in the top Si layer. Another direction is 3D vertical integration. We will bond two SOI wafers face to face by using micro-bump technology of ZyCube Co. Ltd [8]. Minimum pitch of the bump is 5 μm. This will enable higher circuit integration density and separate the sensitive circuit regions from the sensors.

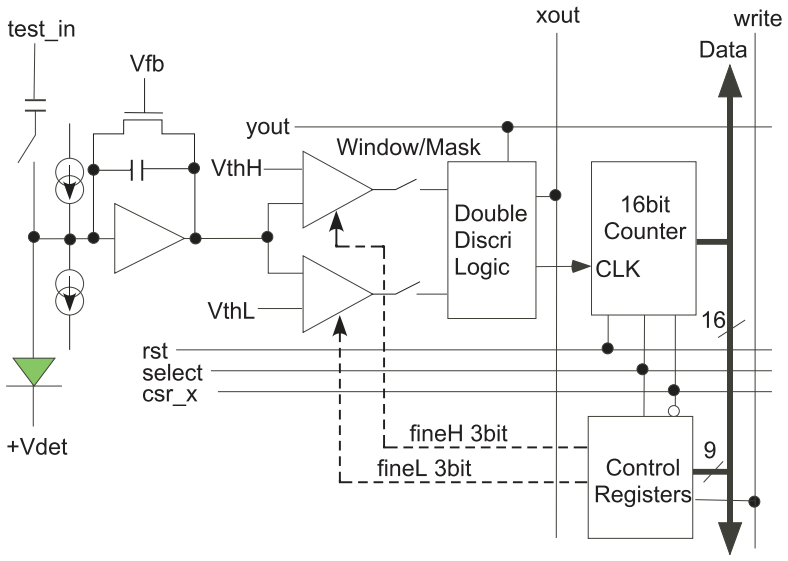

Fig. 5. Circuit of the CNTPIX2 pixel.

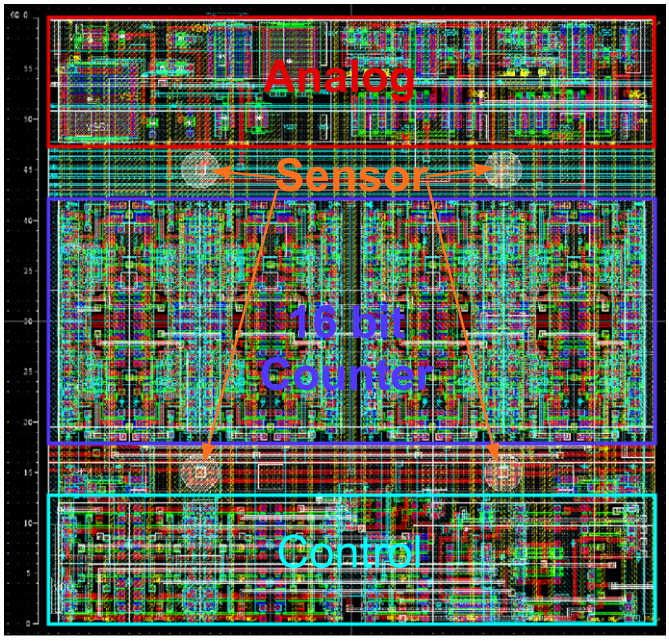

Fig. 6. Layout of a pixel in the CNTPIX2 chip. The size of a pixel is 60 μm by 60 μm, and each pixel contains about 600 transistors.

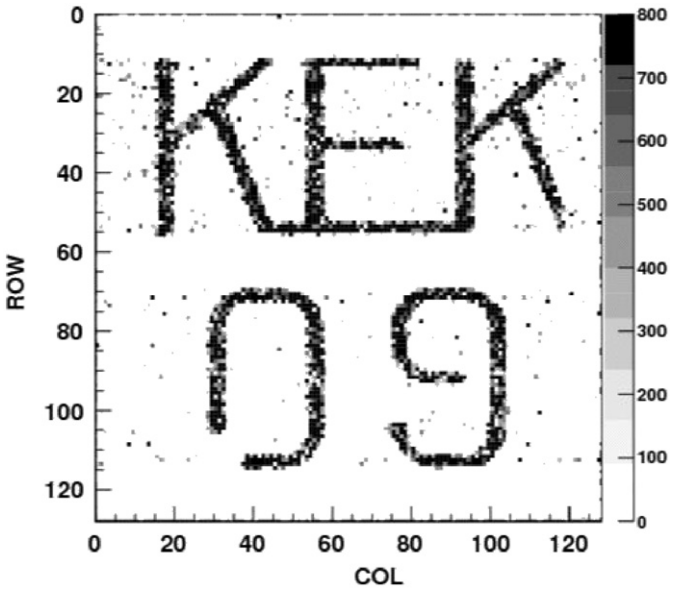

Fig. 7. X-ray Image of a metal mask taken with the CNTPIX2.

5. Summary

We have developed SOI based pixel technology and organized MPW runs by collecting designs from many laboratories and universities. The number of MPW runs will be increased to twice/year. We have demonstrated basic performance of the SOI integration-type and counting-type pixel detectors. To reduce the back-gate effect and improve radiation hardness, we are trying buried p-well technology and 3D integration technology.

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