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DEVICE CIRCUIT ANALYSIS OF FERROELECTRIC FETs FOR LOW POWER LOGIC & MEMORIES

A Thesis in

Electrical Engineering

by

Shreya Gupta

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The thesis of Shreya Gupta was reviewed and approved* by the following:

Sumeet Kumar Gupta

Assistant Professor of Electrical Engineering

Thesis Advisor

Mehdi Kiani

Assistant Professor of Electrical Engineering

Kultegin Aydin

Professor of Electrical Engineering

Head of Electrical Engineering Department

*Signatures are on file in the Graduate School.

ABSTRACT

Ferroelectric FETs (FEFETs) are emerging devices with an immense potential to replace conventional MOSFETs by virtue of their steep switching characteristics. The ferroelectric (FE) material in the gate stack of the FEFET exhibits negative capacitance resulting in voltage step up action which entails sub-60mV/decade sub-threshold swing at room temperature. The thickness of the FE layer (T_{FE}) is an important design parameter, governing the device-circuit operation. This thesis extensively analyzes the impact of T_{FE} on the characteristics of FEFET devices and circuits and presents important design insights for logic and SRAM design. While it is well known that increasing T_{FE} yields higher gain albeit with the possibilities of introducing hysteresis, our analysis points to other unconventional effects arising from T_{FE} optimization. Depending on the attributes of the underlying transistor, increasing T_{FE} beyond a certain value may lead to loss in saturation and/or negative differential resistance in the output characteristics. While the former effect results in the loss in gain of a logic gate, the latter yields hysteretic voltage transfer characteristics. We also discuss the effect of T_{FE} on the inherent polarization lag in the FE with respect to the applied voltage and its important consequences on the circuit performance. We show that for high T_{FE}, the delay of the circuit may increase with an increase in supply voltage. We also observe that SRAMs based on FEFETs show better performance in terms of access time and read/hold stabilities but at the cost of higher write time. All these factors need to be considered while optimizing T_{FE} for logic and memory applications. With proper T_{FE} optimization, FEFETs show an immense promise yielding 25% lower energy at iso-delay for supply voltages < 0.25 V. SRAMs based on FEFET show 5%–12% larger read stability and 9%–26% lower access time, albeit with an increase in the write time.

Table of Contents

List of Figures

List of Tables

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Chapter 1

Introduction

1.1 Motivation for Steep Switching Devices

In today's electronics industry, there is a huge demand for low power circuits due to the increased growth of personal computing devices, wireless communication systems and biomedical implantable devices [1]. This entails the requirement for multi-functional, high performance and ultra-low power integrated circuits. Now, to meet the needed requirements of high speed and low power, the size of semiconductor devices has been continuously decreasing. Moore's law has been a popular and widely used rule for scaling device dimensions [2]. Minimum feature sizes of MOSFET devices have shrunk considerably, thereby, increasing the number of transistors in a single integrated circuit [2] as shown in Figure 1.1. One of the downsides of the increased computing power and increased number of transistors per chip is the higher power dissipation per chip. [2]. Now, the power dissipation of a CMOS based circuit can be expressed as [2].

$$P = f_{clk}\, \sigma\, C_{tot}\, V_{DD}^{\,2} + V_{DD}\, I_{SC} + V_{DD}\, I_{leakage} \qquad (1.1)$$

Here f_{clk} is the clock frequency, σ is the average switching activity, C_{tot} is the total capacitance, I_{SC} is the short circuit current between the rail-to-rail supply voltage and $I_{leakage}$ is the leakage current. The dynamic power is directly proportional to the square of the supply voltage, and short circuit power is proportional to the supply voltage. In addition, the leakage current depends exponentially on the supply voltage. Thus, supply voltage (V_{DD}) scaling is an effective strategy for low-power circuit design. The V_{DD} scaling trends as technology node shrinks are depicted in Figure 1.2. However, V_{DD} scaling close to the transistor threshold voltage (V_{TH}) results in a significant loss in speed. If the technique of lowering V_{TH} is used then the performance penalty with V_{DD} scaling is mitigated, although at the cost of leakage increase [1-2]. The design conflict between speed and power is associated with the fundamental limit of 60 mV/decade on the subthreshold swing (SS) at room temperature for the MOSFETs. Surpassing this limit could enable more aggressive V_{DD} scaling, alleviating the speed-power conflict. Therefore, devices that exhibit steep switching characteristics (i.e. SS < 60mV/decade at room temperature) are being actively explored. Physics governing the operation of these devices let them achieve sub-60 mV/decade subthreshold swing at room temperature. This leads to higher drive currents and lower off-state leakage currents. At near-threshold and subthreshold voltages, steep-slope devices exhibit the potential to achieve better performance than the traditional CMOS devices [12-17].

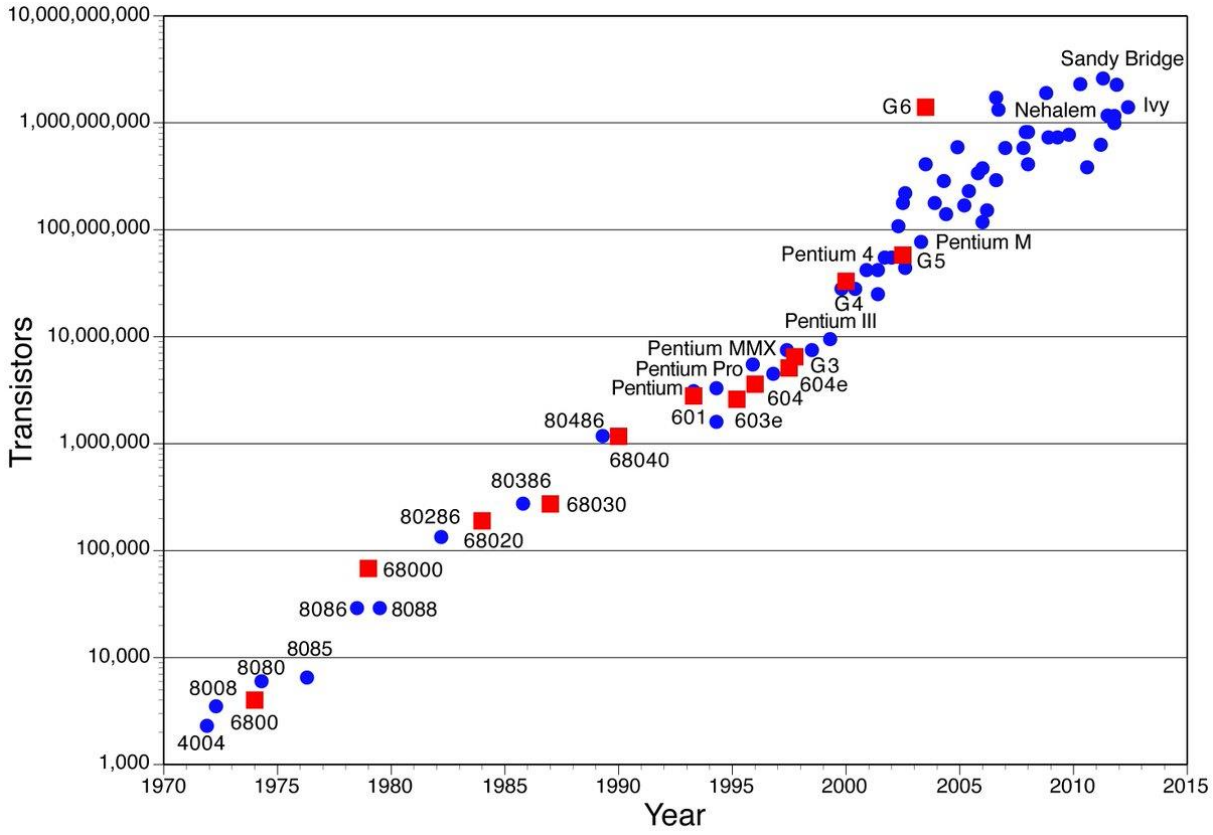

Figure 1.1 Moore's Law – The number of transistors on integrated circuit chips (1970-2015). (Source – Wikipedia, Intel Corp).

Several steep slope devices have emerged in the recent past because of their ability to deliver higher ON current at low voltages compared to the standard MOSFETs. Tunnel FETs (TFETs) [3-6] and Ferroelectric FETs (FEFETs) [7-17] are two popular examples of steep slope devices. TFETs use quantum-mechanical band-to-band tunneling mechanism to minimize the subthreshold swing. The interband TFET, is an assuring steep slope device alternative due to its better operation stability and improved fabrication compatibility than other emerging steep slope devices [5]. TFETs show huge potential for scaling supply voltages and for bringing down the power consumption [3]. However, since TFETs are unidirectional devices and have asymmetric current conduction, therefore, design of TFET based SRAM cells and other circuits is still challenging [5-6].

On the other hand, Ferroelectric FETs (FEFETs) employ a ferroelectric (FE) material in the gate stack and utilize the negative capacitance of the FE to induce a voltage step-up action during the device operation achieving steep switching [7-15]. This yields higher ratio of ON and OFF currents (I_{ON}/I_{OFF}), especially at low voltages, which is of great advantage for low power

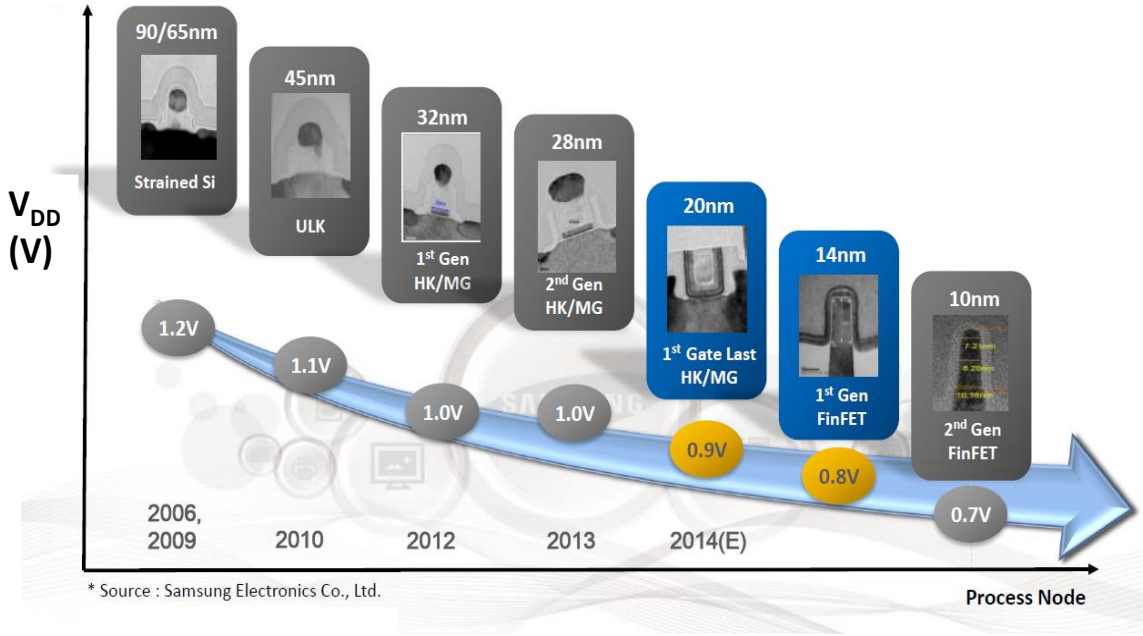

Figure 1.2 Trends for the supply voltage (V_{DD}) scaling.

applications. However, because of the presence of ferroelectric material in the gate stack, the gain in the ON current is accompanied by an increase in the gate capacitance. As the delay and the power of a circuit depend on both the ON current and the capacitance, the overall advantages of FEFETs at the circuit level need to be evaluated. Furthermore, the interactions of the highly non-linear FE capacitance with other capacitances present in the devices and circuits lead to unconventional device characteristics, which, in turn, yields atypical circuit behavior. Such attributes need to be properly analyzed in order to harness the useful properties and avert the deleterious features.

Moreover, since static random-access memories (SRAMs) are extensively used in low power circuits [1], therefore, it is important to analyze the performance and the potential of ferroelectric transistor based SRAMs as well. In order to understand the tradeoffs involved in their design, we perform an in-depth analysis in this research work. The objective of the SRAM analysis is to comprehend the implications of device level characteristics of ferroelectric transistors on the characteristics of 6-T SRAM cell based on ferroelectric transistor.

In this work, we perform a detailed analysis of FEFETs with a focus on the impact of the thickness of FE (T_{FE}) on the device-circuit performance. We present the relevant concepts from the perspective of digital logic and SRAM design. Analysis for analog circuits requires a separate treatment; nevertheless, some of the trends with respect to T_{FE} introduced in this work may be useful generally as well. T_{FE} is an important design parameter, directly governing the interactions of the FE with other device components and therefore, needs to be properly optimized. The analysis in this work not only provides useful insights into circuit-driven optimization of T_{FE} but

also highlights some unconventional device-circuit features that arise due to the unique FE properties.

The contributions of this work are as follows

- We discuss the impact of FE coupling with drain on the device and circuit characteristics. We point out the effects that become important at high T_{FE} such as negative drain-induced barrier lowering (DIBL) and negative differential resistance (NDR), and their impact on circuit behaviour such as hysteretic voltage transfer characteristics (VTC).
- We present the conditions for ensuring proper saturation in the output characteristics, which, in turn, determine the gain and regenerative action of the logic gates.
- We report that at higher T_{FE}, the delay of FEFET based circuits may increase with an increase in V_{DD} and describe the conditions for the same considering the effects of kinetic coefficient of the FE (ρ) and the wire capacitance (C_W).
- We analyse the effect of T_{FE} and FE-drain coupling on the energy-delay characteristics of a ring-oscillator.
- We describe quantitatively, the effects of T_{FE} as well as the kinetic coefficient of the FE (ρ), on the FEFET based SRAM characteristics.

1.2 Thesis Organization

This thesis is organized as follows: Chapter 2 familiarizes the basics of Ferroelectric FETs. It describes the FEFET device structure as well as the proposed modelling and simulation framework being used. Chapter 3 elucidates the FEFET and FEFINFET device characteristics, describing the possibilities of NDR, negative DIBL and non- saturation in the output characteristics. It clarifies the conditions for the same with respect to FE material thickness (T_{FE}) and voltage biases. Chapter 4 explains the implications of the FEFET and FEFINFET device characteristics on the voltage transfer characteristics of FEFET and FEFINFET inverter in addition to the energy-delay characteristics of FEFINFET based 7-stage ring oscillator (RO). Chapter 5 explicates the effects of T_{FE} on the FEFINFET SRAM characteristics. The contributions, conclusion and scope for future work are presented in Chapter 6.

Chapter 2

Modeling and Simulation of Ferroelectric FETs

2.1 Introduction

In this chapter, first we give a background and explain the fundamentals of the ferroelectric FETs. After establishing the basics, we elaborate and discuss our proposed equivalent circuit representation of ferroelectric FETs. Then we elucidate the device model and the simulation parameters being used in this research work. Based on this circuit- model framework, next we describe our proposed simulation methodology. The contributions of this chapter we summarize at the end.

2.2 Basics of Ferroelectric FETs

FEFETs comprise of a ferroelectric (FE) layer in the gate stack as shown in Figure 2.1 (a). The distinctive properties of the FEFET device are obtained by virtue of the interactions of the negative capacitance of the FE layer with the positive capacitance of the underlying transistor. As suggested in the first work on FEFETs [7], the negative capacitance arises because of a unique relation between the electric field (E) and polarization (P) of the FE (Figure 2.1(b)). This relation can be modeled with time dependent Landau Khalatnikov (LK) equation [11] given as follows

$$E = \alpha P + \beta P^3 + \gamma P^5 + \rho \, dP/dt \tag{2.1}$$

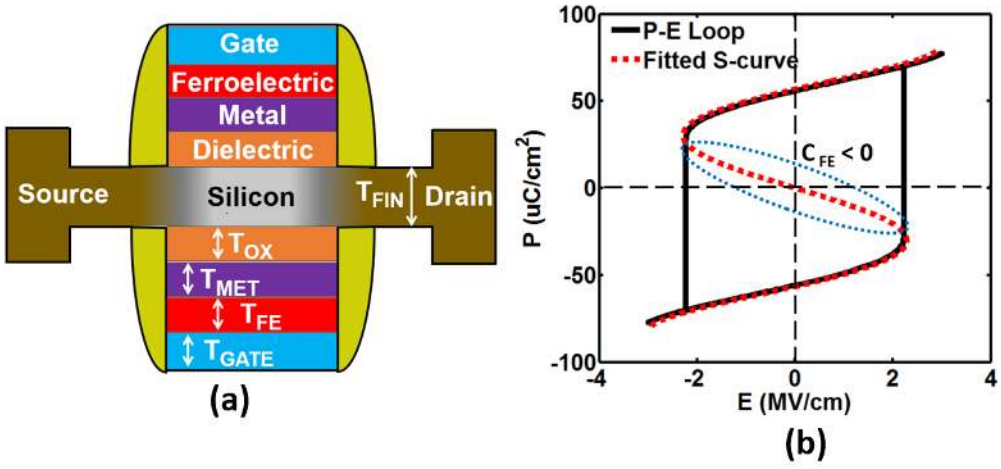

Figure 2.1 (a) Schematic of the cross section of Ferroelectric Transistor (b) P-E loop of ferroelectric capacitor.

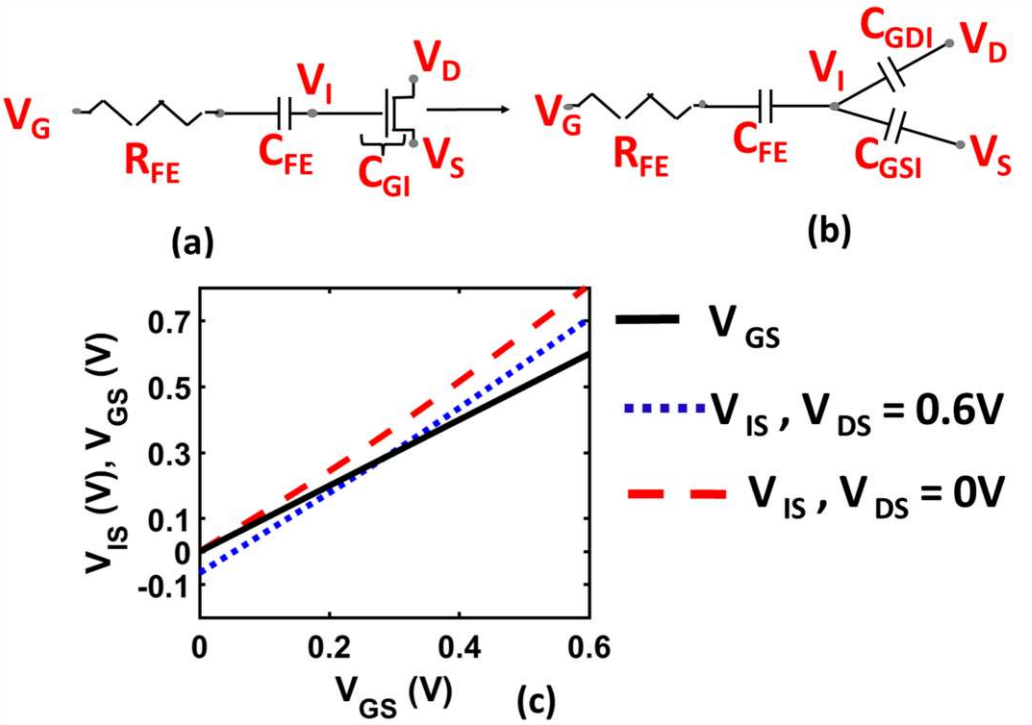

Figure 2.2 (a) Equivalent circuit representation of FEFET (b) Equivalent capacitance representation of FEFET with C_{GI} separated into C_{GSI} and C_{GDI} (c) Voltage Amplification in FEFET at V_{DS} = 0V and 0.6V.

Here, P is the polarization, E is the electric field, α, β, γ are static coefficients and ρ is the kinetic coefficient related to the time constant associated with the change of polarization of the FE over time. The P-E characteristic of the ferroelectric capacitor is shown in Figure 2.1(b). For FE, $\alpha < 0$, which results in hysteretic P-E characteristics (Figure 2.1(b)) [7-8]. There is a region in the P-E plot around the origin where the slope of the curve is negative which implies a negative FE capacitance, $C_{FE} < 0$. [9-10]. Steep switching FEFETs (to be employed as logic transistors), are designed to operate in this region so as to exploit the negative capacitance of the FE [12-15].

2.3 Proposed Equivalent Circuit Representation

The behavior of the FEFET device can be understood from the simple proposed equivalent circuit representation of the device as shown in Figure 2.2 (a, b). Here, C_{GI} is the positive gate capacitance associated with the underlying transistor, V_G, V_S, V_D are the applied voltages at the gate, source and drain of the FEFET and V_I is the voltage at the boundary of FE and the dielectric of the underlying transistor which is subsequently referred to as the gate of the underlying transistor. Since C_{GI} has two components - C_{GSI} (gate to source capacitance) and C_{GDI} (gate to drain capacitance), therefore, the circuit in Figure 2.2 (a) can be extended to the circuit shown in Figure 2.2 (b). R_{FE} ($=\rho T_{FE}/A_{FE}$) models the term '$\rho\ dP/dt$' in (2.1), as discussed in [14]. Here A_{FE} is the area of the FE layer and it is same as the cross-sectional area of the underlying device.

The equivalent voltage, V_{IS} that is obtained at the gate of the underlying transistor at steady state can be derived from Figure 2.2 (b) and is given by the following equation(s) when the FE operates in the negative capacitance region [15].

$$dV_{IS} = \frac{dV_{GS}}{1-\frac{C_{GI}}{|C_{FE}|}} - \frac{dV_{DS}}{\frac{|C_{FE}|-C_{GI}}{C_{GDI}}} = \eta dV_{GS} - \eta_D dV_{DS} \tag{2.2}$$

$$V_{IS} = \int_0^{V_{IS}} dV_{IS} = \int_0^{V_{GS}} \eta\, dV_{GS} - \int_0^{V_{DS}} \eta_D\, dV_{DS} \tag{2.3}$$

Here,

$$\eta = \frac{1}{1-\frac{C_{GI}}{|C_{FE}|}} = \frac{1}{1-\frac{C_{GI}/A_{FE}}{|C_{FE}|/A_{FE}}} = \text{Gain due to FE} > 1 \tag{2.4}$$

$$\eta_D = \frac{1}{\frac{|C_{FE}|-C_{GI}}{C_{GDI}}} = \frac{C_{GDI}}{|C_{FE}|-C_{GI}} = \text{Drain coupling factor} \tag{2.5}$$

It can be easily seen that

$$\frac{\eta}{\eta_D} = \frac{|C_{FE}|}{C_{GDI}} \tag{2.6}$$

From the above equations, we make the following four important observations

- The change in V_{IS} (dV_{IS}) is dependent on the change in V_{GS} (dV_{GS}) and the change in V_{DS} (dV_{DS}). The value of V_{IS} is obtained by the integration of equation (2.2) and is depicted in equation (2.3).

- The internal voltage, V_{IS} that determines the gain in I_{ON}/I_{OFF} depends not only on the applied gate voltage, V_{GS} but also on the drain voltage, V_{DS} of the ferroelectric transistor. This is due to the coupling between the gate and drain terminals of the underlying transistor, C_{GDI}. For instance, for a non - zero value of V_{DS} and $V_{GS} = 0$, V_I is negative as shown in Figure 2.2 (c) due to C_{GDI} (This effect is captured by the term η_D). We will discuss the implication of this effect in detail in later chapters of the thesis.

- As $|C_{FE}|$ reduces (for example with the increase in the FE thickness T_{FE}), the amplification (η) provided by the negative capacitance increases [3]. As a result of this amplification, subsequently, V_I becomes greater than V_G (Figure 2.2 (c)) resulting in reduced subthreshold swing (SS) and higher ratio of ON and OFF currents (I_{ON}/I_{OFF}). However, at the same time, η_D also increases, which yields unconventional characteristics, as discussed later.

- Since the total gate capacitance (C_{GFE}) of the FEFET is determined by the series equivalent of its positive and negative capacitance and equals $|C_{FE}|C_{GI}/(|C_{FE}|-C_{GI})$ or ($C_{GI} * \eta$), FEFETs exhibit relatively higher gate capacitance compared to the standard transistors. It is also easy

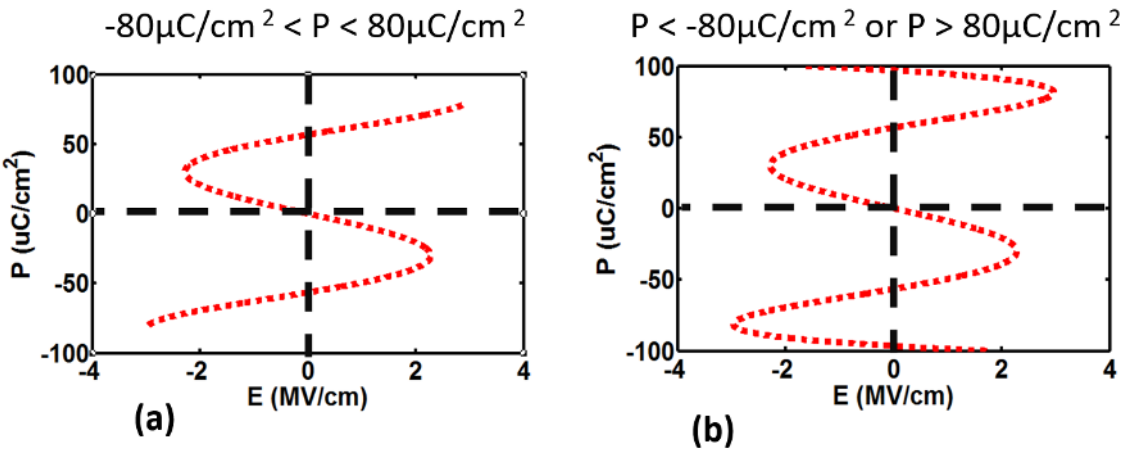

Figure 2.3 S curve plots for Polarization (a) between -80μC/cm^2 and 80μC/cm^2 (b) greater than 80μC/cm^2 or less than -80μC/cm^2

to deduce that as $|C_{FE}|$ reduces, C_{GFE} increases. Thus, an increase I_{ON} is always accompanied by an increase in the gate capacitance of the FEFET.

It is also noteworthy that as T_{FE} is increased beyond a certain value, the FEFET device characteristics may show hysteresis [14] and even non-volatility [16]. Since our work focuses on logic applications and SRAM design, we limit our discussions to the region of non-hysteretic device operation only.

With the understanding of the basic operation of FEFETs, now we discuss the effect of T_{FE} on the device-circuit characteristics in the rest of the thesis. To perform this analysis, we employ an in-house SPICE model for FEFETs [14] and a device-circuit simulation framework, which we describe next.

2.4 Modeling and Proposed Simulation Methodology

The analysis in this work employs our in-house SPICE model for FEFETs [14] that is based on the time dependent LK equation (2.1) solved self-consistently with the transistor equations. As a part of this self-consistent solution, we obtain the device currents, voltage at the internal gate (V_I) and FE polarization as a function of the applied gate/drain/source voltages. It is noteworthy that the FEFET model just has four assigned electrodes (gate, source, drain and body) as in standard transistor models. Voltage at the internal gate (V_I) is obtained as a part of the device-circuit simulations. However, V_I can be monitored during device-circuit simulations, by virtue of the SPICE based implementation of the model which enables the analysis of V_{IS} as a function of V_{GS} and V_{DS}, as discussed subsequently.

We employ predictive technology model (PTM) high performance 10 nm FINFET model [18] for the standard/underlying transistor. It is worthwhile to clarify that the effects of diffusion barriers and fin tuck have not been taken into account in this work. However, this assumption does not impact the trends that we describe in the subsequent chapters. If we consider the additional

Table 2.1. Simulation Parameters of FE

α	-1.17e9 m/F
β	4.9e9 m^5 /F/C^2
γ	-3.9e9 m^9/F/C^4
ρ	0.05 Ω m

capacitances due to fin tuck and other structural features of the FINFETs, the FE thickness at which the subsequently discussed unconventional effects occur will change, but the trends will remain the same. It may be noted that the objective of this work is not to characterize FEFETs at the 10nm node but to highlight generic unconventional aspects of the behavior of FEFETs in digital logic, for which we take the 10nm predictive technology models as examples. To analyze the output characteristics of FEFETs more closely, we also employ 22nm MOSFET model [18]. The 10nm and 22nm predictive technology models are referred as FINFETs/FEFINFETs and MOSFETs /FEFETs respectively in the rest of the thesis. The list of parameters and their corresponding nominal values used for our analysis are given in Table 2.1. The values of the static coefficients (α, β and γ) are extracted from our experiments on Hafnium Zirconium Oxide (*HZO*). The nominal value of the kinetic coefficient, ρ, is estimated as mentioned in [9]. Note that we have assumed α, β, γ and ρ to be independent of T_{FE} (as in other works [7-17]) and the trends with respect to T_{FE} presented later need to be understood in the context of this assumption. The analysis of unconventional characteristics of FEFETs still remains valid (albeit those effects will occur at a different T_{FE} value if the dependence of the coefficients on T_{FE} is taken into account). Also, the LK coefficients that we have used in this work have been extracted based on the best fit of the S-curve with experimental data on HZO. While extracting the parameters, we found the negative values of gamma is fine, as long as we restrict the usage of model in a certain polarization range. In other words, the model is valid only for the range of polarizations, for which the S curve is obtained. Using the extracted parameters, we get the S-curve as shown in Figure 2.3 (a). The model is valid for polarization lying the range of -80μC/cm^2 to 80μC/cm^2. Outside this range, we get unphysical characteristics and therefore the model should not be used if the device exhibit polarization outside the valid range (Figure 2.3 (b)). For the analysis in this work, the polarization remains within -20μC/cm^2 to 20μC/cm^2 (i.e. in negative capacitance region) and therefore, the results do not have any unphysical trends. It may also be mentioned that the calibrated value of γ (for which the best fit with experiments was achieved) is negative, which leads to non-physical FE characteristics for large $|P|$. However, as long as we restrict the usage of model in a certain polarization range (in this case between -80μC/cm^2 to 80μC/cm^2), the model predicts the expected characteristics of FE (as shown in Figure 2.3 (a)) and FEFETs. We have verified that the trends we present in this work remain the same for positive values of γ as well. We also analyze the trends for different values of ρ later. The nominal supply voltage, V_{DD} is 0.6V for 10nm FINFETs model and 0.8V for 22nm MOSFET model.

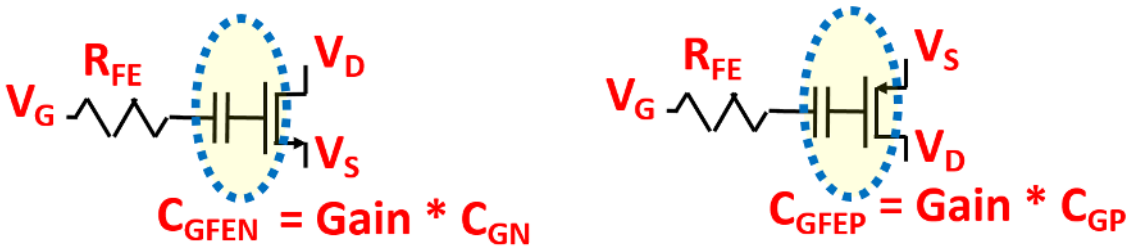

Figure 2.4 Circuit symbol for (a) NFEFINFET (b) PFEFINFET

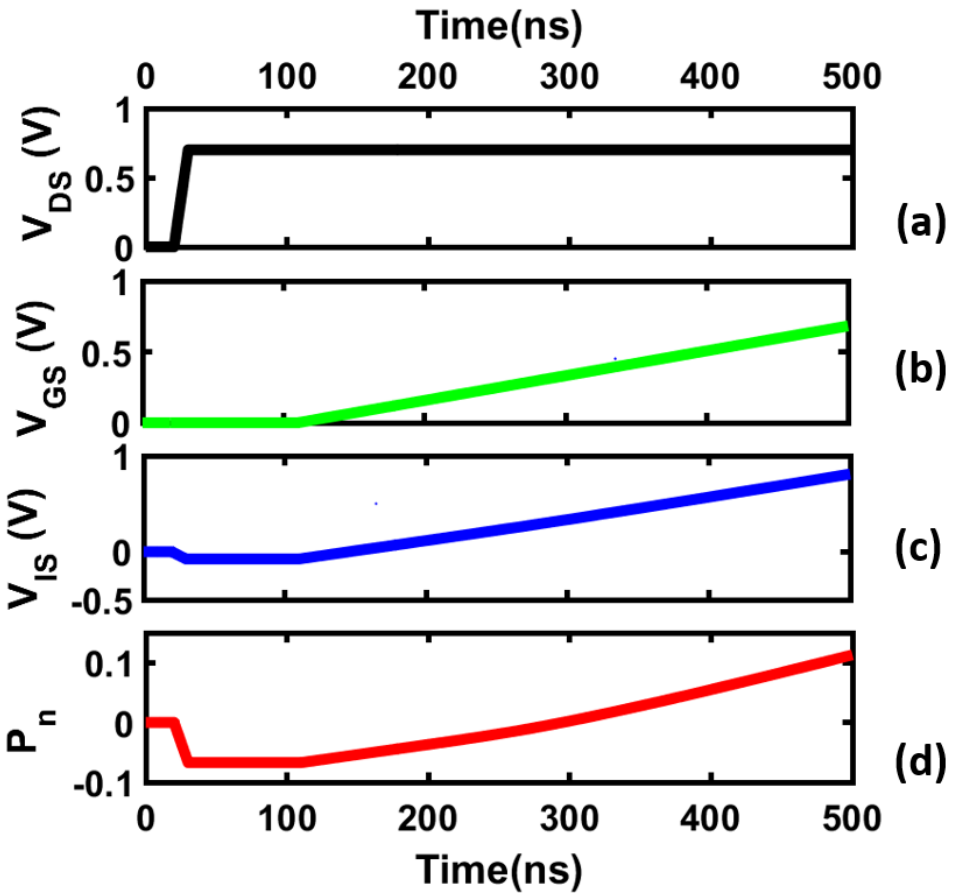

Figure 2.5 An illustration of the simulation methodology for V_{GS} sweep of FEFINFETs at V_{DS} = 0.6 V. (a) Applied V_{DS} being ramped up from 0 to 0.6 V. (b) Applied input gate to source voltage V_{GS} being swept from 0 to 0.6 V. (c) Obtained voltage at the internal gate node of the FEFINFET. (d) Normalized polarization of the FE capacitor. Here, P_n is the normalized polarization defined as P/P_c, where, P_c is the polarization at which $dE/dP = 0$ in (2.1) at steady state

From the model [14], which is a capacitance based model, we see that C_{FE} has been modeled as C_0 in parallel with the series combination of non-linear capacitor C_{LK} and resistor R_{LK} (depends on

ρ and T_{FE}). When a transient voltage is applied at the gate of the FEFINFET device, the charge associated with the polarization is stored in C_{LK} and the charge due to the electric field is stored in C_0. Since the bulk of the total charge associated with the ferroelectric capacitor gets stored in C_{LK}, therefore, we can approximate C_{FE} as C_{LK}. Also, R_{LK} is being represented as R_{FE} for our simplicity in this work. The equivalent gate capacitance for a ferroelectric transistor as explained in section 2.1 will be $C_{MOS} * \eta$. The circuit representations for NFEFINFET and PFEFINFET that we will use for representing FEFINFET based circuits throughout the thesis are shown in Figure 2.4 (a) for NFEFINFET and Figure 2.4 (b) for PFEFINFET.

In this work, we obtain the DC and time-dependent characteristics based on transient simulations [14]. Figure 2.5 depicts an example of our proposed simulation methodology [15] for V_{GS} sweep of FEFINFETs at V_{DS} = 0.6V. We begin our simulations with all the voltages at zero. We then ramp up the voltages to the desired values so that the polarization of the FE layer and V_{IS} in the FEFETs evolve in a self-consistent fashion. For the DC characteristics, we perform quasi-DC simulations by applying a triangular waveform at the gate/drain terminals with frequency << 1/ (the time constants of the device). For transient simulations of a logic gate, we first ramp up the supply voltage from 0 to V_{DD} and once all the voltages in a circuit stabilize, we apply the input signals. This approach enables us to capture the effect of η and η_D on V_{IS} (equation (2.2)) in a self-consistent fashion. Employing this simulation framework, we perform the device-circuit analysis of FEFETs and describe the effects of T_{FE} optimization in the following chapters. We complement the self-consistent simulation based quantitative analysis with the explanations employing the equivalent circuit in Figure 2.2 and equations (2.2-2.6) to provide qualitative insights.

2.5 Summary

Following are the contributions of this chapter:

- We proposed an equivalent circuit representation of Ferroelectric FETs and introduce drain coupling factor (η_D) that captures the effects of the coupling between the gate and drain terminals of the underlying transistor, C_{GDI}
- We established that the internal voltage, V_{IS} on the applied gate voltage, V_{GS} and on the drain voltage, V_{DS} of the ferroelectric transistor as well.
- We proposed and illustrated our simulation methodology that we have used throughout this work.

Chapter 3

Analysis of Device Characteristics

3.1 Introduction

In this chapter, we analyze the FEFINFET/FEFET device characteristics and their dependence on T_{FE} by employing the previously discussed modeling and simulation framework. To explain the behavior of FEFINFET/FEFET based circuits, analysis of device characteristics is important. We discuss the transfer characteristics for different values of T_{FE} at a fixed $V_{DS.}$ We also explain the behavior of I_D - V_{GS} characteristics at a fixed T_{FE} for lower and higher V_{DS} values. Similarly, we analyze the output characteristics of ferroelectric transistor for different T_{FE} and V_{DS} values. Moreover, the behavior of equivalent gate capacitance of the device with respect to V_{GS} at different T_{FE} values is also discussed in this chapter. We summarize the contributions at the end of this chapter.

3.2 Transfer Characteristics

Figure 3.1 shows the transfer characteristics of FEFINFETs for different T_{FE}. It is evident that as T_{FE} increases, switching characteristics become steeper due to the increase in the voltage amplification provided by the FE layer (as discussed before and shown in previous works [3-8]). Additionally, as T_{FE} increases, the reduction in OFF current is more pronounced. Considering the characteristics at a fixed T_{FE} (Figure 3.2), we observe that FEFINFETs show reduction in the OFF current compared to FINFETs at high V_{DS}. At lower V_{DS} (=0.05V), the OFF current is almost same as the standard transistors for all T_{FE} values. The reason behind these effects is explained as follows. From Figure 2.5 we see that an increase in the drain voltage leads to a decrease in the polarization and as a result, the voltage at the internal gate node becomes negative even though the applied gate voltage is 0. This is due to the presence of the coupling between the drain and gate of the underlying transistor, C_{GDI} that reflects the transitions at the drain terminal to the internal gate terminal of the FEFET (through η_D- see equation (2.2)). Due to negative V_{IS}, FEFINFETs exhibit lower OFF current. Moreover, as T_{FE} increases, η_D increases (as discussed in chapter 2), which leads to the reduction in the OFF current as seen from Figure 3.1 (b).

Conventionally, the OFF current of a device is directly proportional to V_{DS}. However, we observe from the transfer characteristics of FEFETs (shown in Figure 3.2(c)) that the OFF current at lower V_{DS} can be more than that at higher V_{DS} values, especially for large T_{FE}. This phenomenon is referred to as the negative DIBL [17] (Drain induced barrier lowering) as it is the reverse of the traditional DIBL. This reason for such a behavior is attributed to the fact that $V_{IS,}$ which controls the OFF current in FEFINFETs, is smaller at larger values of V_{DS} (equation (2.3)). As a

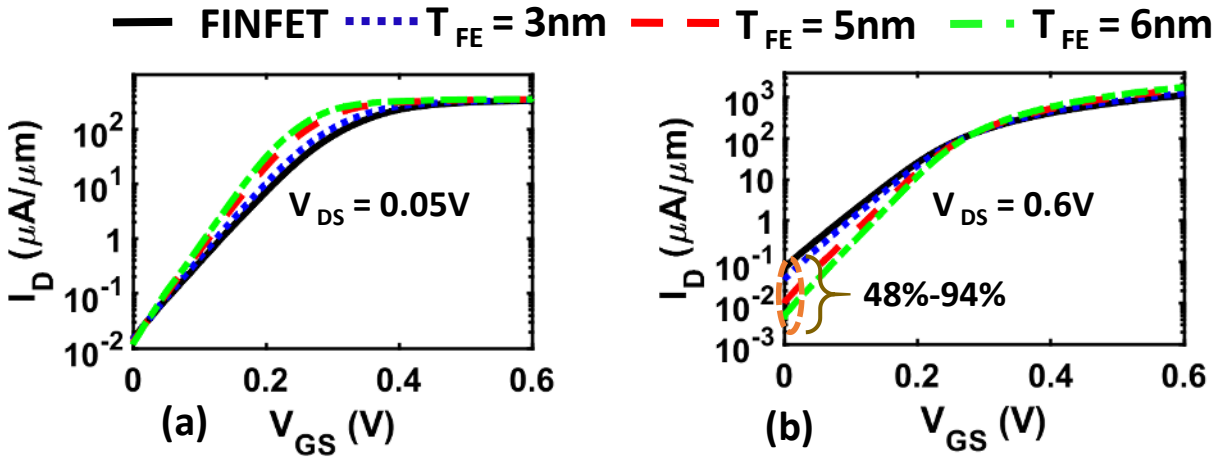

Figure 3.1 I_D-V_{GS} characteristics for different values of T_{FE} showing steeper switching characteristics at (a) V_{DS} = 0.05V (b) V_{DS} = 0.6V. FEFINFETs show reduction in OFF current by 48% - 94% for high V_{DS} values.

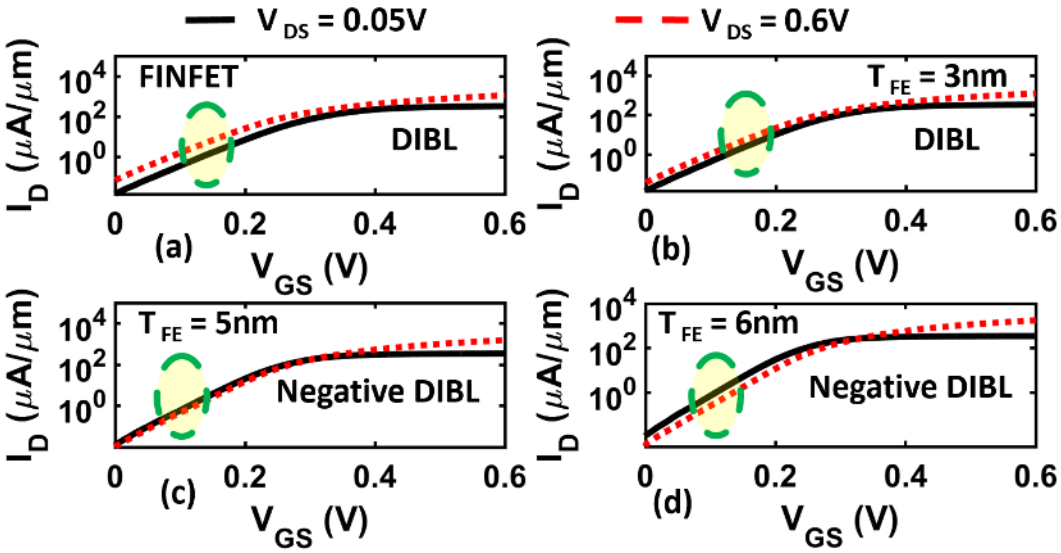

Figure 3.2 DIBL in (a) FINFETs (b) FEFINFETs at T_{FE} = 3nm and Negative DIBL in FEFINFETs at (c) T_{FE} = 5nm (d) T_{FE} = 6nm

consequence of the FE-drain coupling, current gain due to steep switching is observed for a partial range of V_{GS}, as shown in Figure 3.2 (b). Moreover, increasing V_{DS} has two opposing effects on the sub-threshold current due to (1) larger electric fields which tend to increase the current and (2) negative impact on V_{IS}, which tends to reduce the current. These opposite effects lead to reduction in the drain induced barrier lowering (DIBL), as can be seen in Figure 3.2 (a-b). In fact, at large T_{FE}, OFF current may reduce with increase in V_{DS}, due to the dominance of the second effect. This yields negative DIBL (Figure 3.2 (c-d)).

3.3 Output Characteristics

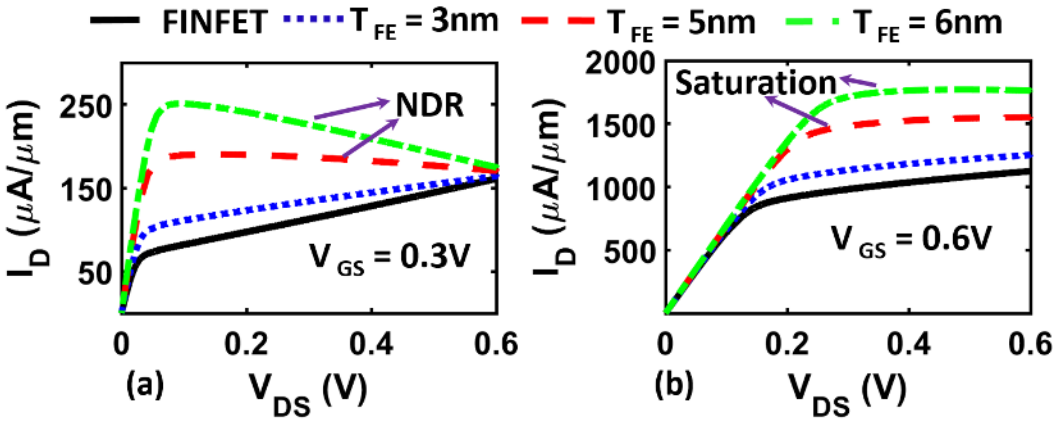

Figure 3.3 $I_D - V_{DS}$ characteristics of FEFINFETs for different values of T_{FE} for (a) V_{GS} = 0.3V showing NDR (b) V_{GS} = 0.6V showing saturation in the ON current at T_{FE} = 5nm and 6nm.

In this section, we discuss the FEFET device output characteristics for different values of T_{FE} at a fixed $V_{GS.}$ We also explain the behavior of I_D - V_{DS} characteristics at a fixed T_{FE} for lower and higher V_{GS} values.

When T_{FE} is small, proper saturation is observed as in a standard transistor (Figure 3.3 and Figure 3.4). However, for large T_{FE}, negative differential resistance (NDR) is observed in the output characteristics [18] at low $V_{GS,}$ (Figure 3.3 (a) and Figure 3.4 (a)). However, as V_{GS} is increased, the devices do not exhibit the NDR behavior. In this case, depending on the characteristics of the underlying transistor, the drain current (I_D) may saturate (as in the case of 10nm FINFET- Figure 3.3 (b)) or may not show saturation at all (as observed for 22nm MOSFET - Figure 3.4 (b)). These trends can be understood by considering the effect of V_{GS} and V_{DS} on V_{IS} (equations (2.2-2.6)). Moreover, the impact of the voltage step-up action (V_{IS}/V_{GS} > 1) on the

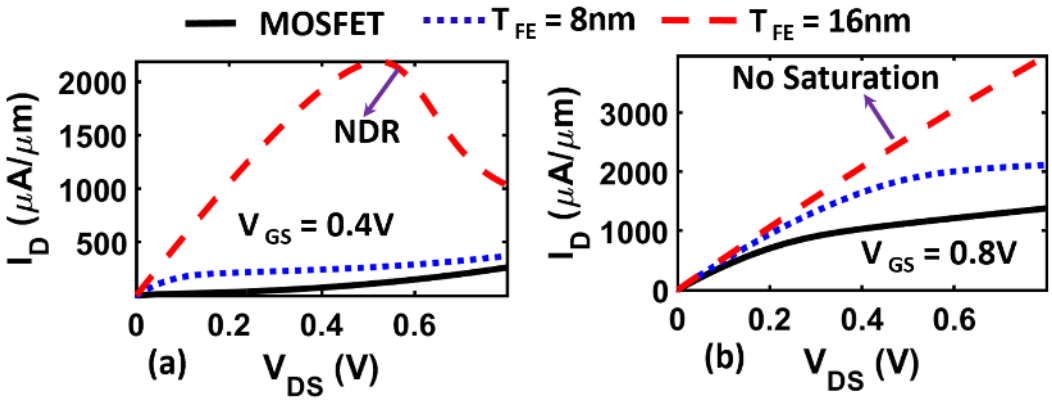

Figure 3.4 $I_D - V_{DS}$ characteristics of FEFETs for different values of T_{FE} for (a) V_{GS} = 0.4V showing NDR (b) V_{GS} = 0.8V showing no saturation in the ON current at T_{FE} = 16nm.

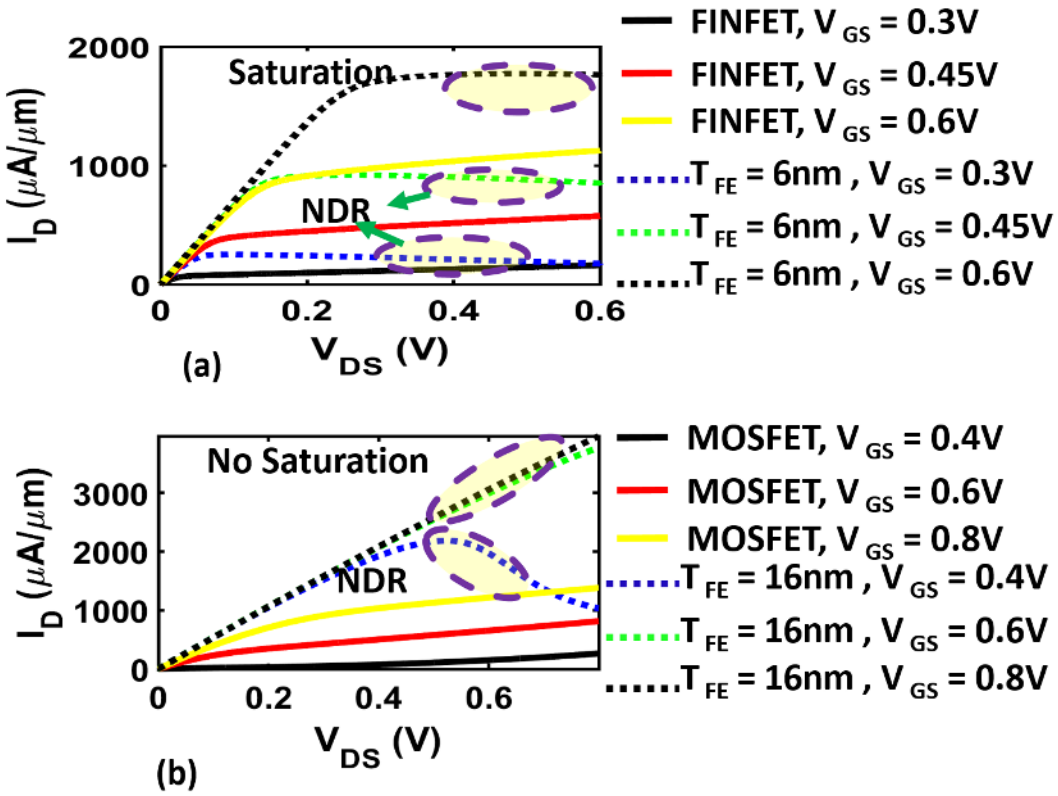

Figure 3.5 I_D – V_{DS} characteristics of (a) FEFINFETs for different values of V_{GS} and T_{FE} = 6nm (b) FEFETs for different values of V_{GS} and T_{FE} = 16nm.

saturation voltage V_{DSAT} plays a key role in governing the device operation. All these effects are explained in detail below. The dependence of current on V_{DS} is manifested in the output characteristics (Figure 3.3 – 3.5). However, the overall trends also depend on V_{GS}, T_{FE} and the characteristics of the underlying transistor. To discuss this in detail, we consider different cases as outlined below.

At low values of T_{FE}, $|C_{FE}|$ is large compared to C_{GDI} and hence, $\eta >> \eta_D$ (equation (2.6)). Therefore, the positive effect of $\int_0^{V_{GS}} \eta \, dV_{GS}$ on V_{IS} dominates over the negative effect of $\int_0^{V_{DS}} \eta_D \, dV_{DS}$ (equation (2.3)). Moreover, the voltage step-up is still sufficiently small such that saturation voltage, $V_{DSAT} < V_{DD}$. Consequently, the behavior of I_D at lower T_{FE} values is similar to the conventional transistor, albeit with a larger I_{ON} (due to voltage step-up action) and lower output conductance (due to two opposing effects of V_{DS} on current, as explained before) (Figure 3.3 – 3.5).

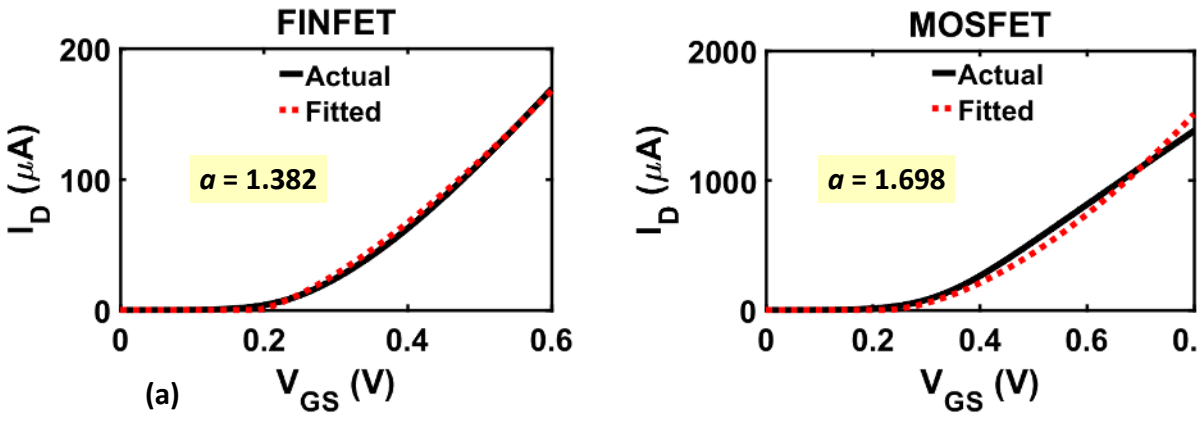

Figure 3.6 Approximate value of a based on alpha power law model for (a) FINFET (PTM 10nm) and (b) MOSFET (PTM 22nm).

- At higher T_{FE} values, $|C_{FE}|$ decreases [14] and may become comparable to C_{GDI}. Consequently, η and η_D also become comparable (equation (2.6)). Therefore, in this case, the relative values of V_{GS} and V_{DS} control V_{IS} (Figure 3.3 – 3.5)).
    - For low V_{GS}, $\int_0^{V_{DS}} \eta_D \, dV_{DS}$ dominates over $\int_0^{V_{GS}} \eta \, dV_{GS}$ and therefore, increasing V_{DS} leads to reduction in V_{IS}. As a result, the current decreases with positive change in V_{DS} and the output characteristics exhibit negative differential resistance [17] (NDR - Figure 3.3-3.5).
    - In contrast, for high V_{GS}, $\int_0^{V_{GS}} \eta \, dV_{GS}$ becomes the dominant factor and offsets the effect of $\int_0^{V_{DS}} \eta_D \, dV_{DS}$ .For this reason, NDR is not observed at high V_{GS}. Figure 3.3 – 3.5).

Also, V_{IS} at higher T_{FE} becomes large enough so as to significantly impact V_{DSAT}. The overall impact on the device characteristics is determined by the behaviour of the underlying transistor with respect to the dependence of V_{DSAT} on the gate voltage (V_{IS}). In general, V_{DSAT} can be written as $(V_{IS}\text{-}V_{TH})^{a}$, where V_{TH} is the threshold voltage of the underlying transistor and a is the exponent dependent on the mechanism of the current saturation in transistors [20]. It is well known that $1 < a < 2$, with the two extreme values corresponding to the extreme short channel FETs and long channel FETs, respectively. Figure 3.6 shows the values of a for FINET (10nm PTM) and MOSFET (22nm PTM). If V_{DSAT} is a weak function of V_{IS} (i.e. a is small, as in case of 10 nm FINFET technology), increase in V_{IS} due to the negative capacitance of FE mildly affects V_{DSAT}, yielding $V_{DSAT} < V_{DD}$. Thus, the output characteristics exhibit saturation (Figure 3.3). On the other hand, for larger a, (as in case of bulk MOSFETs at the process node of 22nm), we observe that under the influence of large V_{IS}, V_{DSAT} exceeds V_{DD}, thus, I_D fails to saturate. (Figure 3.4 – 3.5)).

It may be noted that larger FE thickness is required for FEFETs (compared to a larger gate length) compared to FEFINFETs to achieve similar voltage step-up. This is because the gate

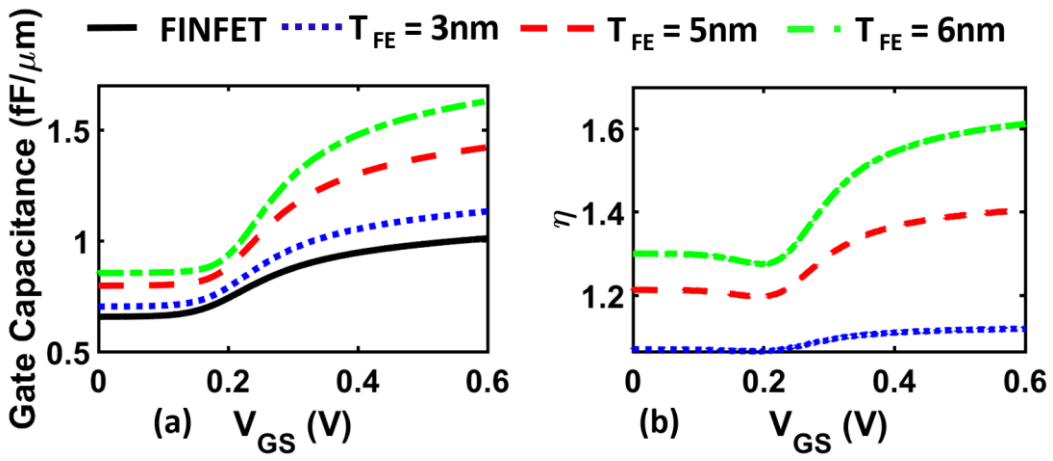

Figure 3.7 a) C_G-V_{GS} characteristics of FEFINFETs (b) Variation of η with respect to V_{GS} for different values of T_{FE} at V_{DS} = 0.6V.

capacitance per unit area (C_{GI}/A_{FE}) of the underlying FINFETs is more than that of MOSFETs (as per the transistor scaling trends). Hence, as per (2.2), for the same T_{FE} or C_{FE}/A_{FE} value, the gain η for FEFETs will be lower than that of FEFINFETs. In other words, to get a similar gain, larger T_{FE} is required for FEFETs.

3.4 Gate Capacitance Characteristics

Besides the dependence on the ON current, the delay and energy characteristics of a circuit also depend on the gate capacitance of the device. From Figure 3.7 (a), we note that as T_{FE} increases, the total gate capacitance increases (by factor η) due to the increase in the gain provided by the negative capacitance of the FE layer, as discussed in chapter 2. This factor η also depends on V_{GS} (a non-monotonic trend), as can be observed from Figure 3.7 (b). As seen from equation (2.4), η increases with increasing C_{GI}, but decreases with increasing $|C_{FE}|$. Now, the behavior of $|C_{FE}|$ with respect to V_{GS} can be understood by considering the following equation (derived from equation (2.1) for $C_{FE} < 0$).

$$|C_{FE}| = \left|\frac{dQ}{dV}\right| = \frac{A_{FE}}{|\alpha|\, T_{FE} - (3\,\beta\, T_{FE}\, P^2 + 5\,\gamma\, T_{FE}\, P^4)} \tag{3.1}$$

As V_{GS} increases, charge and FE polarization (P) also increase. From equation (3.1), it can be observed that this leads to an increase in $|C_{FE}|$. The dependence of C_{GI} on V_{GS} can be observed from the dotted line (corresponding to FINFETs) in Figure 3.7 (a). At low V_{GS}, increase in C_{GI} with V_{GS} is negligible. However, at high values of V_{GS}, the increase in C_{GI} is significant. Considering all the aforementioned factors, the following can be concluded (A) at low V_{GS}, the ratio $C_{GI}/|C_{FE}|$ decreases with increasing V_{GS} (due to increase in $|C_{FE}|$ and negligible change in C_{GI}); (B) at high V_{GS}, the ratio $C_{GI}/|C_{FE}|$ increases with increasing V_{GS} (because of a large increase in C_{GI}). From equation (2.4), one can observe that η increases with $C_{GI}/|C_{FE}|$, which explains the non-monotonic trend observed in Figure 3.7. These trends have important circuit implications, as discussed later. An important point to be noted is that the trends of η with respect to V_{GS} is

dependent on the signs of β and γ. The above discussion was for $\beta > 0$ and $\gamma < 0$ (see Table 2.1). If an FE material has $\beta > 0$ and $\gamma > 0$, similar trends are observed as $|C_{FE}|$ increases with V_{GS} and η shows a non-monotonic trend, as discussed above. However, if $\beta < 0$ and $\gamma > 0$, then, depending on the values of β and γ, the term in the parenthesis of the denominator of the right-hand side of equation (3.1) becomes negative for small $|P|$, leading to decreasing $|C_{FE}|$ with increasing V_{GS}. As a result, η increase monotonically with increasing V_{GS}.

3.5 Summary

To sum up, following are the contributions of this chapter,

- We discussed the possibilities of negative DIBL, NDR and non- saturation in the output characteristics and presented the conditions for the same with respect to T_{FE} and voltage biases.
- W explained that to get a similar gain, larger T_{FE} is required for FEFETs as compared to FEFINFETs.
- We also discussed the increase in capacitance with increasing T_{FE}, which is expected to offset the benefits of high drive-ability of FEFINFET.
- In addition, we showed that if $\alpha < 0$, $\beta > 0$ and $\gamma < 0$, then, η first decreases and then increases with respect to V_{GS}. This behavior of η has effects at circuit level which we will elaborate in the next chapter.

To further develop our understanding of such distinct characteristics of FEFINFETs/FEFETs, we examine their circuit implications next.

Chapter 4

Analysis of FEFINFET and FEFET Circuits

4.1 Introduction

In this chapter, we analyze the characteristics of FEFINFET/FEFET- based inverter and 7 stage ring oscillators based on our understanding of the corresponding device characteristics. We perform detailed DC and transient analysis in order to understand the behavior of these FEFINFET/FEFET-based circuits. Firstly, for FEFINFET/FEFET-based inverter, we perform a DC analysis and our focus is on understanding the impact of the unconventional effects observed in FEFINFET/FEFET (such as NDR and non-saturation) on the voltage transfer characteristics (VTC) of these inverters. Next, we analyze a 7- stage ring-oscillator (RO) and we use transient analysis to explain the energy-delay characteristics of FEFINFET-based circuits. The contributions of this chapter are summarized at the end.

4.2 FEFINFET Inverter

Figure 4.1 compares the VTC of an FINFET based inverter with the FEFINFET based inverter at different values of T_{FE}. It is evident that due to the voltage amplification provided by the FE layer, the switching characteristics of the FEFINFET inverter become sharper i.e the gain in the transition region increases. Moreover, as T_{FE} increases, the voltage enhancement provided by the FE increases, as a result of which VTCs approach ideal characteristics. A new aspect that we can observe in Figure 4.1 is that at T_{FE} = 6nm, there is hysteresis in the inverter VTC, even though the corresponding device characteristics (Figure 3.3) were non-hysteretic. The hysteretic circuit response can be associated with the occurrence of NDR in the output characteristics (Chapter 3). To substantiate this claim, we perform the load line analysis of the FEFINFET inverter for input voltage (V_{in}) = $V_{DD}/2$ = 0.3 V at T_{FE} = 5nm (Figure 4.2 (a)) and T_{FE} = 6nm (Figure 4.2 (b)). The different points of intersection of the two load lines are also translated to the Inverter VTC (Figure 4.1). From these plots, we observe that,

- At T_{FE} = 6nm when V_{in} is reduced from V_{DD} to 0, (i.e. the output voltage (V_{out}) increases from 0 to V_{DD}), the operating point is A. However, when V_{in} increases from 0 to V_{DD} (or V_{out} decreases from V_{DD} to 0), the operating point is B. (Figure 4.2 (b)). Thus, due to two different operating points at $V_{in} = V_{DD}/2$, we observe a hysteresis in the VTC at T_{FE} = 6nm as shown in

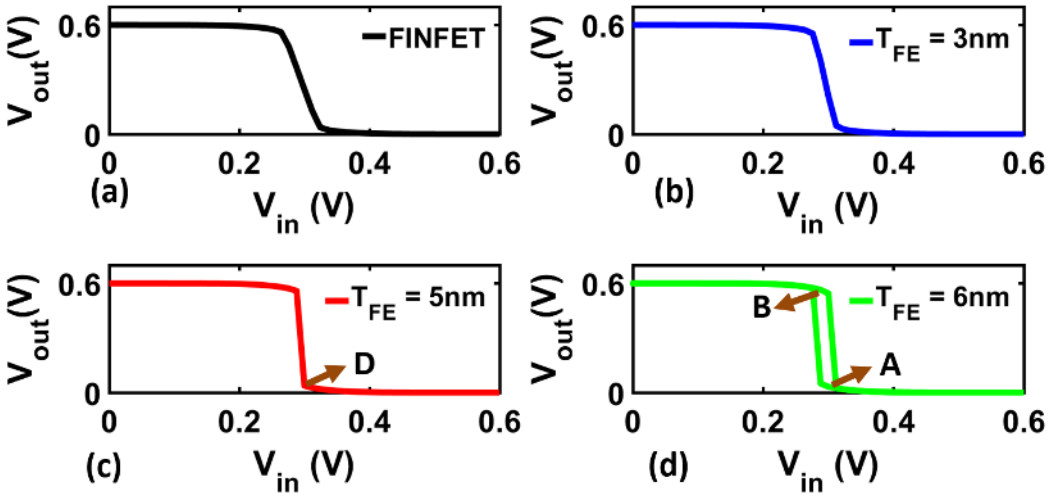

Figure 4.1 Voltage transfer characteristics of inverter for (a) FINFET and FEFINFETs at (b) T_{FE} = 3 nm (c) T_{FE} = 5 nm (d) T_{FE} = 6 nm showing hysteresis.

Figure 4.1. This hysteresis in VTC leads to higher noise margins and hence better noise immunity, similar to a Schmitt trigger [19].

- However, performing a similar analysis at T_{FE} = 5nm, we obtain only one point of intersection (D in Figure 4.2 (a)) despite the occurrence of NDR in the output characteristics (Figure 4.2 (a)). Therefore, no hysteresis is observed in the VTC.

Therefore, we conclude that NDR may lead to hysteresis but it is not a sufficient condition for the same.

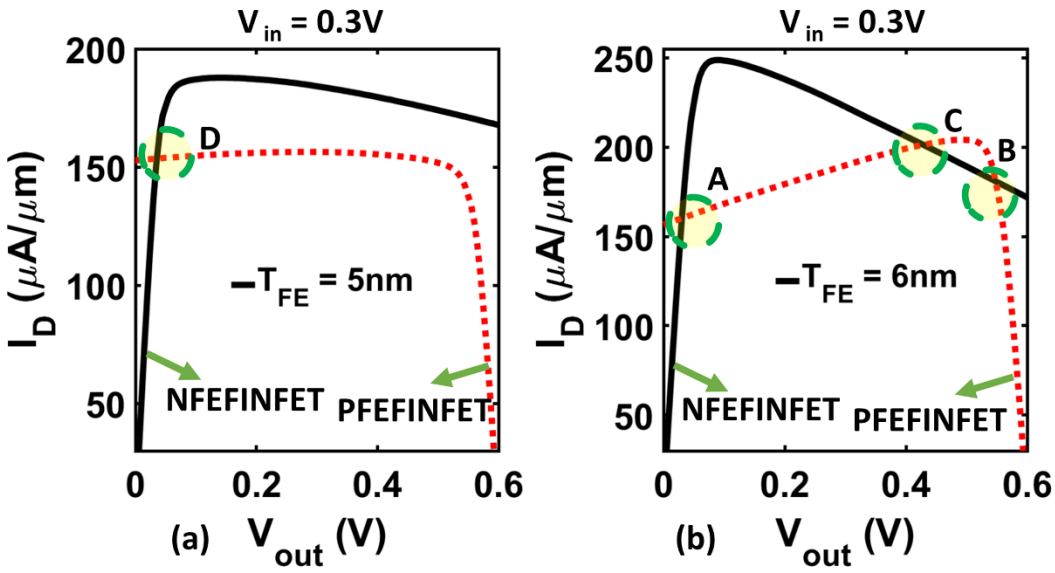

Figure 4.2 Loadline analysis of FEFINFET inverter for (a) T_{FE} = 5nm with one operating point D (b) T_{FE} = 6nm with two operating points A and B.

4.3 FEFET Inverter

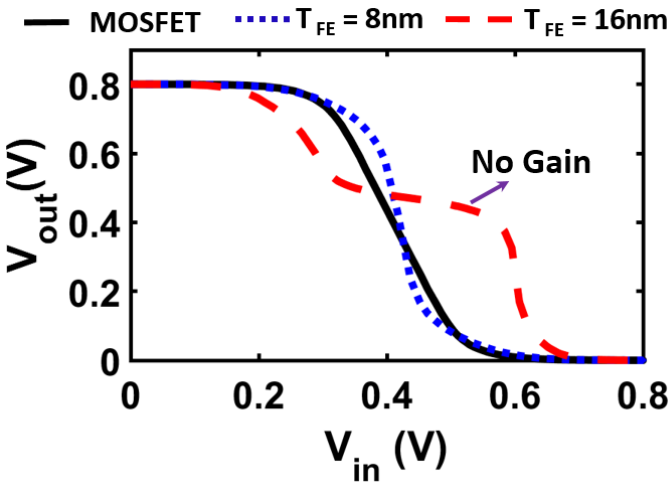

Figure 4.3 Voltage transfer characteristics of FEFET inverter for different values of T_{FE}. No gain in the VTC is observed at T_{FE} = 16nm.

Let us now discuss the effect of non-saturation in the output characteristics of FEFETs (observed for FEFETs at T_{FE} > 16nm) on the inverter VTC. From Figure 4.3, we observe that there is no gain in the voltage transition region due to non-saturation and therefore, FEFET-based inverter fails to work as a binary logic gate. Thus, optimization of T_{FE} must be performed to ensure that the transistor shows saturation in the output characteristics at V_{GS}~V_{DD}/2 and V_{DS}~V_{DD}/2 to obtain regenerative action in the logic gates.

Before we conclude this sub-section, let us summarize the differences between FEFETs and FEFINFETs. As discussed before in chapter 3, we observe that the benefits obtained from FEFETs are at higher T_{FE} values as compare to FEFINFETs due to the differences in the capacitance per unit area of the underlying FETs. Furthermore, no saturation is observed in the output characteristics of FEFETs for large T_{FE} values whereas FEFINFETs exhibit saturation at the entire range of T_{FE} considered due to lower sensitivity of V_{DSAT} on V_{IS} in FEFINFETs. However, at low V_{GS}, NDR is observed in FEFINFETs. Consequently, an inverter based on FEFINFET may show hysteresis whereas an FEFET inverter may fail to show the gain in the voltage transfer characteristics at large T_{FE}.

Next, we expand our grasp on the capabilities of FEFINFET to work as a logic device and gain more insights about the energy delay characteristics of FEFINFETs circuits by performing the ring oscillator analysis.

4.4 FEFINFET Ring Oscillator

In this section, we analyze a 7-stage inverter based ring oscillator to discuss the transient characteristics of FEFINFETs. Figure 4.4 (a-c) compare the delay and energy for FEFINFET and FINFET based ring oscillators. It can be observed that FEFINFETs show reduction in delay,

leakage energy and total energy for V_{DD} < 0.25 V. However, for super-threshold voltages, all the three metrics are degraded with respect to FINFETs. The energy-delay plots (Figure 4.4 (d)) also show a cross-over point. In addition, we report an atypical behavior of FEFINFET-based circuits in this research work. As can be observed in Figure 4.4 (a), the plot for T_{FE}=5nm shows an increase in delay with increasing V_{DD} in the super-threshold region.

To explain all these trends, including the atypical behavior, we consider an equivalent circuit of two contiguous FEFINFET based inverters in a ring oscillator as illustrated in Figure 4.5. (Note, the results shown in Figure 4.4 - 4.8 have been obtained using proper simulations. The simple equivalent circuit is considered only to explain the trends). The gate stack of the FEFINFETs are modeled as resistance R_{FE} in series with the capacitance $|C_{FE}|C_{GI}/(|C_{FE}|-C_{GI}) = \eta C_{GI}$ (see chapter 2). R_{FE} $(=\rho\ T_{FE}/A_{FE})$ models the $\rho dP/dt$ term in (2.1), as explained in chapter 2. In Figure 4.5, we consider $C_{GI}=C_{GPI}$ for p-FEFINFETs and $C_{GI} = C_{GNI}$ for n-FEFINFETs. The driving strength of the transistors is modeled as R_{PI}/η_R and R_{NI}/η_R for p- and n-FEFINFETs, respectively. Here, R_{PI} and R_{NI} are the resistances of the underlying transistors (i.e. without considering the FE); and η_R is the factor by which the current increases in FEFINFETs due to the negative FE capacitance. Note, η_R depends on (i) η and η_D which determine V_{IS} (as per equation (2.2)) and (ii) the region of operation of the FET. Specifically, for $V_{IS} < V_{TH}$, $\eta_R > \eta$ since the current is exponentially dependent on voltage step-up provided by the negative capacitance. On the other hand, for $V_{IS} > V_{TH}$, η_R is comparable to η since the current is only sub-quadratically dependent on $(V_{IS}-V_{TH})$. Moreover, the effect of η_D further reduces η_R, which has a more pronounced effect at high voltages. We also consider the effect of wire capacitance C_W and fan-out, FO. Our simulations not only treat the effect of wire capacitance as an additional load due to interconnects but also account for the self-consistent interaction of FE capacitance, C_{GSI}, C_{GDI} and C_W. Both these effects impact the transient evolution of P and V_I during the circuit operation. Now, employing Elmore's delay model on the circuit in Figure 4.5, the time constants associated with the low-to-high and high-to-low transitions (τ_{LH} and τ_{HL}) are obtained as

$$\tau_{LH} = FO.\frac{\eta}{\eta_R}R_{PI}(C_{GPI} + C_{GNI}) + \eta R_{FE}(C_{GPI} + C_{GNI}) + \frac{1}{\eta_R}R_{PI}C_W \quad (4.1.1)$$

$$\tau_{HL} = FO.\frac{\eta}{\eta_R}R_{NI}(C_{GPI} + C_{GNI}) + \eta R_{FE}(C_{GPI} + C_{GNI}) + \frac{1}{\eta_R}R_{NI}C_W \quad (4.1.2)$$

Also, since in case of FINFETs, $R_{FE} = 0$, $\eta = \eta_R = 1$ and therefore, equation (4.1) will get changed to equation (4.2) as

$$\tau_{LH} = FO.R_{PI}(C_{GPI} + C_{GNI}) + R_{PI}C_W \quad (4.2.1)$$

$$\tau_{HL} = FO.R_{NI}(C_{GPI} + C_{GNI} + R_{NI}C_W \quad (4.2.2)$$

From the equations above, we make the observations outlined below. For the time being, the wire capacitance is neglected in order to simplify the discussion. We will discuss its impact subsequently.

- At high V_{DD}, $R_{NI}/\eta_R < R_{FE}$ and $R_{PI}/\eta_R < R_{FE}$ i.e. the inherent speed of the driving transistor is greater than the time constants associated with polarization transients. Thus, the second term in (4.1) dominates. As a result, the benefit of FEFINFETs in terms of higher ON current is offset by the extra resistance introduced by the FE layer, leading to lower circuit speed compared to FINFETs. As T_{FE} increases, R_{FE} $(=\rho T_{FE}/A_{FE})$ increases, yielding larger delay.

- As V_{DD} is scaled to sub/near-threshold values, R_{NI}/η_R and R_{PI}/η_R begin to dominate R_{FE}, as a result of which the first term in (4.1) starts to play a key role. Now, in the sub-threshold region, $\eta_R/\eta > 1$, as discuss before. This yields superior performance in FEFINFET-based circuits. Our results show similar η_R and hence, similar delay for T_{FE} = 3nm and 5nm. This is because increasing T_{FE} not only boosts $\int_0^{V_{GS}} \eta \, dV_{GS}$ term in (2.3) but also increases $\int_0^{V_{DS}} \eta_D \, dV_{DS}$, yielding similar V_{IS}. This leads to a mild dependence of ON current on T_{FE}.

- To understand the atypical behavior of increasing delay with increasing V_{DD} in the super-threshold region, we need to examine the V_{DD} dependence of different terms (especially the dominant second term) in (4.1). Since R_{FE} dominates R_{NI} and R_{PI}, the reduction in delay that one expects typically with increasing V_{DD} (due to reduction in the inherent delay of the transistor) is nullified. On the contrary, η increases as V_{GS} (or V_{DD}) increases, as discussed before (see Figure 3.7 (b)). This results in an increase in delay with V_{DD}. Note, this effect is observed when R_{FE} is large (and therefore, more dominant compared to the transistor's inherent resistance). This explains why the atypical behavior is observed at larger T_{FE}.

Next, we discuss the comparison of energy consumption of FEFINFETs and FINFETs. Leakage energy (V_{DD}*I_{OFF}*Delay) primarily follows the trends of the delay and therefore shows an increase in FEFINFETs compared to FINFETs at high V_{DD}, but a decrease at low V_{DD}. The dynamic energy is higher in FEFINFETs due to increase in the gate capacitance. The total energy is higher in FEFINFETs at high V_{DD} due to the dominance of the dynamic energy. As V_{DD} is lowered, leakage energy begins to increase its contribution, thereby reducing the total energy in FEFINFETs compared to FINFETs. As a result of all these factors, FEFINFETs show ~25% lower energy at iso delay at V_{DD}<0.25V (Figure 4.4(d)). Also, ρ is the time constant associated with the change in FE polarization. It determines the delay in switching of the polarization of an FE layer once the electric field has been applied. This delay is actually the time it takes for the polarization to switch from a positive extreme value to a negative extreme value or vice versa. In this research work, this delay is approximately 1ns. Now, in FEFET based circuits, the polarization range is limited around the origin, that is, in the negative capacitance ($C_{FE} < 0$) region where the slope of P-E curve is negative. Since, the entire polarization range is not being considered while designing FEFET based circuits for logic and memories, therefore, the circuit delay is approximately 100 ps or lesser than the inherent delay of the FE layer.

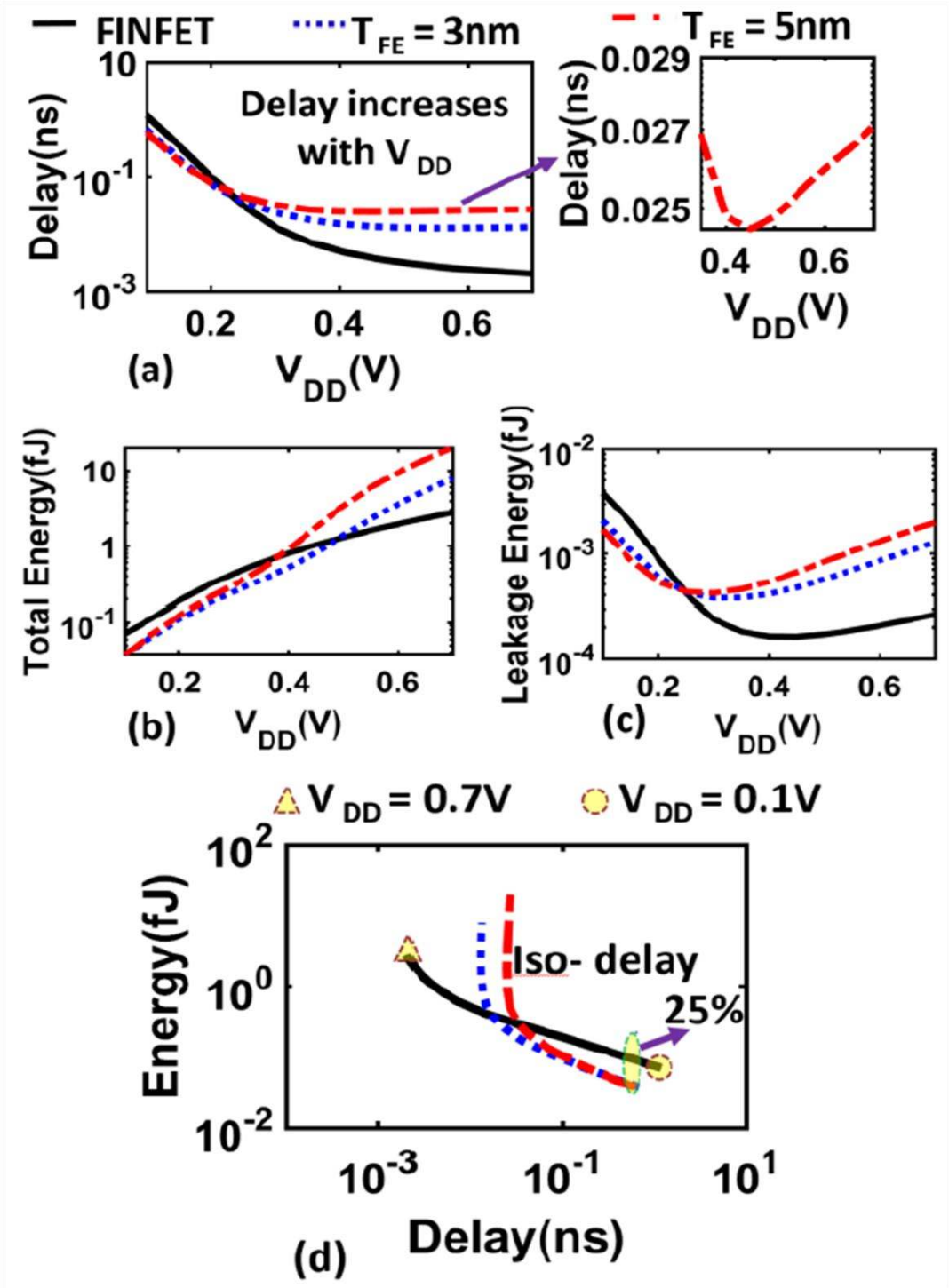

Figure 4.4 (a) Delay–V_{DD} plots illustrating the increase in delay w.r.t. to V_{DD} for higher values of V_{DD}. (b) Total energy–V_{DD} plots. (c) Leakage energy–V_{DD} plots. (d) Energy–delay plots showing reduction in energy at iso-delay of an inverter stage in the seven-stage RO circuits for different values of T_{FE} at C_W = 0 fF, ρ = 0.05 Ω m and FO = 4.

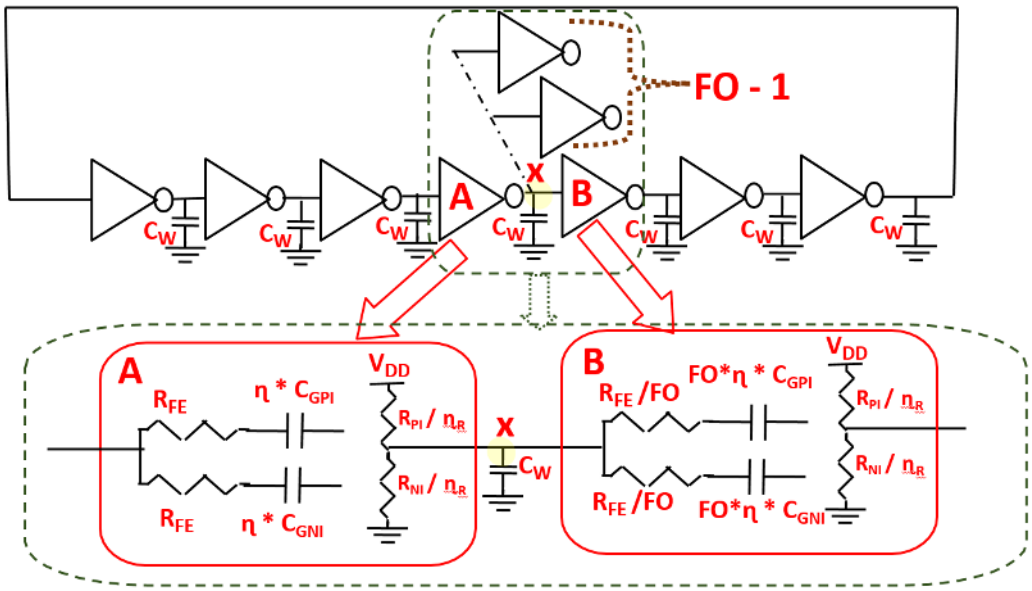

Figure 4.5 The equivalent RC circuit of two adjacent FEFINFET based inverters in a ring oscillator

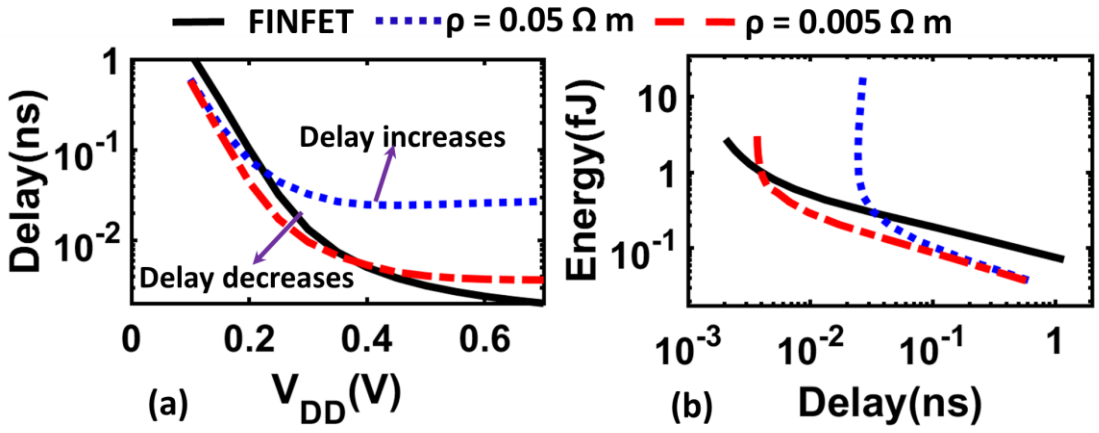

Figure 4.6 (a) Delay–V_{DD} plots showing increase in delay w.r.t. to V_{DD} for higher value of ρ. (b) Energy–delay plots of an inverter stage in the seven stage RO circuits for different values of ρ at C_W = 0 fF, T_{FE} = 5 nm and FO = 4.

4.4.1 Impact of kinetic coefficient of FE (ρ)

To analyze these trends further, we compare the energy-delay trends at different ρ (Figure 4.6). As expected, lower ρ enhances the benefits of FEFINFETs to a larger range of V_{DD} due to the reduction in R_{FE}. Therefore, material optimization and device design for non-hysteretic steep switching

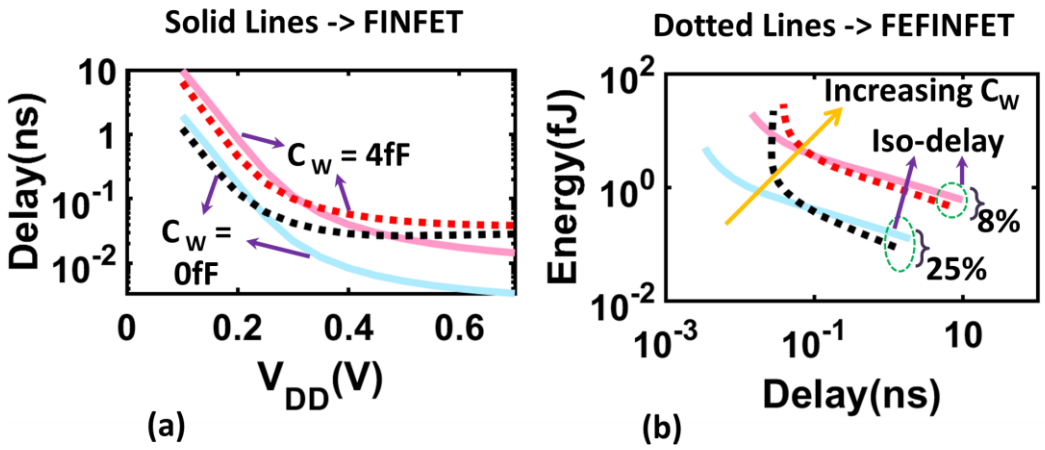

Figure 4.7 (a) Delay- V_{DD} Plots and (b) Energy-Delay Plots showing reduction in energy at iso-delay of an inverter stage in the seven-stage RO circuits for C_W = 0 and 4 fF at ρ = 0.05 Ω m, T_{FE} = 5 nm and FO = 4.

operation of FEFINFETs should target the minimization of polarization lag in ferroelectrics with respect to the applied electric field. Moreover, FEFINFETs no longer exhibit anomalous behavior with respect to V_{DD} scaling at lower ρ. This is due to the fact the second term in (4.1) does not remain as dominant anymore.

4.4.2 Wire Capacitance Sweeps

Now, we consider the effects of C_W. It is easy to deduce that the inclusion of the third term in (4.1) mitigates the loss in performance of FEFINFETs compared to FINFETs at high V_{DD}. This is because FEFINFETs have a better strength (lower resistance) to drive C_W. However, at the same

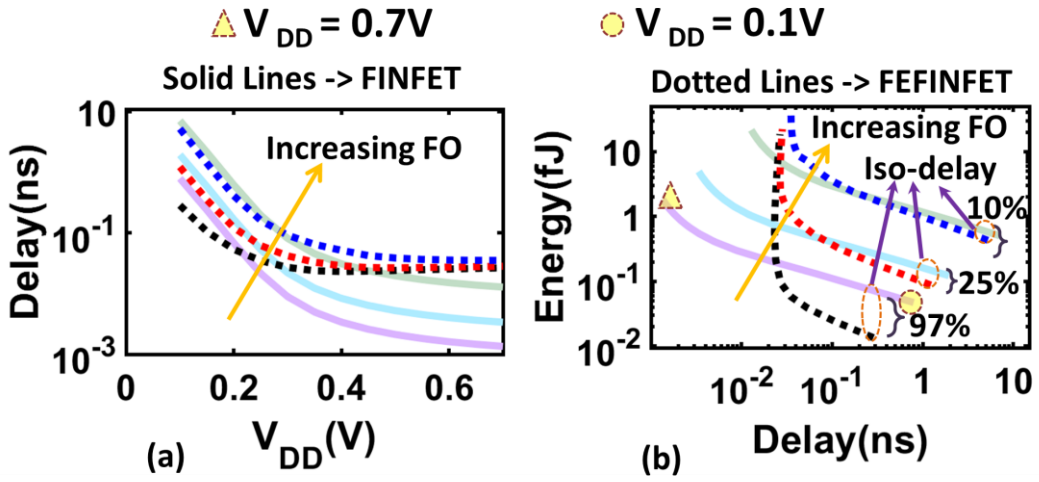

Figure 4.8 (a) Delay-V_{DD} plots and (b) Energy–delay plots of an inverter stage in the seven-stage RO circuits for FO = 1, 4, and 16 at C_W = 0 fF, T_{FE} = 5 nm and ρ = 0.05 Ω m.

time, the dynamic energy increases with increasing C_W, enhancing its contribution to the total energy. This reduction in the ratio of leakage to dynamic energy dwindles the energy benefits of FEFINFETs at low V_{DD} as C_W increases. As an example, (Figure 4.7), at C_W=4fF, FEFINFETs exhibit 8% reduction in energy at iso-delay in the sub-threshold region, as opposed to 25% energy reduction for $C_W = 0$. Another effect of increasing C_W is that the atypical behavior of FEFINFETs at high V_{DD} is not observed for sufficiently large C_W. This is because the third term in (4.1) starts to become comparable to the second term. This re-instates the decrease in delay due to reduction in R_{NI} and R_{PI} with increasing V_{DD}.

4.4.3 Fan Out Sweeps

Additionally, increasing the fan-out decreases the benefits of FEFINFETs as shown in the Figure 4.8. This is because as FO increases, the contribution of the dynamic energy component in the total energy increases. Since FEFINFETs exhibit larger dynamic energy compared to the standard FETs (due to higher gate capacitance), the energy benefits of FEFINFET (observed at lower V_{DD}) drops. At FO=16, FEFINFETs exhibit 10% reduction in energy at iso-delay in the sub-threshold region, as opposed to 25% energy reduction for FO = 4 and 97% energy reduction at FO = 1.

4.5 Summary

Following are the contributions of this chapter

- We show that the negative NDR may yield hysteretic voltage transfer characteristics of the logic gates yielding higher noise margins.
- We also discuss that if the underlying transistor shows a strong dependence of the saturation drain voltage on the gate voltage, the corresponding FEFET may fail to exhibit saturation in the output characteristics, leading to the loss in gain of the voltage transfer characteristics.
- Our analysis shows that at high V_{DD} and high T_{FE}, ferroelectric transistors have degraded performance and may even show an increase in delay with increasing V_{DD}. However, FEFINFETs show a significant promise for low V_{DD} operation, yielding 8% - 25% higher energy efficiency at iso-delay compared to standard transistors.
- Our analysis establishes that the lower ρ enhances the benefits of FEFINFETs to a larger range of V_{DD} due to the reduction in R_{FE}. Additionally, FEFINFETs no longer exhibit anomalous behavior with respect to V_{DD} scaling at lower ρ.
- From our analysis, we conclude that circuits based on FEFINFETs are more energy efficient at lower voltages compared to FINFET circuits.

Chapter 5

Design of FEFINFET SRAM

5.1 Introduction

In this chapter, we analyze FEFINFET based SRAM extensively. First, we give a brief overview of the standard (6T) SRAM bit cell, its operation and its various characteristics. Then we discuss in detail the FEFINFET based 6T SRAMs. We explain the effects of ferroelectric thickness on SRAM stability and latency. We summarize the contributions of this chapter at the end.

5.2 Fundamentals of SRAM

Static Random-Access Memories (SRAMs) are widely used in electronics industry as a cache memory in state of the art systems [22]. They are examples of volatile memories because they cannot hold the data if the power supply is removed. In addition, they are random-access memories because they have same read/write latencies for different address locations [22]. Also, since the data stored in an SRAM cell is retained indefinitely without the requirement of refresh option, provided that the power supply is on, therefore, it is called a static memory. Furthermore, SRAMs have higher cost because of their faster speed [23]. SRAM mostly consists of an array of memory cells and the peripheral circuitry (row decoders, column decoders, drivers etc.) [23]. In, this work, our focus is on the 6T SRAM cell which is explained next.

A conventional SRAM is a type of semiconductor memory that utilizes a bi stable latching circuit with two stable operating points to store data as depicted in Figure 5.1. This bi stable circuit makes a 6T SRAM very stable and thus increases its noise immunity [22]. Now, the data being saved in the memory cell is interpreted either as logic 0 or as a logic 1, based on the stored state of the two-inverter latch circuit. Additionally, to read the data stored in the memory cell or to write data into the memory cell, we use two bit lines – BL and BLB (Figure 5.1). In addition, we need two access transistors as well to connect/disconnect the bit lines to the bi-stable circuit. These access transistors are controlled by the word line (WL) as shown in Figure 5.1. It is very easy to deduce that there are 6 transistors in total are being used in SRAM bit cell and hence the name is 6T- SRAM. The schematic of a 6T SRAM cell is shown in Figure 5.2. In Figure 5.2, WL is the word line, Q is the data stored and QB is the complement of the stored data. BL is the bit line and BLB is the complement of the bit line. V_{DD} is the maximum supply voltage. Now, the read and write operations of the SRAM are explained as follows-

- **Read Operation:** Let us assume that the voltage at node QB, V_{QB} = 0 and at node Q, V_Q = V_{DD}. For the read operation, BL and BLB are first pre- charged to V_{DD} and then WL is set to V_{DD}. From the SRAM circuit configuration during the read shown in Figure 5.3, we observe that access transistors A1, A2 are turned on, pull down transistor N2 is turned on and so is pull up transistor P1. Due to the read current I_R, flowing through A2 and N2, voltage at node QB, V_{QB} starts to rise and the BLB starts to discharge as shown in Figure 5.5 (a). The differences in the voltages of BL and BLB are then sensed after amplification through a sense amplifier to obtain the value stored in the SRAM cell. The rise in voltage value at the node QB, V_{READ}, depends on the relative driving strengths of A2 and N2. In order to ensure that a read is stable, V_{READ} should not become greater than the V_M (logic threshold voltage) of the inverter formed by N1 and P1. Therefore, to increase the read

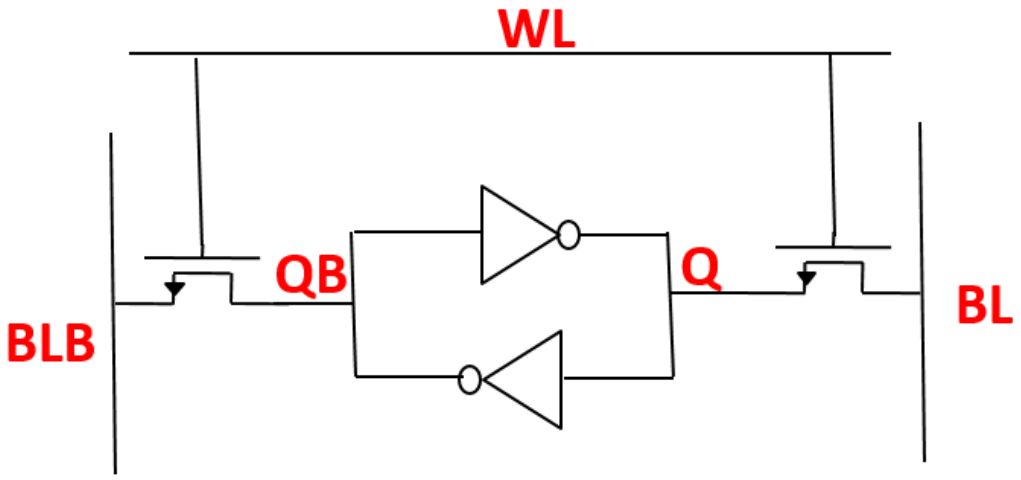

Figure 5.1 Gate level view of 6T SRAM cell.

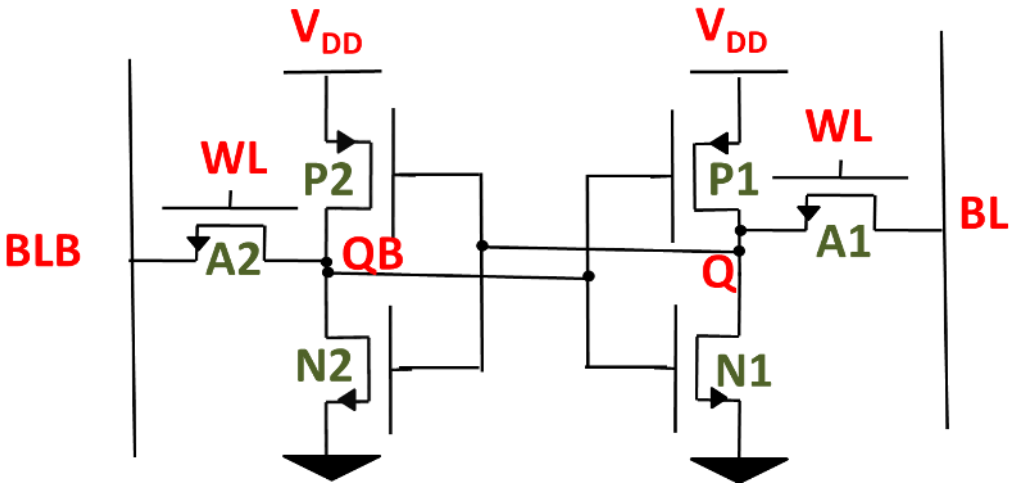

Figure 5.2 Schematic representation of 6T SRAM cell.

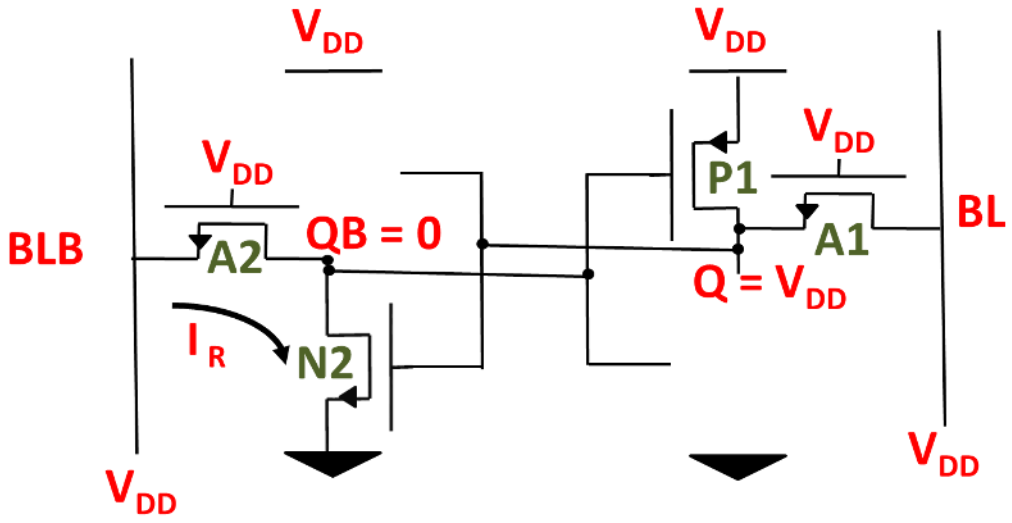

Figure 5.3 SRAM cell during read mode.

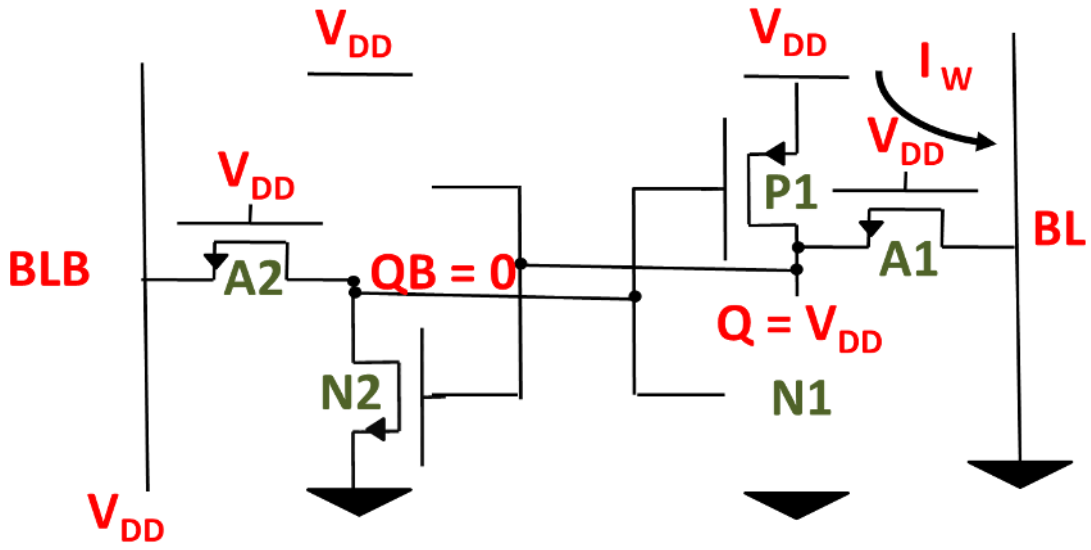

Figure 5.4 SRAM cell during write mode.

stability of the SRAM cell, the driving strength of the pull-down transistors should be greater than the access transistors [23].

- **Write Operation:** Similarly, during the write operation, let us assume that we want to write data = 0, that is, V_{QB} should go to V_{DD} and V_Q to 0. For the write operation, BLB is driven to V_{DD}, BL is driven to 0 and the WL is asserted. As shown in Figure 5.4, during this operation, I_W flows through the pull up transistor P1 and the access transistor A1,

resulting in a discharge at node Q from its initial value of V_{DD} to V_{WRITE}. If V_{WRITE} is smaller than the V_M of the inverter formed by N2 and P2, then 0 will get stored in the SRAM cell. To increase the write ability of the SRAM cell the driving strength of the access transistor should be more than the driving strength of the pull up transistor. The write transient operation of an SRAM cell is shown in Figure 5.5(b) [23].

From the above description of read and write operations, it is important to note that SRAM has conflicting design requirements to achieve read stability and write ability simultaneously. In order to have higher read stability, driving strength of the access transistor should be less whereas for higher write ability, the corresponding driving strength should be high [23]. For a FINFET based SRAM, let us assume, that the number of fins in the pull down, pull up and access transistors are N_{PD}, N_{PU} and N_{AC} respectively. As discussed before, for higher read stability, $N_{PD} > N_{AC}$ and for higher write ability, $N_{PU} < N_{AC}$. In order to fulfill this design requirement, one design option is to have $N_{AC} = 1$, $N_{PU} = 1$ and $N_{PD} = 2$ so as to achieve both read stability and write ability at once [23]. Additionally, the optimum value of supply voltage being used in this research work for SRAM cell operation is 0.5V throughout [23]. Furthermore, there are following 4 metrics which are used to characterize a 6T SRAM [23]:

- **Access Time**: Access time or read time is defined as the amount of time it takes for the bit-line to discharge to certain voltage level that can be sensed by a sense amplifier once the word lines are asserted [23].

- **Write Time**: Write time is the amount of time it takes to write the SRAM cell or the time taken to flip the values of Q and QB after the word lines are asserted [23].

- **Hold SNM:** The hold SNM (Static Noise Margin) is used to quantify the hold stability of an SRAM cell [24]. Hold SNM measures the ability of an SRAM cell to retain the data when the cross-coupled inverters are disconnected from the bit-lines and an external DC noise is applied. The hold SNM can be found graphically from the butterfly curve. It is defined as the side of the largest square that can be fit in the lobes in the butterfly curve [22]. If the inverters are exactly identical, then this butterfly curve is symmetric However, if the inverters are not identical due to variations [21], then the SNM is determined by the smaller lobe in the butterfly curve. [22].

- **Read SNM:** An SRAM cell should have two stable states during the read operation. The read SNM measures how much external DC noise can be applied to the inputs of the two cross - coupled inverters before a stable state is lost during the read operation [22]. Read SNM is determined graphically from the read butterfly curve in the same way as hold SNM is calculated form the hold butterfly curve. Moreover, hold SNM is always greater than the read SNM [23].

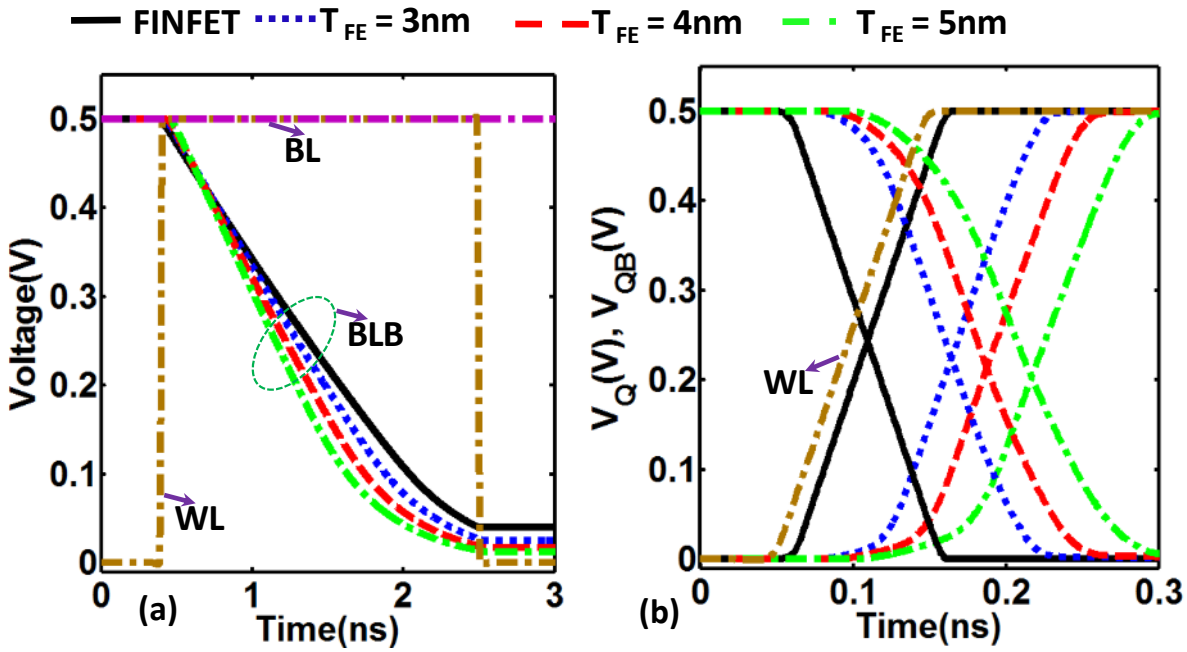

Figure 5.5 Transient waveforms of SRAM based on FINFET and FEFINFET for different values of T_{FE} during (a) read and (b) write.

In this work, we compare the above discussed 4 metrics - the access time (read time), write time, hold SNM and read SNM of the FEFINFET based SRAM with the FINFET based SRAM cell for different values of T_{FE}. We also analyze the impact of kinetic coefficient of FE (ρ) on the read and write operations of SRAM. We employ the same simulation methodology and FEFINFET device modelling as discussed in chapter 2. An important point to be noted is that at higher T_{FE} values, hysteretic Inverter VTC are observed as discussed in chapter 4. However, design of FEFINFET SRAM at such higher thickness value requires additional treatment and is beyond the scope of this work.

5.3 Comparison of FEFINFET SRAM and FINFET SRAM Characteristics

5.3.1 Access Time

The access time or read time of an FEFINFET SRAM is lesser as compared to the FINFET SRAM (Figure 5.5 – Figure 5.7). Additionally, with increase in T_{FE} values at a fixed value of ρ, access time decreases further as shown in Figure 5.5. FEFINFET based SRAM shows 1%-9% decrease in read time as compared to FINFET based SRAM. This can be attributed to the increase in the I_{ON} of an FEFINFET device as T_{FE} is increased due to increase in the amplification factor (η) provided by the negative capacitance. This has been discussed in detail in chapter 2. A higher I_{ON} helps in the faster discharge of the bit lines and thus, aids in lowering down the access time of a 6T SRAM cell. Moreover, if at a fixed value of T_{FE}, ρ is decreased, then also the access time shows

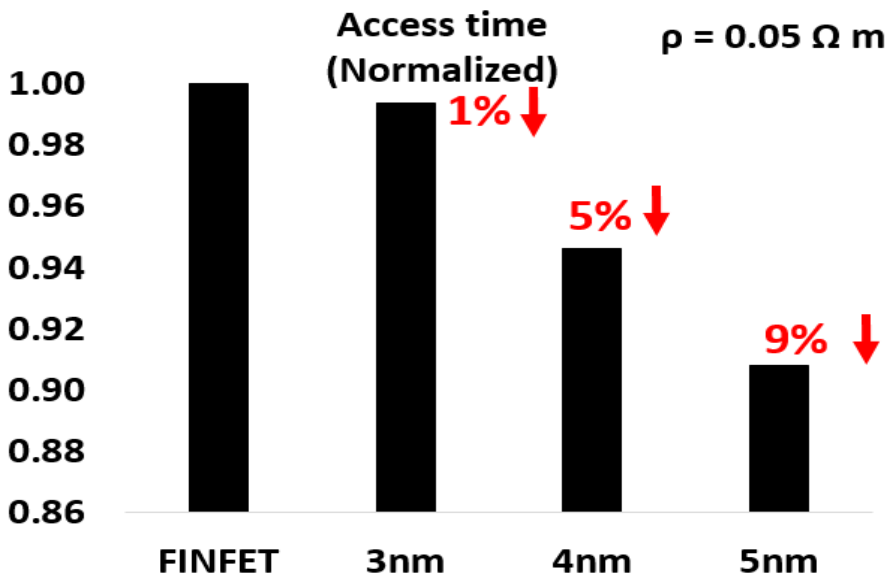

Figure 5.6 At ρ = 0.05 Ω m, a comparison of access time of SRAM based on FINFET and FEFINFET for different value of T_{FE}

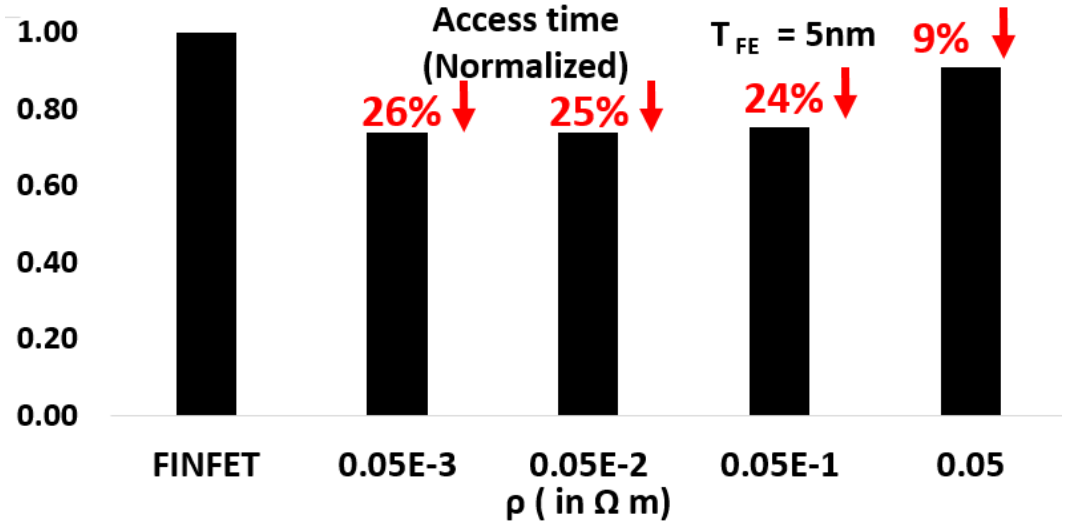

Figure 5.7 At T_{FE} = 5nm a comparison of access time of SRAM based on FINFET and FEFINFET for different values of ρ

a reduction of 26% as compared to FINFET based SRAM. This is because when ρ is decreased, FE polarization switching time of the FEFINFET device decreases and this accelerates the voltage enhancement action of FE layer. This leads to faster rise of the gate terminal voltage of the underlying transistor in an FEFINFET device, thereby, resulting in lower access time for lower values of ρ.

5.3.2 Write Time

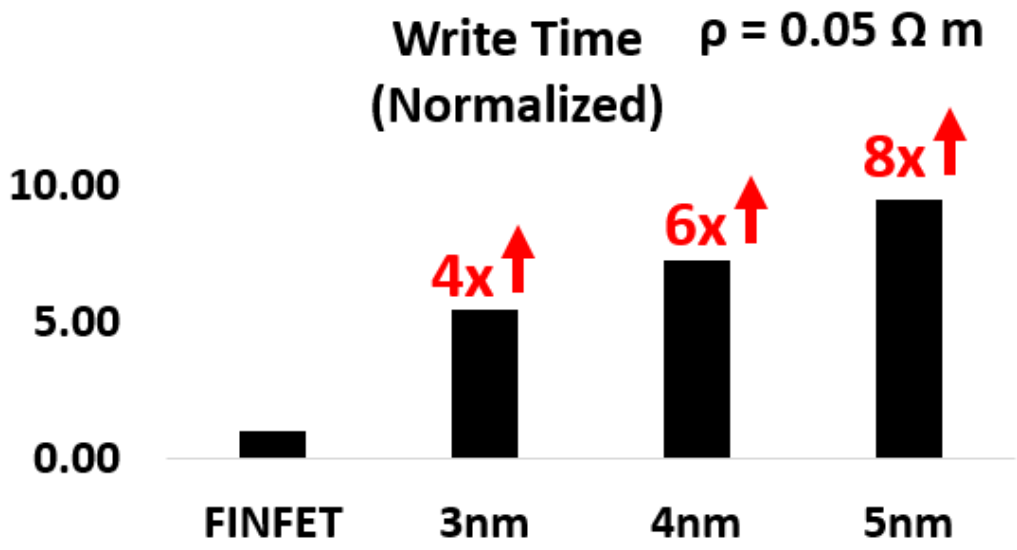

Figure 5.8 At ρ = 0.05 Ω m, a comparison of write time of SRAM based on FINFET and FEFINFET for different values of T_{FE}.

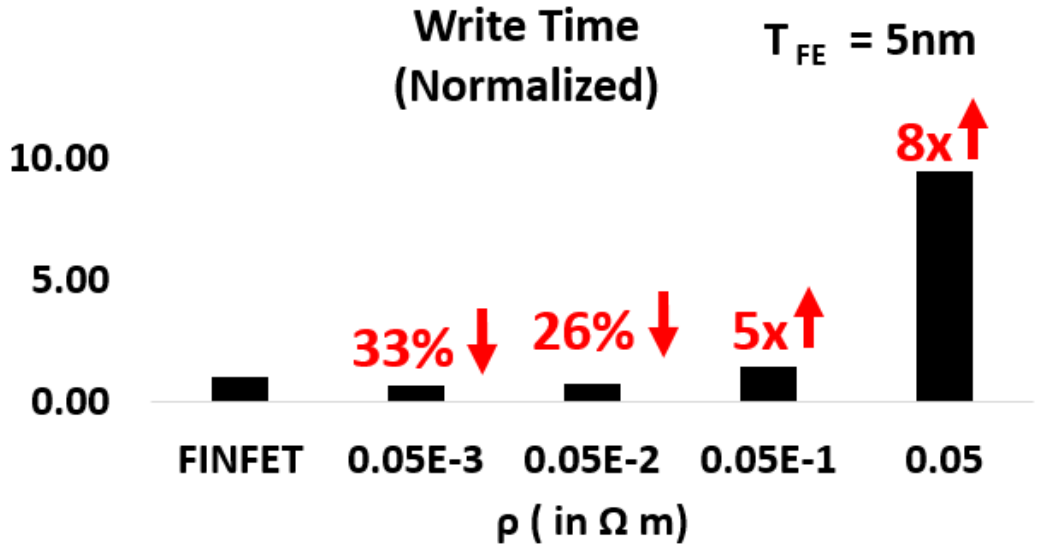

Figure 5.9 At T_{FE} = 5nm, a comparison of write time of SRAM based on FINFET and FEFINFET for different values of ρ.

As shown in Figure 5.8, FEFINFET based SRAMs exhibit higher write times as compared to the FINFET SRAMs. This is because of the higher gate capacitance of an FEFFINFET device as compared to FINFET. Write time of FEFINFET SRAM is approximately 8 times of the write time of FINFET SRAM at ρ = 0.05 Ω m and T_{FE} = 5nm. Additionally, as T_{FE} increases, write time increases further. However, if we decrease the value of ρ, then as explained previously, the

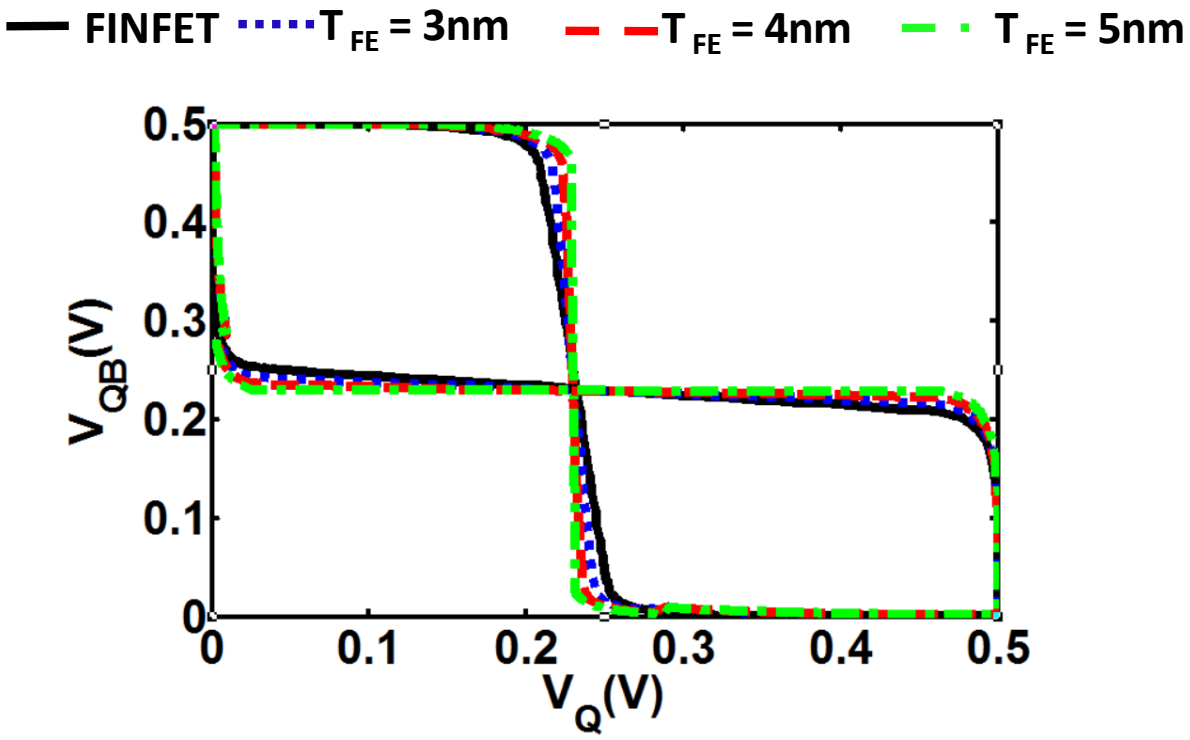

Figure 5.10 Butterfly curves to calculate Hold SNM of SRAM based on FINFET and FEFINFET for different values of T_{FE}.

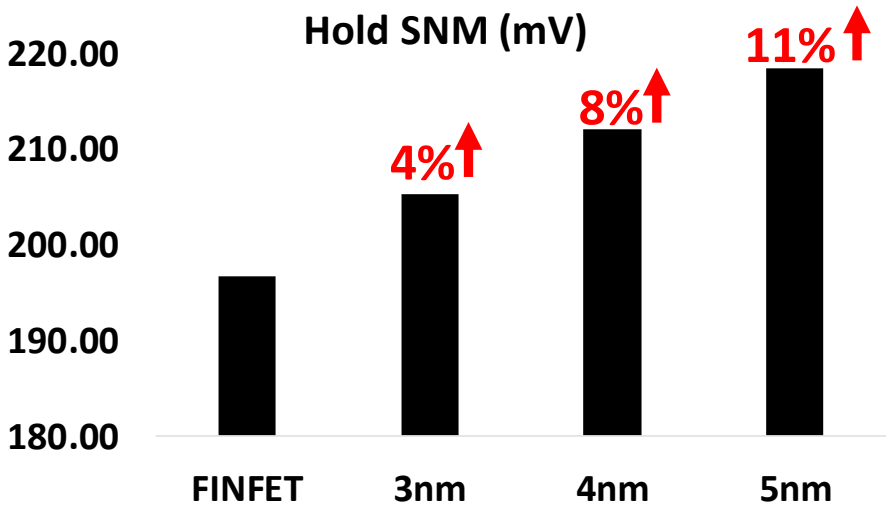

Figure 5.11 At ρ = 0.05 Ω m, a comparison of Hold SNM of SRAM based on FINFET and FEFINFET for different values of T_{FE}.

amplified voltage at the internal node FEFINFET (as explained in chapter 2) is obtained faster and hence results in lower write time. As shown in Figure 5.9, for ρ = 0.005 Ω m and T_{FE} = 5nm, write time for FEFINFET SRAM is 33% lower as compared to FINFET SRAM.

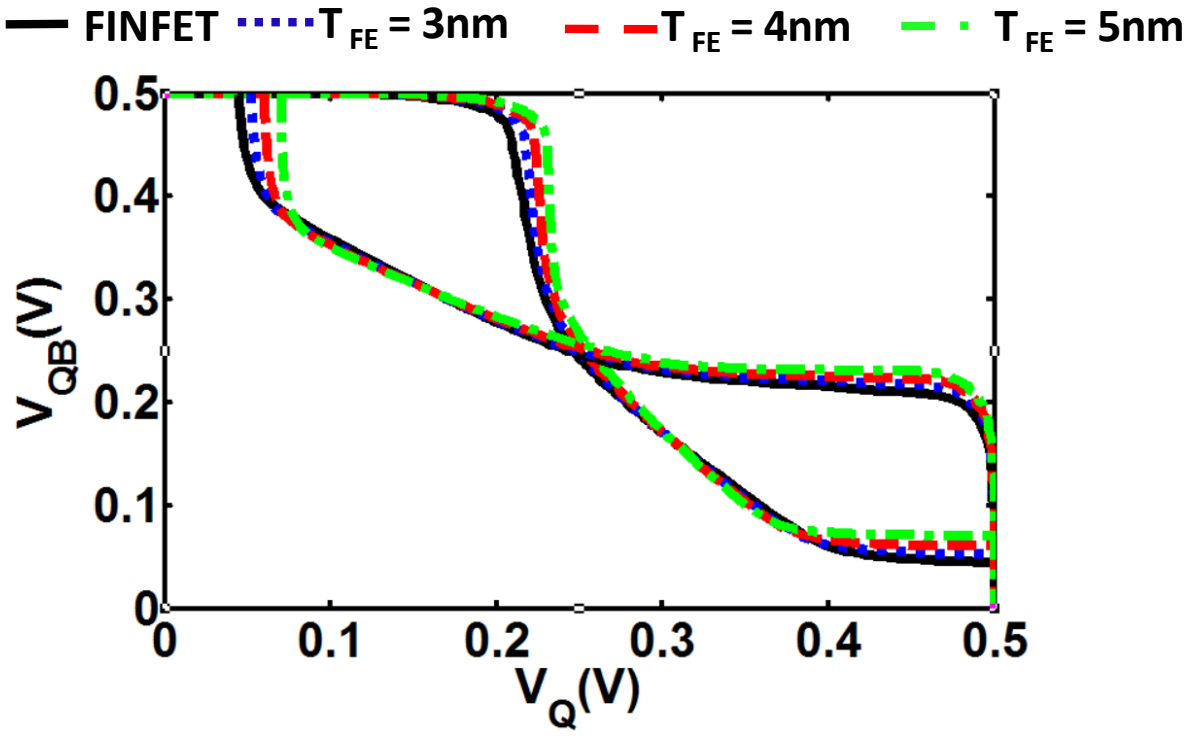

Figure 5.12 Butterfly curves to calculate Read SNM of SRAM based on FINFET and FEFINFET for different values of T_{FE}.

5.3.3 Hold SNM

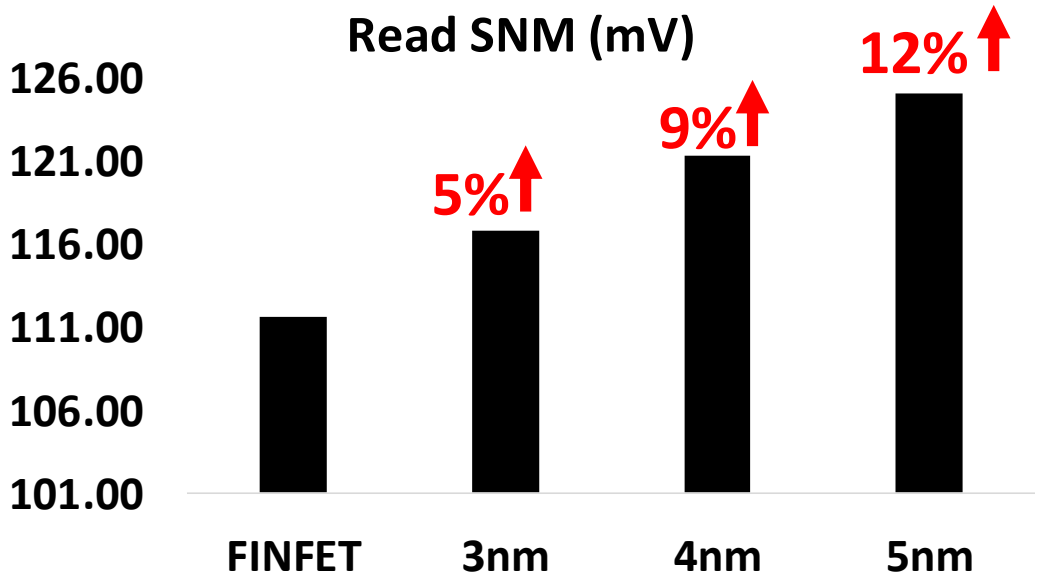

Figure 5.13 At ρ = 0.05 Ω m, a comparison of Read SNM of SRAM based on FINFET and FEFINFET for different values of T_{FE}.

Hold stability of an FEFINFET SRAM is more as compared to FINFET SRAM, because of higher ratio of I_{ON}/I_{OFF}. Additionally, as T_{FE} increases, hold stability increases further. This is shown in Figure 5.11. SRAMs based on FEFINFET exhibit 4% - 11% higher hold stabilities as compared to FINFET based SRAMs. Moreover, the parameter ρ has negligible effect on Hold SNM because hold stability analysis is done in quasi-DC conditions as explained in chapter 2.

5.3.4 Read SNM

Because of higher ratio of I_{ON}/I_{OFF}, read stability of an FEFINFET SRAM is more as compared to FINFET SRAM. Additionally, as T_{FE} increases, read stability increases further. FEFINFET based SRAMs exhibit 5% - 12% higher read stabilities as compared to SRAMs based on FINFET. This is shown in Figure 5.13. Moreover, the parameter ρ has negligible effect on read SNM as well because read stability analysis is done in quasi-DC conditions that are explained in chapter 2.

5.4 Summary

Following are the contributions of this chapter:

- Our analysis on 6T SRAMs shows that FEFINFET based SRAMs offer lower access time due to higher ON current and higher read stability and larger hold stability due to higher value I_{ON}/I_{OFF} ratio, enabling quicker discharging of the bit-lines and improved voltage retention. They show 5%–12% larger read stability and 9%–26% lower access time as compared to FINFET based SRAMs.
- However, FEFINFET SRAM exhibits write time penalty due to increased overall gate capacitance.
- We show that write time also reduces for FEFINFET SRAM as compared to FINFET SRAM if the kinetic coefficient (ρ) is lowered. This is attributed to the quicker turning ON of the FEFINFET transistors because of faster FE polarization switching at lower ρ.

Chapter 6

Conclusions and Future Work

In this research work, we extensively explored the effects of ferroelectric thickness and FE-drain coupling on the device-circuit characteristics of FEFINFET/FEFET by considering the operation of ferroelectric transistors only in the non-hysteric steep switching region. For the analysis of the circuits based on FEFINFETs/FEFETs, we investigated the characteristics of logic (inverter and ring oscillators) as well as memories (6T- SRAMs) based on these transistors. In this thesis work, we performed the extensive analysis of ferroelectric transistors by employing a novel equivalent circuit representation and simulation methodology for a ferroelectric transistor. Based on this original framework, we proposed that the voltage at the internal node of the underlying transistor (V_{IS}), depends not on the applied gate voltage (V_{GS}), but also on the drain terminal (equation (2.3)). We establish that for $V_{GS} = 0$ and $V_{DS} > 0$, we get $V_{IS} < 0$. Note that the effects of FE-drain coupling are captured by the term η_D.

Our device analysis showed the possibility of higher ON current and lower OFF current as well, especially at larger T_{FE}. Additionally, we pointed out at the occurrence of negative DIBL in the transfer characteristics and NDR in the output characteristics of FEFINFET/FEFET at high T_{FE}. These behaviors were attributed to the coupling of the drain capacitance with the FE capacitance. We also discussed that if the underlying transistor shows a strong dependence of the saturation drain voltage on the gate voltage, the corresponding FEFET device may fail to exhibit saturation in the output characteristics. Moreover, we showed that the equivalent gate capacitance of ferroelectric transistors is η times the equivalent gate capacitance of the conventional transistor. In addition, we explained that if $\alpha < 0$, $\beta > 0$ and $\gamma < 0$ (as is in this research work), then η shows a non - monotonic behavior with respect to V_{GS} (V_{DD}).

All these trends that we observed at device level, have implications on the FEFINFET/FEFET based circuits. We explained that due to the voltage enhancement provided by the FE, the FEFINFET inverter VTCs approach ideal characteristics. Also, we established that NDR may yield hysteretic voltage transfer characteristics of the logic gates yielding higher noise margins. Furthermore, we demonstrated that the non-saturation in the output characteristics leads to the loss in gain of the voltage transfer characteristics. Another noteworthy point we explained that to get a similar voltage amplification, larger T_{FE} is required for FEFETs as compared to FEFINFETs.

Our exploration also showed that at high V_{DD} and high T_{FE}, ferroelectric transistors may show an increase in delay with increasing V_{DD}. This is because of the dominant effect of the

transients associated with the switching of the FE polarization as well as because of the increase in η at high V_{DD} values. In addition, FEFINFETs exhibit similar delay at lower V_{DD} values for different T_{FE}. This we explained is because of weak dependence of ON current on T_{FE}. Additionally, our ring oscillator's energy-V_{DD} analysis showed that the leakage energy for FEFINFETs is higher as compared to FINFETs at high V_{DD}, but lesser at low V_{DD}, whereas, the dynamic energy is always higher in FEFINFETs due to increase in the gate capacitance. However, the total energy is higher in FEFINFETs at high V_{DD} due to the dominance of the dynamic energy. Additionally, we discussed that the advantages of FEFINFETs are obtained for a larger range of V_{DD} if ρ is lowered due to the reduction in R_{FE}. Moreover, we also conclude that as wire capacitance (C_W) and fanout (FO) are increased, the contribution of the dynamic energy component in the total energy increases which results in the dwindling of energy benefits of FEFINFET (observed at lower V_{DD}). Therefore, all in all, from our energy-delay trends of ring oscillator, we established that FEFINFETs show a significant promise for low V_{DD} operation, yielding 8% - 25% higher energy efficiency at iso-delay compared to standard transistors.

Furthermore, SRAMs based on FEFINFETs, show 5%–12% larger read stability and 9%–26% lower access time due to steep switching characteristics which results is faster discharge of bit lines and better voltage retention capabilities. However, FEFINFET SRAMs show an increase in the write time due to higher equivalent gate capacitance as compared to FINFET SRAMs. Moreover, our analysis showed that the write time penalty can be mitigated by lowering the kinetic coefficient (ρ). This is due to the faster turning ON of the FEFINFET transistors due to lower switching time of the FE polarization.

Based on this thesis work we conclude that ferroelectric transistors have huge potential to replace conventional transistors in design of circuits for low power domain. Nevertheless, as discussed, optimization of FE thickness is crucial for the design of circuits based on ferroelectric transistors. In sum, with a suitable FE thickness, ferroelectric transistors are a suitable candidate for low power design.

A future line of research could be the employment of write-assist techniques such as negative bit line and boosted word line to remove the write time penalty exhibited by FEFINFET SRAMs. In addition, FEFINFET SRAMs need to be analysed at those high T_{FE} values for which hysteretic inverter VTCs are obtained. Furthermore, another good scope of future work is to analyse the impact of static coefficients of FE – α, β, and γ on the logic design and SRAM characteristics. Moreover, analysis of other logic gates based on FEFINFETs should be explored. In sum, by utilizing the device – circuit co-design analysis presented in this work, the benefits of other circuits based on FEFINFETs need to be explored more exhaustively.

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