DEVICE MODELS, CIRCUIT SIMULATION, AND COMPUTER–CONTROLLED MEASUREMENTS FOR THE IGBT *

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Abstract – The implementation of the recently developed IGBT device model into a circuit simulation program is described. It is shown that the circuit simulation program rapidly and robustly simulates the dynamic behavior of the IGBT for general external drive, load, and feedback circuit configurations. The algorithms used to extract the IGBT device parameters from computer-controlled measurements are also described, and it is shown that the model accurately describes experimental results when the extracted parameters are used.

I. Introduction

Figure 1 shows the IGBT (Insulated Gate Bipolar Transistor) equivalent circuit superimposed on the schematic of a cross section of the structure of one of the many thousand cells of an n-channel IGBT. The structure of the IGBT in Fig. 1 is similar to that of the VDMOSFET (Vertical double Diffused MOSFET) with the exception that the n^+ drain contact of the conventional MOSFET is replaced by the p^+ anode for the IGBT. Basically, the IGBT functions as a bipolar transistor that is supplied base current by a MOSFET, as indicated by the MOSFET and bipolar transistor symbols in Fig. 1. The other components connected between the emitter (e), base (b), and collector (c) nodes are associated with the bipolar transistor, and those connected between the gate (g), source (s), and drain (d) nodes are associated with the VDMOSFET. In order to describe IGBTs made with MOSFET structures other than the VDMOSFET, only the components of Fig. 1 associated with the MOSFET portion of the device need to be changed.

The VDMOSFET gate-source capacitance C_{gs} consists of the gate oxide capacitance of the source overlap C_{oxs} and the source metallization capacitance C_m. The VDMOSFET gate-drain feedback capacitance (or Miller capacitance) consists of the series combination of the gate-drain overlap oxide capacitance C_{oxd} and the gate-drain overlap depletion capacitance C_{gdj}. The VDMOSFET drain-source capacitance C_{dsj} consists of the depletion capacitance of the drain-source junction. In the equivalent circuit representation, the bipolar transistor base-collector depletion capacitance is coincident with and is thus represented by the drain-source and gate-drain depletion capacitances of the MOSFET.

In addition to these depletion capacitances, the bipolar transistor of the IGBT also contributes a collector-emitter redistribution capacitance C_{cer}. This capacitance is a result of the non-quasi-static behavior of the bipolar transistor base charge for the changing base-collector depletion width. It was shown in refs. [1-3] that this capacitance is orders of magnitude larger than the depletion capacitances and thus dominates the effective output capacitance of the IGBT during turn-off. The bipolar transistor also contributes a charge control collector current indicated by the bipolar transistor symbol, a conductivity-modulated base resistance R_b, an emitter-base diffusion capacitance C_{ebd}, and an emitter-base depletion capacitance C_{ebj}. In the equivalent circuit representation, the drift region resistance of the VDMOSFET is coincident with and is thus represented by the conductivity-modulated base resistance R_b of the bipolar transistor.

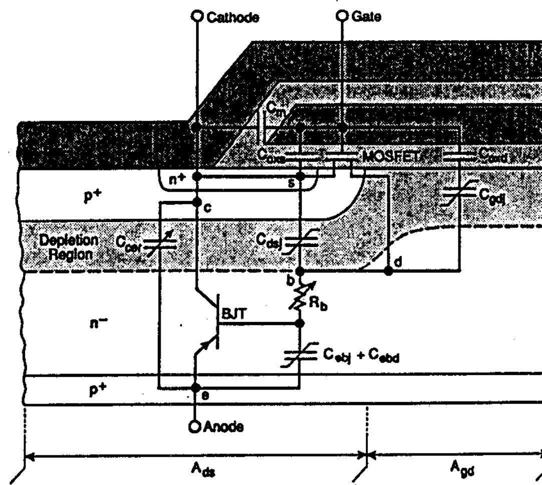

Fig. 1. The configuration of the MOSFET and bipolar equivalent circuit components superimposed on a schematic of one-half of the symmetric IGBT cell.

It was shown in ref. [1] that the analytical model for the IGBT based upon ambipolar transport describes the steady-state current-voltage characteristics of IGBTs with different base lifetimes. It was shown in ref. [2] that the non-quasi-static analytical model for the IGBT describes the output current and voltage turn-off switching waveform for general loading conditions, and in ref. [3] it was shown that traditional quasi-static models are not adequate for the bipolar transistor of the IGBT. In ref. [4] a model for the VDMOSFET characteristics was combined with the non-quasi-static model for the bipolar transistor, and it was shown that the combined model describes the input and output, current and voltage, turn-on and turn-off switching waveforms for the general external drive, load, and feedback circuit conditions.

In this paper, it is shown how the previously developed analytical model for the IGBT is implemented into a user-friendly FORTRAN program that can be used to simulate the dynamic operation of multiple IGBTs for general external circuit conditions. This circuit simulation program, INSTANT – IGBT Network Simulation and Transient ANalysis Tool, and its documentation [5] can be obtained from the author. The IGBT model can also be implemented into commercial circuit simulators such as SABER and IGSPICE. Algorithms are also given in this paper that enable the parameters of the IGBT model to be extracted from the terminal electrical characteristics of the device. It is shown that the device model accurately describes experimental results when the extracted parameters are used.

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II. IGBT Dynamic Model

The basic IGBT dynamic model described in refs. [1-5] is summarized in Tables 1 through 3. The IGBT model consists of three state equations (Table 1) that describe the evolution of the state of the base-collector voltage V_{bc}, the base charge Q, and the gate-source voltage V_{gs}. The right-hand sides of these state equations are expressed in terms of functions of the instantaneous values of the state variables V_{bc}, Q, and V_{gs} (Table 2) and in terms of the functions of the external circuit state variables, I_T and I_g, where these functions depend upon the external circuit configuration as described below.

TABLE 1
IGBT State Equations

$$\frac{dV_{gs}}{dt} = \frac{I_g}{C_{gs}+C_{gd}} + \frac{C_{gd}}{C_{gs}+C_{gd}} \cdot \frac{dV_{bc}}{dt}$$

$$\frac{dV_{bc}}{dt} = \frac{I_T - \frac{4D_p}{W^2}Q + \left(1+\frac{1}{b}\right)\left[\frac{C_{gd}}{C_{gs}+C_{gd}}I_g - I_{mos}\right]}{\left(1+\frac{1}{b}\right)\left[C_{dsj} + \frac{C_{gs}C_{gd}}{C_{gs}+C_{gd}} + \frac{C_{bcj}}{3}\cdot\frac{Q}{Q_B}\right]}$$

$$\frac{dQ}{dt} = I_{mos} + (C_{dsj}+C_{gd})\frac{dV_{bc}}{dt} - C_{gd}\frac{dV_{gs}}{dt} - \frac{Q}{\tau_{HL}} - \frac{Q^2}{Q_B^2}\cdot\frac{4N_B^2}{n_i^2}I_{sne}$$

TABLE 2
Functions of IGBT State Variables

$$V_{bc} = V_{ds}$$
$$W_{gdj} = \sqrt{2\epsilon_{si}(V_{ds} - V_{gs} + V_{Td})/qN_B}$$
$$W_{dsj} = \sqrt{2\epsilon_{si}(V_{ds} + 0.6)/qN_B}$$
$$W_{bcj} = \sqrt{2\epsilon_{si}(V_{bc} + 0.6)/qN_B}$$
$$W = W_B - W_{bcj}$$
$$Q_B = qAWN_B$$
$$C_{bcj} \equiv A\epsilon_{si}/W_{bcj}$$
$$C_{dsj} = (A - A_{gd})\epsilon_{si}/W_{dsj}$$
$$C_{gdj} = A_{gd}\epsilon_{si}/W_{gdj}$$

$$C_{gd} = \begin{cases} C_{oxd} & \text{for } V_{ds} \le V_{gs} - V_{Td} \\ C_{oxd}C_{gdj}/(C_{oxd}+C_{gdj}) & \text{for } V_{ds} > V_{gs} - V_{Td} \end{cases}$$

$$I_{mos} \approx \begin{cases} K_p(V_{gs}-V_T)V_{ds} - K_p\frac{V_{ds}^2}{2} & \text{for } V_{ds} \le V_{gs} - V_T \\ K_p(V_{gs}-V_T)^2/2 & \text{for } V_{ds} > V_{gs} - V_T \end{cases}$$

Because the right-hand sides of the IGBT state equations are expressed in terms of the system state variables (IGBT state variables and external circuit state variables), they can be integrated simultaneously with the state equations of the external circuit to describe the dynamic behavior of the IGBT within the circuit, where the initial conditions are obtained from a known steady-state condition. To do this, the IGBT anode voltage is first expressed in terms of the system state variables (Table 3) because the load circuit state equations are expressed in terms of the IGBT anode terminal voltage.

The expressions for V_{ebd} and R_b in Table 3 are obtained by identifying these terms in eqs 10 and 11 of ref. [2], where the expressions for V_{ebd} and μ_{eff} given in Table 3 have been augmented to ensure a continuous transition of the model to low-level injection conditions. Also, the expression for V_{ebj} is used to include the emitter-base depletion capacitance for negative emitter-base voltages (reverse blocking) and for small emitter-base voltages. To ensure a continuous transition between the diffusion and depletion capacitance voltages, the emitter-base

TABLE 3
Anode Terminal Voltage

$$V_A = V_{bc} + V_{ebq} + R_b \cdot I_T$$

$$V_{ebq} = \begin{cases} V_{ebj} & \text{for } Q < 0 \\ \min(V_{ebj}, V_{ebd}) & \text{for } Q_0 > Q \ge 0 \\ V_{ebd} & \text{for } Q \ge Q_0 \end{cases}$$

$$V_{ebd} = \frac{kT}{q}\ln\left[\left(\frac{P_0}{n_i^2} + \frac{1}{N_B}\right)\left(N_B + P_0\right)\right] - \frac{D}{\mu_n}\ln\frac{P_0+N_B}{N_B}$$

$$V_{ebj} = 0.6 - (Q - Q_0)^2/(2qN_B\epsilon_{si}A^2)$$

$$R_b = \begin{cases} W/(q\mu_n A N_B) & \text{for } Q < 0 \\ W/(q\mu_{eff} A n_{eff}) & \text{for } Q \ge 0 \end{cases}$$

$$n_{eff} \equiv \frac{\frac{W}{2L}\sqrt{N_B^2 + P_0^2\operatorname{csch}^2(\frac{W}{L})}}{\operatorname{arctanh}\left[\frac{\sqrt{N_B^2 + P_0^2\operatorname{csch}^2(\frac{W}{L})}\tanh(\frac{W}{2L})}{N_B + P_0\operatorname{csch}(\frac{W}{L})\tanh(\frac{W}{2L})}\right]}$$

$$\mu_{eff} = \mu_n + \mu_p Q/(Q + Q_B)$$

$$Q_0 = A\sqrt{2\epsilon_{si}qN_B 0.6}$$

$$P_0 = Q/\left(qAL\tanh\frac{W}{2L}\right)$$

capacitor voltage V_{ebq} is chosen to be equal to the minimum of V_{ebd} and V_{ebj} for small forward biases, which effectively uses the larger of the two capacitances.

To describe the interaction of the IGBT with external circuits, the gate current and anode current must be expressed in terms of the external circuit state variables. For example, consider switching the IGBT with the series resistor-inductor load and with a resistive gate drive (Fig. 2). The load circuit state equation for this circuit is:

$$\frac{dI_L}{dt} = \frac{1}{L_L}(V_{AA} - R_L\, I_L - V_A), \tag{1}$$

where

$$I_T = I_L \tag{2}$$

is the state variable for this load circuit. As previously stated, this external circuit state equation is expressed in terms of the anode terminal voltage which is given in terms of the system state variables by the expressions in Table 3. The gate current for the circuit of Fig. 2 is given by:

$$I_g = (V_{gg} - V_{gs})/R_g, \tag{3}$$

where the gate pulse generator voltage is given by:

$$V_{gg} = \begin{cases} 0 & \text{for } t \leq t_{on} \\ V_{gon} & \text{for } t_{on} < t < t_{off} \\ 0 & \text{for } t \geq t_{off} \end{cases}. \tag{4}$$

The initial conditions of the state variables before the initiation of the gate pulse are $V_{gs} = 0$, $Q = 0$, $V_{bc} = V_{AA}$, and $I_L = 0$.

To describe the dynamic behavior of IGBTs in different circuits, only the circuit state equations (eqs 1 through 4) need to be changed. In general, this is accomplished by applying Kirchhoff's current and voltage laws, assuming that the IGBT terminal voltages and the state variables of the external circuit are known (e.g., inductor currents and capacitor voltages). The first expression in Table 3 is then used to relate the anode voltages of the IGBTs to the anode currents, assuming that R_b and V_{ebq} are known because they are evaluated directly in term of the IGBT state variables. This results in the expressions for the gate and anode currents of the IGBTs that are needed to evaluate the IGBT state equations, and in the expressions for the inductor voltages and capacitor currents that are needed to evaluate the state equations of the external circuit.

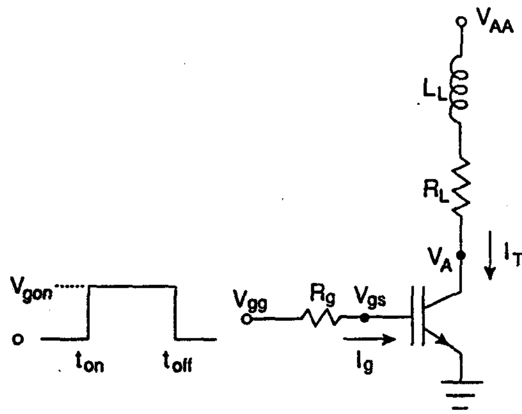

Fig. 2. The circuit configuration of an IGBT with a series resistor-inductor load and a resistive gate drive.

III. INSTANT – IGBT Network Simulation and Transient ANalysis Tool

To simulate the interaction of the IGBT with the external drive, load, and feedback circuits, the state equations of the IGBT (Tables 1 and 2) are integrated simultaneously with the state equations of the external circuit, where the expressions for I_T and I_g depend upon the external circuit configuration and where V_A is given in terms of the state variables by Tables 2 and 3. The simultaneous integration of the state equations is made using the readily available RKF45 subroutine (an automatic Runge-Kutta-Fehlberg method) [6], where the initial conditions are obtained for a known steady-state condition. To simplify the implementation of different circuits and to simplify the description of circuits with multiple IGBTs, the IGBT model within INSTANT is implemented in two subroutines; the first subroutine IGBTSEQ evaluates the IGBT state equations (Tables 1 and 2), and the second subroutine IGBTVeb evaluates the emitter-base capacitor voltage and the conductivity-modulated base resistance (Table 2 and 3) [5].

Figure 3 shows the simplified flowchart for the INSTANT program where the user-defined subroutines for a given circuit are explained on the right. To simulate a given circuit, the user needs only to create the three subroutines and to link them with the INSTANT software package. The program begins by calling the user-defined subroutine INPUT. This subroutine reads the IGBT parameters from a parameter input file by calling the subroutine IGBTINP provided within the INSTANT software package, and reads the circuit parameters for the given circuit. Subroutine INPUT then sets the initial conditions for the state variables and sets the output and plotting parameters to be used by subroutine OUTPUT. The parameters initialized within subroutine INPUT are passed to the other user-defined subroutines using the labeled common blocks /IOpar/, /CIRCpar/, and /IGBTpar/.

After returning from subroutine INPUT, INSTANT calls subroutine RKF45 which repetitively evaluates the user-defined subroutine STATEQ to advance the system state variables to the next time step within the specified precision. The user-defined subroutine STATEQ evaluates the device and circuit state equations for the given circuit. This subroutine first calls the subroutine IGBTVeb supplied within the INSTANT software package to evaluate the emitter-base capacitor voltage and the base resistance for each IGBT in terms of the instantaneous values of the state variables of each IGBT. These values are used to evaluate the circuit expressions for the gate

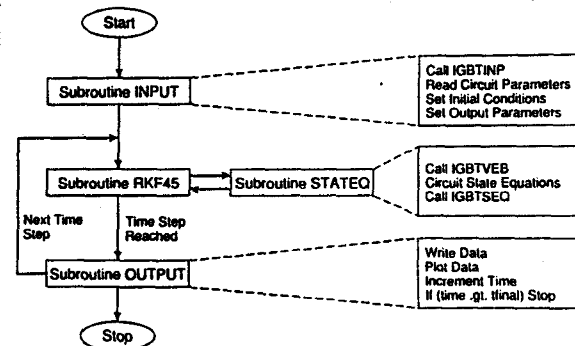

Fig. 3. Simplified flowchart of the INSTANT circuit simulation program where the three user-defined subroutines are explained on the right.

currents, the anode currents, the capacitor currents, and the inductor voltages, so that the state equations of the external circuit and the state equations of the IGBT can be evaluated as described in section II. The IGBT state equations are evaluated by calling IGBTSEQ which requires as its input the gate and anode currents as well as the instantaneous values of the IGBT state variables.

Once RKF45 has reached the next time step, subroutine OUTPUT is called. This subroutine writes and plots the data at that time step. The time step is then incremented within subroutine OUTPUT and control is returned to the INSTANT main program which continues the process of alternately calling subroutines RKF45 and OUTPUT until subroutine OUTPUT detects that the final time step has been reached. For the given circuit to be simulated, the user must supply a file containing subroutines INPUT, STATEQ, and OUTPUT which in turn reference the INSTANT-supplied subroutines IGBTINP, IGBTVeb, and IGBTSEQ to describe the IGBTs. In effect, the three user defined subroutines completely describe the device and circuit equations, the model parameters, and the program control for the simulation, where the IGBT equations are implemented by simply calling subroutines.

Figure 4 shows an example of subroutine STATEQ for the circuit of Fig. 2. The inputs from RKF45 are the time and the instantaneous values of the system state variables (Y), and the outputs are the time-rate-of-change of the state variables (YP) as evaluated by the system state equations. This example has four state variables: one for the inductor current and the

```
c
c
c  State Equations, Input Routine, and Output Routine
c  for the Series Resistor-Inductor Load with a Resistive
c  Gate Drive.
c
c ********************************************************************
c
c
c *** Subroutine to evalutate the state equations of the device and circuit.
c
      SUBROUTINE STATEQ (Time, Y, YP)
c
c *** Designate the number of state equations and declare the calling
c     arrays for the state variables and their time derivatives.
c
      PARAMETER (NEQN=4)
      REAL Y(NEQN),YP(NEQN),time
c
c *** Declare labeled common block for circuit parameters.
c
      REAL              LL,RL,Vaa,Rg,Vggon,ton,toff,trise
      COMMON /CIRCpar/ LL,RL,Vaa,Rg,Vggon,ton,toff,trise
c
c *** Declare names for state variables and their time derivatives.
c
      REAL Vcb,Qte6,IL,Vg
      REAL DVcb,DQte6,DIL,DVg
c
c *** Declare names for functions of state variables.
c
      REAL Va,Ig,Vgg,It,Rb,Vebq
c
c *** Define names for state variables in terms of the calling array.
c
      Vcb   =Y(1)
      Qte6  =Y(2)
      IL    =Y(3)
      Vg    =Y(4)
c
c *** Evaluate functions of state variables.
c
      call IGBTVeb (Qte6,Vcb,Rb,Vebq)
      Va= IL*Rb + Vcb + Vebq
c
      It=IL
      Vgg=Pulsgen(time,ton,toff,trise,trise,vggon)
      Ig=(Vgg-Vg)/Rg
c
c *** Evaluate the state equations.
c
      call IGBTSEQ(Vg,Vcb,Qte6,Ig,It,DVg,DVcb,DQte6)
      DIL=1.0/LL*(-IL*RL-Va+VAA)
c
c *** Define return array for time derivatives of state variables.
c
      YP(1)=DVcb
      YP(2)=DQte6
      YP(3)=DIL
      YP(4)=DVg
c
      RETURN
      END
```

Fig. 4. An example of the user-defined subroutine STATEQ *for the circuit of Fig. 2.*

three IGBT state variables. The circuit parameters that are designated within subroutine INPUT are obtained through the labeled common block /CIRCpar/, but the IGBT parameters are not needed in this subroutine because they are passed directly from subroutine IGBTINP to subroutines IGBTVeb and IGBTSEQ through the labeled common block /IGBTpar/. In the "Evaluate functions of state variables" segment of the subroutine in Fig. 4, IGBTVeb is called to evaluate R_b and V_{ebq} so that the values of V_A, I_g, and I_T can be evaluated in terms of the instantaneous values of the state variables using the circuit equations. These values are used in the "Evaluate state equations" segment to evaluate the state equations for the inductor current and to evaluate the IGBT state equations using IGBTSEQ.

Figure 5 shows the file organization of the INSTANT software package. For a given circuit, the user must create the file called, for example, Circuit.for that contains the three user-defined subroutines: INPUT, STATEQ, and OUTPUT. The user then executes the batch file Linkcirc.bat with the circuit name (e.g., "Circuit" in this example) as a batch file parameter to create an executable program called, in this example, Circuit.exe. The Linkcirc.bat batch file compiles the user-defined circuit subroutines and links them with the INSTANT-supplied subroutines and the graphics library. The user then runs the circuit program and enters the names of the device and circuit parameter input files and the output data file. Figure 6 shows typical device and circuit input files for a 7.1-μs base lifetime IGBT, a 30-Ω, 80-μH load, and a 500-Ω gate resistance. These parameters can be changed with an ASCII text editor without recompiling the circuit routines.

Other second-order effects that are incorporated in the IGBT model but are not described in detail in this paper are: mobility reduction due to high free-carrier levels, velocity saturation in the base-collector depletion region, and carrier multiplication within the base-collector depletion region. The mobility reduction due to high free-carrier levels has a second-order effect on the on-state emitter-base voltage [1] and is implemented iteratively within the IGBTVeb subroutine [5]. Using the parameter ccsflg in the device input parameter list, this effect can be neglected (ccsflg <0) for faster computation speed, or included for more accuracy of on-state voltage (ccsflg >0). The space charge concentration due to the velocity saturation within the base-collector depletion region has a second-order effect on the time-rate-of-change of the base-collector voltage [1] and is implemented iteratively within the IGBTSEQ [5]. This

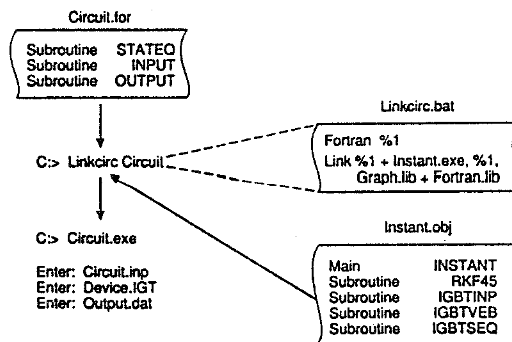

Fig. 5. File organization of the INSTANT software package indicating the use of Linkcirc.bat *to create a circuit simulation program from the three user-defined subroutines.*

Device.IGT

```
7.1e-6      t_HL      (s)
0.0093      w_B       (cm)
2.0e4       N_B       (cm**-3 * E-10)
0.1         A         (cm**2)
6.5e-14     Isne      (A)
4.7         Vt        (V)
0.38        Kp        (A/V**2)
0.62e-9     Cgs       (F)
0.05        Agd       (cm**2)
1.75e-9     Coxd      (F)
-1.0        ccsflg    (+/-)
-1.0        sclflg    (+/-)
1.0e7       vpsat     (cm/s)
1.0e7       vnsat     (cm/s)
4.0         BVn
2.0         BVf
```

Circuit.inp

```
30.0        RL
80.e-6      LL
300.0       Vaa
500.0       Rg
20.0        Vgon
1.0e-6      ton
20.0e-6     toff
0.1e-6      trise
30.0e-6     tfinal
0.0e-6      tplot
```

Fig. 6. Example of device and circuit input files for the series resistor-inductor load with a resistive gate drive.

effect can be implemented or neglected using the parameter sclflg. Carrier multiplication is included explicitly by augmenting the state equations in Table 1. The parameters BVn and BVf are used by the carrier multiplication model [5].

As an example, Fig. 7 demonstrates a typical graphics output of INSTANT for an IGBT being switched on and off for the circuit of Fig. 2. When the circuit program name is entered, the program first requests the names of the input and output files. After the file names are entered, the plot of Fig. 7 appears on the graphics computer screen and the curves are drawn as they are computed at each time step of the integration. The curves of Fig. 7 are scaled in subroutine output so that the expected range of the curves will fit on the plot, and the gate current is offset to the vertical center because it is negative at turn-off. This simulation takes about 30 seconds on a 12-MHz, 386 micro-computer, and can be interrupted at any point of the integration to speed the design process. When the simulation is complete, the plot can be printed directly on a graphics-compatible dot-matrix printer or laser printer. The INSTANT software is written in generally portable FORTRAN which should compile readily on most computers, and the graphics routines used in INSTANT are available for various SUN, VAX, and PC FORTRAN compilers.

Initially at $t = 0$, the gate voltage is zero and the IGBT is in the off-state. Because the IGBT is in the off-state, the anode current is zero, and the anode voltage is equal to the anode supply voltage (300 V). At $t = 1$ μs the pulse generator is switched on, so gate current begins to flow into the gate, and the gate voltage begins to rise. Once the gate voltage exceeds the threshold voltage, the anode voltage falls rapidly to near its on-state value, and the anode current begins to rise at a rate that is determined by the load inductance. At $t = 20$ μs the device and circuit have nearly reached the steady steady-state condition. At this point the gate voltage pulse generator is switched off so current begins to flow out of the gate and the gate voltage begins to fall. Once the gate voltage has fallen to the value where the MOSFET current becomes saturated, the anode voltage begins to rise slowly, and the gate voltage remains constant as the gate-drain overlap oxide capacitance is discharged. Once the gate-drain overlap becomes depleted, the gate-drain capacitance is reduced by about two orders of magnitude, and the anode voltage rises at a rate that is determined by the IGBT effective output capacitance and the anode voltage overshoots the supply voltage due to the large load inductance. The anode current initially falls at a rate that is determined by the load inductance, and then tails off at a slower decay rate due to the slowly decaying excess carrier charge in the base.

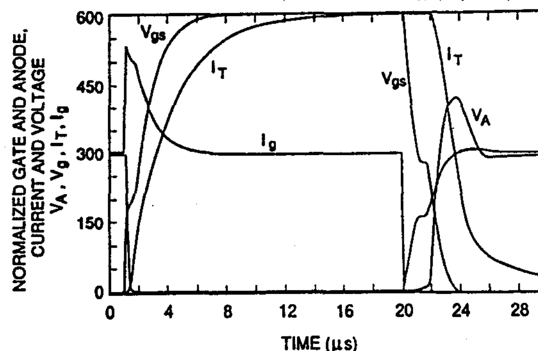

Fig. 7. Example of graphics output of the INSTANT software for the example of a series resistor-inductor load with a resistive gate drive.

IV. Parameter Extraction Algorithms

In this section, the algorithms that have been developed to extract the IGBT model parameters from computer-controlled measurements are discussed. Because the characteristics of the internal MOSFETs and bipolar transistors are convoluted in the steady-state terminal characteristics of merged power devices such as the IGBT, and because the conductivity-modulated devices exhibit non-quasi-static behavior, the dynamic characteristics must in general be examined to characterize the devices and to extract model parameters. This is in contrast to microelectronic devices where the steady-state current-voltage terminal characteristics in conjunction with interelectrode capacitance-voltage characteristics are sufficient to extract most of the device model parameters. The dynamic measurements require high precision and the ability to make calculations on waveforms obtained from computer-controlled measurements. The basic measurement system is shown in Fig. 8 and consists of a computer that controls power supplies, a waveform digitizer, a temperature controller, and a curve tracer. Because this equipment may vary from one laboratory to another, only the basic parameter extraction algorithms are discussed, and hardware specific details are not discussed.

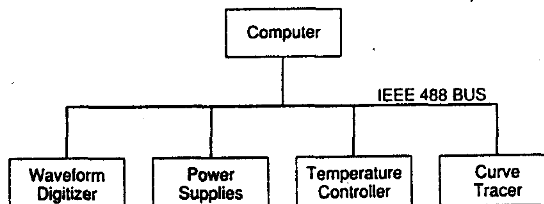

Fig. 8. Configuration of laboratory equipment necessary to extract the IGBT model parameters.

Table 4 gives a list of the IGBT model parameters indicating their nominal values and the device characteristics that are used to extract each parameter. The physical constants of silicon listed in Table 5 are not expected to change between the different IGBT devices. The device active area is extracted by visual inspection of the chip size. Four basic types of measurements are used to extract the remaining model parameters: 1) The turn-off current tail decay rate versus anode current is used to extract the base lifetime τ_{HL}. 2) The relative size of the turn-off current tail versus anode current and anode voltage is used to extract the emitter electron saturation current I_{sne}, the metallurgical base width W_B, and the base doping concentration N_B. 3) The saturation current versus gate voltage is used to extract the MOSFET channel transconductance parameter K_p and the MOSFET channel threshold voltage V_T. 4) The gate charge and the gate-drain charge characteristics are used to extract the gate-source capacitance, the gate-drain overlap oxide capacitance, and the gate-drain overlap area. The four measurements are made in this order because some of the calculations made on the measurements to extract the parameters require the knowledge of the parameters extracted from the preceding measurements.

TABLE 4
Parameter Extraction Algorithms

A	0.1 cm^2	Chip size
τ_{HL}	0.3 – 8.0 μs	Tail decay rate
I_{sne}	6.0×10^{-14} A	Tail size -vs- current
W_B	93 μm	Tail size -vs- V_A
N_B	2×10^{14} cm^{-3}	Tail size -vs- V_A
V_T	5.0 V	Saturation current -vs- V_{gs}
K_p	0.36 A/V^2	Saturation current -vs- V_{gs}
C_{gs}	0.6 nF	Gate charge
C_{oxd}	1.6 nF	Gate charge
A_{gd}	0.05 cm^2	Gate-drain charge

TABLE 5
Physical Constants of Si at $T = 25°C$

n_i	1.45×10^{10} cm^{-3}
μ_n	1500 $cm^2/V \cdot s$
μ_p	450 $cm^2/V \cdot s$
ϵ_{si}	1.05×10^{-12} F/cm

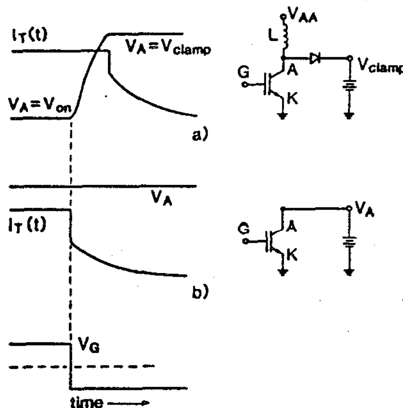

Fig. 9. Circuit configuration and example turn-off switching waveforms for (a) the clamped large inductive load, and (b) the constant anode supply voltage.

The constant anode voltage turn-off current tail decay rate can be measured using either the clamped large inductive load (1-mH) test circuit (Fig. 9a) or the constant anode supply voltage test circuit (Fig. 9b). The clamped inductive load technique is most suitable for small base lifetimes because it results in a larger tail size. When the gate voltage is turned off or when the anode clamp voltage is reached for the clamped inductive load case, the anode current initially falls rapidly and then tails off slowly as the anode voltage remains constant. It is shown theoretically in ref. [1] that the decay time constant of the slowly decaying portion of the current waveform for a constant anode voltage is given by:

$$\frac{\mathrm{d}\ln I_T}{\mathrm{d}t} = \frac{\mathrm{d}I_T}{\mathrm{d}t} \Big/ I_T = -\frac{1}{\tau_{HL}}\left(1 + \frac{I_T}{I_k^\tau}\right) , \qquad (5)$$

where

$$I_{sne} \equiv \frac{q^2 A^2 D_p n_i^2}{I_k^\tau \tau_{HL}}. \qquad (6)$$

Figure 10 shows the measured current decay time constant versus instantaneous tail current for devices with five different base lifetimes. Each curve is composed of several segments measured at different initial currents because the current scales of the measurement equipment need to be changed to maintain adequate precision. The measured values of the current decay time constant are obtained by taking the time derivative of the log of the digitized current waveforms as indicated in Fig. 10. From eq 5 it is expected that the maximum value of this decay rate is equal to the device base lifetime so the maximum value is used to extract the device base lifetime as indicated for the 8.1-μs device in Fig. 10. The emitter electron saturation current can also be extracted from the current dependence of the current decay rate using eq 6.

Figure 11a shows a typical constant anode voltage turn-off current waveform, which consists of an initial rapid fall followed by a slowly decaying current tail. It was shown in ref. [1] that a finite time is required after the initial rapid fall in current for the excess carriers to assume a distribution that can be described by a simple model. However, if the current tail is extrapolated back past the redistribution phase to the time of the initial rapid fall in current using the current tail of a larger initial current waveform, as shown in Fig. 11b, then

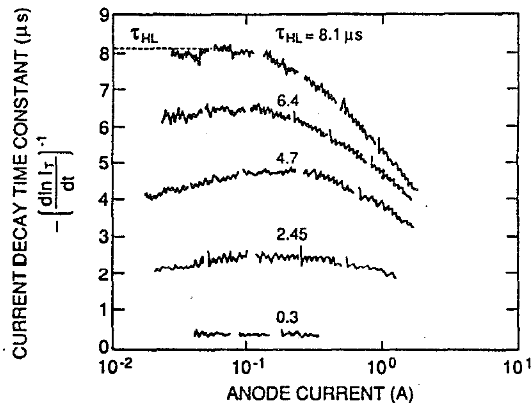

Fig. 10. Experimental values of the current decay time constant versus current, calculated from digitized waveforms for different device base lifetimes and different initial currents. The value of base lifetime extracted for the 8.1-μs device is indicated.

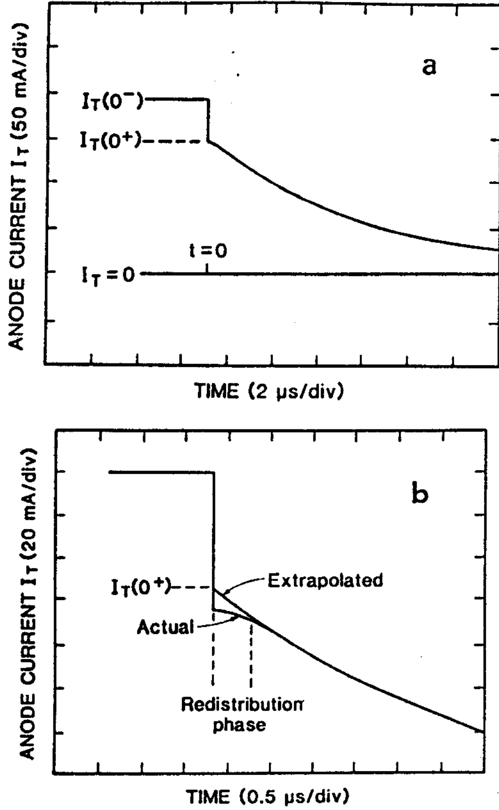

Fig. 11. (a) Constant anode voltage turn-off current waveform, indicating the current before and after the intial rapid fall. (b) A diagram of the redistribution phase on an expanded scale, showing the extrapolated value of $I_T(0^+)$.

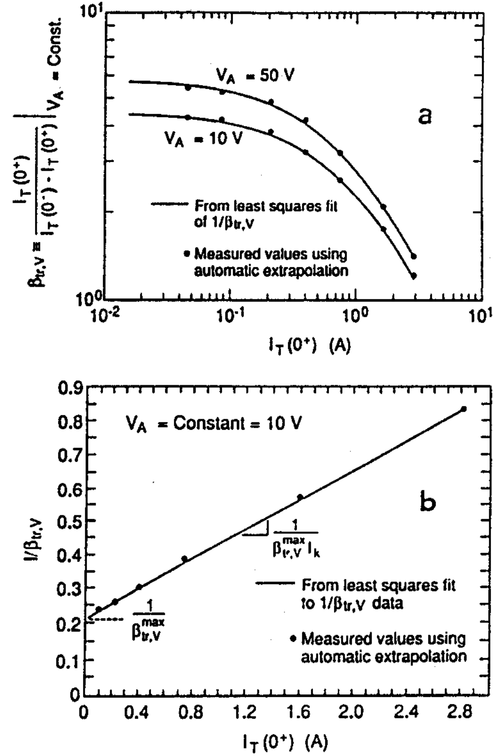

Fig. 12. (a) Measured values of the relative size of the extrapolated current decay tail $\beta_{tr,V}$ versus current for two different values of constant anode voltage. (b) Measured values and linear least-squares fit to $1/\beta_{tr,V}$ versus $I_T(0^+)$ indicating quantities obtained from slope and intercept.

the relative size of the extrapolated current tail for constant anode supply voltage switching is given by:

$$\beta_{tr,V} = \beta_{tr,V}^{max}\left(1 + \frac{I_T(0^+)}{I_k}\right)^{-1}, \qquad (7)$$

where

$$\beta_{tr,V}^{max} = \left(\left(\frac{W}{L}\right)^2 \frac{\coth(\frac{W}{L})}{2\tanh(\frac{W}{2L})} - 1\right)^{-1} \qquad (8)$$

and

$$I_{sne} \equiv \frac{\tanh^2(\frac{W}{2L})}{(\frac{W}{L})^4}\left(\frac{(4qn_iAD_p)^2}{L^2(1+\frac{1}{b})}\right)\cdot\frac{1}{\beta_{tr,V}^{max} I_k}. \qquad (9)$$

Figure 12a shows the measured values of the relative size of the extrapolated current tail $\beta_{tr,V}$ for two different values of constant anode supply voltage. The extrapolations are made using a larger initial current waveform which is automatically aligned with the current tail by a computer-fitting algorithm. Figure 12b shows the measured values of $1/\beta_{tr,V}$ versus the initial tail current which is expected from eq 7 to be linear with a slope of $1/(\beta_{tr,V}^{max} I_k)$ and with a zero current intercept of $1/\beta_{tr,V}^{max}$. The solid curves in Fig. 12 are obtained from a least-squares linear fit to the $1/\beta_{tr,V}$ data. The slope of the least-squares fit is used with eq 9 to extract the parameter I_{sne}, and the zero current intercept is used to obtain the value of W at the given anode voltage from eq 8. Because the base width is expected to be given in terms of anode voltage by [1]:

$$W \approx W_B - \sqrt{2\epsilon_{si}V_A/qN_B}, \qquad (10)$$

the values of W versus the square root of anode voltage can be used to extract the values of W_B and N_B.

Figure 13 defines the IGBT saturation current at a given gate voltage. The IGBT anode current saturates because the internal MOSFET channel current saturates where the MOSFET saturation current is magnified (gain enhancement) by the steady-state common collector current gain of the bipolar transistor $(1+\beta_{ss})$. Figure 14a shows the bipolar transistor common collector current gain versus anode current predicted using the bipolar transistor parameters that were isolated and extracted from the dynamic characteristics described in the previous paragraphs. Hence, the saturation characteristics of the internal MOSFET are obtained from IGBT saturation characteristics by dividing out the bipolar transistor current gain:

$$I_{mos}^{sat} = I_T^{sat}/(1+\beta_{ss}). \qquad (11)$$

In the model used for the MOSFET channel current, the square root of the saturation current is linearly related to the gate voltage with a zero current intercept V_T and with a slope of $\sqrt{K_p/2}$ [1]:

$$\sqrt{I_{mos}^{sat}} = \sqrt{K_p/2}(V_{gs} - V_T). \qquad (12)$$

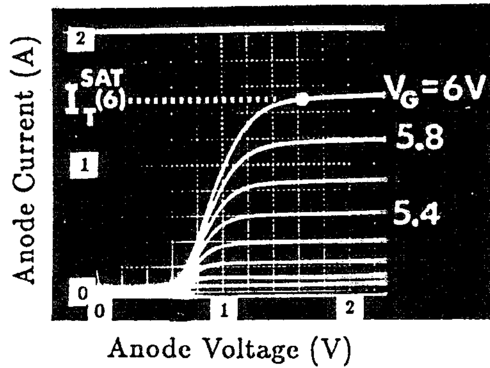

Fig. 13. An oscillogram of the steady-state characteristics of the IGBT, defining the value of the IGBT saturation current at a given gate voltage.

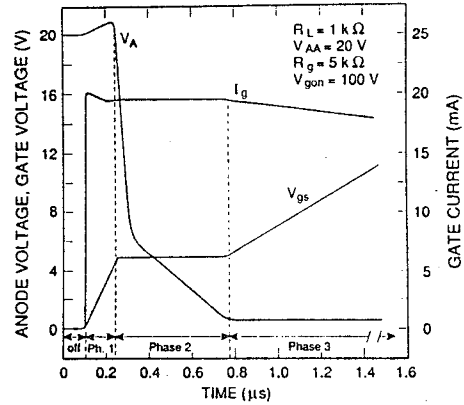

Fig. 15. Measured gate and gate-drain charging characteristics for a low anode current and a relatively constant ~ 20 mA gate current pulse.

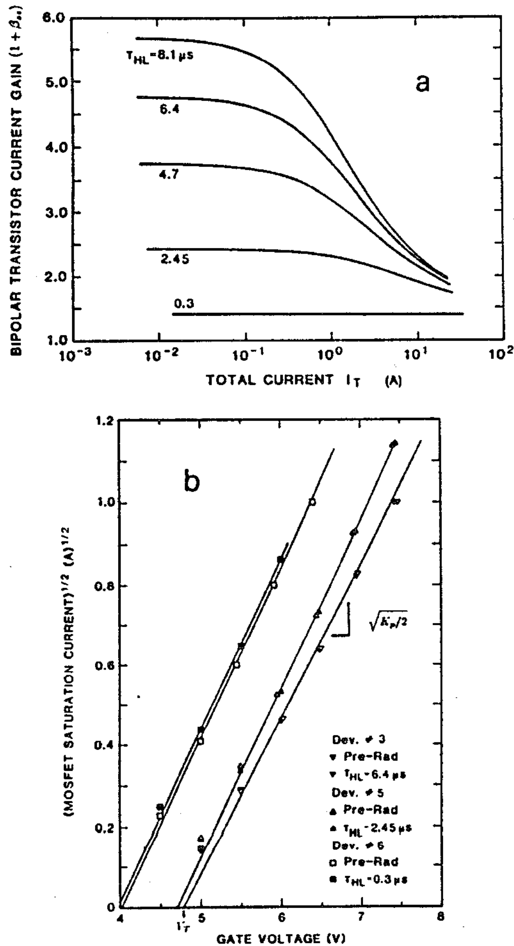

Fig. 14. (a) The steady-state common collector current gain versus anode current for the bipolar transistor of IGBTs with different base lifetimes. (b) The square root of the MOSFET saturation current indicating that the slope is used to extract K_p and the zero current intercept is used to extract V_T.

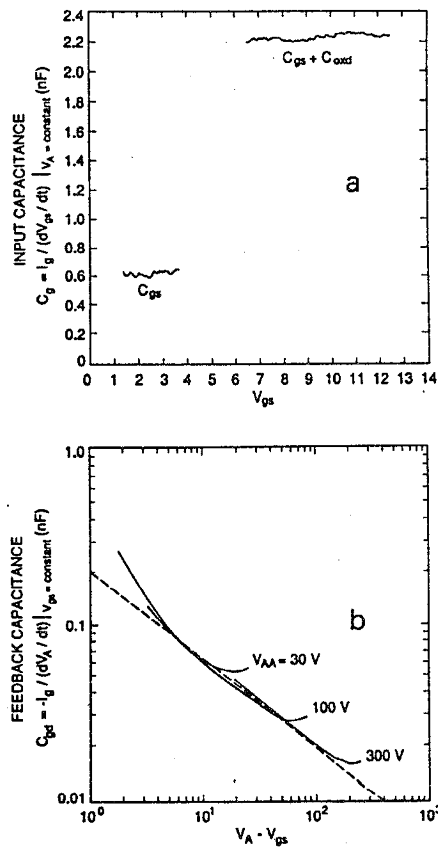

Fig. 16. (a) The measured input capacitance versus gate voltage characteristics for V_{AA} = 300 V obtained from digitized gate current and gate voltage waveforms similar to those in Fig. 15. (b) The measured gate-drain feedback capacitance versus anode-gate voltage obtained from digitized gate current, gate voltage, and anode voltage waveforms similar to those in Fig. 15 for anode supply voltages of 30 V, 100 V, and 300 V.

Figure 14b shows the square root of the MOSFET saturation current versus gate-source voltage obtained by dividing the measured IGBT saturation current by the common collector current gain for devices with different base lifetimes. The values of K_p and V_T are extracted from the slope and intercept of these curves. This method results in similar values of K_p and V_T before and after the bipolar transistor current gain of each device is reduced by neutron exposure which is not expected to change the values of the MOSFET parameters [7].

Figure 15 shows typical IGBT turn-on gate and anode voltage waveforms for a nearly constant gate current and for a load that results in a low anode current [4]. These waveforms are used to examine the gate and gate-drain charge characteristics. For the low anode current, $Q \approx 0$ and the gate charge characteristics are similar to those of the structurally equivalent power MOSFET. The gate voltage waveform consists of three phases as indicated in Fig. 15. During the first phase, V_{gs} rises with a constant slope as the constant gate current charges the constant gate-source capacitance. Therefore, the gate-source capacitance is extracted from this phase as indicated in Fig. 16a by dividing the digitized gate current waveform by the time rate of change of gate voltage computed from the digitized gate voltage waveform. During the second phase, V_{gs} remains virtually constant, and V_A falls as the gate current charges the voltage-dependent gate-drain feedback capacitance. Therefore, the voltage dependence of the gate-drain depletion capacitance is ascertained by dividing the digitized gate current waveform by the time-rate-of-change of gate-to-anode voltage computed from the digitized gate and anode voltage waveforms, as shown on Fig. 16b. For the VDMOSFET structure, the gate-drain depletion capacitance is expected to be given in terms of gate-to-anode voltage by [4]:

$$C_{gdj} \approx \frac{A_{gd}\epsilon_{si}}{\sqrt{2\epsilon_{si}(V_A - 0.6 - V_{gs} + V_{Td})/qN_B}}. \quad (13)$$

Therefore, the measured values of C_{gdj} for high anode voltages are used to extract A_{gd}, and $1/C_{gdj}^2$ versus $V_A - V_{gs}$ can be used to extract V_{Td}. During the third phase of the gate voltage waveform, V_A remains relatively constant, and the gate-source voltage rises as the gate current charges the sum of the gate-drain overlap oxide capacitance and the gate-source capacitance. Therefore, the value of C_{oxd} is extracted by subtracting the value of the input capacitance during the first phase from that during the third phase.

V. Model Verification

In this section, it is shown that the IGBT model presented in section II and implemented into INSTANT gives accurate results when the parameters are extracted as described in section IV. Results are shown for IGBTs with the parameters listed in Tables 4 and 5 and for devices with different base lifetimes (an exception to Table 4 is that the base width of the 0.3-μs device is 110 μm). The values of W_B and N_B obtained using the extraction algorithms are consistent with the values previously obtained from spreading resistance measurements [1].

Comparisons of the IGBT model presented in section II with experiments have been made for different device base lifetimes, different external circuit configurations, and different circuit component values. For example, it is shown in ref. [1] that the model describes the on-state characteristics shown in Fig. 17 and the saturation characteristics defined in Fig. 13 for different IGBT base lifetimes. It is shown in ref. [2] that the model describes accurately the turn-off anode current and anode voltage waveforms for series resistor-inductor loads both with and without snubber capacitors. The comparisons are made for different values of device base lifetime, load inductance, and snubber capacitance. In ref. [4] it was shown that the model describes accurately the turn-on and turn-off, gate and anode, current and voltage waveforms for the circuit of Fig. 2 with different values of gate resistance. For example, the turn-off waveforms for the circuit of Fig. 2 are shown in Fig. 18 for different device base lifetimes and different gate resistance. It was also shown in ref. [4] that the model describes accurately the switching waveforms including the feedback circuit of a polarized active turn-off snubber.

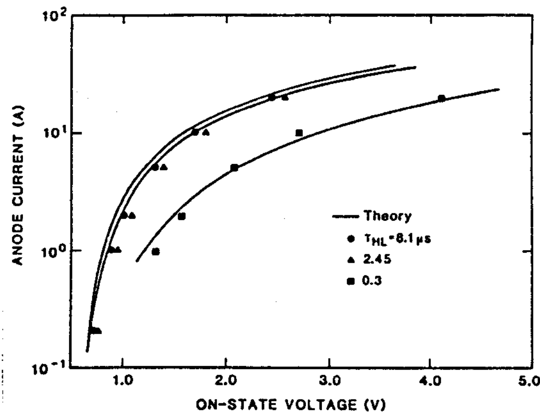

Fig. 17. Predicted and measured on-state characteristics for IGBTs with different base lifetimes.

VI. Conclusions

A compact IGBT model suitable for incorporation in circuit simulators has been presented. A circuit simulation program called INSTANT has been developed to implement the IGBT model for any external drive load and feedback circuit configuration. The INSTANT modeling tool solves the systems of differential equations (state equations) that describe each of the components of the circuit, where the equations for the individual components are coupled by the circuit configuration.

Because the characteristics of the internal MOSFETs and bipolar transistors are convoluted in the steady-state terminal characteristics of merged power devices such as the IGBT, and because the conductivity-modulated devices exhibit non-quasi-static behavior, the dynamic characteristics must in general be examined to characterize the devices and to extract model parameters. The dynamic measurements require high precision and the ability to make calculations using waveform values.

The IGBT model accurately describes the steady-state and dynamic behavior of the IGBT if the device model parameters are extracted from the computer-controlled measurements described in this paper.

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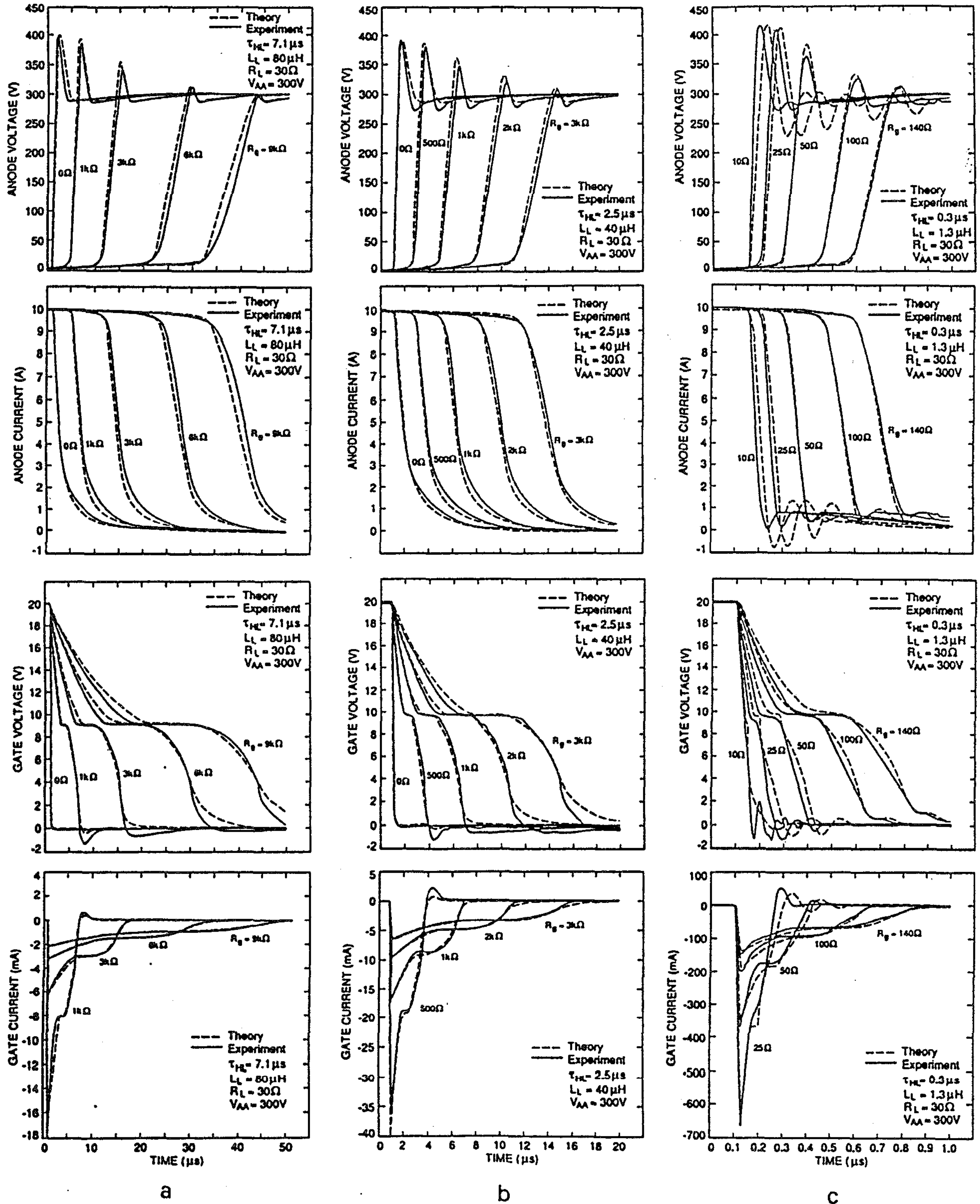

Fig. 18. Comparison of the measured and simulated, gate and anode, current and voltage turn-off waveforms for the circuit of Fig. 2 with different values of gate resistance, where (a) is for a 7.1-μs device, (b) is for a 2.5-μs device, and (c) is for a 0.3-μs device.

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Certain commercial equipment, instruments, or materials are identified in this paper in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the materials or equipment identified are necessarily the best available for the purpose.

The INSTANT program is provided AS IS without warranty, expressed or implied, including, but not limited to, fitness for a particular purpose.

NOMENCLATURE

A	Device active area (cm^2).
$A_{ds} \equiv A - A_{gd}$	Body region area (cm^2).
A_{gd}	Gate-drain overlap area (cm^2).
$b \equiv \mu_n/\mu_p$	Ambipolar mobility ratio.
C_{bcj}	Base-collector depletion capacitance (F).
C_{dsj}	Drain-source depletion capacitance (F).
C_{ebj}	Emitter-base depletion capacitance (F).
C_{ebd}	Emitter-base diffusion capacitance (F).
C_{ebq}	Emitter-base capacitance (F).
C_{gd}	Gate-drain capacitance (F).
C_{gdj}	Gate-drain overlap depletion capacitance (F).
C_{gs}	Gate-source capacitance (F).
C_{oxd}	Gate-drain overlap oxide capacitance (F).
$D \equiv 2D_nD_p/(D_n + D_p)$	Ambipolar diffusivity (cm^2/s).
D_n, D_p	Electron, hole diffusivity (cm^2/s).
I_g	Gate current (A).
I_k	Tail size knee current (A).
I_k^τ	Tail decay rate knee current (A).
I_L	Load inductor current (A).
I_{mos}	MOSFET channel current (A).
I_{mos}^{sat}	MOSFET channel saturation current (A).
I_{sne}	Emitter electron saturation current (A).
I_T	IGBT anode current (A).
I_T^{sat}	IGBT anode saturation current (A).
K_p	MOSFET transconductance parameter (A/V^2).
$L \equiv \sqrt{D\tau_{HL}}$	Ambipolar diffusion length (cm).
L_L	Series load inductance (H).
n_i	Intrinsic carrier concentration (cm^{-3}).
N_B	Base doping concentration (cm^{-3}).
n_{eff}	Effective base carrier concentration (cm^{-3}).
P_0	Excess carriers at emitter edge of base (cm^{-3}).
q	Electronic charge ($1.6 \times 10^{-19} C$).
Q	Instantaneous excess carrier base charge (C).
Q_B	Background mobile carrier base charge (C).
Q_0	Built-in emitter-base depletion charge (C).
R_b	Conductivity modulated base resistance (Ω).
R_g	Gate drive resistance (Ω).
R_L	Series load resistance (Ω).
V_A	Device anode voltage (V).
V_{AA}	Anode supply voltage (V).
V_{bc}	Applied base-collector voltage (V).
$V_{ds} = V_{bc}$	Applied drain-source voltage (V).
V_{ebq}	Emitter-base capacitor voltage (V).
V_{ebd}	Emitter-base diffusion potential (V).
V_{ebj}	Emitter-base depletion potential (V).
V_{gg}	Gate pulse generator voltage (V).
V_{gon}	Gate pulse voltage amplitude (V).
V_{gs}	Gate-source voltage (V).
V_T	MOSFET channel threshold voltage (V).
V_{Td}	Gate-drain overlap depletion threshold (V).
W	Quasi-neutral base width (cm).
W_B	Metallurgical base width (cm).
W_{bcj}	Base-collector depletion width (cm).
W_{dsj}	Drain-source depletion width (cm).
W_{gdj}	Gate-drain overlap depletion width (cm).
β_{ss}	Steady-state common emitter current gain.
$\beta_{tr,V}$	Constant anode supply voltage tail size.
ϵ_{si}	Dielectric constant of silicon (F/cm).
μ_{eff}	Effective ambipolar mobility ($cm^2/V \cdot s$).
μ_n, μ_p	Electron, hole mobility ($cm^2/V \cdot s$).
τ_{HL}	Base high-level lifetime (s).