DATE 2006 Special Session: DFM/DFY Design for Manufacturability and Yield - Influence of Process Variations in Digital, Analog and Mixed-Signal Circuit Design

DATE'06 Munich, March 8th, 2006

Dr. Ralf Sommer

COM BTS DAT DF AMF

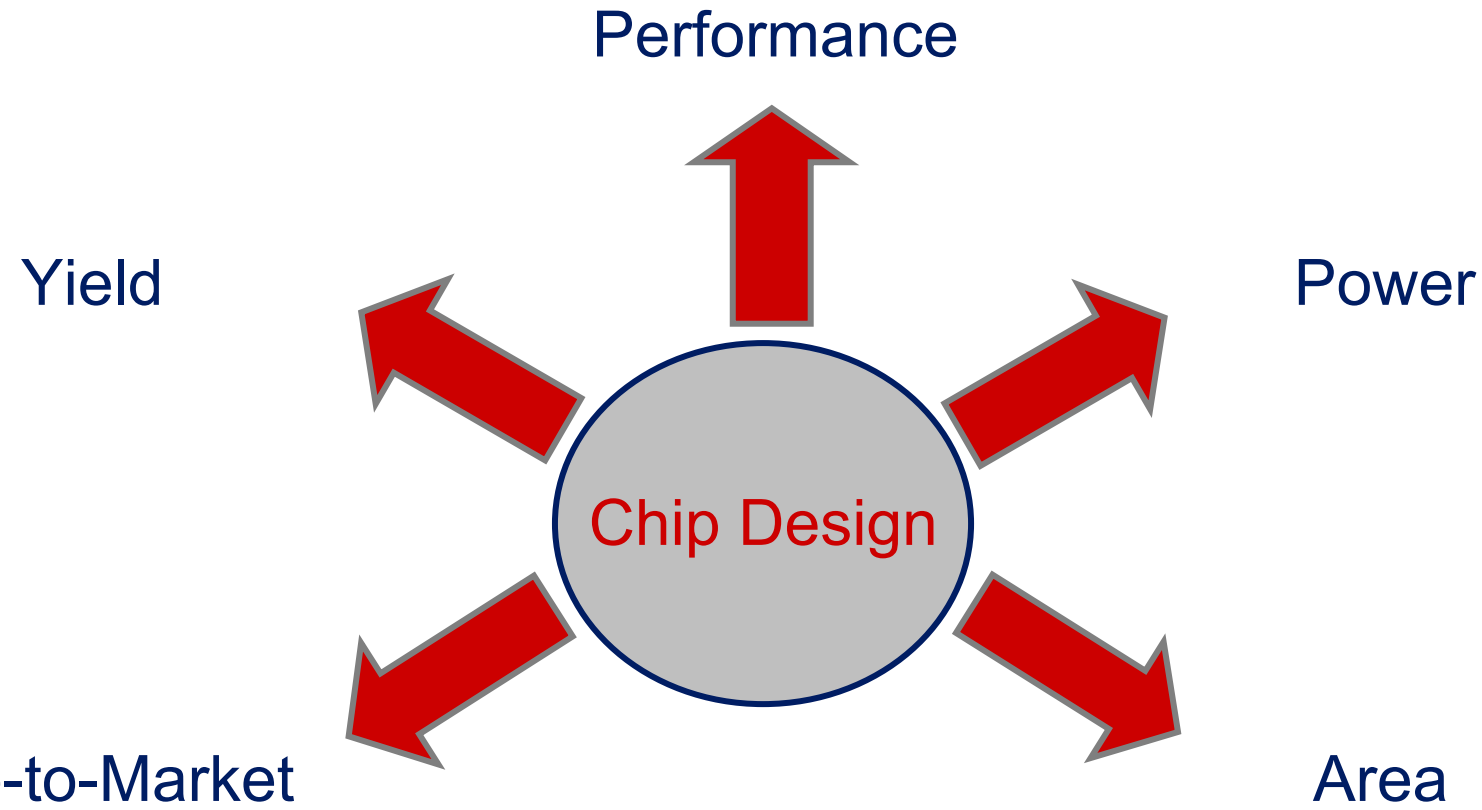
Infineon

Never stop thinking

Outline

- Trouble in Chipmaker's Paradise
- Mismatch Impact on Circuit Design for Advanced Technologies
- Circuit Simulation and Yield Optimization Methods
- History of Requirements from Circuit Designers
- Sizing and Yield-Optimization Flow – Inway 5.x/Powerflow
- Summary and Outlook

The Major Drivers of Chip Design



thanks to E. Barke

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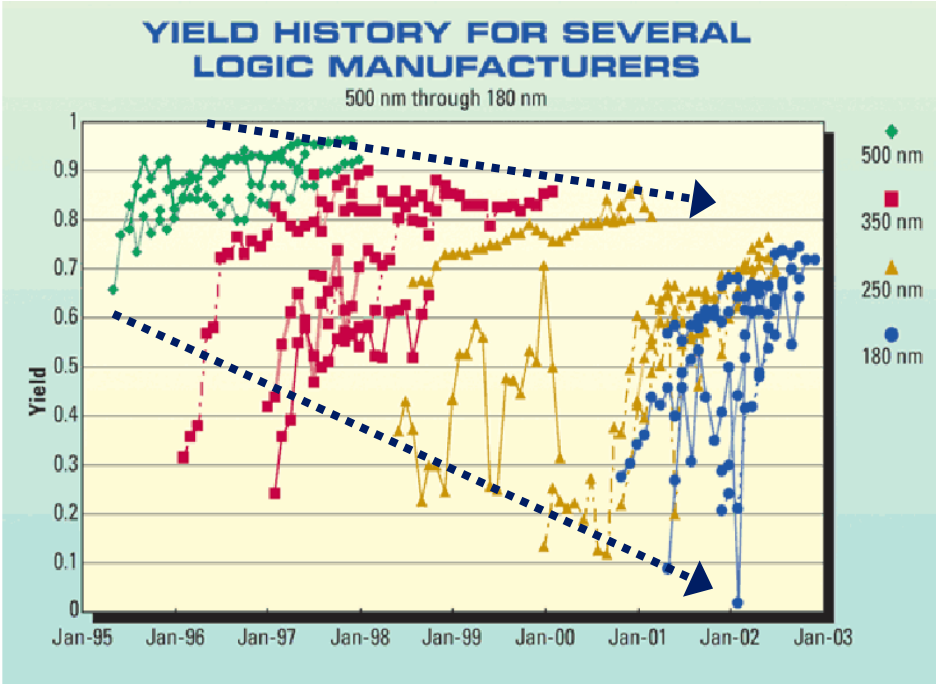
Trouble in Chipmaker's Paradise

- Data from 4 logic companies show initial yield has not improved from the 0.5 µm to 180 nm generation
- Yield learning rates also have not improved and mature yields have declined



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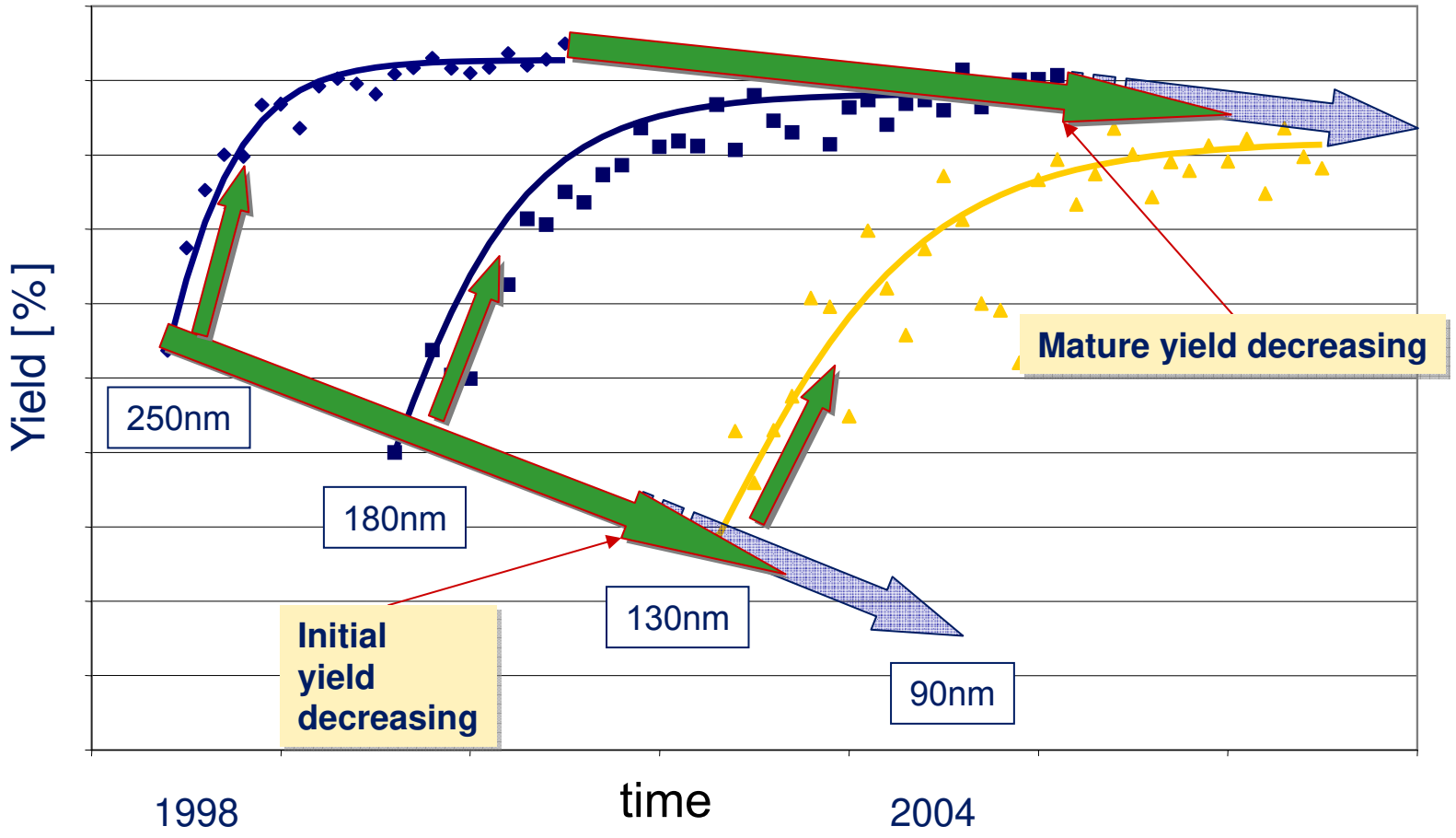
Thanks to Uwe Gäbler

Trouble in Chipmaker's Paradise: Yield Ramp and Final Yields



Yield history for several logic manufacturers

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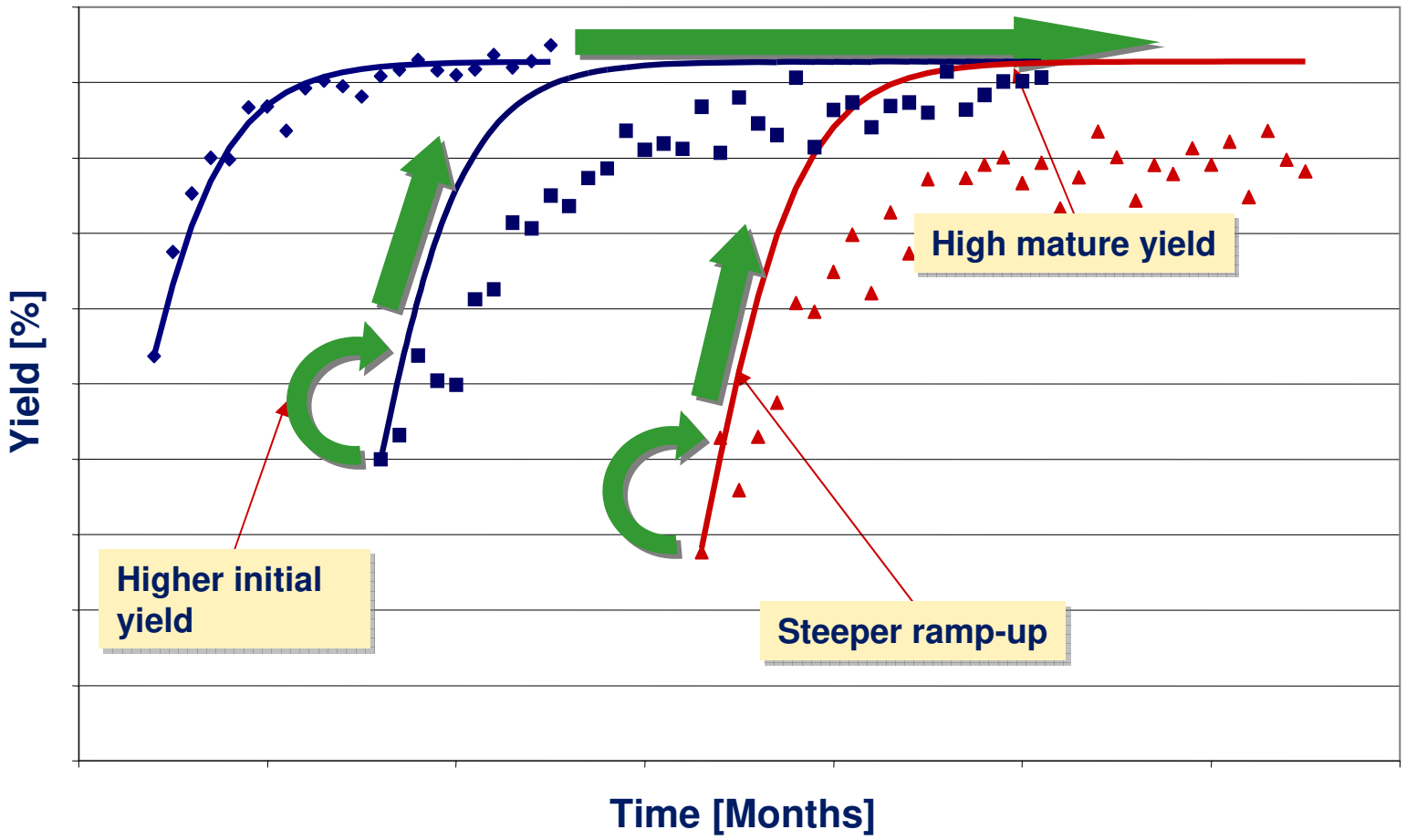
Where We Have To Go



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On-Chip Variation

Technology Node	On-Chip-Variation (*)
180 nm	8 – 13 %
130 nm	22 %
90 nm (to be validated)	30 – 40 %
65 nm (estimated)	45 – 55 %

(*) 3-σ limits of V_{th}

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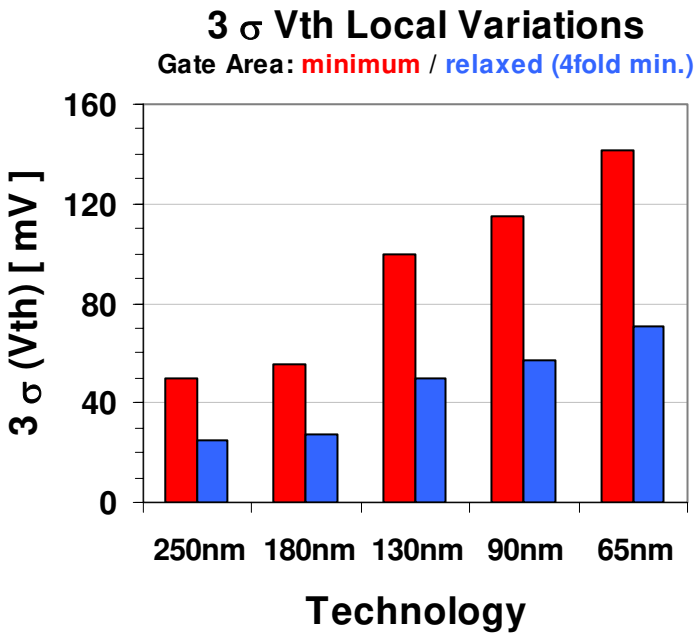
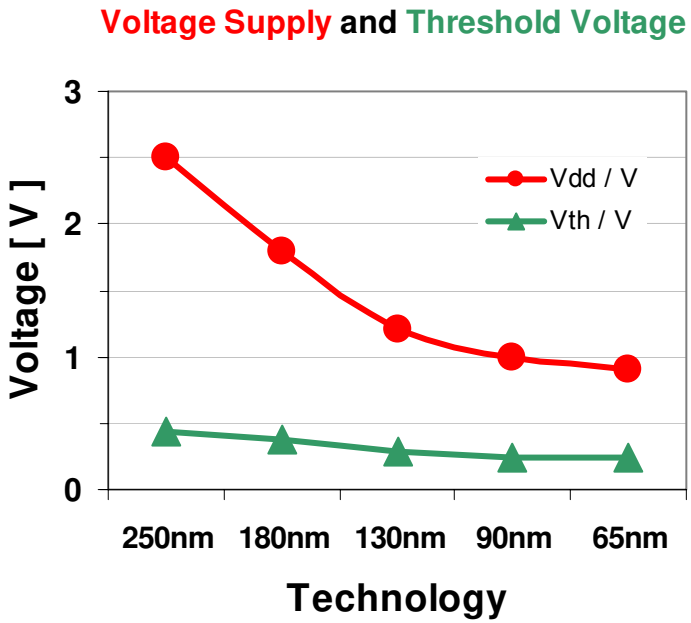
Limits: Mismatch Impact on Circuit Design for Advanced Technologies





- **Reduction of available voltage range**
- **Reduction (scaling) of transistor area**

➔ **Increasing transistor mismatch**

➔ **High effort to maintain circuit accuracy**

Thanks to Ulrich Schaper

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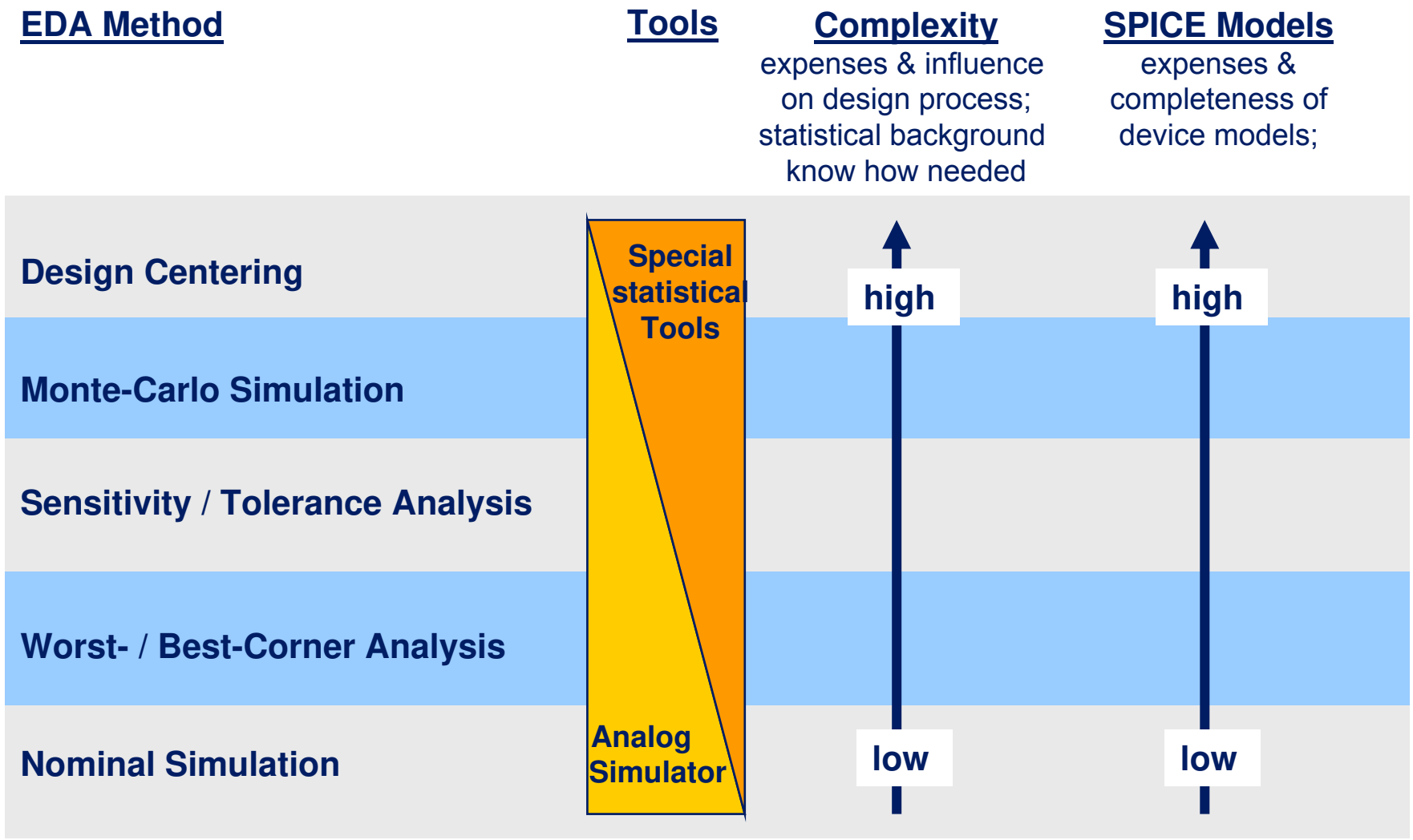
Circuit Simulation and Yield Optimization Methods



Thanks to B. Lemaitre

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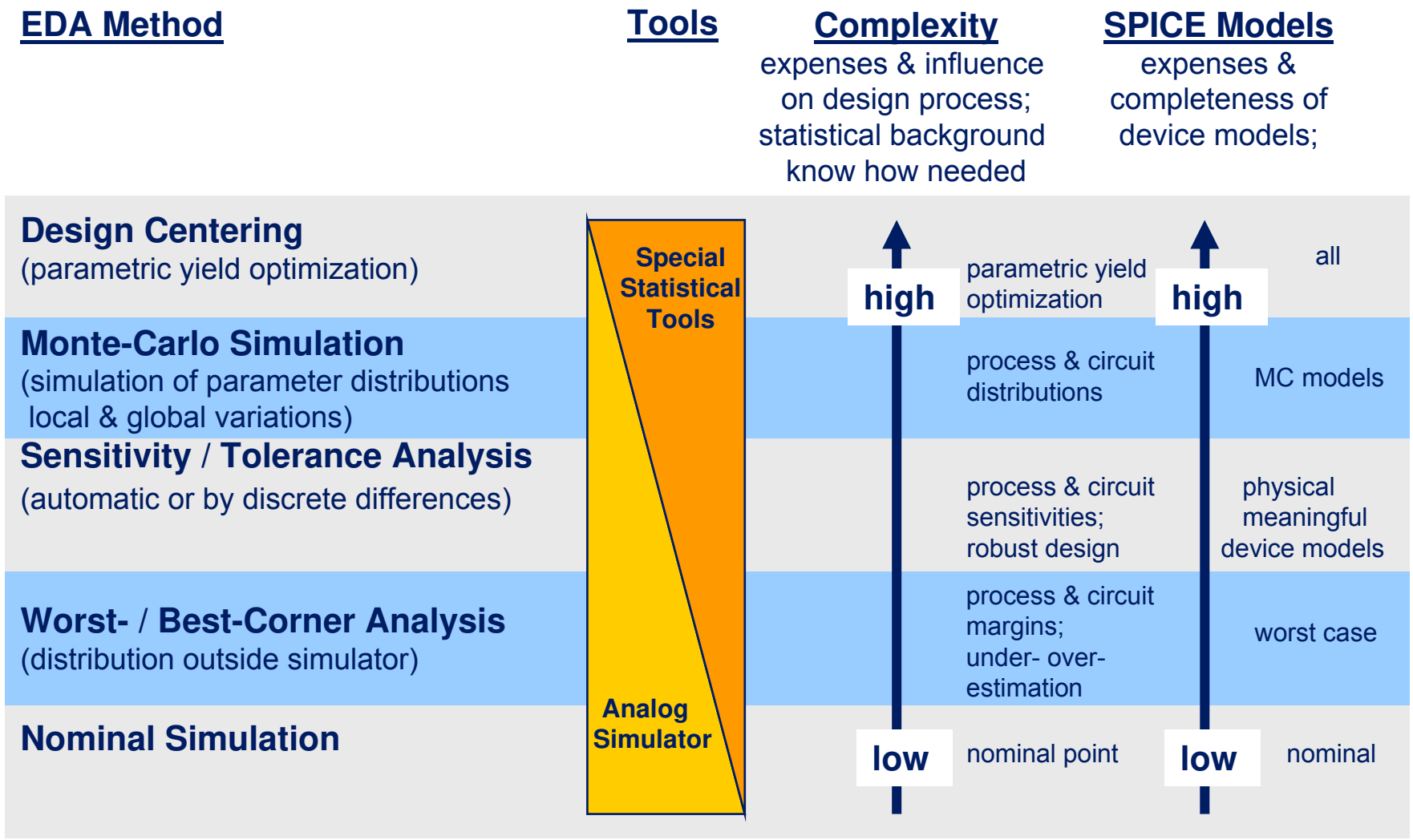
Circuit Simulation and Yield Optimization Methods



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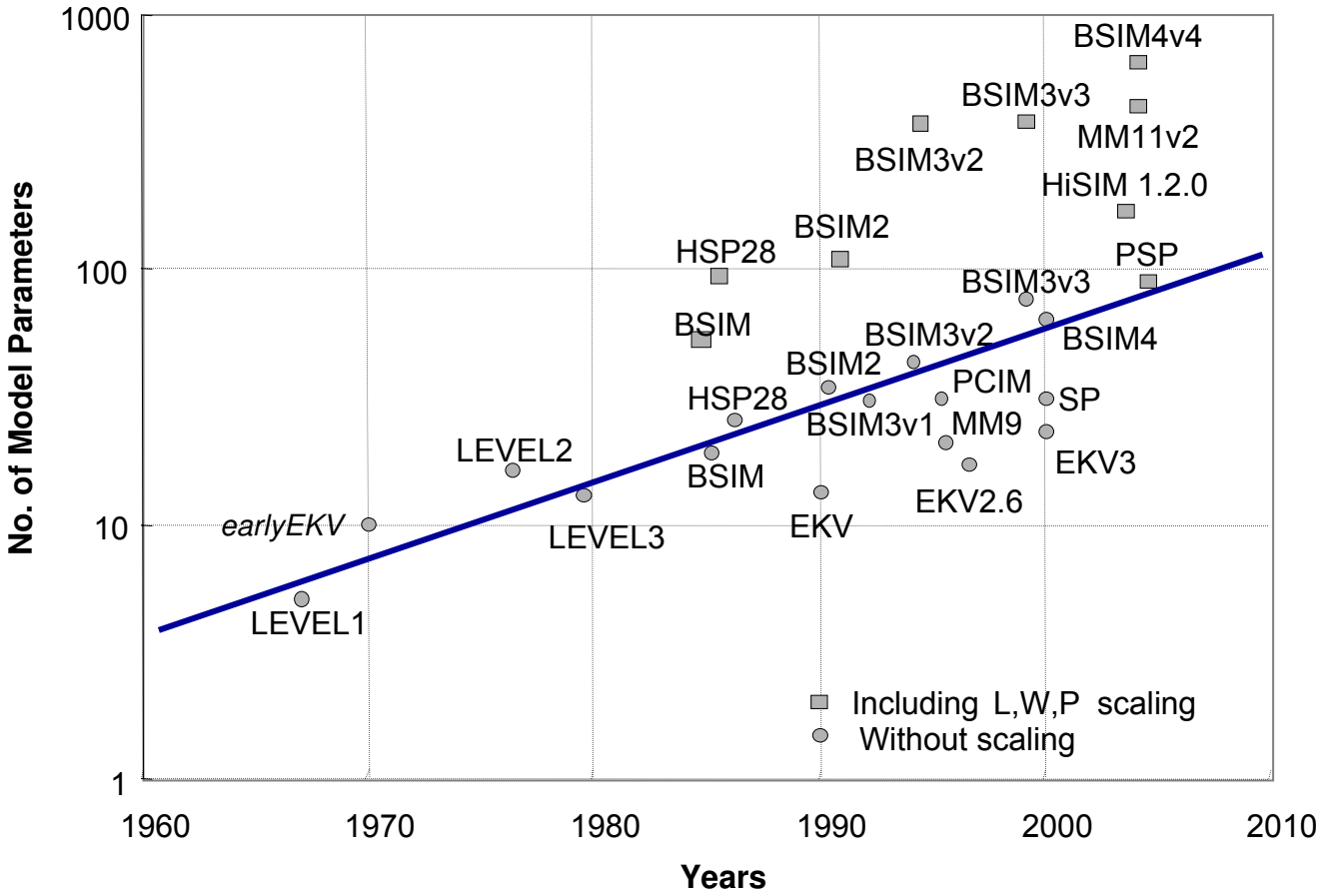
Developments of Compact Models



- Number of DC model parameters vs. year of introduction of the model
- Significant growth of parameter number that includes geometry (W/L) scaling
- How can we handle the complexity (without tools)?

Thanks to W. Grabinski

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History of Requirements from Circuit Designers (cont.)

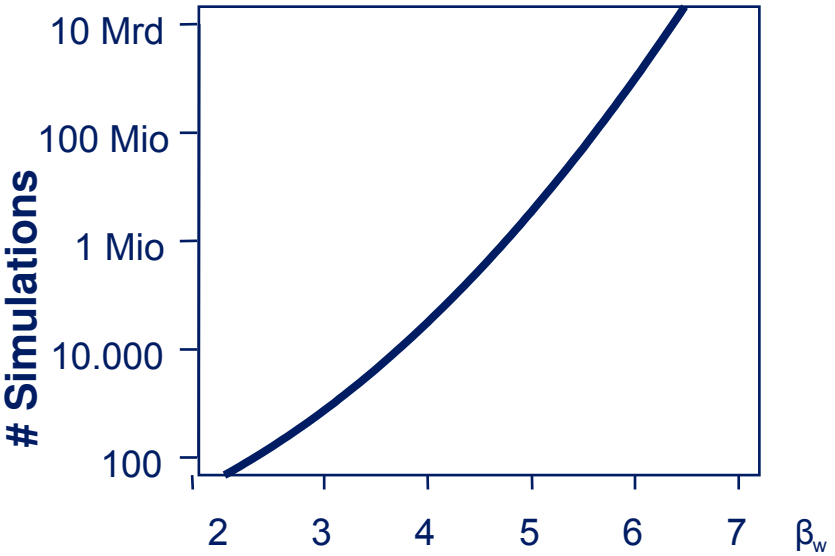
- Corner analysis
  - not suited for analog behavior and mismatch-dominated effects
- Monte-Carlo analysis (without & with operating conditions)
  - no information on how to tune design parameters to improve yield
- Contributor identification
  - Note: Contributor identification does not necessarily describe the impact on yield!
  - Restricted to statistical parameters (and not designables, operating parameters, bias-currents,...)

Monte Carlo: Effort of Yield Estimation

Verification of a yield $Y > Y_{min}$
with 95% confidence:

$$N \blacklozenge c^2 / (1 - Y_{min})$$

Y_{min}	$1-Y_{min}$	β_w	N
98%	2%	2σ	150
99.9%	0.1%	3σ	3 000
99.997%	0.003%	4σ	100 000



Rem.: for 99% confidence, about
1.7 · *N* simulations are needed

→ Better methods needed for very robust circuits:
- Deterministic tolerance analysis and worst-case points
- Importance sampling / stratified sampling

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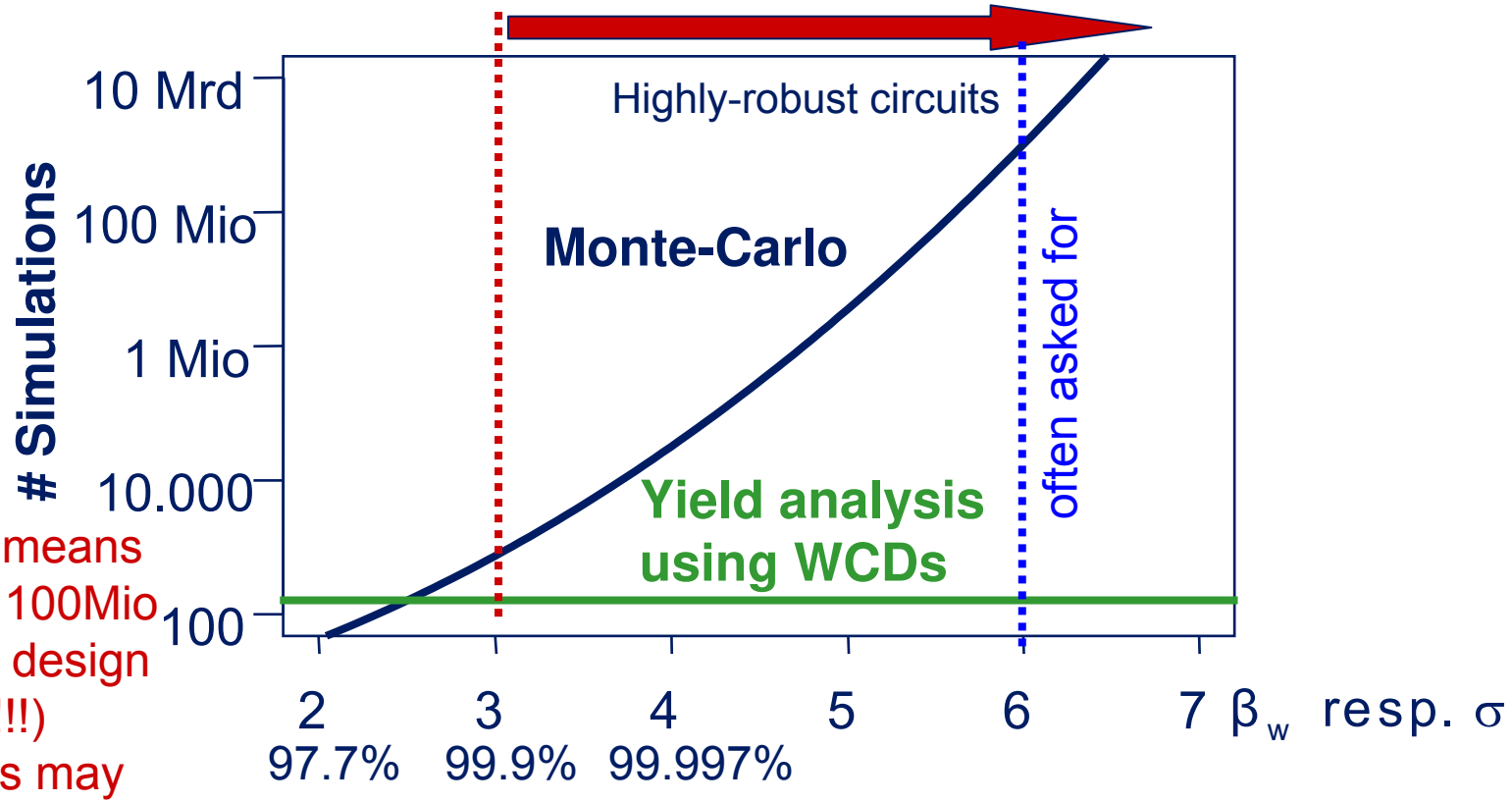
DfM: Why Non-Monte-Carlo-Methods?
Cost Comparison: Yield Analysis with WCDs vs. Monte-Carlo



Note: 3σ means that for a 100Mio transistor design 100000 (!!!) transistors may fail!

Advantage Worst-Case-Distances (WCDs):
More efficient and accurate than MC for yield > 3σ (99,9%)

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  - Note: Contributor identification does not necessarily describe the impact on yield!
  - Restricted to statistical parameters (and not designables, operating parameters, bias-currents,...)
- Yield sensitivities → Worst-case points, distances and circuit performance linearization
- Yield optimization
- Nominal sizing

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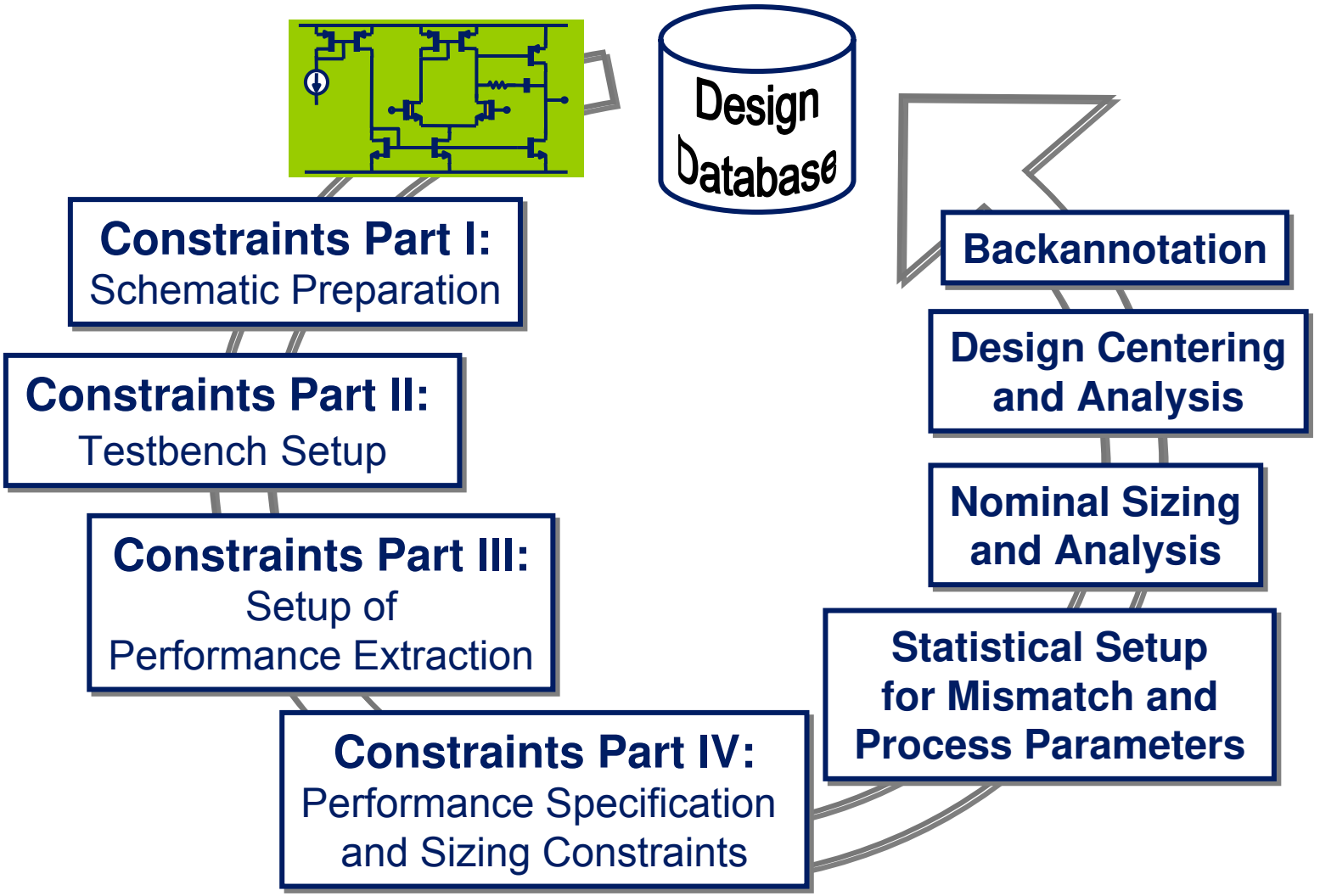
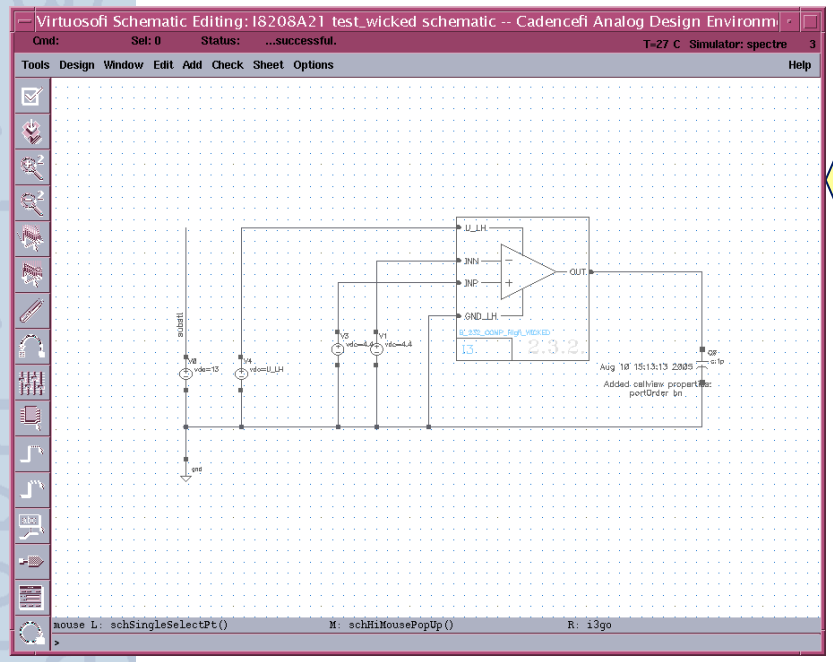
Methodology Development (IFX-DfY & public R&D projects): Sizing and Yield-Optimization Flow – Inway 5.x/Powerflow



Selected References from >200 WiCkeD Optimization Projects within Infineon – RF Design, High-Speed Analog, High-Speed Digital, Automotive Power, Embedded Memory, Enhanced Digital Cell Library Modeling

Application Field	Circuit Design Task (IFX-Project)
RF Design	Coilless LNA for GSM
	Power supply for RF circuits
High-Speed Analog	RF input amplifiers (LNA) and comparators for) High-speed serial memory interface
	Bias chain for A/D conversion
High-Speed Digital	4GHz Master-Slave Flip-Flop of Advanced Memory Buffer Interface
	Digital Carry Select Adder
Automotive Power	Comparator in SMART5 Technology
Embedded Memory	6T SRAM - 6sigma design
Enh. Digital Cell Library Modeling	Statistical static timing analysis for L90 logic (SSTA)

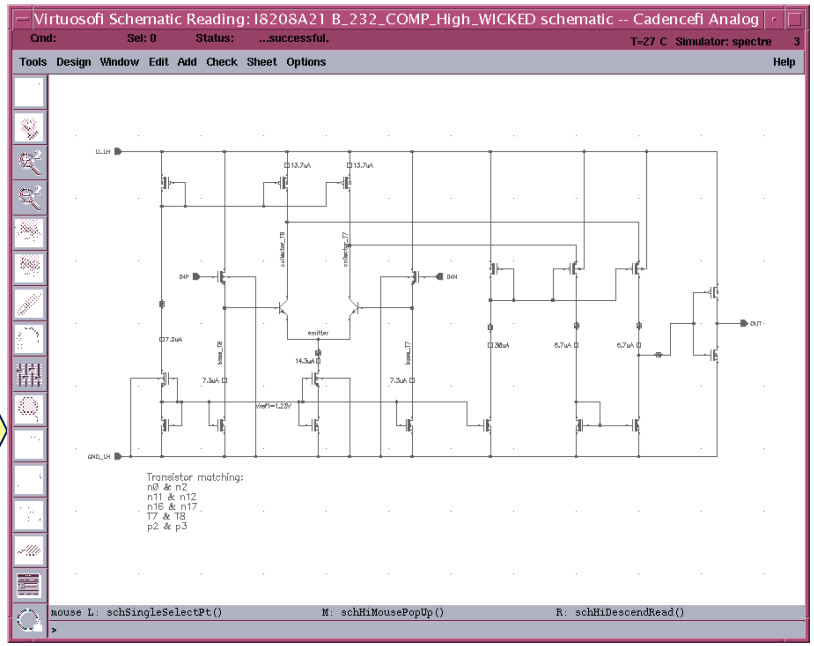
Testbench and Schematic of the Comparator Circuit



Operating conditions:	■ Supply Voltage U_LH: from 6.0 V to 7.0 V (nominal 6.6 V) ■ Temperature Range: from 0°C to 80°C (nominal 27°C)
Performances:	■ Offset upper: 2 mV ■ Offset lower: -2 mV

19 MOSFETs, 2 bipolar transistors:

- Current Mirror
- Level Shifter
- Differential-pair



WiCkeD Reference Projects

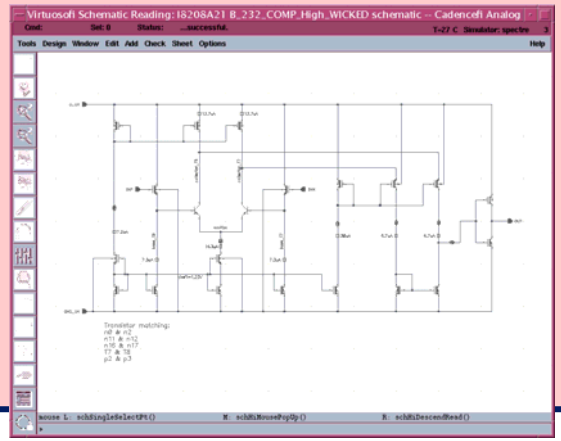
Design Problem & Consequences

Comparator circuit in SMART5 technology

Initial design:

↘ Performances too low (offset, temperature sensitive, matching problem)

↘ Overall design yield: < 5%



WiCkeD

Solution & Results using WiCkeD

↗ Using WiCkeD's optimization engines: Feasibility, Nominal Sizing and Yield Optimization

↗ Total setup & optimization time using 4 hosts: 3 hours

↗ Yield improvement after Nominal Optimization: <5% → 78%

↗ Yield optimization with design centering: 78% → 92,6% yield

↗ Verified with Monte-Carlo

↗ Significant performance improvements for offset, gain (35dB → 57dB) and others

Yield ramp-up from <5% → 92 % in 3 hours

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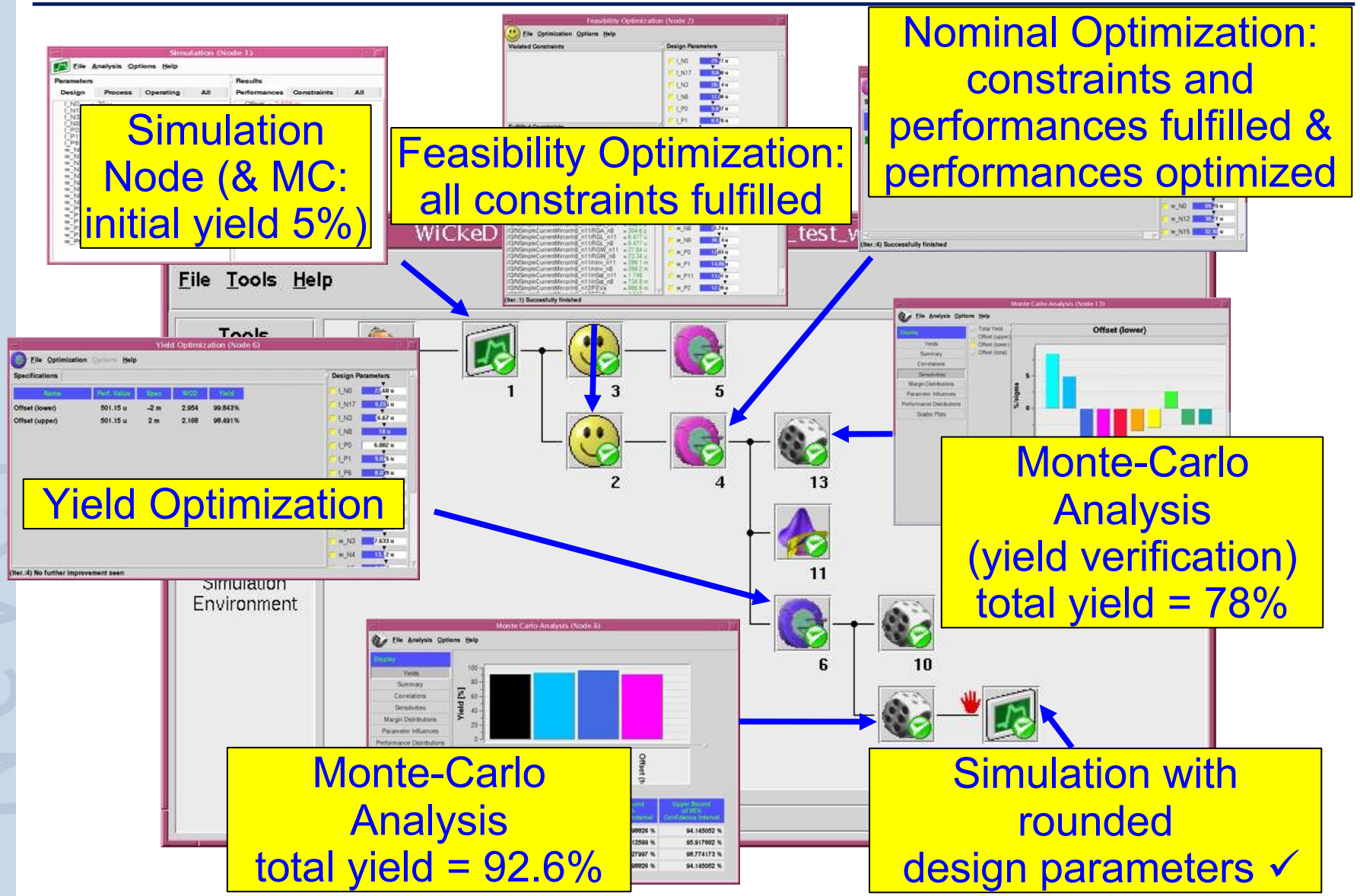
Overview: Circuit Analysis and Optimization Steps



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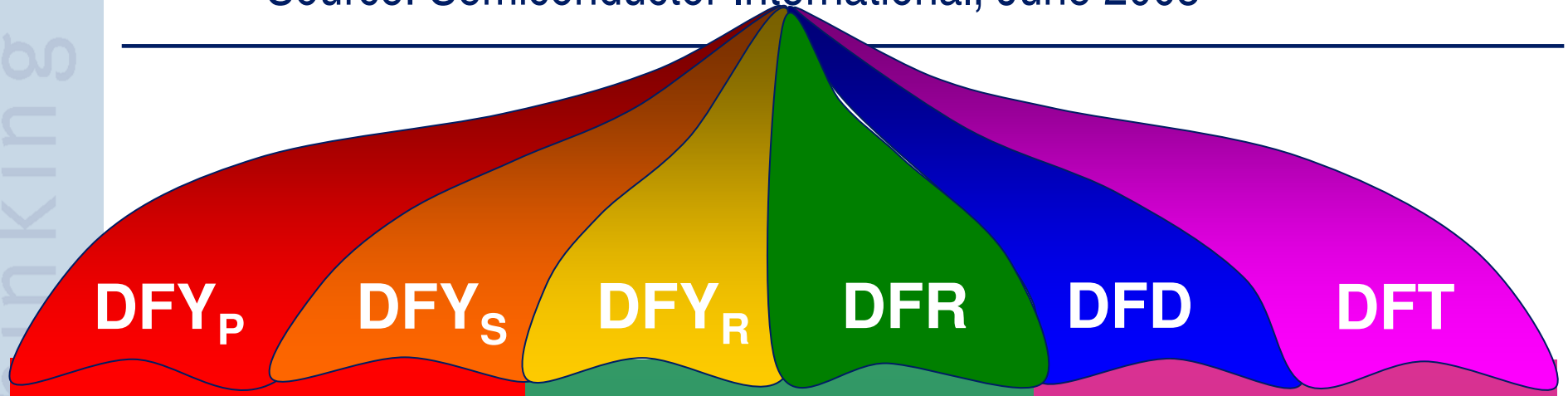
Design for [X] Umbrella - Df[X]
Source: Semiconductor International, June 2005



→ Parametric
→ Systematic
Examples:
- Performance
- Leakage
- Misalignment

...

→ Random
→ Reliability
Example:
- Library optimization

→ Diagnostics
→ Test
Example:
- Fault Coverage / Models

Yield as the 4th Design Target

Chip behavior in Face of Environmental and Manufacturing Variations

Yield

Functional / Systematic Yield

- **Functional Yield Analysis**
  - Critical Area, Printability
  - Layout, design style & litho dependent performance
- **DfM-Aware Physical Design**
  - Redundant via insertion
  - Wire bending / spreading
  - OPC (Optical proximity correction) / PSM (Phase Shift Mask) aware routing
- **Layout Restrictions**
  - Transistor orientation restricted to improve manufacturing control

Parametric (digital & analog) Yield

Address Process and Environmental Variations

- **Digital**
  - Statistical timing/power (SSTA)
  - Timing aware OPC & PSM
  - Statistical Physical Design
  - Adaptive Chip design
- **Analog**
  - Design Centering by Statistical Analog Simulation, Monte-Carlo & Non-Monte-Carlo (e.g. WiCkeD)

Thanks to B. Lemaitre

Summary and Outlook

- Monte-Carlo analysis is suited for yield estimation. Computational effort to ensure high yields is considerable → enormous (is the better word)
- Extensions of MC-analysis allow for handling operating conditions as well as to perform a contributor identification
- Worst-Case methods are superior to MC-methods with respect to efficiency, post processing possibilities e.g. for design centering
- Structural constraints help to obtain better results from the optimization, especially e.g. robustness (performances w.r.t. variation of operating parameters) and computational effort for the optimization loop
- No push-button solution available, but we are working towards improvement of user-friendliness

Summary and Outlook

- Design and technology are in equal measure responsible for yield. Close collaboration is more and more crucial for business success.
- Systematic yield loss is a big problem. Combined efforts of design and manufacturing groups are necessary for improvements here.
- First time right is essential. Don't "throw a design over the fence" and look if it works. Every carelessness will cost valuable ramp-up time.
- Yield maximization should have higher priority than pure cost optimization. Cost reduction measures are only effective in a mature situation.
- Simulator costs and resources: Methodology training mandatory & → **use your brain to avoid computational pain!** (i.e. before you activate thousands of simulations)

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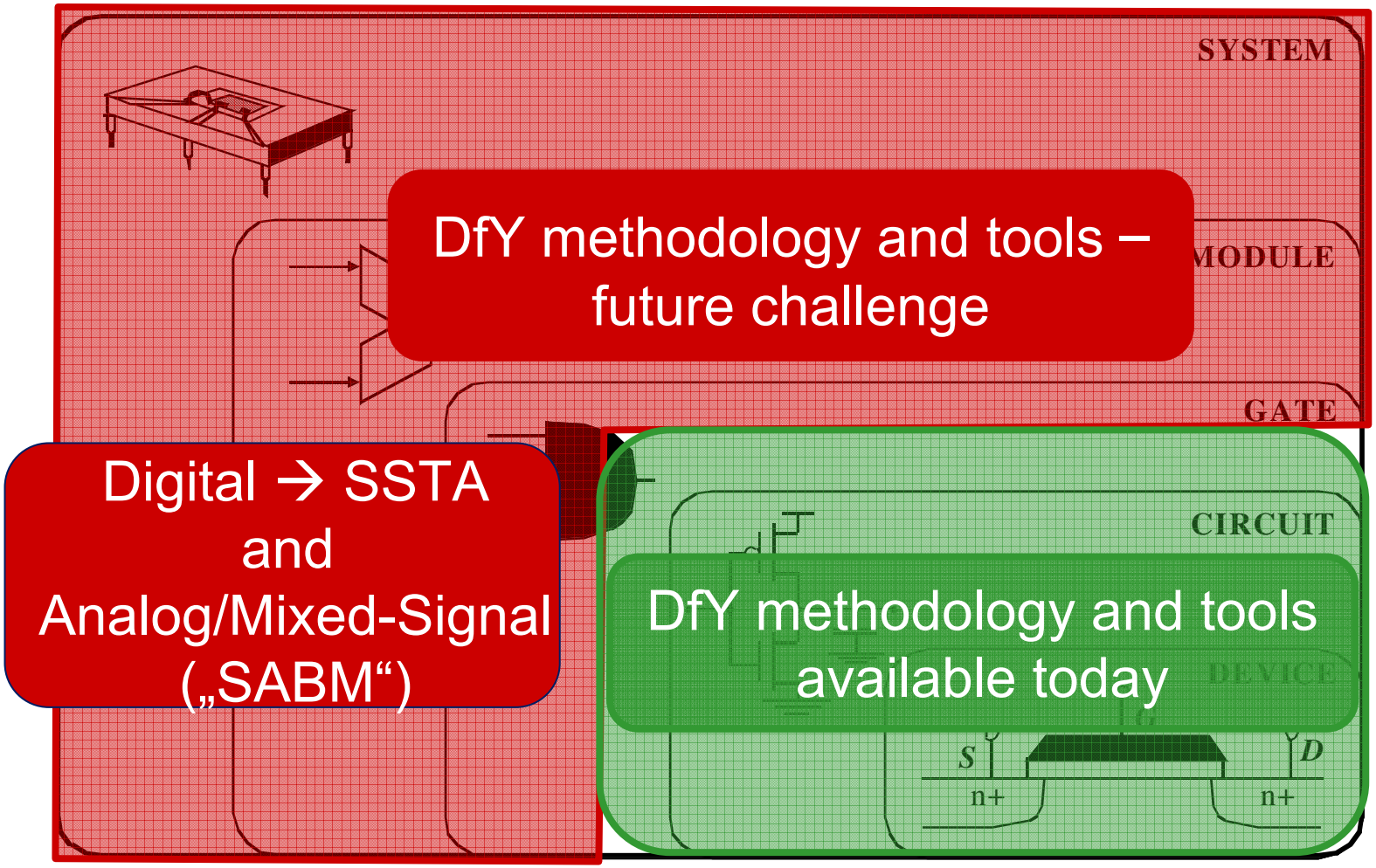
Thanks to R. Schledz

Outlook:
Design Abstraction Levels – Challenges for DfY



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