DFT for Test Optimisations in a Complex Mixed-Signal SOC – Case Study on TI's TNETD7300 ADSL Modem Device

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Abstract

The design and integration challenges for SOCs include DFT for test integration to meet the test quality and test cost goals. This paper describes the DFT implementation on TNETD7300, a single chip ADSL modem SOC with analog and digital sub-systems, IP cores and embedded memories, to address several test optimisation requirements, including scan architecture support for high-end and low-cost testers, concurrent test of digital logic with analog functions, at-speed testing for logic operating in different clock domains and clock frequencies, testing non-homogeneous IP cores together, configurable memory BIST operation, static and dynamic burn-in, and a comprehensive set of SOC test modes to support these operations. These techniques have significantly influenced the silicon test of this device, and have also influenced the design and test methodology adopted in other similar designs in Texas Instruments.

Keywords: SOC test, embedded core test, mixed-signal test, SOC test modes, test integration.

1. Introduction

As SOC (System-on-Chip) designs become more complex, the problem of testing them becomes complex too. This is compounded by the fact that the visibility and controllability only scale inversely in comparison to the functionality that is integrated into an SOC. Comprehensive DFT (Design for Testability) techniques must be employed to meet the conflicting objectives of test quality and test cost. While it is relatively simple to integrate several IP (Intellectual Property) blocks and other peripherals together into an SOC, it is relatively more difficult to test them together, due to their heterogeneous test access mechanisms and test methodologies [1,2,3]. DFT support is, therefore, needed to test all sub-modules together and the device as a whole, under different test conditions and different fault models, while still meeting the stringent cost and quality requirements.

TNETD7300 is a single chip ADSL (Asynchronous Digital Subscriber Line) modem SOC designed in Texas Instruments, India. It consists of four major sub-systems, namely the DSP (Digital Signal Processing) sub-system, DSL (Digital Subscriber Line) sub-system, networking sub-system and analog sub-system. It is the first in its class of devices, (with high levels of integration of high performance mixed-signal components), in Texas Instruments. It includes two IP cores, several embedded memories and an ADSL PHY sub-system with codec and power management functions.

This paper describes the DFT implementation in TNETD7300 to address several test optimisation requirements, including scan architecture support for high-end and low-cost testers, (amenable to the available SOC test interface and for adequate design partitioning and test parallelism), concurrent test of digital logic with analog functions, scan and clock control for at-speed ATPG for logic in multiple clock domains and clock frequencies, testing non-homogeneous IP cores together through suitable test integration, configurable memory BIST operation for test and debug, static and dynamic burn-in for improved stress test effectiveness, and a comprehensive set of SOC test modes to support these operations. The main contributions of this paper are two-fold, namely (i) it describes the DFT requirements in a mixed-signal complex SOC, highlighting the constraints imposed by the individual IP cores and other modules therein, and (ii) it describes the DFT implementation techniques to meet these requirements, which, in turn, impact the overall test quality and test cost. These techniques have significantly influenced the silicon test program development and manufacturability of this device. They are also being applied to a similar class of other designs in Texas Instruments.

Case studies of complex microprocessor cores and devices have been reported in the literature. Relevant designs include the PowerPC [4,5], UltraSPARC [6], Alpha [7] and ARM processors [8]. The techniques used therein are driven by the stringent test requirements of high performance microprocessors, without any specific constraints which are commonly encountered in SOC designs. The DFT techniques described in this paper, therefore, complement those techniques reported earlier. While the techniques presented here have been developed in the context of an ADSL modem device, they are generic enough to be used in other complex mixed-signal SOC designs as well.

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This paper is organised into five sections. Section 2 discusses the test requirements for TNETD7300 and motivates the need for a comprehensive set of DFT techniques. Section 3 describes the individual techniques in detail. The resulting test optimisations are also explained. Section 4 lists some design and test parameters for TNETD7300 and explains how they have been influenced by these DFT techniques. Section 5 concludes the paper.

2. DFT Requirements for TNETD7300

DFT for high performance and complex SOCs influences their design and integration. Being a mixed-signal SOC, the DFT requirements for TNETD7300 were correspondingly more complex. This section describes the device architecture and important DFT requirements.

2.1 TNETD7300 Architecture

TNETD7300 is a single chip ADSL modem SOC with four major sub-systems. These are the DSP sub-system (DSPSS), DSL sub-system (DSLSS), networking sub-system (NWSS) and analog sub-system (ASS). The device contains two IP cores, namely MIPS-4KEc processor and C6200D01 DSP processor, several embedded memories, an ADSL PHY sub-system with codec and power management functions, together with peripherals designed to serve as a broadband network controller for residential and small office applications, and an analog front end (AFE) interface. Refer to Figure 1 [9].

2.2 Test Goals

Standard test goals for high performance and high volume consumer market products include an affordably high test coverage and defect coverage to guard against customer returns, and low test application time and low test cost. In addition, due to the complex nature of this mixed-signal SOC, there were other considerations. These are listed below:

(a) Stuck-at coverage of 95% for the entire device, including the IP blocks and the digital logic inside the analog sub-system.
(b) Iddq coverage of 80% with 10 stops for the entire device, with analog modules in power down state.
(c) Transition fault coverage of 85%, covering all logic in different clock domains and different frequencies.
(d) High coverage of all stress tests, (burn-in and voltage - VBox - stress tests).
(e) Simultaneous testing of all IP blocks along with other peripherals, for all kinds of tests, (normal mode and stress mode).
(f) Simultaneous testing of all digital logic along with analog modules, for all kinds of tests, (normal mode and stress mode).
(g) At-speed testing of all memories.
(h) Application of all ATPG tests on high-end tester as well as TI's low cost test platform, namely VLCT (Very Low Cost Tester).
(i) Design for debug and manufacturability in the form of repair for large memories, selective testing of individual memory cores, independent testing of logic in different IP blocks and peripheral modules in different clock domains, independent test application for digital logic and analog modules, diagnosis during burn-in, isolation between digital logic and analog modules for leakage current and noise measurements, and parametric measurements through internal scan test structures.

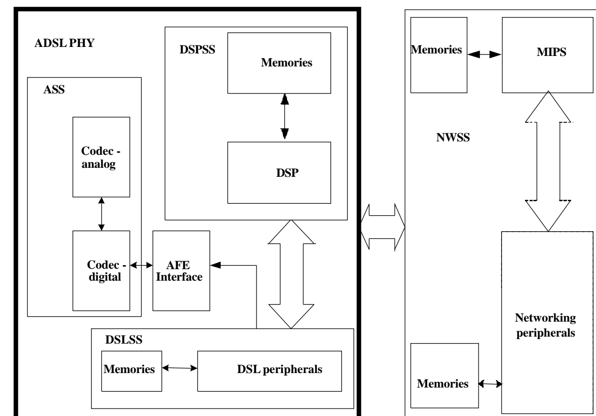


Figure 1. TNETD7300 block diagram.

2.3 DFT Requirements

All the coverage goals for the digital sub-systems were required to be met using ATPG techniques alone. The above considerations, therefore, translated into the specific requirements for:

(a) **Comprehensive set of SOC test modes** for serial and parallel application of manufacturing tests, and for debug.
(b) **Scan architecture and design partitioning** for a suitable scan interface for different testers, and adequate scan control for at-speed testing.
(c) **Common test interface and test control for different IP cores** to test them simultaneously.
(d) **Serial and parallel memory BIST** with export of status signals for debug purposes.

(e) **Clock control for at-speed ATPG** to cover the logic in different scan chains, corresponding to different clock domains and clock frequencies.
(f) **Partitioning of digital logic and analog functions** for test application, and their integration for test parallelism.
(g) **Test mechanisms for stress burn-in** of analog and digital modules.

3. DFT Techniques in TNETD7300

The various DFT techniques implemented in this device are described in this section. The need for a specific technique is motivated and its implementation to meet the various requirements identified in Section 2 is identified. The design and implementation issues discussed here also highlight the challenges in DFT for such a mixed-signal SOC.

3.1 Test Modes

In addition to the normal device operating modes, TNETD7300 has a comprehensive set of test modes. These test modes are implemented to meet the diverse requirements of:

(a) Test pattern generation and application, targetting different faults. These include tests for stuck-at, Iddq and transition faults, and other device I/O (input/output) parametric tests, applied through the test interface.

(b) Test parallelism. These include concurrent analog and digital scan testing, concurrent scan and memory burn-in, and concurrent digital and analog burn-in.

(c) Test interface pins. These are driven by the target testers being considered, (high-end versus low-end), re-use of different pins between functional and test modes and between the various test modes themselves, and pin availability across different packages. (TNETD7300 is, however, a single package device).

(d) Device JTAG TAP interface. The device has three internal JTAG TAPs, one each inside the two IP cores, and one at the device level. These are merged into two at the primary I/Os, based on boundary scan and core emulation requirements.

(e) Diagnosis and debug. These include modes for selecting one or more memory BIST controllers, parametric measurements with internal test structures, selective monitored burn-in, individual IP core testing, separate test of analog and digital modules, etc.

The device has twenty-one test modes to support the above requirements. These are implemented using five external pins and internal configuration registers. These are functional pins which are re-used in the test mode, using a "TEST" select pin. Refer to Figure 2.

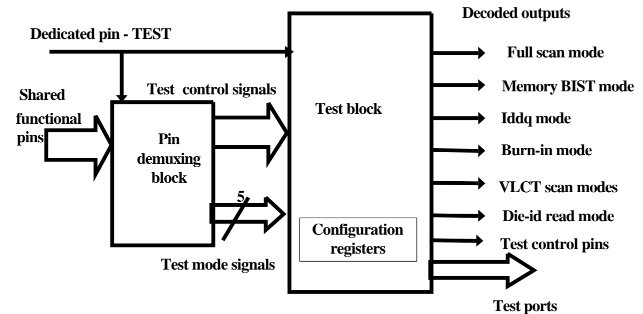


Figure 2. Test modes implementation.

3.2 Scan Architecture

The scan chains definition in TNETD7300 is influenced by various requirements. These include:

(a) Test interface for high-end and low-end testers. TI's very low cost tester, (namely VLCT), supports only upto eight scan chains. The device is, therefore, configured into two scan modes. In one mode, there are upto 32 parallel scan chains. In the other, there are four groups of scan chains, with each group having upto eight scan chains. This test interface has also driven the scan architecture and clock control for this device, so as to be compatible with a VLCT. (A generic VLCT description can be found in [10]).

(b) Clock control during at-speed ATPG. The first three scan groups are derived based upon clock domains. The last group has scan chains running through modules with different clock domains and frequencies.

(c) Testing IP cores. A scan group or part of it is dedicated for each IP core. The MIPS core and surrounding wrapper consist of eight scan chains in one group. The DSP core has four internal scan chains in another half group. (However, subsequently, these four scan chains were merged into one for efficient pattern generation using balanced scan chains. The total number of scan chains was, therefore, reduced from 32 to 29).

Such grouping facilitates at-speed test clocking and pattern re-use. Examples include not merging scan chains (flip-flops) operating on different clocks within the same scan group (chain), and restricting all scan chains in an IP core to lie within the same group. The requirements of scan chain balancing for improving the test pattern efficiency may, therefore, have to be relaxed. Subsequent ATPG experiments, however, have suggested a possibility of recovering the efficiency. Let us assume that the total number of patterns that can be

accommodated for test application is N and the total number of scan chains is C. In the case of a restricted scan test interface, (number of scan I/Os < $2C$), it is now possible to target ATPG to give higher coverage with $N1 + N2$ patterns, $(N1 + N2 = N)$, such that $N1$ patterns are generated with $C1$ scan chains, and $N2$ patterns with $C2$ scan chains, $(C1 + C2 = C)$, than is achievable with the original N patterns each using C scan chains. This scheme can be similarly extended to more than two groups of scan chains and two sets of patterns.

Support for operating all the scan chains in parallel or as four different groups serially is provided through the test modes. The clock controller suitably generates the scan clocks for simultaneous or group-wise serial shifts and captures during different test modes. For ease of implementation, the device boundary scan chain and the die identification (for wafer co-ordinates) scan chain are kept separate. The former can be operated in parallel with the other scan chains also for additional coverage.

Figure 3 illustrates the scan grouping mechanism. (Refer to the end of the paper). For ease of depiction, only three scan groups are shown. Table 1 gives the specific scan architecture for TNETD7300. The scan architecture implemented in this device is based on partitioning of the scan chains into groups for wide and narrow test interfaces. The scan chains are not re-configurable, as suggested in the architecture in [11].

Table 1. Scan architecture.

Subsystems	Clock frequency (MHz)	# chains	# FF / chain	Group
DSLSS	50	8	4 K	A
NWSS	150, 75	4, 4	1.5 K, 3.5 K	B
MIPS	150	8	1.1 K	B
DSPSS	200	2	4.5 K	D
Codec-digital	35	1	5 K	D
Miscellaneous				
Ethernet PHY	50	2	1.5 K	D
Die-id chain	50	1	64	-
Boundary scan	50	1	286	-

3.3 Testing IP Cores

IP cores often have their own test modes, and scan and clock control requirements. These are often conflicting and, therefore, not easy to merge. As a result, these cores are ATPGed individually in an SOC context. This approach results in inefficient pattern sets, potentially lower coverage at the interfaces and additional (duplicate) test modes. Testing such IP cores in parallel is, therefore, important. However, this can be difficult since a combined set of test modes must be implemented, and suitable control for the scan enable, shift clock and capture clock signals must be provided at the SOC level. Control must be provided to derive the specific phase relationships between these signals at the boundary of the individual IPs from the single set of inputs provided externally to the SOC.

The two IP cores on TNETD7300, namely MIPS-4KEc and C6200D01, have their own internal test modes, and scan and clock control mechanisms. (A P1500 type core test interface would help to simplify the test access mechanism; however, it will not unify the internal test modes and test control requirements, since these are hard IP cores [12,13,14]). A comprehensive scan and clock control mechanism is provided to test the two cores in parallel or in isolation. The implementation is outlined in Figure 4. Its important features include:

(a) Scan chain grouping and pattern re-use as explained in Section 3.2. This permits targetted ATPG for different scan groups and IP cores, with all scan groups operating in parallel or sequentially one after another.

(b) Generation of scan and clock control signals with appropriate phases for each core. These cores have conflicting phase requirements, and this support is required to enable parallel test application.

(c) Support in (b) above through a configuration register as illustrated in Figure 4(a). Depending upon the bit value selection, the scan enable signal can be registered on the rising or falling edge of test clock, making it easier to close timing with one particular edge of the scan enable signal as against the other. This also permits both sequential and simultaneous modes of testing.

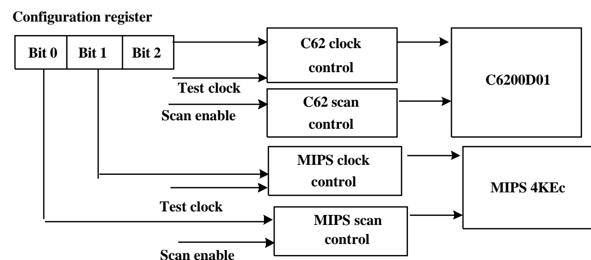
(d) At-speed coverage of interface paths leading to either core by operating the IP cores in phase and out of phase with the surrounding peripheral logic, using this programmable support. This is illustrated in Figure 4(b). This is a two step approach wherein a single clock is used for conditional captures on either edge. Circuit and test program modifications as in [15] are not directly applicable.

Table 2 lists the various modes of operation of the two cores. In Mode 1, all logic uses an inverted clock. The paths between the DSP and its peripherals are tested at-speed. In Mode 2, the DSP uses an inverted clock and the rest of the logic uses the regular clock. Here the interface between the DSP and its peripherals is not tested. In Mode 3, the clock to the DSP is frozen and the remaining logic uses the regular clock. This mode is easier to use than Mode 1 on account of conflicting requirements between the MIPS and DSP cores. All these modes are

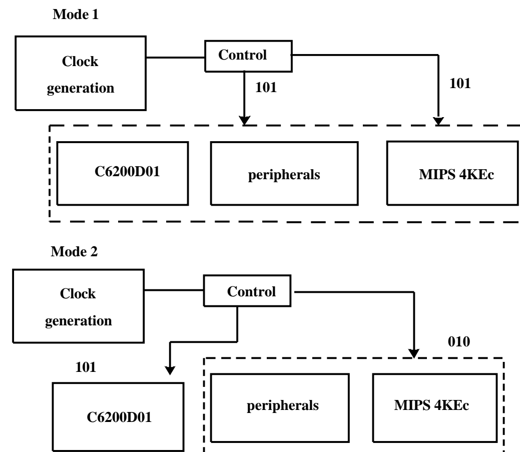
selected through the configuration register bits in Figure 4(a).

3.4 Memory BIST Control

TNETD7300 has several embedded memories, totalling to about two megabits. Sixty-three memory cores are BISTed using fourteen controllers as shown in Table 3. (In comparison, it may be noted that some scan logic in Table 1 is over-designed for creating frequency compatible scan groups for at-speed testing). This is based on the memory sizes, speed of operation, need for repair and physical placement. Requirements supported for memory BIST control include:



(a) Test configuration for individual control for MIPS and DSP.



(b) At-speed clocking for MIPS and DSP.

Figure 4. Scan enable and clock control for IP cores.

Table 2. Test modes for IP cores.

	DSP		MIPS		Other peripherals	
Mode 1	101	↓	101	↑	101	↑↓
Mode 2	101	↓	010	↓	010	↑↓
Mode 3	Off	↓	010	↓	010	↑↓

↓ / ↑ - scan enable registered on negative/positive edge.
101 – Return to one clock waveform
010 – Return to zero clock waveform

(a) Selective enabling of specific BIST controllers. One or more controllers can be enabled depending upon the need for clocking, memory repair and debug. For at-speed testing, sets of memory BIST controllers operating at the same frequency are run together. The memories are exercised at the rated operational frequency, and the logic surrounding the memories is synthesized at the corresponding (higher) scan group frequency. For stress testing, all the controllers are run in parallel at a lower frequency.

(b) Different operating modes. These are depicted in Table 4 and controlled through suitable device test modes. It may be noted that all memory BIST control logic is covered in scan based ATPG. Concurrent burn-in through scan patterns and memory BIST is also possible, depending upon the test modes selected.

(c) Starting BIST operation. The selection of individual controllers is supported through a configuration register, which is writeable in memory BIST test modes. As BIST support allows for testing of the device in the system (application) context, access is also provided to the BIST ensemble through the JTAG interface or through the MIPS processor interface to initiate the BIST operation and probe for failures. The corresponding "enable" and "fail" registers are memory-mapped.

(d) Exporting status from various controllers. The pass / fail status signals from all active controllers are individually latched into a status register, and combined into a single pass / fail indication on a device output pin. Upon encountering a failure, the status register can be scanned out and the failing controller identified for further diagnosis or repair. Cycle specific fail information is also latched for the selected controller. The failing address and data are "data-logged" and scanned out to facilitate repair in the case of repairable memories.

Table 3. Memory BIST controller configuration.

Sub-system	Controller: associated memory cores	Frequency of operation (MHz)	Total Kbits
DSLSS	1 : 2	50	6.1
	2-6 : 5		89.4
DSPSS	7 : 8	200	524.3
	8 : 12		786.4
Codec-digital	9 – 10 : 4	35, 50	4.35
NWSS	11 – 12 : 2	150	49.2
	13 : 14	150, 24, 50	90.4
	14 : 16	150	315.39

Table 4. Memory BIST operating modes.

Test Mode	Controller and collars	Enable and status registers	Data logging register	Other design logic
Logic scan	On scan	Do not care	On scan	On scan
Memory BIST	Memory BIST	Memory BIST	Memory BIST	Do not care
Burn-in	Memory BIST	Memory BIST	Memory BIST	On scan
Iddq	Memory BIST / On scan	Memory BIST	On scan	On scan

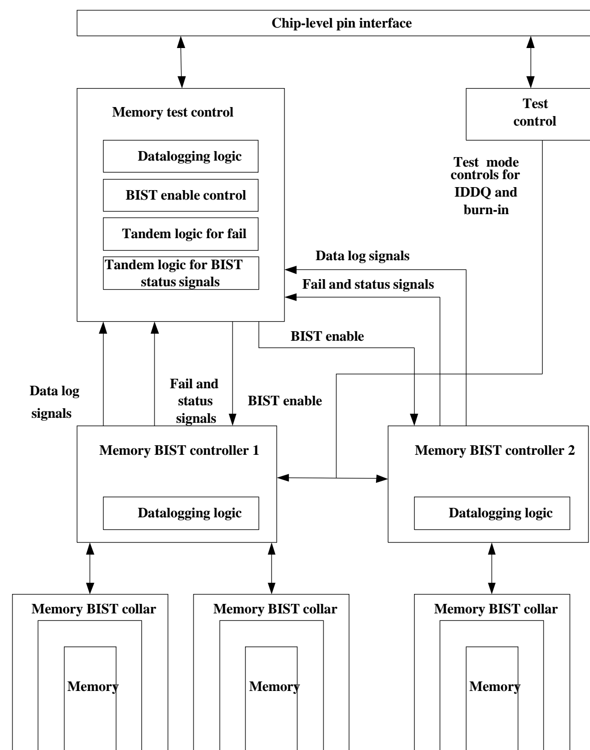


Figure 5. Memory BIST configuration

3.5 At-speed ATPG

Delay defect coverage in this device is primarily targetted through scan based ATPG patterns for transition faults and path delay faults. Logic BIST was precluded due to the BIST non-readiness of the two IP cores. (The comprehensive at-speed ATPG support on TNETD7300, however, is largely facilitating the implementation of logic BIST in its successor device). Requirements supported for at-speed ATPG include:

(a) Scan grouping based on clock domains and clock frequencies, as described in Section 3.2, to (i) facilitate testing on the VLCT, (ii) alleviate the problem of testing inter-clock domain paths, and (iii) generate a more effective set of patterns.

(b) Support for generating launch off shift (scan justified) and launch off capture (functional justified) patterns [16], through corresponding scan and clock control mechanisms.

Towards this, to ease timing closure on the scan enable signal paths, the scan enable signal is internally pipelined. This also allows external control of this signal at lower speed through a low cost tester.

(c) Conditional scan shift and captures. Slow speed scan shift is performed in one or more scan groups in any order, without disturbing the flip-flops in the other groups. At-speed capture clocks are applied to the group of interest, while those to other groups can be gated off selectively. Inter-clock domain paths are also suitably covered, if the frequency of the capture clock matches that of the capturing scan group. Various capture clock combinations supported in this implementation are illustrated in Figure 6. Only launch off capture mechanism is shown, considering three scan groups for brevity. However, similar support exists for launch off shift patterns as well. Both these modes have been used during ATPG.

(d) The VLCT scan modes together with this clock control mechanism give rise to various combinations in accessing the four scan groups over a common set of scan inputs and outputs, and switching amongst them. Hence a reduced pattern set can be generated by operating one or more scan groups, considered individually or paired together. This is significant, since the number of patterns for transition fault coverage is typically large.

(e) All multi-cycle and false paths are re-synthesised to operate at-speed wherever possible. As a result, there is need for minimal masking. (This possibility is precluded in the two hard IP cores). This also facilitates a top level ATPG run across all scan groups to cover the faults on all inter-clock domain paths, which are not covered in the individual scan groups.

At-speed ATPG – pattern generation and application – has attracted wide attention. [17] describes the clock control mechanism for generating transition fault patterns. [18] describes issues in their application on low cost testers. [19] describes a P1500 core wrapper architecture for multiple frequency tests. In comparison, the implementation techniques described here are different in terms of their applicability to wide or narrow scan test interfaces for hard IP cores with multiple clocks.

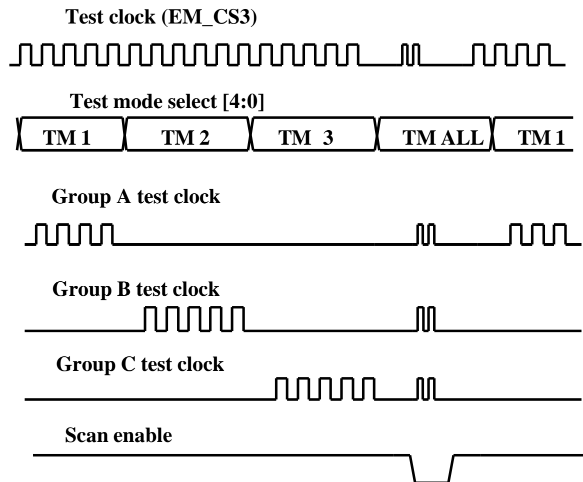


Fig. 6(a). Capture clock in all clock domains.

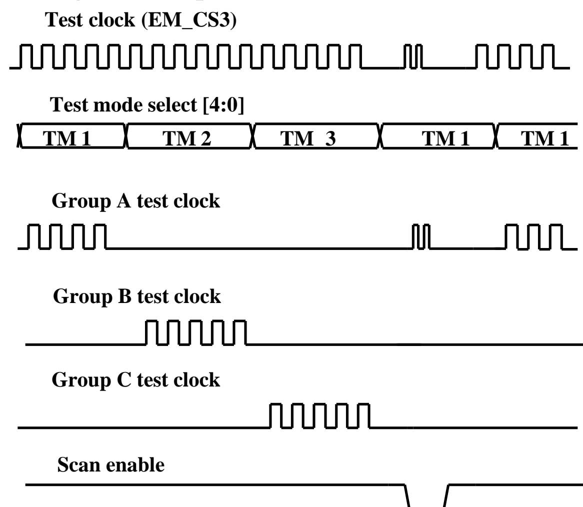


Fig. 6(b). Capture clock in only one clock domain.

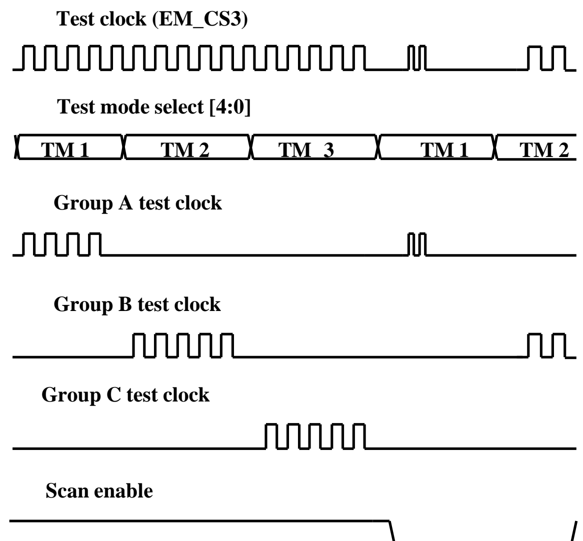


Fig. 6(c)Capture clock in successive clock domains.

Figure6.Clock control for at-speed testing on VLCT.

3.6 Concurrent Test of Analog and Digital Modules

The methodology for testing digital and analog modules is different. Digital logic is tested for modelled defects using algorithmically generated test patterns. Analog functions, on the other hand, are tested for functionality and characterized for specific parameters. During the test of the digital logic using scan or BIST patterns, the device functionality is lost. For analog tests like signal-to-noise ratio (SNR) and total harmonic distortion (THD) measurement, the device must be functional. Mixed-signals SOCs, therefore, traditionally test the analog and digital modules sequentially to avoid any conflict between the test and functional modes, while providing for power control and adequate pin muxing for testing the individual modules. The disadvantage is the large test time involved.

For the AFE (Analog Front End) module, the following mixed-signal tests are applied:

(a) Gain error tests for receive and transmit channels.
(b) Receive and transmit channel missing-tone performance tests.
(c) Receive and transmit channel corner frequency tests.
(d) Programmable Gain Amplifier (PGA) test to verify its functionality.

The above tests are applied concurrently with the digital logic scan and memory BIST tests. This requirement for concurrent test on TNETD7300 has forced the need for additional design support in the form of:

(a) Creating specific partitions of analog and digital modules to permit concurrency. The analog partition is further split into "codec-analog" and "codec-digital". The former consists of analog and mixed-signal blocks alone. The latter consists of digital filters which are required for the functional / parametric verification of a sigma-delta ADC (analog-to-digital converter). All the remaining digital logic in the SOC, (together with memories), is grouped in the partition "ADSL-digital". These partitions are listed in Table 5. The "codec-digital" and "ADSL-digital" partitions can also be grouped together for better coverage.

(b) Isolation at the interfaces, together with control for any internal re-configuration during testing. This permits application of ATPG and BIST tests to the digital logic and memories, and characterisation tests to the analog functions. These tests are de-coupled and scheduled independently of each other. Different schedules are possible during testing under normal conditions and under stress conditions. Isolation also allows debugging of noise coupling issues. This is in contrast to conventional techniques where the partitions not being tested are put into quiescent mode (inactive or powered down).

(c) Dedicated test modes to support the above configurations, thereby permitting simultaneous operation. At the same time, the traditional non-concurrent test modes are retained to adequately test the interface logic and for ease of debug.

(d) Appropriate control for each partition for test mode decodes, clock and test pin multiplexing, isolation at the interfaces, separate scan chain stitching and grouping, and control for BISTing embedded memories.

For the application of these tests, special care is taken in the load board design to ensure that the coupling between digital test signals and AFE analog test signals is minimal. Additionally, silicon characterisation tests are applied at all performance corners to ensure that the mixed-signal test results are not impacted by the digital tests.

Figure 7 depicts how concurrent test is performed on the analog and digital sub-modules. It may be noted that this form of concurrent test also requires hardware support on the ATE (automatic test equipment) to provide independent stimuli and timing control for each partitioned module.

Apart from the savings in test time, (it can be halved if the test times for analog and digital modules are comparable), concurrent testing also permits independent test program development for the two partitions, which can be integrated later. On TNETD7300, the concurrent test modes were successfully used for burn-in stress tests, where the analog modules were statically or dynamically (using loop-back tests) burnt-in, together with the rest of the digital logic. (Tester limitations, however, prevented this support from being fully exploited during application of normal mode tests).

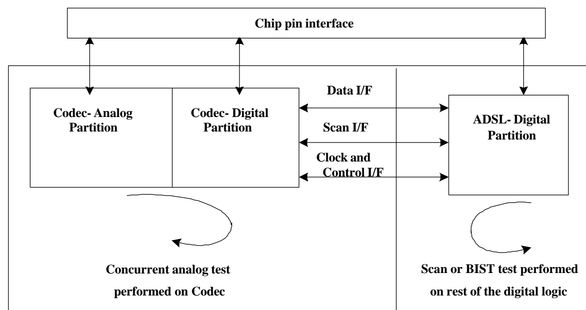


Figure 7: Concurrent testing of analog and digital modules.

Table 5. Operating modes for analog and digital partitions.

Partition	Operation during test modes		
	Concurrent	Non-concurrent	
Codec-analog	Functional	Powered down	Functional
Codec-digital	Functional	Test mode	Functional
ADSL-digital	Test mode	Test mode	Idle

3.7 Burn-in

Burn-in is a stress test carried out to eliminate weak devices that are likely to fail during their early life. Tests causing a high level of activity in the device are recommended. The support in TNETD7300 for burn-in includes:

(a) Application of scan patterns to the digital logic, BIST patterns to memories, and static (power only) and dynamic (changing via loop-back) stimuli to analog modules.

(b) The tests in (a) above can be applied concurrently to the analog and digital modules, (as described in Section 3.6), for reduced burn-in time, or serially for debug. The various modes for burn-in are depicted in Table 6.

(c) A single output pin "monitored" burn-in to identify failing devices is supported, driven by the burn-in tester requirements and the large number of devices that are put on the burn-in board. The various scan outputs and memory BIST controller pass / fail signals are combined through an Ex-Or logic cone to drive this output.

(d) For ease of debug and fault isolation, any combination of one or more scan chains, together with the status output of one or more memory BIST controllers, can be selected for monitoring, using the mechanism shown in Figure 8. It may be noted that using this configuration register, it is not necessary to add test modes to access individual scan groups.

(e) Such form of grouping can also potentially improve the coverage using a given number of scan patterns, as explained in Section 3.2. Since the burn-in oven has a limited memory per input channel, efficient pattern generation using groups of scan chains, targetting different sub-systems for improved coverage, is desirable.

Table 6. Different burn-in configurations.

	ADSL digital		Codec-digital	Codec-analog
	Logic	Memories		
Static burn-in mode	Scan	Don't care	Scan	Powered down
	Don't care	Memory BIST	Memory BIST	Powered down
	Scan	Memory BIST	Scan and memory BIST	Powered down
Dynamic burn-in mode	Scan	Don't care	Loop-back test	Loop-back test
	Don't care	Memory BIST	Loop-back test	Loop-back test
	Scan	Memory BIST	Loop-back test	Loop-back test

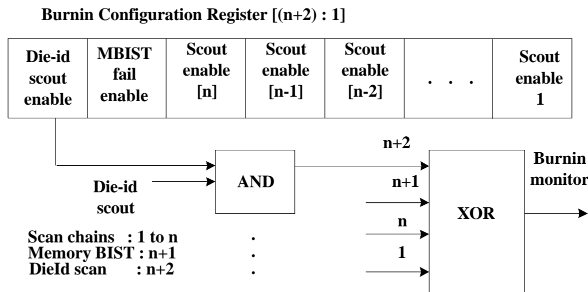


Figure 8. Configurable scan and memory burn-in.

4. TNETD7300 Test Data

Refer to Table 7. The data therein is indicative of the complexity of the design. MemBIST-IC from Logic Vision [20] and FastScan from Mentor Graphics [21] were used for memory BIST and ATPG. The DFT techniques listed in Section 3 have impacted the test time and test quality in several ways:

Table 7. Test data.

Test mode	Coverage	#Patterns	#Cycles
Stuck-at	95%	5.2 K	28 M
IDDQ	78%	Scan-10 + BIST-4	293 K
Burn-in	74%	Scan-100 + BIST	1.4 M
VBOX	82%	100	541 K
Transition	85%	45 K	135 M
Memory BIST	NA	NA	1.3 M

(a) The test modes support test pattern generation and application not only for manufacturing tests but also for those tests which are required for debug.

(b) The scan configuration has provided means to generate efficient pattern sets, by targetting modules specific to sub-systems and clock domains, on different tester platforms. An average reduction of about 25% to 40% patterns can be obtained for transition and stuck-at fault patterns.

(c) The test time and test cycles in Table 7 are the outcome of the test parallelism that has been achieved by the seamless integration of two IP cores with different scan and clock control requirements.

(d) The memory BIST implementation supports selective BIST for at-speed test application and debug. Also, unlike normal implementations, test coverage in the BIST logic is not sacrificed.

(e) The at-speed ATPG support with scan control and clocking options is being used to prioritise pattern sets for specific modules in higher frequency domains.

(f) Concurrent test of analog and digital modules has a direct impact on the test time, for both normal mode and stress mode tests. The test time, excluding burn-in, is reduced to 53%.

(g) High quality burn-in for analog and digital modules is supported with selectable groups of scan chains for debug.

This implementation and the resulting optimizations have helped meet the test cost and test quality goals, and have also significantly influenced the silicon test program development of this device. The scan architecture definition, memory BIST configuration, at-speed ATPG implementation, and concurrent test and burn-in methodology have been re-used in other similar SOC designs in TI. Such newer designs have benefited in one or more ways from amongst: (i) exclusive migration to low cost test platforms, (ii) ease of implementation of logic BIST, (iii) additional automation for pattern generation and validation for various clock and scan controls, (iv) creation of an optimal set of transition fault patterns, (v) additional infrastructure for concurrent testing, and (vi) various test program optimisations based on the above.

5. Conclusion

This paper has presented DFT techniques employed in TNETD7300, a complex mixed-signal ADSL modem SOC. The techniques described include scan architecture support for high-end and low-cost testers, concurrent test of digital logic with analog functions, at-speed testing for logic operating in multiple clock domains and clock frequencies, testing non-homogeneous IP cores together, configurable memory BIST operation, static and dynamic burn-in, and a comprehensive set of SOC test modes to support these operations for test and debug.

The application of these techniques has helped address various optimisations in the test quality and test time, and have influenced the silicon test program for this device. As part of the product development process, these techniques have helped identify several pattern generation and test cost optimisation possibilities, which are being

further investigated and applied to a similar class of SOCs designed in TI.

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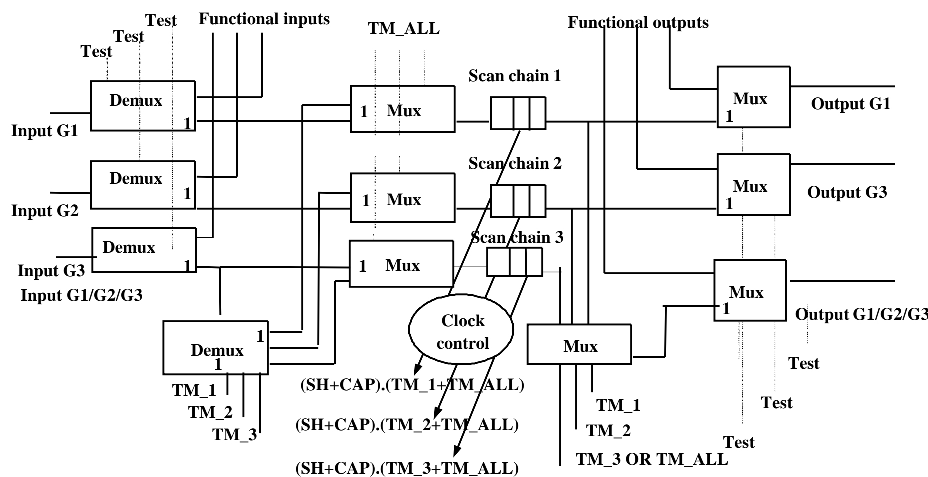

SH = Shift. CAP = Capture. TM_1/2/3 = Testmode1/2/3. TM_ALL = Testmode All.

Figure 3. Scan configuration with different scan groups.