Dielectric Breakdown in a 45 nm High-K/Metal Gate Process Technology

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INTRODUCTION AND BACKGROUND

The 2005 ITRS roadmap [1] predicted that SiON dielectrics would run into leakage/power limitations by the 45/32nm node. High-k (HK) dielectrics are a solution to overcome these limitations. When coupled with metal gate electrodes (MG); high CMOS performance can be achieved, and such stacks can provide 25X-100X reduction in gate leakage [2] relative to SiON while simultaneously reducing electrical oxide thickness by 0.7X. However, as has been reported extensively in the literature [1,3,4], several challenges need to be met, such as dielectric reliability, suppressing barrier leakage and Frenkel-Poole tunneling through process trap density control. In this paper, we present extensive breakdown results on our 45nm HK+MG technology. Polarity dependent breakdown and SILC degradation mechanisms have been identified and are attributed gate and substrate injection effects. Processing conditions were optimized to achieve comparable TDDB lifetimes on HK+MG structures at 30% higher E-fields than SiON with a reduction in SILC growth. Extensive long-term stress data collection results and a change in voltage acceleration are reported.

EXPERIMENTAL DETAILS

The HK+MG structures evaluated in this work were fabricated on 45nm process technology and have an Hafnium-based gate dielectric, a SiO_2-like interface layer (IL) and dual work-function metal gate electrodes to enable full CMOS operation. The transistor formation processing involves a HK first and MG last flow as reported by Mistry *et al.* [2]. The full stack (including the HK layer and the interfacial layer) has SiO_2 equivalent oxide thickness of 1.0nm and electrical T_{OX} of 1.40nm. Both single transistors and arrays of transistors are evaluated in this work. All transistor legs have a drawn gate length of 40nm/60nm and the electrical length is smaller. The TDDB stresses reported in this work were at Constant Voltage (CVS) unless specified otherwise. Gate leakage monitoring was performed by interrupting the stress; with the measurements conducted at two biases – nominal operating bias for the technology and a low voltage condition consistent with the low voltage sleep state of the processor. Process optimization impact is illustrated using samples fabricated with two processing schemes; an early unoptimized process flow (designated as *Initial*) and the fully optimized process flow (designated as *Final*). For reference purposes, we have used measurements and data collected on ultra-thin SiON+PolySi devices fabricated using a 65nm process flow [5]. To simplify notations, we designate NMOS inversion and accumulation as N_{INV} and N_{ACC} and the corresponding PMOS counterparts as P_{INV} and P_{ACC} respectively.

RESULTS AND DISCUSSION

The use of dual work-function metals leads to significant levels of asymmetry in the barriers for NMOS and PMOS gate leakage (Figure 1). In the N_{INV} mode, the effective tunnel barrier that the electrons see transitions from a trapezoidal one at lower gate biases to a triangular one in the HK layer at higher gate biases leading to a change in the rate of increase of gate fluence at these points. Band asymmetry and the work function values of the MG dictate that this transition occurs at relatively higher voltages in the P_{INV} and in the N_{ACC} modes as compared to N_{INV}/P_{ACC} modes of operation – correspondingly, higher values of dielectric breakdown voltage (V_{DB}) are observed for the N_{ACC}/P_{INV} modes as compared to the N_{INV}/P_{ACC} modes. However the relative magnitude of V_{DB} depends on the thickness and quality of the IL and HK layers. N_{INV} is the TDDB limiter for our gate stack.

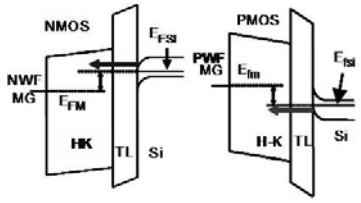

Figure 1. Band structure diagrams for N and P in inversion.

HK+MG band asymmetry also leads to polarity dependent SILC degradation driven by differences in trapping under gate vs substrate injection conditions. To illustrate this in greater clarity, data from the *Initial* unoptimized process is shown in Figure 2, where N_{INV} and P_{ACC} exhibit as high as 20X ~ 50X SILC increase before the onset of HBD, but P_{INV} and N_{ACC} modes show less than 5X corresponding SILC increase. The substrate injection cases can be attributed to electron trapping in the bulk HK. Such polarity dependent SILC behavior has been reported by several others in the literature [6-8] and the gate injection cases have been attributed to interface state creation and hole trapping in the IL. Gavartin *et al.* and others [7-10] attribute oxygen vacancies near the interface as the cause for these electron traps.

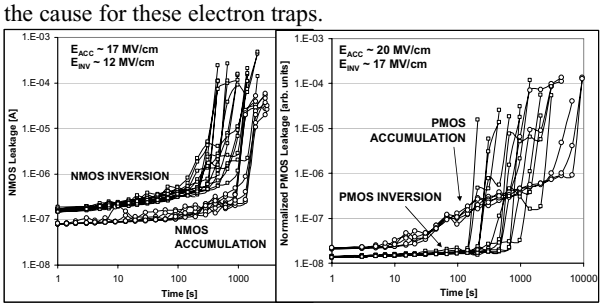

Figure 2. NMOS and PMOS data for inversion vs accumulation.

The density of electron traps is very strongly dependent on the fabrication and processing techniques involved. For the N_{INV} mode, the *Initial* process exhibits 20X ~ 50X SILC degradation (as shown in Figure 2). Zahid *et al*. and Degraeve *et al*. have proposed trap-assisted SILC models with one and two-trap clusters [11,12] whereas Okada *et al.* have attributed such SILC increases to the creation of multiple soft BD spots [13] on large area structures. SILC power law fit exponents observed in our data are consistent with those seen by Degraeve *et al.* [11]. High levels of SILC degradation are causes of concern for product applications, where this SILC degradation can have an unacceptable impact on long-term standby power stability. Through extensive process optimizations, we demonstrate that the trap density in the HK film was reduced dramatically. As can be seen in Figure 3, the *Final* optimized process flow exhibits negligible SILC degradation until the onset of HBD, even in the N_{INV} mode. We observe a strong correlation between this SILC degradation level and the trap density measured using charge pumping conducted – details in Pae *et al.* [14]. Charge pumping in the kHz range can probe shallow traps in the HK layer and we propose that these traps cause both SILC degradation as well as V_{TN} instability in N_{INV} operation.

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Corroborating evidence is provided by a 3X reduction in the NMOS PBTI Vt shift with the *Final* process flow as compared to the *Initial* flow [14]. Similar behavior has been reported by Crupi *et al.* and others [15,6] in the literature. All subsequent data presented in this paper are on the optimized *Final* process flow unless specified otherwise.

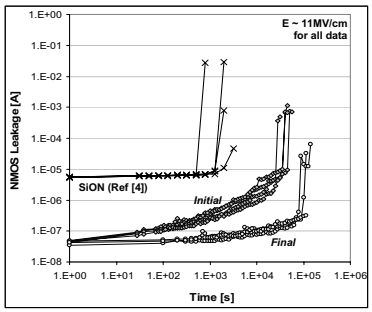

Figure 3. SILC degradation on *Initial* vs *Final* process flows – with SiON reference data [5] for comparison.

The results reported in this work use a HBD definition of transistor failure for TDDB lifetime. We observe qualitatively consistent gate leakage vs time trends under N_{INV} CVS conditions as those reported by Chowdhury *et al.* [16]. Extensive levels of optimization were performed to improve TDDB lifetime and Figure 4 compares matched field TDDB on the *Final* HK+MG flow vs SiON+PolySi and shows that the optimized HK+MG stack can support 30% higher E-field [2] at equivalent TDDB lifetimes. This represents a significant intrinsic reliability improvement over the reliability of the mature and established 65nm Si process [5]. TDDB lifetimes were measured for structures ranging from cache bitcell transistors to 4.5Mb SRAM cache test vehicles as shown in Figure 4; and we report consistent scaling with gate area over a range of 8 decades - evidence that defectivity levels on the *Final* optimized process flow are well managed. The area-scaling data corresponds to a Weibull Beta value of 1.4 with a conventional model, which is in line with expectations for the thickness of the gate stack.

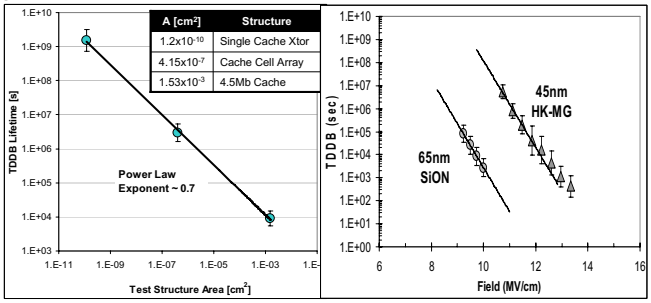

Figure 4. Right plot shows TDDB vs Field data for HK-MG [2] and SiON [5] and left plot shows area scaling of TDDB measured on cache bitcell transistors, array cells and 4.5Mb SRAM cache.

As a consequence of reliability improvement on the optimized HK+MG flow, TDDB characterization requires e-fields greater than 14MV/cm in order to have feasible time-scales for high volume testing. Extensive low stress bias TDDB experimentation was performed to ensure the accuracy of extrapolating high e-field TDDB to operating lifetimes. Data collection was performed on several process variants, where each leg of the experiment consisted of up to 3+ months of CVS testing to encompass the 10~16MV/cm e-field range. Figure 5 shows the median TDDB lifetimes collected on the *Final* process, and the data exhibits a clear transition in the acceleration behavior that occurs at ~12MV/cm. This acceleration factor change is observed to occur at an e-field value similar to the point of transition in gate leakage from a direct tunneling (DT) regime to a Fowler-Nordheim tunneling (FN).

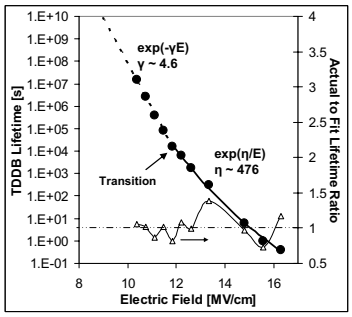

Figure 5. Long-term TDDB measured on the *Final* process flow shows a change in the acceleration slope at ~12MV/cm.

Such a change in the tunneling mechanism is expected for bilayer dielectric stacks and has been predicted for HK+MG by Dunga *et al.* [17]. At lower biases, direct tunneling through the entire HK+MG stack causes gate fluence to drop rapidly – and Degraeve *et al.* [6] have used a fluence driven model to predict a strong increase in TDDB lifetimes at voltages near the operating range. However, very limited data exists in the literature for such low voltage TDDB data on HK+MG stacks, and the extensive data reported in this research work aims to address this gap. This behavior is not unique to HK+MG stacks and a similar transition in the TDDB acceleration slopes has been reported by Hu *et al.* [18] in SiO_2 data at high e-fields, where the authors have attributed this effect to a DT to FN tunneling transition. With accurate empirical fitting, an exp(E) relation was used in the low field regime, and the high field regime data were fit with an exp(1/E) relation which are consistent with Hu *et al.* and McPherson *et al.* [18,19]. The existence of an acceleration factor transition places strong emphasis on the importance of TDDB data collected at low e-fields. Such data is extremely important for the accurate modeling and assessment of use-condition reliability of HK+MG stacks that can support high e-fields.

CONCLUSION

Dielectric breakdown was studied on 45nm HK+MG process flow through extensive experimentation. An unoptimized process showed large trap-related SILC degradation consistent with literature reports, but this degradation was made negligible through process flow optimizations. Low voltage long-term TDDB lifetime results on HK+MG transistors with the optimized process flow demonstrate excellent intrinsic TDDB reliability that supports 30% higher e-field as compared to SiON+PolySi. The observed data scales well with gate area from single transistors up to fully integrated SRAM test blocks.

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