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We present a new logic family, Differential Current Switch Logic (DCSL) for implementing clocked CMOS circuits. The circuit is in principle a differential cascode voltage switch logic circuit (DCVS). In comparison to other forms of clocked DCVS, DCSL achieves better performance both in terms of power and speed by restricting internal voltage swings in the N tree. Automatic lock-out of inputs on completion of evaluation is a novel feature of the circuit and allows new implementation of logic functions and the possibility of operating with reduced voltage swings. SPICE simulations carried out with the MOSIS 1.2μ process indicate that DCSL is better than similar clocked DCVS circuits by a factor of two both in terms of power and speed, for moderate tree heights.

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1 Introduction

In the quest for achieving low-power, circuit design techniques have largely overlooked differential cascode logic circuits (DCVS) in favor of traditional CMOS styles. The high activity of DCVS gates and the need to route differential signals cause them to compare unfavorably with respect to implementations using static CMOS, complementary pass transistor logic, and differential pass transistor logic [1, 2]. However DCVS gates do offer the potential of having high fan-in which leads to a reduction in logic depth, high speed, and the capability of generating completion signals for asynchronous operations.

This paper presents a new clocked DCVS logic family called Differential Current Switch Logic(*DCSL*). The salient features of this logic family are: sensing of differential currents

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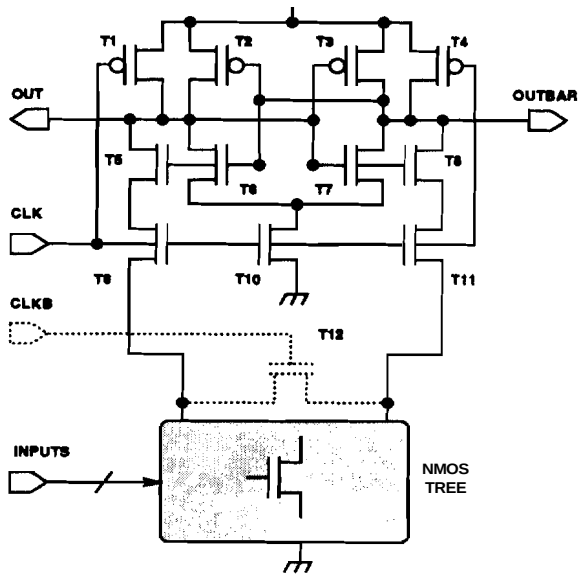

Figure 1: Precharge high *DCSL*

in an evaluation NMOS transistor tree, a very low voltage swing in internal nodes of the NMOS transistor tree, and an automatic lock-out of inputs once gate evaluation is complete. These features directly translate into high fan-in gates, low power consumption, and the possibility of implementing logic functions in new ways. We first describe the *DCSL* gate and its operation. The new implementation of logic functions, and the possibility of operating the gate with reduced voltage swings are illustrated next. SPICE simulations using the *MOSIS* 1.2μ process indicate the advantages of this gate over similar clocked *DCVS* gates which do not restrict the voltage swing of internal nodes.

Differential Current Switch Logic

Differential current switch logic *(DCSL)* belongs to the class of clocked differential cascode voltage switch logic circuits. *DCVS* gates operate at all times with both true and complementary signals. Evaluation is carried out with a complementary NMOS transistor tree connected to the true and complementary outputs of the gate. The design constraint for the NMOS transistor tree is that for all possible input combinations at most and at least one path to ground exists from one of the output nodes. Various forms of *DCVS* gates differ in the circuitry present for generating the output.

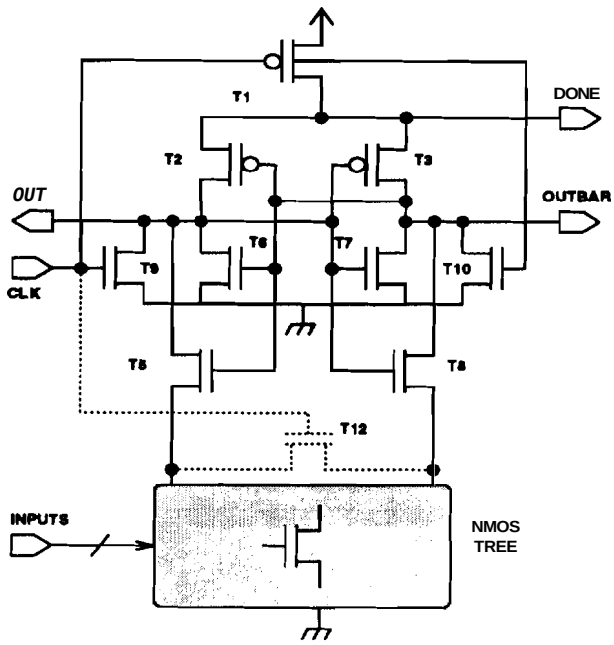

Figure 2: Precharge low *DCSL*

The structure of the *DCSL* gate is shown in figure 1. It consists of an N evaluation tree, a cross coupled inverter pair (*T2, T3, T6* and *T7*) and precharge transistors (*T1* and *T4*). The presence of transistors *T5* and *T8* is what differentiates this gate from other *DCVS* logic gates. Operation of the gate starts with *CLK* low and nodes *OUT* and *OUTBAR* being charged high. Gate evaluation begins with stable inputs to the N tree and *CLK* going high. *CLK* high switches *T9, T10* and *T11* on while *OUT* and *OUTBAR* being high ensure that *T5, T6, T7* and *T8* are switched on. *OUT* and *OUTBAR* discharge towards ground through *T6, T7* and *T10*. The discharge of *OUT* and *OUTBAR* is not symmetrical because the N tree assures that one of the outputs say *OUT* has a stronger path to ground. This causes *OUT* to fall faster than *OUTBAR*. The cross-coupled inverter functions as a sense-amplifier and boosts the output voltage differential in the right direction. Once the inverter switch threshold is crossed by *OUT*, *OUTBAR* swings high. The low going transition of *OUT* disconnects the N tree from *OUTBAR* by progressively cutting of transistor *T8*. This is unlike other *DCVS* circuits where the NMOS pull-down tree is never disconnected from the output. DCVS circuits charge the internal nodes of the NMOS tree up to $V_{CC} - V_{tn}$ (V_{CC} is the supply voltage *5volts* and V_{tn} is the threshold voltage of the N device around *lvolt*), whereas *DCSL* charges internal nodes to much smaller voltages of the order of *lvolt*. The gate comes to rest in a state

with OUT low and $OUTBAR$ high. $T12$ may be required to prevent charge buildup on internal nodes of the gate.

On completion of evaluation, the fact that the high output ($OUTBAR$ in the previous case) is disconnected from the NMOS tree assures us that further changes in inputs do not propagate to the output. This is unlike most *CMOS* logic styles, where changes in the inputs of clocked logic, cause DC through currents, or the gate output being destroyed. Strict adherence to the design constraint of building *DCVS* NMOS trees is no longer required. Gate inputs may cause paths to ground in both halves of the NMOS tree. However assuring that one of the paths has a stronger pull-down than the other, allows the *DCSL* gate to evaluate its inputs. On completion of evaluation no static: current paths from V_{CC} to GND exist.

The above discussion considers *DCSL* logic with outputs precharged high. Figure 2 shows a *DCSL* gate with outputs which are charged low. The gate imposes a lower clock load and has the advantage of generating completion signals *(DONE)*. Our simulations compare the above gates with similar *DCVS* design styles, namely Latched Cascode Differential Logic *(LC'DL)* [3], and Enable Disable Cascode Logic *(EDCL)* [4]. *LCDL* has a structure similar to figure 1 while *EDCL* is similar to to figure 2. *DCSL* gates in both cases show much better rise times, as well as lower power consumption in comparison to comparable *DCVS* gates. The lower power consumption is primarily due to smaller internal voltage swings in the range of lvolt as compared to 4volts in *DCVS* designs. All the above logic circuits use a cross-coupled inverter between the output nodes which allows construction of high fan-in gates that are free from charge leakage problems.

DCSL introduces transistors *T5* and *T8* in order to cut-off the NMOS tree from the output which is driven to a logic high. The strong positive feedback inherent in this structure can upset the operation of the gate if the two halves are not balanced. The circuit will not only amplify differential currents arising from the NMOS tree but also any other current differentials arising from unbalanced output loads. This is especially true for the circuit in figure 2. Balanced layout techniques need to be employed to ensure symmetrical halves for *DCSL* gates. In cases where the output loads cannot be guaranteed to be the same, buffering close to the gate needs to be employed.

DCSL circuit techniques

In this section we illustrate circuit techniques using features of *DCSL* gates. We particularly refer to the self-lockout of inputs which occurs when the gate evaluates. A

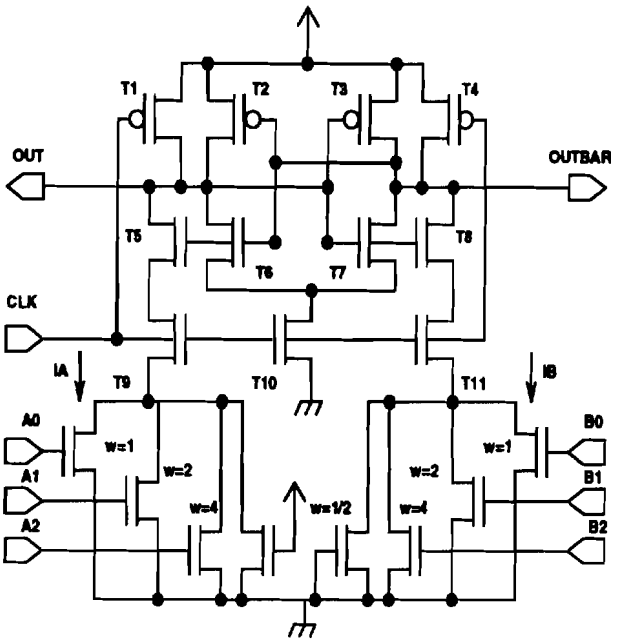

Figure 3: *DCSL* Magnitude Comparator (A $\geq$ B)

DCSL gate on completion of evaluation does not have any paths from the supply to the ground irrespective of the state of the NMOS tree.

Figure 3 shows a magnitude comparator circuit. The circuit as shown, compares inputs A and *B* (3 bit vectors) and generates outputs indicating whether *A* is greater than B. This (circuit converts the input say *A* into an analogue current value (IA in figure **3).** The *DCSL* circuit compares IA and IB and generates an output dependent on the differential of IA and IB. Both halves of the NMOS tree, have paths to ground for all values of *A* and B (except B =0). The functionality of the gate is correct as long as the accuracy of the conversion of logic inputs to currents is preserved. For the circuit shown this translates into accurate logic high values. Area of the gate would increase drastically with increase in the number of bits being compared, and hence the design as shown may be impractical for more than a few bits. The circuit does illustrate the possibly of using *DCSL* for the comparison of differential currents.

More important from a system level viewpoint is the design shown in figure 4. The fact that the transistors in the NMOS tree for *DCSL* gates need not be turned off completely is utilized in evaluating inputs with a restricted voltage swing. Figure 5 shows the performance of a *DCSL* gate with inputs which swing partially. Such circuits would be advantageous in driving logic voltages on lines which are heavily loaded. In the circuit

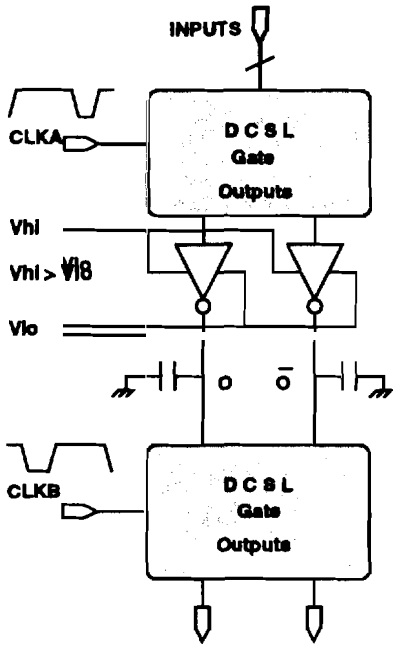

Figure 4: Reduced Voltage Swing *DCSL*

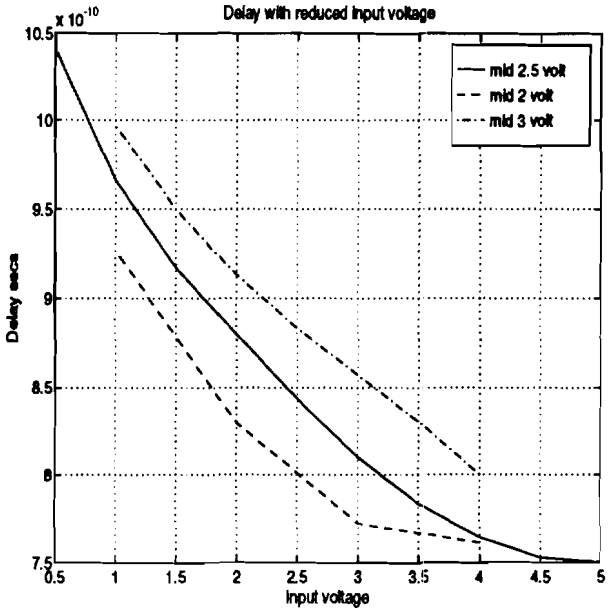

Figure 5: performance with reduced input swings

shown $GND \leq V_{LO} < V_{HI} \leq V_{CC}$ (V_{CC} and GND are the supply and ground voltages). The voltage swing on lines is limited to $V_{HI} - V_{LO}$.

4 Simulation Results

SPICE simulations for the circuits described in this paper were carried out using the *MOSIS* 1.2μ *CMOS* process. Results obtained with various tree heights for a parity generator circuit are shown in figure 6 and figure *8.* All transistors in the circuits simulated are equally size with width 3μ, except for transistor *T1* in figure 2 which is of size 6μ. SPICE simulations are carried out using the level three spice model at 27°C.

Figure 6 shows the power advantage of the new circuits in comparison to enable-disable DCVS circuits and *LCDL* gates. This graph shows that energy consumption per transition shows a lower dependence on the number of internal nodes for *DCSL* gates. *DCSL* logic favors implementing higher complexity gates. Figure 8 shows that *DCSL* in general exhibits far superior delay times. This advantage increases as tree height :increases. The circuit shown in figure 2 has the lowest power consumption while the *DCSL* circuit in figure 1 has the best delay characteristics. The power advantage of *DCSL* is primar-

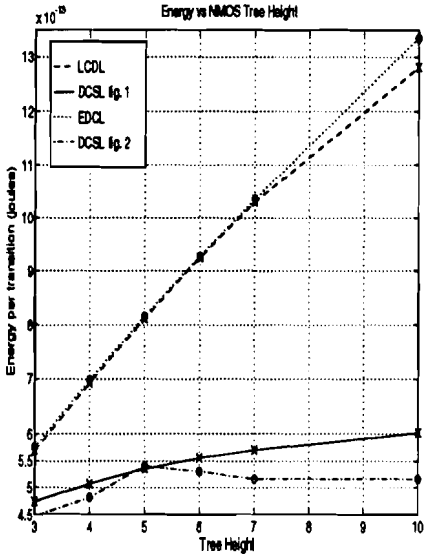

Figure 6: Energy consumption

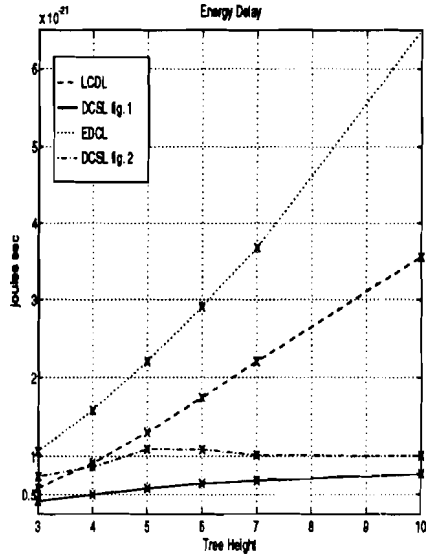

Figure 7: ***Energy*** x ***Delay*** vs. Tree Height

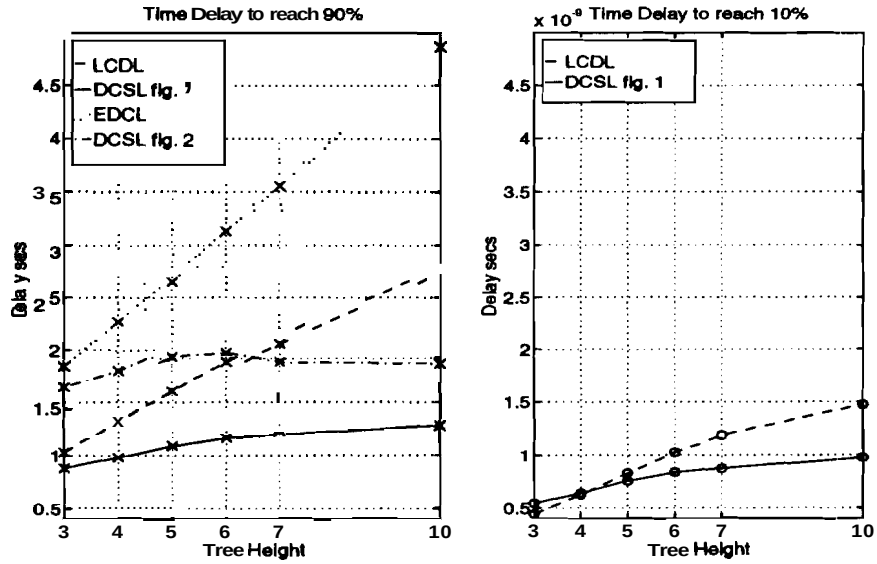

Figure 8: Comparison of gate delays

ily because of the very low internal voltage swings. Internal node voltages in standard *CMOS* gates is of the order of 3.5volts. Internal node voltage swings for the *DCSL* circuit in figure 1 and figure 2 are of the order of lvolt and 0.3volts, respectively.

A plot of the energy delay product shows the merits of the new circuits. Figure 7 indicates the better energy delay products of *DCSL* gates. The energy delay products for *DCSL* gates rises slowly with respect to an increasing NMOS tree height. Delays shown in this graph are the gate delay for outputs to rise to 90% since this is the largest delay for these circuits.

5 Summary

A new clocked logic family, Differential Current Switch Logic *(DCSL)* is presented in this paper. By reducing internal voltage swings in the gate, we achieve appreciable power savings and better speed as compared to comparable clocked cascode voltage switch circuits. In our opinion the circuit technique used to cut off NMOS evaluation trees is fairly generic and should be applicable to most cascode voltage switch logic families. In fact this paper illustrates two forms of *DCSL* gates. Insensitivity to inputs after completion of evaluation allows us to reduce the restrictions on the design of the NMOS tree. This allows simpler implementation of logic functions, and the possibility of operating logic with reduced output voltage swings. *DCSL* circuit techniques can be fully exploited in system designs which impose stringent requirements on power and delay of combinatorial logic bloclks. The ease of generating completion signals, automatic lock-out of inputs, and the low-power of *DCSL* gates make it a candidate for asynchronous logic design styles. The drawback of *DCSL* is that layouts should ensure a symmetrical load on the outputs as well as the NMOS tree, for proper gate operation.

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