Missouri University of Science and Technology
Scholars' Mine

Electrical and Computer Engineering Faculty Research & Creative Works

Electrical and Computer Engineering

01 Aug 2008

Differential Vias Transition Modeling in a Multilayer Printed Circuit Board

Matteo Cocchini

Wheling Cheng

Jianmin Zhang

John Fisher

et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele_comeng_facwork/748

Follow this and additional works at: https://scholarsmine.mst.edu/ele_comeng_facwork

Part of the Electrical and Computer Engineering Commons

Recommended Citation

M. Cocchini et al., "Differential Vias Transition Modeling in a Multilayer Printed Circuit Board," *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility (2008, Detroit, MI)*, Institute of Electrical and Electronics Engineers (IEEE), Aug 2008.
The definitive version is available at https://doi.org/10.1109/ISEMC.2008.4652164

This Article - Conference proceedings is brought to you for free and open access by Scholars' Mine. It has been accepted for inclusion in Electrical and Computer Engineering Faculty Research & Creative Works by an authorized administrator of Scholars' Mine. This work is protected by U. S. Copyright Law. Unauthorized use including reproduction for redistribution requires the permission of the copyright holder. For more information, please contact scholarsmine@mst.edu.

Differential Vias Transition Modeling in a Multilayer Printed Circuit Board

Matteo Cocchini[1], Wheling Cheng[2], Jianmin Zhang[2], John Fisher[2], Jun Fan[1], James L. Drewniak[1], Yaojiang Zhang[1]
[1]The UMR/MST EMC Laboratory, Missouri University of Science and Technology (former University of Missouri-Rolla), Rolla, MO, USA
[2] Cisco Systems, San Jose, CA, USA

Abstract— **A 26-layer printed circuit board including several test sites has been analyzed. All the sites have a transition from coupled microstrips to coupled striplines through signal vias. Differential measurements have been performed on some of these test sites to estimate the effect on S-parameters and eye diagrams due to via and antipad radius variation, and different lengths of via stub. The focus of this paper is on a test site with a transition from top to the sixth layer. At the same time, a physics based circuit model has been assembled in a spice-based simulation tool and a full-wave model has been generated as well. The paper will show that the process of modeling can require a series of adjustments to get reasonable results. A brief discussion about possible issues associated with fabrication tolerances is presented in the last chapter.**

***Keywords*—Differential signal, noise coupling, signal via transition, via capacitance, cavity model, ground vias**

I. Introduction

The purpose of this paper is to show how a complex geometry with several layers can be simulated quickly using a combination of cavity model and circuit based tools as ADS or HSPICE. During the process of modeling a series of modifications have been applied to the model to take into account all the physical phenomena and differences between nominal and real dimensions. It will also be shown that fabrication tolerances can have a large effect on the resultant S-parameters.

The increasing complexity of modern PCBs with a larger and larger number of layers and very thin dielectric often creates problems in modeling these structures with full-wave tools. The minimum mesh step to represent all the particulars in the structure with good detail should be very small; this means that for a large PCB several million cells are probably needed. Of course, this will likely lead to many hours of simulation time; if the goal is to perform parametric simulations it is better to avoid large memory usage and computational resources. A circuit model can be made based on the geometry to get very quick results and, therefore, control quickly parametric variation of some variable to more easily manage tolerance variations.

Cisco Systems and the MST/UMR EMC Lab have realized the test board used in this article. The test board is a 10x10 inches PCB with several small test sites where differential via transitions are present. The test vehicle is divided into 5 main areas based on via and antipad diameter, via pad diameter, microstrips and striplines shapes and ground via location and shows a 26 layers stack-up with 12 solid copper planes. First, a series of sites having the same via diameter and without ground vias close to the signals have been milled to show the microstrips and striplines pads. Next, a series of differential measurements were performed using microprobe station and network analyzer to extract S-parameters. At the same time a physic-based circuit model has been made. A current signal propagating between top and inner layers and returning to the source generates propagating waves reflected on the board edges. Due to this, the S-parameters show many resonances. The signal propagation depends strictly on the data rate of interest.

After the model realization, an S-parameters comparison was done between differential measurements, circuit model and Microwave Studio.

II. PCB Test Geometry and Measurement Setup

In Fig.1, the PCB area with the sites of interest is shown. The label “P” visible on each site is related to the via-to-via distance, the “D” is associated with via diameter and the “L” is followed by the layer where striplines are connected. Although many sites have been milled, only the P2-D1-L6 test site has been studied in this paper. The nominal via diameter for these geometry is 22 mils with an antipad diameter of 50mils. The distance between the two vias, center to center, is 60 mils.

The PCB stack-up is shown in Fig.2. The geometry consists of 26 layers with 12 copper solid planes and 12 possible positions to connect the traces; for the site of interest, the transition is between top to sixth layer.

978-1-4244-1699-8/08/$25.00 ©2008 IEEE

Authorized licensed use limited to: University of Missouri. Downloaded on January 5, 2009 at 11:55 from IEEE Xplore. Restrictions apply.

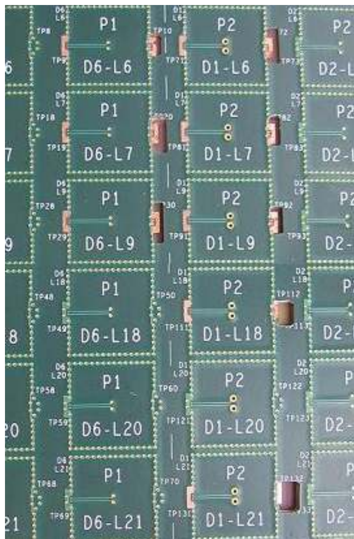

Figure 1. Top view of P2-D1 series of test sites

With these test structures, it is possible to study only microstrip to stripline transitions and not stripline to stripline. All the test sites are separates each other by means of several ground vias those limit the field propagation inside a confined region 500x500 mils large.

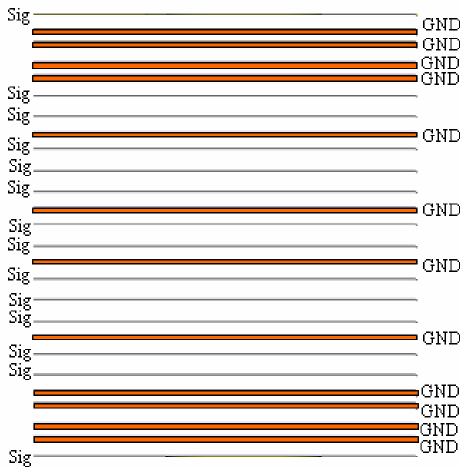

Fig.2. Board Stack-up

To perform differential measurements an Agilent 8720ES with an ATN 4110 test set operating at 40 GHz was utilized. The maximum frequency selected to compare measurements and simulations was 18GHz due to the maximum frequency allowed by the microprobes. The microprobes used are Cascade 500um pitch ACP probes and the microprobe station is a Cascade analytical probe station. The test sites were milled out to expose the launching structures and allow the signal to smoothly transition from the probe to the device under test. Figure 3 shows a cross-section of one of the sites that has been milled from top to sixth layer.

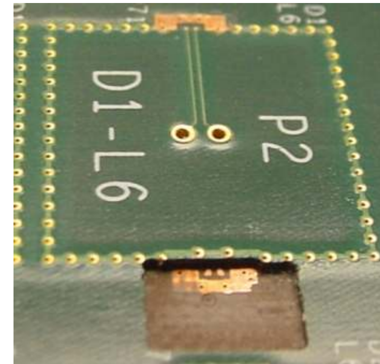

Figure 3. Detail of test site P2-D1-L6

III. MODELING APPROACH

A physics-based via-plane model combined with transmission lines models for traces is the approach used in this paper. The main idea is to divide the whole stack-up into several subsections, each corresponding to one solid power/ground plane pair [1,2]. Each block is then modeled using the cavity model theory; this method has been widely validated in previous publications and allows an accurate evaluation of the power-plane impedances [3]. At the end, the blocks are linked by enforcing current and voltage continuity conditions across the via-to-antipad region. This assumption is valid since it is possible to define interconnection ports across the antipads: in the antipad region the field is considered purely TEM since it shows a coaxial geometry. Using this approach saves time and computational resources compared to the classical full-wave models. Furthermore, a physics-based circuit model relates geometric features to circuit elements in a manner that it is easy to optimize the design and integrate the whole structure with external components as ICs or decoupling capacitors. With this kind of circuit, it is possible to perform simulations in both frequency and time-domain; complex structures where tens of power plane pairs and vias are supported as imposed by modern PCB design.

The differential circuit model is composed of four main parts: transmission lines (coupled miscrostrips and striplines), transmission line-to-via transition, antipad capacitances and cavities as shown in Figure 4. Coupled microstrips and striplines have be represented using a cascade of Π cells since the coupled transmission lines model implemented in ADS does not consider a reference for the return path and the maximum frequency of interest does not allow to represent the traces as simple single lumped element. As for the transition from traces to via, different effects as capacitive and inductive

Authorized licensed use limited to: University of Missouri. Downloaded on January 5, 2009 at 11:55 from IEEE Xplore. Restrictions apply.

coupling between the non-TEM part of the traces, the two via pads and between pad and solid plane have been computed for the geometries P2-D1 (related to a via radius of 11mils and antipad radius of 22mils nominal) using full wave methods. The capacitances across the antipad between vias and copper solid planes were calculated using an empirical formula based on curve fitting.

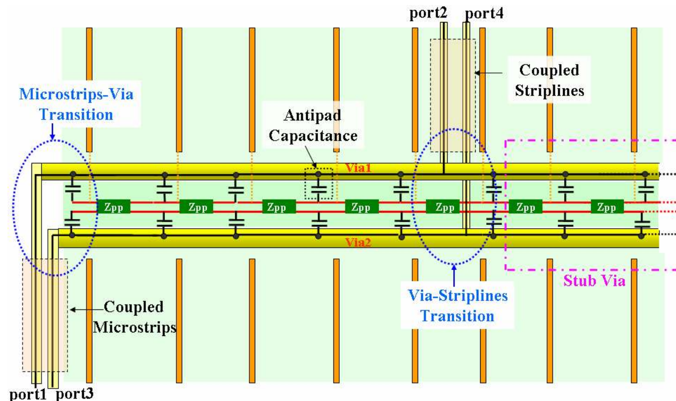

Figure 4. Geometry and equivalent circuit model

To represent the power-plane impedance, including frequency dependent metal and dielectric losses, reflection at boundaries and mutual inductive effects between the two vias, a tool based on cavity model has been utilized.

IV. Model vs. Measurements – Model Improvements

During the process of modeling and measurements, several difficulties have been encountered due to the complexity of the board. In this chapter, a series of improvements on the model based on fabrication process variations and theoretical observation will be shown.

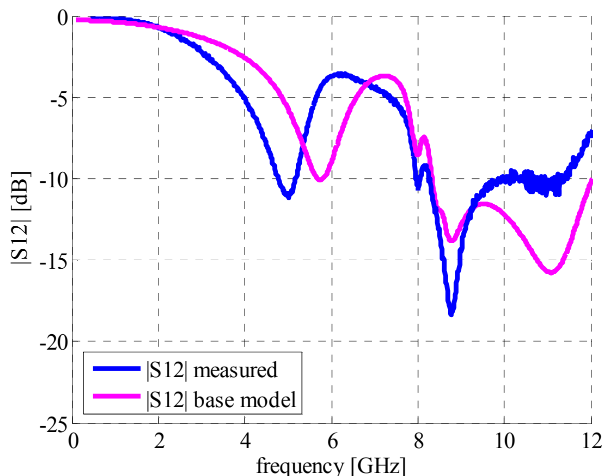

Figure 5. |S12| measurements vs. initial model

In Figure 5 the curves are based on the original model used for this geometry. The circuit has been created assuming constant εr for the dielectrics (no Debye) and considering the traces as simple lumped elements. The blue curve is the measured insertion loss and the pink one is obtained by the initial version of circuit model (called "base model" in the label). The measured results presents noise above 10GHz probably due to some difficulties experienced during the calibration procedure; this is one of the reasons why the focus of this analysis has been centered mainly to frequencies below this value. The model catches the large resonance at 9GHz and the small one at about 8GHz, but the big dip at about 5Ghz is completely missed by the circuit. It will be shown later in this article that this first big resonance is associated to the stub length since it does not corresponds to any plane resonance.

Based on the cross-section measurements on the PCB the real thicknesses of the power plane pair have been modeled in ADS. The results are shown in figure 6. The real geometry shows different values of plane thickness compared to the nominal geometry initially used. Even the dielectric constant (still considered frequency independent) was slightly different. This comports a variation in the via inductances, antipad capacitances and even plane resonances resulting in the general shift toward lower frequencies. This is clear comparing the green curve with the pink one. The effect of the stub seems to be represented better by the new model but the variation in the dielectric properties moves far away the plane resonances.

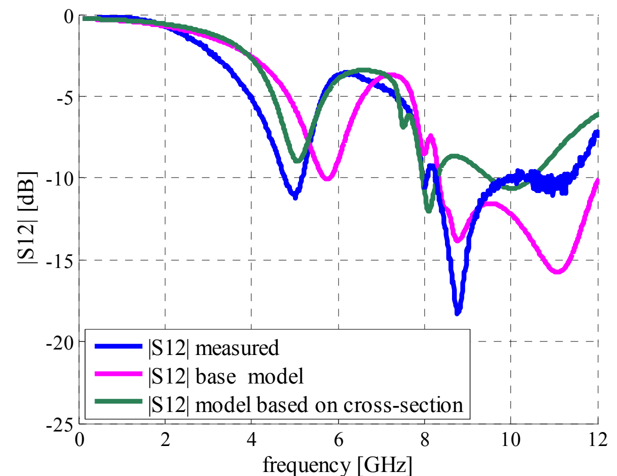

Figure 6. |S12| measurements vs. initial model and model with dimensions based on cross-section measurements

Within the same power-plane pair, more than one dielectric is present. In addition, those dielectrics have frequency-dependent properties. In the simple cavity model approach those aspect are not included so a model that take into account a series of Debye material in the same cavity has been developed. In figure 7, the effect of implementing frequency

Authorized licensed use limited to: University of Missouri. Downloaded on January 5, 2009 at 11:55 from IEEE Xplore. Restrictions apply.

dependent material on the simulated insertion loss is shown for test site P2D1L6. The frequency dependence of the dielectric leads to an improvement on the results especially observing the "shape" of the curves. Actually, the black curve with Debye material looks similar to the measurements except for a general shift of about 400MHz and 2dB in amplitude.

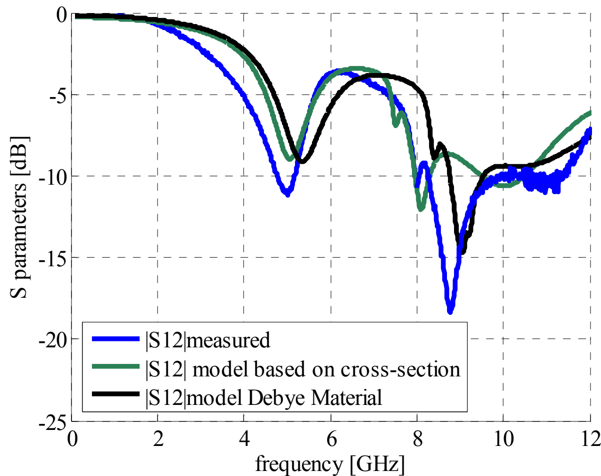

Figure 7. $|S_{12}|$ including Debye materials

Another model of the test site P2D1L6 has been realized using CST Microwave studio (Figure 8). Debye materials and dimensions based on the cross-sectional measurements are taken into account. The launching pads, including the hole made to give signal to the striplines, have been accurately modeled.

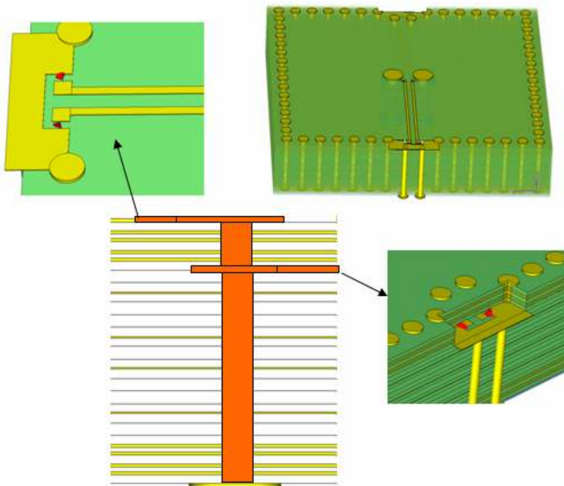

Figure 8. P2D1L6 site - Microwave Studio model, via and launching pads

The comparison between the circuit and full-wave in figure 9 shows that the two methods agree in a surprising mode considering the complexity of the geometry. Anyway, the results show clearly that both the models do not correctly represent something in the real geometry.

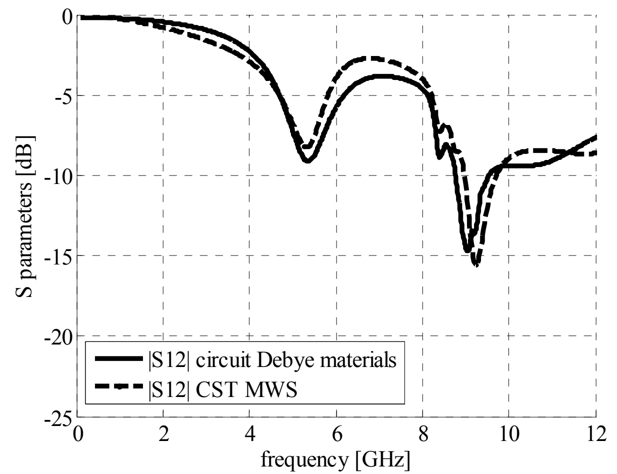

Figure 9. $|S_{12}|$ Microwave Studio vs. circuit model

Another modification has been applied to the circuit based on field distribution considerations. Observing the via-to- antipad region shown in figure 10, a term considering the radial electric field (red capacitor in figure) has to be added to the overall capacitance [1][2].

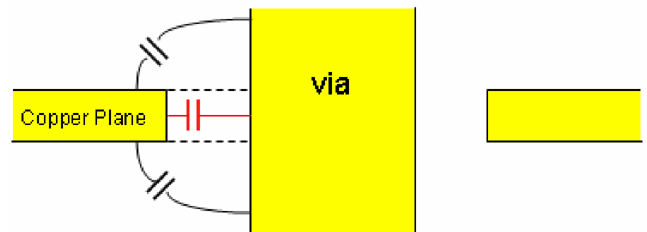

Figure 10. Via-to- antipad capacitance components

Figure 11 shows the impact of this modification on the curves. The stub resonance is the only one shifting adding this additional capacitance, whereas the plane resonances remain almost constant. Using this additional capacitance the frequency discrepancy at 5GHz is reduced to about 150MHz.

In figure 12 the impedances looking at one of the ports where the via is defined is shown for the different cavities composing the circuit model. In the same graph, the overall |S12| parameter is included.

Authorized licensed use limited to: University of Missouri. Downloaded on January 5, 2009 at 11:55 from IEEE Xplore. Restrictions apply.

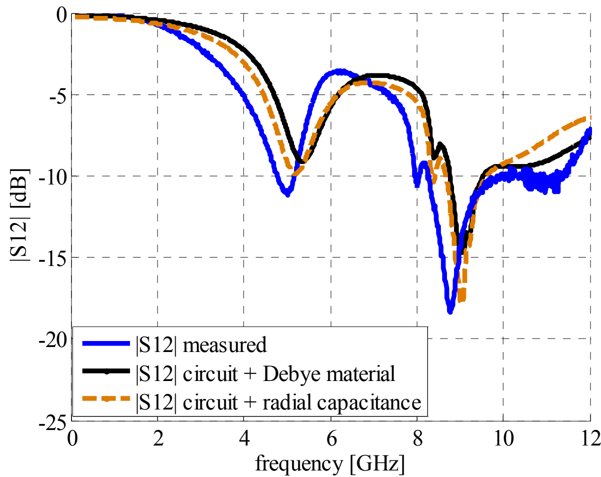

Figure 11. Effect on |S12| of radial capacitance term

It is possible to notice that, in correspondence of the peaks in the impedances, there is a dip in the S-parameter; these are the resonances associated to the planes. It can be observed that the resonance at about 5GHz is not related to planes so it depends on the stub length; the dominant parameter that defines a shift in frequency of this stub is the capacitance across the antipad region. This fact explains as the 9GHz resonance (planes) is not shifted toward low frequency as the stub resonance does.

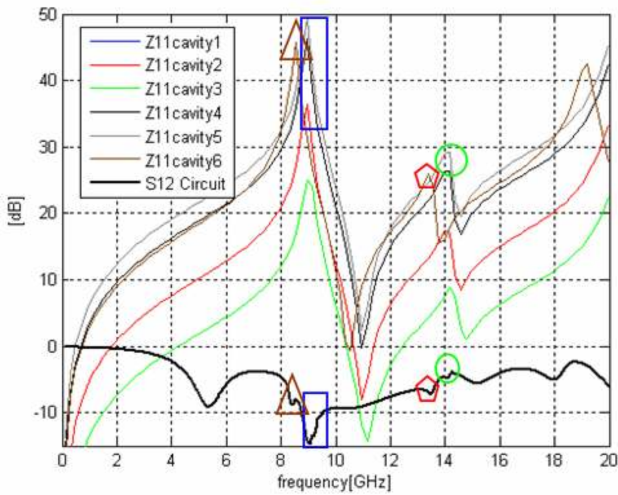

Figure 12. simulated |S12| curve plotted with the plane impedances

In figure 11 a noticeable discrepancy at high frequency between model and measurements has been observed. To try to represent better the behavior at this frequencies range, a cascade of 10 small Π cells has been used to represent the TL. In Figure 13 the capacitance within the red square represents the capacitive coupling between the first 25mils of microstrips. In the same figure, the elements included in the green rectangle are the self and mutual inductances for this small portion of coupled traces. Previously, the transmission lines where modeled as a single cell; this approximation starts to fail at high frequency when the traces are not anymore electrically short.

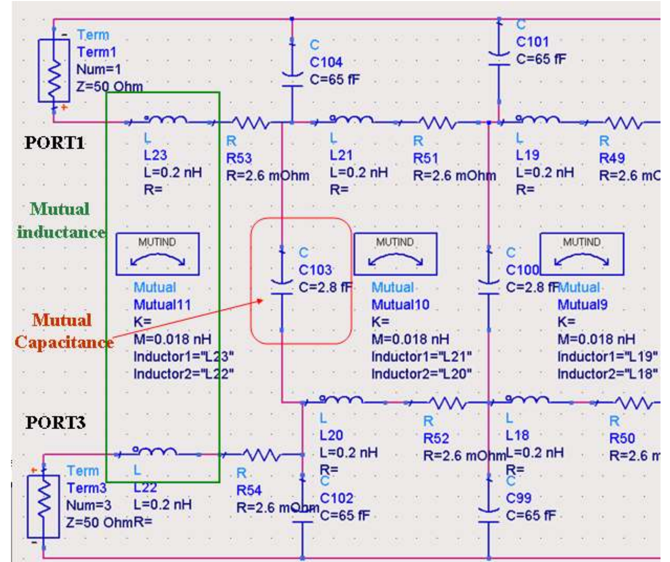

Figure 13. Cascade of the first two Π blocks related to coupled microstrips

Adding this feature to the model, the model results agrees better with the measured data above 9 GHz as expected and remain almost identical for lower frequencies. These results are illustrated in figure 14.

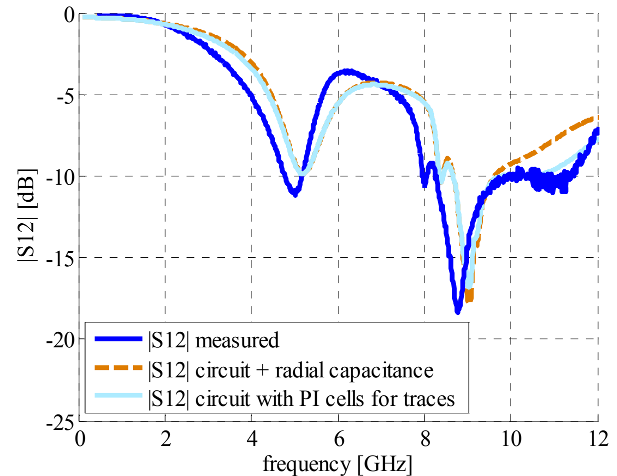

Figure 14. Effect on |S12| of the cascade of Π cells to represent transmission lines

Authorized licensed use limited to: University of Missouri. Downloaded on January 5, 2009 at 11:55 from IEEE Xplore. Restrictions apply.

Another problem found during this study is related to measurement. In fact, as noticed at the begin of this paragraph, a evident noise affect the measurements for high frequency, resulting in difficulty to use them as a solid reference to compare with the model. In addition, the S-parameters data violated passivity in almost the entire frequency range, especially above 5 GHz, possibly due to calibration errors or bad probes contact. This is shown in Figure 15: the passivity check of the measure data is done using a 2-norm of the scattering matrix for each frequency. Passivity is violated for a large range of frequency, especially above 11 GHz.

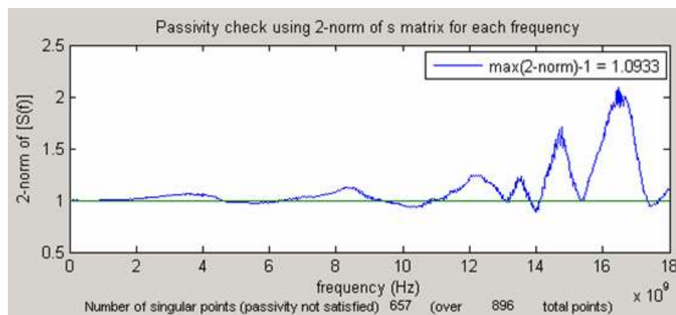

Figure 15. Measurements passivity check

V. Effects of Tolerances on Modeling

The impact of a +/- 20% variation in the dielectric constant is shown in figure 16 and a +/- 20% variation of via-to-antipad capacitance in figure 17. This has been done to study the effect of possible fabrication tolerances in the material and especially in the via placement process.

Figure 16 shows that modification of the dielectric constant has a relevant impact on the plane-related 9.5GHz resonance in the amplitude of the differential mode $|S_{DD12}|$. It is apparent from the model results that the resonances always occur at lower frequencies compared to the measurements, but a dielectric constant decrease of 20% can improve the accuracy of the circuit model, thus reducing the discrepancy with measurements from about 400MHz to 200MHz. This effect can be explained considering the formula relating resonant frequencies and dielectric constant in a rectangular cavity:

$$f_{res} = \frac{1}{2\pi\sqrt{\varepsilon\mu}}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \qquad (1)$$

where a and b are the largest and smallest dimensions of the rectangular parallel-plates, respectively; ε and μ are the dielectric constant and permittivity of the dielectric material respectively. In formula (1), the resonant frequency and the dielectric constant are inversely proportional [4].

Observation of the geometry cross-section shows relevant changes in the via geometry compared to the nominal values.

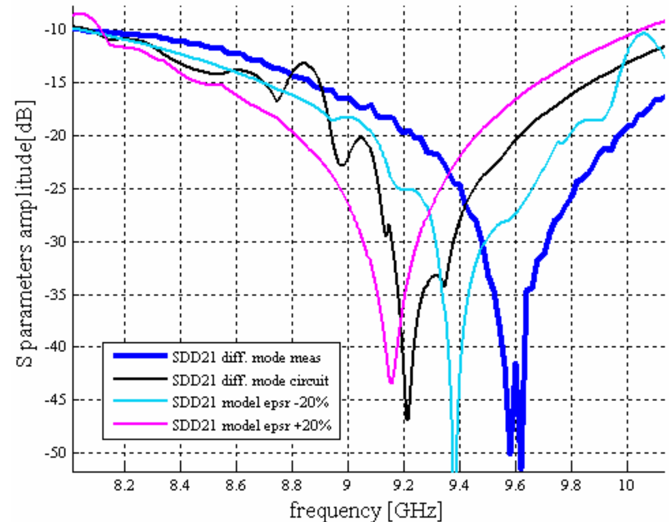

Figure 16. $|S_{DD12}|$ measurement vs. model varying dielectric constant value

An offset with respect to the vertical axis has been observed, as well as a large offset with respect to the nominal via center. Obviously, these geometric variations affect strongly the results: even a 20% variation in the via-to-antipad capacitance can generate an approximate 200MHz shift of the 5GHz stub-related dip as shown in figure 18.

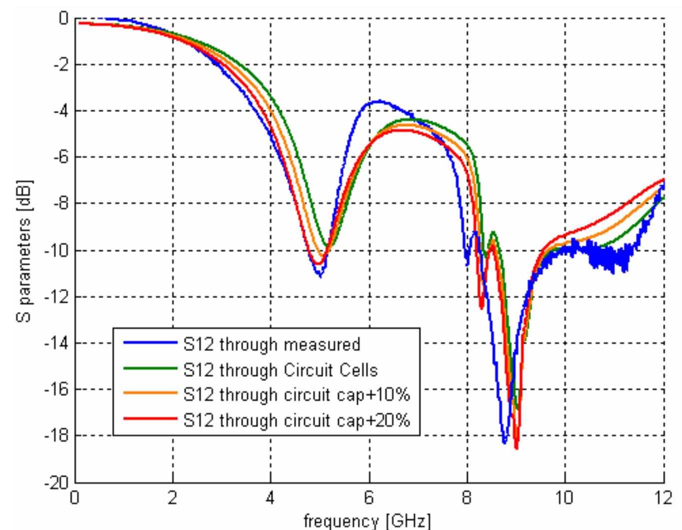

Figure 17. $|S_{12}|$ model varying via-to-antipad capacitance

In this figure it can be seen that a variation in the antipad capacitance causes a shift in the 5GHz resonance in the insertion loss S_{12} but not around 9 GHz. This is additional verification that the resonances at 5GHz are directly related to the stub length. In fact, the stub resonance in the circuit model

Authorized licensed use limited to: University of Missouri. Downloaded on January 5, 2009 at 11:55 from IEEE Xplore. Restrictions apply.

depends on the thicknesses of the cavities and port inductances but also on the antipad capacitances, calculated externally to the power plane impedances.

Based on some cross-section photographs, the assumption of a larger antipad capacitance is correct since the real via size is about 15 to 20% larger than the nominal drill size used during the modeling process.

VI. CONCLUSIONS

In this paper, differential via transition measurements are presented and compared with simulations results of an equivalent circuit model. During the modeling, several issues have been encountered and circuit modifications implemented to get a better correlation between model and measurements. The effect of fabrication tolerances on the S-parameters has been shown as well.

REFERENCES

[1] C. Schuster, Y. Kwark, G. Selli, and P. Muthana, "Developing a 'physical' model for vias," *DesignCon 2006*, February 6-9, 2006, Santa Clara, CA.

[2] G. Selli, C. Schuster, Y. H. Kwark, M. B. Ritter, and J. L. Drewniak, "Developing a physical model for vias – part II: coupled and grounded return vias," *Designcon 2007*, Santa Clara, 2007.

[3] T.Okoshi, Y. Uehara, and T. Takeuchi, "The segmentation method – an approach to the analysis of microwave planar circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. MTT-24, no. 10, pp. 662-668, Oct. 1976

[4] J. Knighten, J., B. Archambeault, J. Fan, G. Selli, L. Xue, S. Connor, J. Drewniak, "PDN Design Strategies: III. Planes and Materials – Are they Important Factors in Power Bus Design?," *IEEE EMC Society Newsletter*, Issue No.. 208, Winter 2006, pp. 56-67.

[5] F. de Paulis, J. Diepenbrock, B. Archambeault, S. Connor, J. Fan, J. Drewniak, "Link path analysis on a block-by-block basis", *submitted at IEEE International Symposium on Electromagnetic Compatibility* - August 18-22, 2008, Detroit USA

Authorized licensed use limited to: University of Missouri. Downloaded on January 5, 2009 at 11:55 from IEEE Xplore. Restrictions apply.