DIGITAL COMPUTER SIMULATION OF INDUCTOR-ENERGY-STORAGE DC-TO-DC CONVERTERS WITH CLOSED-LOOP REGULATORS

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INTRODUCTION

Inductor-energy-storage dc-to-dc converters combined with closed-loop regulators frequently are encountered in a wide variety of power conditioning systems for aerospace, computer and instrumentation applications. The power-channel networks in these converters usually maybe simplified to one of four basic circuit forms: voltage step-up, current step-up, one-winding or two-winding voltage step-up/current step-up. Analyses of these circuits under steady-state conditions and design procedures based on equilibrium conditions have appeared in the literature and will not be discussed here.[1-8] The ability to predict transient current and voltage waveshapes in these circuits is important since periodic switching of currents through the semiconductor elements is an integral part of the operation of these circuits. Transients which occur as a result of transistor and diode switching with each cycle as well as transients of longer duration occurring at converter start-up and shut-down times and when the input-voltage or output-load levels are disturbed are particularly important since it is at such times that overstressing of circuit components is most likely to take place. Analytical methods for obtaining the transient response of converter systems, including the power-channel and controller networks, which have been reported in the literature generally have approached the problem by

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This work was supported in part by the National Aeronautics and Space Administration under Research Grant NGL-34-001-001 to Duke University.

replacing the nonlinear p on of the system with some form of equivalent linear transfer characteristic. Examples of linearizing techniques for obtaining the system transient response are found in References 3 and 6. These methods lead to valuable insight into the overall transient behavior and stability characterisitics, but usually are unable to provide information about many of the converter internal currents and voltages of importance to the designer. A need exists, therefore, for a method of investigating relatively complex converter designs which include circuit elements and topology of both the converter power channel and the controller.

In this paper, simulation of converter-controller combinations by means of a flexible digital computer program which produces output to a graphic display device is presented as an attractive alternative to mathematical analysis of converter systems which might require severe model simplification and possible loss of vital information in order to obtain a tractable problem statement. A number of software systems are available for simulating nonlinear system behavior. These software systems can be divided into two broad categories. The first type of programming involves the transformation of user data which describe the elements and the topology of the network into a set of simultaneous equations which is then solved for the appropriate response. The user of this type of program enters data for each circuit element in terms of its model description and its interconnections. Examples of this type of program are ECAP, SCEPTRE and ASTAP.

The second type of programming system for simulating nonlinear systems requires that the user describe the network in block diagram form. The data entered by the user consist of a description of each block and its input and output connections. The block diagram prepared by the user to represent a nonlinear system must accurately portray the flow of information represented

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by the differential and algebraic equations which have been written to describe the network under study. The blocks consist of linear elements such as weighted summers, sign inverters, unit delays and integrators, nonlinear elements such as comparators, clippers, limiters, relays and transcendental functions, and logic elements such as AND's, OR's and flip-flops. Examples of this type of program are CSMP and MARSYAS.

Both the circuit-topology and the block-diagram approaches will yield the transient current and voltage waveforms in the simulated systems. However, where computer run time is limited by computation center policy or user economics, it usually is prohibitively expensive to obtain sufficient simulation data on the effects of long-term transients, such as those which occur as a result of the initial application of power even in a relatively simple regulated converter. The use of small computers on which several hours of run time may be scheduled combined with the use of graphic output devices and interactive control of the program make it economically and computationally feasible to investigate transients of long duration, including those due to start-up, shut-down, and severe input and output changes. Programs which work directly from the description of circuit-element interconnections are available for small computers, but present versions with large overhead requirements due to procedures requiring frequent program overlays are too slow to make them attractive at this time. The simulation program used in studying closed-loop-regulated dc-to-dc converters in this paper is a modified version of the block-diagram software originally written for the IBM 1130 Computing System known by the name Continuous System Modeling Program (CSMP). A number of new features have been added to the 1130 CSMP which has been modified to run on a Digital Equipment Corporation PDP-11/45 computer equipped with a Tektronix 4013 storage-tube graphics console. The simplicity of the input language and console procedures enables the user to simulate a complex converter system with relative ease.

Once prepared, a user's block-diagram configuration and parameter assignments may be stored on the computer-system magnetic disk and later recalled for modification and use.

Four sets of configuration and parameter data corresponding to the four basic circuit forms for inductor-energy-storage dc-to-dc converter power-channel networks have been stored permanently on magnetic disk. These preprogrammed configurations contain all of the logic needed to switch the various differential and algebraic equations according to the requirements of the circuit variables. The user need only assign numerical values to the parameters and add the additional blocks required to simulate the controller. The interactive nature of the programming system permits the user to halt a simulation run at any point, to change parameters, and either to continue on with the computation or to start over with time reinitialized to zero. Using the display software and graphics console the user may observe and record up to five system variables (block outputs) plotted versus time or versus any other system variable. In addition, the user may obtain a numerical print-out of up to five variables plus the independent variable time on a print-time interval of his choosing. Because all computation is performed in the time domain, CSMP as used here is not adapted to provide frequency response information such as Bode or Nyquist plots or signal spectra.

CONVERTER ANALYSIS AND STATE REPRESENTATION

Since the computer simulation program deals directly with time-domain equations, the first step toward preparing data for a system simulation is to derive the state and algebraic equations for the converter-controller network. From these equations, the block diagram of the system-simulation program is prepared. Parameters of the linear and nonlinear blocks in the diagram are

determined by the parameters of the system under study. If no additional state-equation switching is needed beyond that already programmed into the stored configuration being used, the output-voltage and power-transistor blocks of the power channel are connected to the input and output blocks of the controller. If additional state variables are required to describe the converter because of the presence of additional energy-storage elements from, for example, an added input filter, it will be necessary to rewrite the network equations and may be necessary to modify the switching logic.

In the simulation research discussed here, the four basic forms of inductor-energy-storage converter power channels shown at the top of Table 1 are used as the starting point in the analysis leading to the four stored converter power-channel models available to the CSMP user. These same circuit forms have been used as the basis for computer-aided design procedures in References 7 and 8 and are modified here to include the resistance of the source, parasitic resistances in the circuit elements, and the saturation and forward resistances of the transistors and diodes. The transistors and diodes are represented as open circuits when reverse biased.

There are two possible modes of operation for an inductor-energy-storage converter.[7] A converter operating in Mode 1 has current flowing in the energy-storage inductor at all times. When the power-channel transistor Q is turned on, the inductor current rises from a nonzero value to a larger value over the time interval t_{on}. When the transistor is turned off during the succeeding interval t'_{off}, a portion of the energy stored in the inductor is transferred into the load circuit through diode D. In Mode 1 operation, the inductor current never dwells at zero. When a converter operates in Mode 2, the inductor current initially is zero when the transistor is turned on. The inductor current builds up in the interval t_{on}, starting from zero. When the transistor is turned off, during interval t'_{off} all of the energy stored in

the inductor is transferred to the load. There then follows a finite time interval t''_{off} after the inductor current reaches zero before the transistor is turned on again. In setting up the state equations for the converter, all three time intervals are accounted for by providing separate expressions corresponding to each of the conditions below:

Time Interval	Associated Subscript	Circuit Conditions
t_{on}	α	Transistor Q on, diode D off
t'_{off}	β	Transistor Q off, diode D on
t''_{off}	γ	Transistor Q off, diode D off

Two state variables are chosen for each of the four basic configurations. They are the magnetic-core flux ϕ and the voltage v_C across the pure capacitance C. The linear model for the magnetic core allows for a residual flux Φ_R when the current through the inductor winding is zero.[7] The effective series resistance (ESR) internal to the capacitor is represented by r_C. State equations for the four configurations during the three time intervals t_{on}, t'_{off} and t''_{off} are listed in Table 1. Expressions for the inductor current i_X and the output voltage v_0 also are given in the table.

SWITCHING LOGIC FOR SELECTING THE APPROPRIATE STATE-VARIABLE EQUATIONS

As explained above, for each converter configuration, state equations must be written for the three possible network conditions which depend on whether transistor Q is turned on, and if not turned on, whether the magnetic-core flux ϕ has fallen to the residual level Φ_R (inductor current has fallen to zero) or not. The simulation block-diagram connections for computing the state variables for these three time intervals from their respective derivatives are shown in Figure 1. The signal from the controller and the output of the comparator block may assume one of two levels, high or low. A high-level

signal applied to the control input of a relay causes the two-pole switch of the relay to move to the upper position. A low-level signal causes the switch of the relay to move to the lower position on the diagram. The subscripts, α,β and γ identify the values of $\dot{\phi}$ and $\dot{v}_C$ from Table 1 corresponding to conditions during the three time intervals t_{on}, t'_{off} and t''_{off} defined above. It is the function of the logic circuitry always to assign the proper values to the state-variable derivatives $\dot{\phi}$ and $\dot{v}_C$. When the controller demands that transistor Q be turned on, the signal from the controller to the pair of relays in the center of the figure is high. These two relay blocks then transmit derivatives $\dot{\phi}_\alpha$ and $\dot{v}_{C\alpha}$ to the inputs of their respective integrators. These two derivatives as well as all others in the figure are generated continuously by combinations of terms from other blocks not shown on this diagram. Since flux ϕ must always increase while transistor Q is on, the output of the comparator sensing the difference between ϕ and Φ_R is at the high level, holding the pair of relays on the left side of the figure in their upper positions. When the controller indicates that transistor Q is to be turned off, the signal to the control inputs of the central pair of relays goes to the low level and these relays switch to their lower positions. The derivatives $\dot{\phi}_\beta$ and $\dot{v}_{C\beta}$ thus are the ones transmitted to the integrators immediately following receipt of the turn-off signal from the controller. As long as the flux ϕ exceeds or is equal to the residual flux level Φ_R, the comparator output will remain high. When ϕ falls ever so slightly below Φ_R, the comparator output goes to the low level and both relays on the left are driven to their lower positions. From then until transistor Q turns on again, $\dot{\phi}_\gamma$ and $\dot{v}_{C\gamma}$ are transmitted to the two integrators. The value of $\dot{\phi}_\gamma$, see Table 1, is zero, corresponding to ϕ held at Φ_R minus a small error, until the controller demands that Q turn on again. When this happens, the center pair of relays returns to their initial

upper positions. The core flux ϕ increases so that it becomes equal to or greater than Φ_R and the comparator output goes to the high level, returning the relay pair at the left side of the figure to their upper positions. A new cycle of operation, thus, commences.

SIMULATION OF TWO EXAMPLE ELECTRONIC POWER CONDITIONING SYSTEMS

To illustrate the power and versatility of the block-diagram programming technique in simulating switching-type electronic power conditioning systems, results of computer simulation investigations of two types of inductor-energy-storage dc-to-dc converters from aerospace applications are presented. The first example is a preregulator which will provide a regulated bus for the electronics of the Cosmic X-ray Experiment, denoted as A2, one of six experiments on the High Energy Astronomy Observatory Satellite (HEAO) scheduled for launch in early 1977. The second illustrative example is a battery-charger circuit used on the Atmosphere Explorer-B Spacecraft (AE-B) launched in May, 1966. These two examples represent two different types of converter power-channel networks with two different types of controllers. The HEAO-A2 preregulator produces a constant output voltage over a considerable range of output power and for a wide range of input voltage. It can be classified as a current step-up converter with a constant-frequency variable-on-time controller. The AE-B battery charger was designed to charge,one battery pack at a time, the various batteries on board the spacecraft which ranged in voltage from 3 to 25 volts. Closed-loop regulation of the array voltage, rather than conventional regulation of the output voltage, was obtained by using a constant-on-time, variable-frequency controller to control a single-winding voltage step-up/current step-up converter.

HEAO-A2 Preregulator Block Diagram

A block diagram illustrating the major subcircuits in the HEAO-A2 preregulator is shown in Figure 2. In the development of procedures for translating the complete circuit diagram into a model adequate to provide sufficient detail for a given investigation, the programmer searches for those parts of the circuit that may be isolated from the system and modeled with minimum coupling to the rest of the system. The partitioning of subcircuits in Figure 2 resulted from such a study of this example system. The subcircuits correspond to:

1. INPUT FILTER WITH START-UP RELAYING for limiting an initial high surge of current.
2. Inductor-energy-storage CURRENT STEP-UP CONVERTER and the output LOAD.
3. REGULATOR FOR VOLTAGE SUPPLY TO CONTROLLER subsystems.
4. JENSEN SQUARE-WAVE OSCILLATOR AND RECTIFIER/FILTER FOR OPERATIONAL-AMPLIFIER SUPPLY voltage and base-drive bias supply.
5. Square-wave INTEGRATOR AND VOLTAGE-REFERENCE CIRCUIT.
6. OUTPUT-VOLTAGE TO SAWTOOTH-PLUS-REFERENCE COMPARATOR AND CURRENT-LIMIT LOGIC plus the BASE DRIVE CIRCUIT.
7. OPERATIONAL AMPLIFIER AND CURRENT REFERENCE.

Because of the importance of the effect of supply voltage V_{CC1} at converter start-up, the regulator for the controller voltage supply is included in the simulation. This regulator also supplies power for the Jensen square-wave oscillator, the output of which is rectified to provide the dual-supply voltages, $+V_{CC2}$ and $-V_{CC2}$, for the operational amplifier. Since the operational amplifier may be overdriven during transients, the saturation levels at its output must take into account the supply voltages available.

The Jensen circuit not only provides supply voltages to the operational amplifier and power transistor base-drive bias circuit, but also provides the square wave to the integrator circuit. The square wave is integrated to become the sawtooth waveform for modulating the on-time of the power-channel transistor Q. The output voltage v_0 is compared with the sum of the sawtooth waveform and the voltage reference in the comparator circuit. When the algebraic sum of these three signals exceeds the comparator threshold level, the power transistor is turned on through the base-drive circuit. The comparator also includes current-limit logic circuitry which allows the operational amplifier and its current-reference offset to hold the output of the comparator in the power-transistor-off condition as long as the load current exceeds a preset value.

HEAO-A2 Preregulator Circuit Diagram

Although the operation of the preregulator circuit will not be explained in full detail, it is necessary to explain certain activities in the circuit in order to discuss the waveforms presented later in the paper. A simplified schematic diagram is shown in Figure 3 in which the subcircuits appearing in the block diagram are identified with captions. The input voltage is permitted to vary from 23 to 33 volts while the output voltage is held at 20 volts over a load power range of 2 to 40 watts. The start-up surge-limit relaying subcircuit consists of a resistor-diode series combination which is switched out of the input path 6.5 milliseconds after initial application of power to the system. The surge-limit subcircuit is followed by a single inductor-capacitor filter section. Resistor R_1 limits the initial rush of current into the L_1C_1 input filter and provides damping to prevent ringing of that circuit during the start-up transient. The input filter provides isolation between the switching currents in the converter power channel and the input power source feeding it. The

current step-up circuit, sometimes identified as a buck or voltage step-down regulator, alternately stores energy in inductor L_2 when transistor Q_1 conducts and releases energy to the load circuit when Q_1 is turned off and diode D_2 conducts. Capacitor C_2 carries most of the ripple current passing through L_2. The output voltage is sensed across the connected load and the output current is sensed as the voltage drop across resistor R_2. These two feedback voltages are used as input signals to the controller.

The regulator for the voltage supply to the controller, consisting of constant-current diode D_6, zener diode D_5, transistor Q_6 and capacitor C_6, provides the supply voltage V_{CC1} to all of the controller subcircuits except the operational amplifier. The current through Q_6 charges C_6 and other filter capacitors with an essentially constant current until D_5 reaches its breakdown voltage. The variation in supply voltage V_{CC1} before the constant value of 20 volts is reached affects a number of the subcircuits in the controller. For example, both the frequency and amplitude of the waveform developed by the Jensen oscillator depend on the supply voltage. During the start-up transient both the frequency and the amplitude of the Jensen-circuit square-wave output increase with the frequency ultimately stabilizing at 25 KHz when V_{CC1} is 20 volts. In addition, supply voltages $+V_{CC2}$ and $-V_{CC2}$ from the bridge rectifier, which are superimposed on output voltage V_0 through the center-tap of a secondary winding on transformer T_1, vary during the start-up period.

A passive integrator consisting of capacitors C_3 and C_4 and resistors R_{14} and R_{15} serves to shape the square wave from the Jensen circuit into a sawtooth wave. This waveform is superimposed on a reference voltage obtained through a network made up of R_{16}, C_5 and zener diode D_4 and is coupled to the comparator circuit. Transistors Q_2 and Q_3 and associated resistors make up the comparator. All of these subcircuits are affected by the build-up in supply

voltage V_{CC1} or by the waveform transient from the Jensen circuit.

The comparator circuit, which monitors the algebraic sum of the sawtooth wave, reference voltage and output voltage, turns the power transistor Q_1 on and off as it is driven back and forth through its threshold. However, if the load current,as sensed by the operational amplifier, exceeds a preset value the current-limit logic circuit will hold the power transistor in the off-condition. The operational amplifier is biased by an offset through resistor R_4 and $+V_{CC2}$ to correspond to a two-ampere current limit which causes diode D_3 to be forward-biased when that limit is exceeded. The input terminal to the comparator from the divider network for the output voltage v_0 is held high enough to cause the comparator to signal the power transistor that turn-off is required.

With this brief description of the converter-controller subcircuits as background, the simulation block diagram for a CSMP program is now discussed.

HEAO-A2 Preregulator Block Diagram for CSMP Simulation

The block diagram shown in Figure 4 depicts the model of the HEAO-A2 preregulator in terms of simulation functions available in the CSMP programming system. To compare the simulation model with the simplified schematic diagram in Figure 3, the block diagram has been partitioned into sections which can be identified with the subcircuits discussed in the previous sections of the paper. The input filter with two energy storage elements requires two integrators to obtain state variables ϕ_1 and v_{C1} for the flux in the core of L_1 and the voltage across the pure capacitance C_1. The derivatives to these two integrators are switched by control signals from a time delay function and from the controller for the power transistor on-state. The converter and load section contains two integrators which compute the state variables ϕ_2 and v_{C2}. The derivatives fed to these two integrators are switched according to the conditions required by the controller demand for the on or off state of the power transistor Q_1 and the flux

level ϕ_2 compared with the residual flux level ϕ_R as explained earlier for Figure 1. The output-voltage to sawtooth-plus-reference comparator establishes the state of one pair of relays while the output of a comparator block in the converter section sensing $\phi_2 - \phi_R$ controls the state of the other relay pair. Unit delay blocks to obtain a delay of six microseconds simulate power-transistor Q_1 storage delay when the comparator control signal goes low.

The output of the regulator for supply voltage V_{CC1} is simulated with a limiter block driven by the independent variable, time. The Jensen circuit uses a relay to alternate between $+V_{CC1}$ and $-V_{CC1}$ as an integrator input. Integration of this supply of one sign continues until the output of a positive or a negative clipper driven by the integrator is different from zero. The clipper outputs serve to set and reset a flip-flop block which in turn drives a comparator block to reverse the relay and the sign of the supply voltage to the integrator. This simulation corresponds to the integration of a portion of the supply voltage coupled through windings to the square-loop magnetic core in the Jensen-circuit transistor base-drive circuit.

The square-wave integrator which produces the sawtooth waveform and the voltage-reference circuit require three integrators for the voltages across C_3, C_4 and C_5. A limiter block simulates the voltage-limiting behavior of zener diode D_4. To simulate the offset in the comparator circuit due to two base-emitter junction voltage drops, the output of the integrator and voltage-reference circuit is passed through a positive clipper.

The operational amplifier in this simulation model is modeled as a single-pole RC network using a single integrator. In addition, the amplifier model includes the effect of saturation at a supply voltage level, positive or negative, depending on the sign of the input signal, and includes the effect

of variable supply voltages at converter start-up time. The relay, comparator, constant, and summer blocks simulate the amplifier gain, current-reference offset, which is dependent on the value of V_{CC2}, and saturation effect. Weighted summers used as coefficient blocks convert $(\phi_2 - \phi_R)$ to current i_{X2} and to current-sense voltage across R_2. Output voltage v_0 is obtained as the sum of v_{C2} and the voltage drop across the effective series resistance r_{C2}. Although in the actual circuit v_0 is coupled to one input terminal of the comparator circuit through a resistive divider network, in the simulation model it is mixed with other appropriate signals in the simulation model of the operational amplifier.

The outputs of the sawtooth-waveform and voltage-reference circuit and the operational amplifier and current reference, including the feedback connection for the output voltage v_0, are used to drive a comparator block which determines the on-time of the power-channel transistor. As long as the load current does not exceed the current-limit set point of two amperes, the sum of the sawtooth waveform and reference voltage is compared with the output voltage, and the controller operates in the normal voltage-limit manner. When the load-current-limit set point is exceeded, the comparator section is disabled and power channel transistor Q_1 can not be commanded to the on-condition until the load current falls below that level.

These brief descriptions of the subcircuit operations and the interconnections of the CSMP programming system blocks to simulate the complete HEAO-A2 preregulator provide the background for discussing some of the results of a number of computer simulation runs and comparing them with results obtained from the actual circuit under development.

Comparison of Simulation and Experimental Results for HEAO-A2 Preregulator

To more easily compare plots of time functions obtained from CSMP computer simulation runs with oscillograms of actual circuit voltages and currents, reproductions of display plots obtained from the graphics console have been photographically reduced so that the lengths of the horizontal (time) axes are the same as those of the experimental oscillograms. The corresponding computer simulation waveforms are placed directly below the circuit oscillograms; and in each pair of computed and actual waveforms, the vertical calibrations are identical. While the scales in volts or amperes per major division are the same between a pair of waveforms, in some of the oscillograms some of the waveforms are offset slightly from their zero positions. These slight offsets do not hinder comparison of computed and actual waveforms, however.

The waveforms shown in Figure 5 illustrate the transients occurring following the connection of the converter system to its power source. The input voltage for these waveforms and all others to follow has been set to 28 volts. The load resistance connected at converter start-up is 13.33 ohms, corresponding to an equilibrium output power of 30 watts when the load voltage reaches 20 volts, the regulated value. At zero time, all currents and voltages displayed are zero. After being connected to the 28-volt source, voltage v_I' at the output of the input filter begins to rise. This causes the output of the voltage supply to the controller network (not shown) to begin to rise and causes the output of the reference voltage circuit v_R to increase. At 6.5 milliseconds, the time-delay relay in the input filter circuit closes, shorting out R_1 and D_1. The effect of the redistribution of voltage drops across L_1, its winding resistance r_1 and the effective series resistance r_{C1} of C_1 may be observed by noting the small discontinuity

in v_I' at that time. Because of the transient rise in supply voltages throughout the controller network power channel, transistor Q_1 is not commanded to the on-state until approximately 9.7 milliseconds after initial application of power. When this first turn-on command occurs, the current i_{X2} in L_2 rises rapidly and exceeds the current-limit set point. This causes transistor Q_1 to be turned off and the inductor current to decrease until it is less than the limit value. Because the output voltage feedback signal is low relative to the reference voltage at this time, the comparator signals for the power-channel transistor to be turned on again. This current-limit self-oscillation mode continues for approximately 2.5 milliseconds until the output voltage v_0 has risen sufficiently high to permit the comparator circuit to begin to function normally. From this point on to approximately 40 milliseconds after start-up, the output voltage v_0 tracks the slowly rising reference voltage v_R. When zener diode D_4 reaches its breakdown potential, v_R stabilizes at 9 volts and the output voltage levels off at 20 volts. The transient period to reach normal operating voltage and power levels in all portions of the converter-controller system after initial application of power is seen to last approximately 40 milliseconds.

The same HEAO-A2 preregulator with the current-limit feature disabled was tested in the CSMP simulation run shown in Figure 6. In this figure the scale factor for the inductor current i_{X2} has been changed from 1 ampere/major division to 5 amperes/major division in order to contain the current waveform on the plot. Note that without the current-limit circuit, the peak current exceeds 10 amperes. Considering that the slowly rising reference voltage is intended to produce a "soft" start-up transient, a casual study of the converter circuit with the current-limit feature removed would not lead one to expect this potentially dangerous high-current peak. The use of the

CSMP programming system to explore circuit variations is one of the most useful features of this approach to computer-aided analysis of power conditioning systems. Using data from simulation runs, system components can be evaluated for voltage and current stresses under normal and failure modes.

In Figure 7 waveforms are shown for a connected load of 13.33 ohms, corresponding to an output power of 30 watts at 20 volts, switched in a stepwise manner to 40 ohms, corresponding to a 10 watt load power. The duration of the sweep time on the horizontal axis has been reduced to 2 milliseconds from 50 milliseconds for the start-up transient plots. The ripple due to the constant-frequency variable-on-time current pulses through the power channel transistor can be seen clearly in the inductor current i_{X2} and output voltage v_0 waveforms. In the simulation plot two additional waveforms have been included. Waveform 3 represents the step change in load resistance and is presented to show clearly the time of the load transition. The fourth waveform represents the state of the current-limit circuit. When the level of waveform 4 lies at position B, the circuit is out of the current-limit mode; at position A, the circuit is in current-limit mode. As the simulation run plot demonstrates, at no time during the 30 watt-to-10 watt transient does the circuit enter the current-limit mode.

The waveforms in Figure 8 are similar to those of the preceeding figure but with the transient due to a decrease in load resistance from 40 ohms to 13.33 ohms. Waveform 4, indicating when the current-limit mode has been entered, shows that near the peak of the transient current in inductor L_2, i_{X2}, current limiting takes place. In both Figures 7 and 8, the simulation plotted waveforms follow the experimental-circuit oscillogram waveforms rather faithfully.

The final set of waveforms comparing circuit performance and CSMP simulation runs for the HEAO-A2 preregulator are shown in Figures 9 and 10.

The plots of inductor current i_{X2} and output voltage v_0 illustrate the output characteristic of the converter system first when a three-ohm fault is connected in parallel with the 13.33 ohm load into which 30 watts of power is being dissipated and then when the fault is later removed. The oscillogram traces and the simulation plots of Figure 9 show that the inductor current rises rapidly to the current-limit set-point value while the output voltage v_0 finally reaches an equilibrium value of approximately 5 volts as predicted by the product of the current-limit value of two amperes and the parallel resistance of the load and fault resistance. Additional information plotted in the simulation results is the display of the transition in the connected resistance and an indication of when the system is in the current-limit mode.

The current and voltage transients which occur when the three-ohm fault is removed are shown in Figure 10. The current-limit feature of the converter-controller system is an important part of its operation during this period of recovery from the fault removal since it prevents overshoot of current and voltage in the power channel. It should be noted that recovery time from this low-output-voltage condition is considerably shorter than that of the comparable transient at converter start-up time due to the fact that all supply voltages and the reference voltage are up to their rated values.

The comparison of results of experimental and simulation investigations of the response of the HEAO-A2 preregulator at start-up time and under a variety of transient load conditions have been presented in this section. The results obtained from the simulation studies illustrate how the long-term responses of a complex converter-controller power conditioning system may be investigated for a variety of conditions, including load faults and subcircuit failures. In the following section, another type of power conditioning

system will be examined, this time from a steady-state cyclic point of view.

AE-B Battery-Charger Block Diagram

The second example of computer simulation of an electronic power conditioning system is the battery-charger converter for the Atmosphere Explorer-B Spacecraft.[9] The block diagram in Figure 11 presents the essential features of the battery charging system. The power source is a solar array connected through an input filter comprised of two capacitors and an inductor. The requirements of the solar array and of the experiments on the spacecraft necessitated a reversal of polarity between the input and output voltages of the converter. This polarity reversal was obtained by using a single-winding voltage step-up/current step-up converter. The converter-controller requirements were also unusual in that the converter was to regulate its input voltage to a nominal 15 volts while charging batteries connected to its output with terminal voltages ranging from 3 to 25 volts. This design constraint required that the feedback signal to the controller network come from the input voltage to the power-channel network, rather than from the output voltage across the connected battery load. The controller network provides a base-drive pulse of constant on-time which varies in frequency to regulate the solar array voltage connected to the input terminals of the converter.

AE-B Battery Charger Circuit Diagram

A simplified schematic circuit diagram of the battery charger is shown in Figure 12. The solar array is represented by the Thevenin equivalent voltage v_I and source resistance r_I and is isolated from the cyclic switching currents in the power channel by input filter $C_1L_1C_2$. Transistor Q_1, diode D_1 and energy-storage-inductor L_2 comprise the main elements of the power-channel network which is connected to the battery load through output filter C_5L_3. When a voltage pulse from the controller network is applied across the

base-emitter junction of Q_1, the power transistor is driven into conduction. Current feedback holds Q_1 saturated through the coupling of current transformer T_1. Winding 1-2 functions as the primary with winding 3-4 serving as the secondary which provides base current. The flux in the square-loop magnetic core of T_1, which initially was saturated at one end of the core characteristic when the trigger pulse from the controller network occurred, moves to the opposite saturation level over a time interval determined by the essentially-constant forward base-emitter voltage drop of Q_1. This voltage drop of approximately 0.7 volt determines the constant Q_1 on-time of 33 microseconds. When the flux in T_1 reaches the opposite saturation-flux level, the increased magnetizing-current requirements reduce the feedback through T_1 and Q_1 ceases to conduct. Following this circuit action, the core of T_1 is reset by the voltage applied across winding 6-5 and the power-channel network awaits the next pulse from the controller network.

The controller network consists of a variable-frequency oscillator made up of unijunction transistor Q_4 and capacitor C_3 charging network consisting of resistors, transistors and a diode. The voltage across zener diode D_2 provides the base-1 to base-2 bias potential for Q_4. When the voltage across C_3 exceeds the hold-off voltage between the emitter and base 1 of Q_4, the latter conducts and provides a discharge path for C_3 through the base of Q_1. This pulse initiates the action described in the previous paragraph, turning Q_1 on in the power channel.

The D_2R_1 network is used to provide a feedback signal to the base of Q_2 proportional to the input voltage to the power transistor, thereby adjusting the charging current into C_3 and consequently controlling the unijunction transistor oscillator frequency. Since the on-time of the power transistor is constant at 33 microseconds, when the input voltage attempts to increase, the

controller pulse-frequency also increases in turn increasing the average current through the power channel and maintaining an essentially constant input voltage.

State equations for the simulation model are obtained from the voltage step-up/current step-up basic circuit in Table 1, and are modified to incorporate the state equations due to the five energy storage elements in the input and output filters. The variable-frequency oscillator is modeled to incorporate the input-voltage feedback path. It also drives a pulse-generator block producing a pulse of fixed duration. This command signal from the controller network is used to control the state-equation switching as in the HEAO-A2 preregulator example. The flux in the magnetic core on which L_2 is wound is compared with the residual flux level to control additional switching of the equations for Mode 2 operation.

Comparison of Silulation and Experimental Results for AE-B Battery Charger

The waveforms in Figure 13 obtained from the battery-charger circuit are for steady-state conditions in contrast with the transient runs for the HEAO-A2 preregulator and show greater detail during a switching cycle. In the first illustrative example, the comparisons were made to show how long-term transients due to start-up and severe load changes can be obtained by use of computer simulation techniques. The battery-charger waveforms which are presented were taken after the start-up transient had died out. Steady-state waveforms of voltage across inductor L_2 and capacitor C_4 are presented. The four sets of waveforms correspond to a constant input power of 9.1 watts, and battery load voltages of 3, 4, 20 and 25 volts. The four oscillograms showing the experimentally determined waveforms are reproduced from Figure 6 of Reference 9. The inductor voltage waveforms show when the converter is operating in Modes 1 and 2. When the battery load voltage is 3 and 4 volts, inductor voltage

$N_2\dot{\phi}_2$ passes through zero rapidly as transistor Q_1 conducts or diode D_1 conducts. For battery load voltages of 20 and 25 volts, $N_2\dot{\phi}_2$ is zero for a significant portion of a complete cycle, indicating that neither Q_1 nor D_1 are conducting. The voltage v_0' across C_5 shows the effect of the effective series resistance r_{C5} in producing a step when the diode is abruptly connected and disconnected by the actions of the power-channel network. In the actual circuit, the converter power-channel network is isolated from the battery load by an output filter consisting of two capacitors and two inductors. The model which was programmed for simulation contains only the single L_3C_5 output filter section. The ripple voltage across C_5 is therefore somewhat larger than it would be with a two-section LC filter.

Results obtained from simulation studies of a spacecraft battery-charger power conditioning system have been presented in this section. Comparison of the waveforms from the actual circuit with those from the simulation model show close agreement over the entire cycle of steady-state operation of the circuit. This example illustrates how detailed observation of waveforms of current and voltage may be made by altering the time scale used for plotting the circuit variables.

CONCLUSIONS

The complexity of power conditioning systems with the attendant mixture of nonlinear and energy-storage components in both the power-channel and controller networks offers a very real challenge to the designer when he attempts to predict detailed behavior of such a system. Analytical techniques presently available generally make use of some form of linearized transfer characteristic to replace the nonlinear sections of the converter-controller network. Obtaining the response of converters to severe disturbances in input-voltage and output-

load levels from a linearized model may not be valid because of major changes in the behavior of the nonlinear portions of the network. Digital computer simulation techniques in which the nonlinear characteristics of a converter-controller network are preserved offer a means of investigating a wider range of system characteristics than possible with linearized models.

Perhaps the most attractive application of computer simulation may be found while the designer is developing the converter-controller network and wishes to test a number of different concepts in the controller portion of the system. The convenience of a "quick look" at the system behavior while the designer is still in the concept formulation stage of circuit development can be seen to be an important advantage. As the circuit design evolves in the mind of the designer, and as he refines his simulation model, he can obtain information on the soundness of the controller concept on which he is working at each step along the way by means of the design-simulation procedure. If the modeling is done with sufficient care and detail, the designer is able to confirm his design, including optimization of components, before constructing a prototype circuit. After having seen the results of simulation and having obtained a better understanding of how the circuit functions, the designer may even find he is able to simplify or delete some portions of his original circuit design. Other important uses of simulation studies in assisting the design process include determining the effects of component-value tolerances and drift.

A second important area of application of simulation studies in power conditioning systems lies in the analysis of system performance under a variety of operating conditions. The earlier portions of this paper have shown how the response of a complete converter-controller system may be obtained for load-level changes, including changes within the normal regulating range and those corresponding to load fault conditions. These studies also show in considerable

detail how the converter behaves when it first is connected to the power source. Another example of an important measurement which is readily made but is difficult to carry out experimentally is the response to a step change in input voltage source. Since it is relatively simple to disable individual subcircuit models in the simulation program, it is possible to simulate the effect of circuit failure, as in the example of the elimination of the current-limit feature in the HEAO-A2 preregulator. Although frequency response data yielding gain and phase margins from which to judge the stability of the regulating system are not available from the simulation studies, it is possible to arrive at some useful stability information by simulation testing. For example, starting from a particular set of design parameters such as those of the energy-storage inductor and filter capacitor in the power channel, the designer could vary these values from run to run until the system became unstable. The information thus gained would be useful in establishing bounds on component tolerances and drift for maintaining stable operation of the converter.

In this paper, the application of simulation techniques using a small computer equipped with a graphic display console has been shown to yield transient and steady-state response information with sufficient detail and accuracy to make this approach to analysis and design useful to the designer of power conditioning systems. Interactive control of the program which permits the user to branch to chosen program segments for modification of the program block diagram, block parameters, integration time step, or variables to be displayed provide him with many options for experimentation.

The results presented herein were obtained through an ongoing cooperative research effort between a government aerospace laboratory and an electrical engineering laboratory in a university. The particular aspect of the effort reported here relates to specific circuits already developed or currently under

development and to detailed investigations of these circuits using digital computer simulation techniques. Using these circuits as examples, computer-aided analysis employing simulation techniques has been demonstrated to be a viable alternative to other approaches for obtaining detailed transient and steady-state response of inductor-energy-storage dc-to-dc converters-with closed-loop regulators.

ACKNOWLEDGEMENT

The authors acknowledge with thanks the contributions of Mr. Ben H. Rimer, who was responsible for the successful translation of the 1130 CSMP software to a graphics-oriented computer system and for the development of additional easily-used enhancements to the CSMP programming system.

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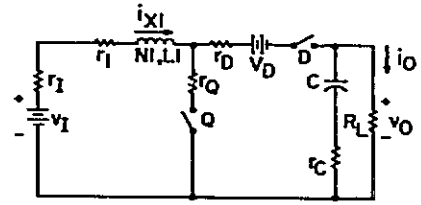
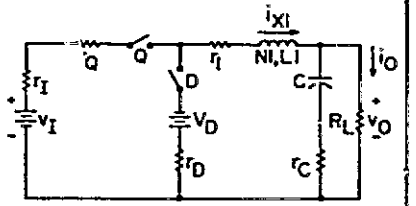
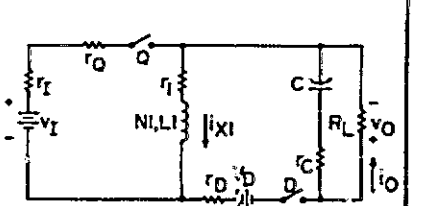
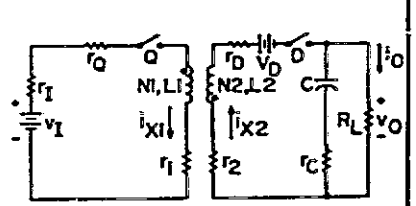
TABLE I

Schematic diagrams, state equations and output equations for four basic forms of inductor-energy-storage dc-to-dc converters

TIME INTERVAL AND ASSOCIATED SUBSCRIPT	VOLTAGE STEP-UP CONVERTER	CURRENT STEP-UP CONVERTER	VOLTAGE STEP-UP/CURRENT STEP-UP CONVERTER	
			SINGLE WINDING	TWO WINDING
				
t_{on} α	$\dot{\phi} = \frac{v_I}{N1} - \frac{(v_I+r_1+r_Q)(\phi-\phi_R)}{L1}$ $\dot{v}_C = -\frac{v_C}{C(r_C+R_L)}$ $v_0 = \frac{v_C R_L}{(r_C+R_L)}$ $i_{x1} = \frac{N1(\phi-\phi_R)}{L1}$	$\dot{\phi} = -\frac{v_C R_L}{(r_C+R_L)N1} - (r_I+r_1+r_Q+\frac{r_C R_L}{r_C+R_L})(\frac{\phi-\phi_R}{L1}) + \frac{v_I}{N1}$ $\dot{v}_C = -\frac{v_C}{C(r_C+R_L)} + \frac{N1R_L(\phi-\phi_R)}{L1(R_L+r_C)C}$ $v_0 = \frac{v_C R_L}{(R_L+r_C)} + \frac{N1R_L(\phi-\phi_R)r_C}{L1(r_C+R_L)}$ $i_{x1} = \frac{N1(\phi-\phi_R)}{L1}$	$\dot{\phi} = \frac{v_I}{N1} - \frac{(r_1+r_I+r_Q)(\phi-\phi_R)}{L1}$ $\dot{v}_C = -\frac{v_C}{C(r_C+R_L)}$ $v_0 = \frac{v_C R_L}{r_C+R_L}$ $i_{x1} = \frac{N1(\phi-\phi_R)}{L1}$	$i_{x1} = \frac{N1(\phi-\phi_R)}{L1}$, $i_{x2} = 0$
t'_{off} β	$\dot{\phi} = -\frac{V_D}{N1} - \frac{v_C R_L}{N1(R_L+r_C)} - (r_I+r_1+r_D+\frac{r_C R_L}{r_C+R_L})(\frac{\phi-\phi_R}{L1})$ $\dot{v}_C = -\frac{v_C}{C(R_L+r_C)} + \frac{N1R_L(\phi-\phi_R)}{L1(R_L+r_C)C}$ $v_0 = \frac{v_C R_L}{(R_L+r_C)} + \frac{N1R_L r_C(\phi-\phi_R)}{L1(r_C+R_L)}$ $i_{x1} = \frac{N1(\phi-\phi_R)}{L1}$	$\dot{\phi} = -\frac{v_C R_L}{(r_C+R_L)N1} - (r_1+r_D+\frac{r_C R_L}{r_C+R_L})(\frac{\phi-\phi_R}{L1}) - \frac{V_D}{N1}$ $\dot{v}_C = -\frac{v_C}{C(r_C+R_L)} + \frac{N1R_L(\phi-\phi_R)}{L1(r_C+R_L)C}$ $v_0 = \frac{v_C R_L}{r_C+R_L} + \frac{N1R_L r_C(\phi-\phi_R)}{L1(r_C+r_L)}$ $i_{x1} = \frac{N1(\phi-\phi_R)}{L1}$	$\dot{\phi} = -\frac{V_D}{N1} - \frac{v_C R_L}{N1(r_C+R_L)} - (r_1+r_D+\frac{r_C R_L}{r_C+R_L})(\frac{\phi-\phi_R}{L1})$ $\dot{v}_C = -\frac{v_C}{C(r_C+R_L)} + \frac{N1R_L(\phi-\phi_R)}{L1(r_C+R_L)C}$ $v_0 = \frac{v_C R_L}{(R_L+r_C)} + \frac{N1R_L r_C(\phi-\phi_R)}{L1(r_C+R_L)}$ $i_{x1} = \frac{N1(\phi-\phi_R)}{L1}$	$\dot{\phi} = -\frac{V_D}{N2} - \frac{v_C R_L}{N2(r_C+R_L)} - (r_2+r_D+\frac{r_C R_L}{r_C+R_L})(\frac{\phi-\phi_R}{L2})$ $\dot{v}_C = -\frac{v_C}{C(r_C+R_L)} + \frac{N2R_L(\phi-\phi_R)}{L2(r_C+R_L)C}$ $v_0 = \frac{v_C R_L}{(R_L+r_C)} + \frac{N2R_L r_C(\phi-\phi_R)}{L2(r_C+R_L)}$ $i_{x2} = \frac{N2(\phi-\phi_R)}{L2}$, $i_{x1} = 0$
t''_{off} γ	$\dot{\phi} = 0$ $\dot{v}_C = -\frac{v_C}{C(R_L+r_C)}$ $v_0 = \frac{v_C R_L}{(r_C+R_L)}$			
	$i_{x1} = 0$	$i_{x1} = 0$	$i_{x1} = 0$	$i_{x1} = 0$ $i_{x2} = 0$

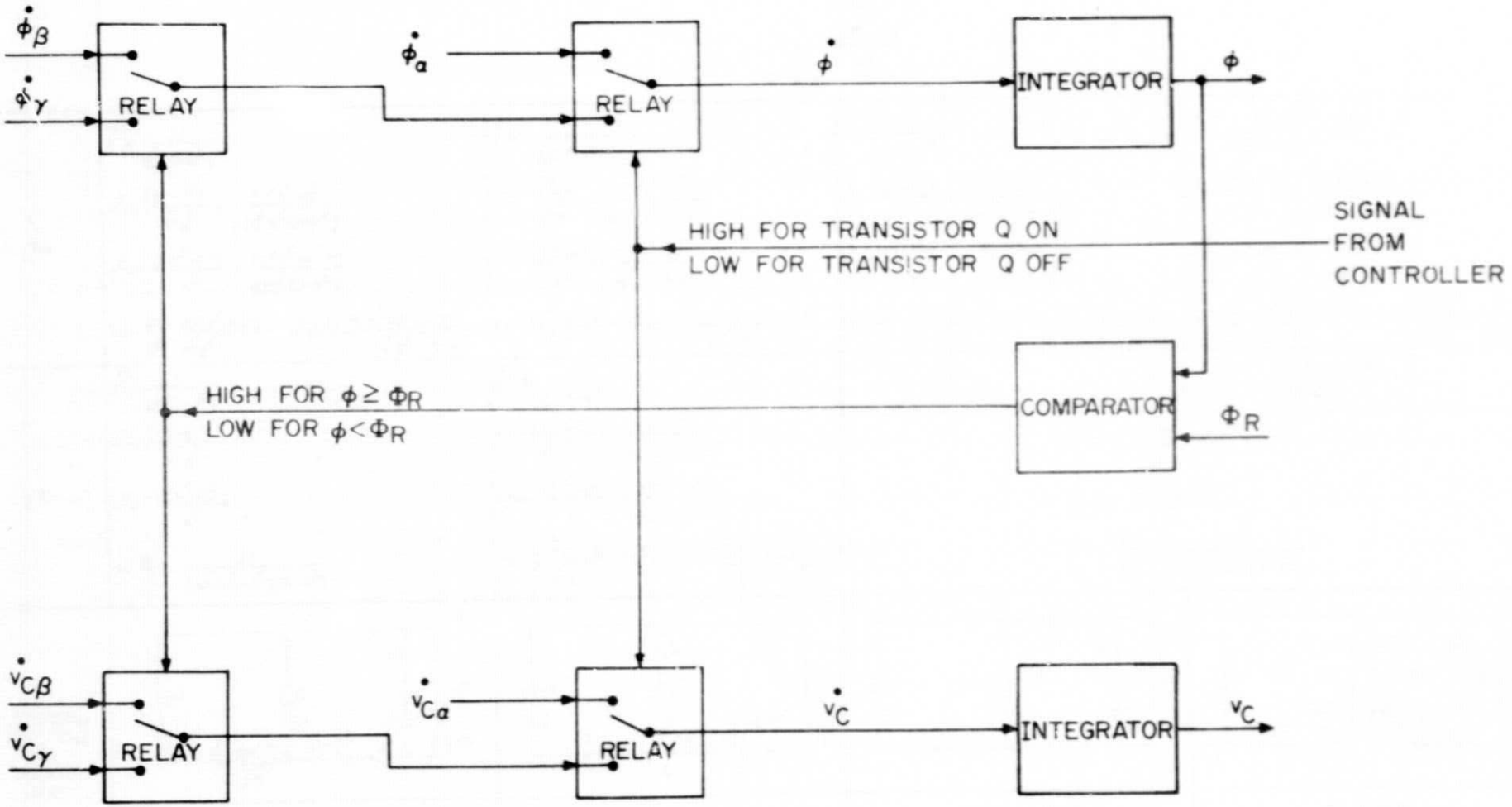


Figure 1. Switching logic for selecting the appropriate state-variable equations.

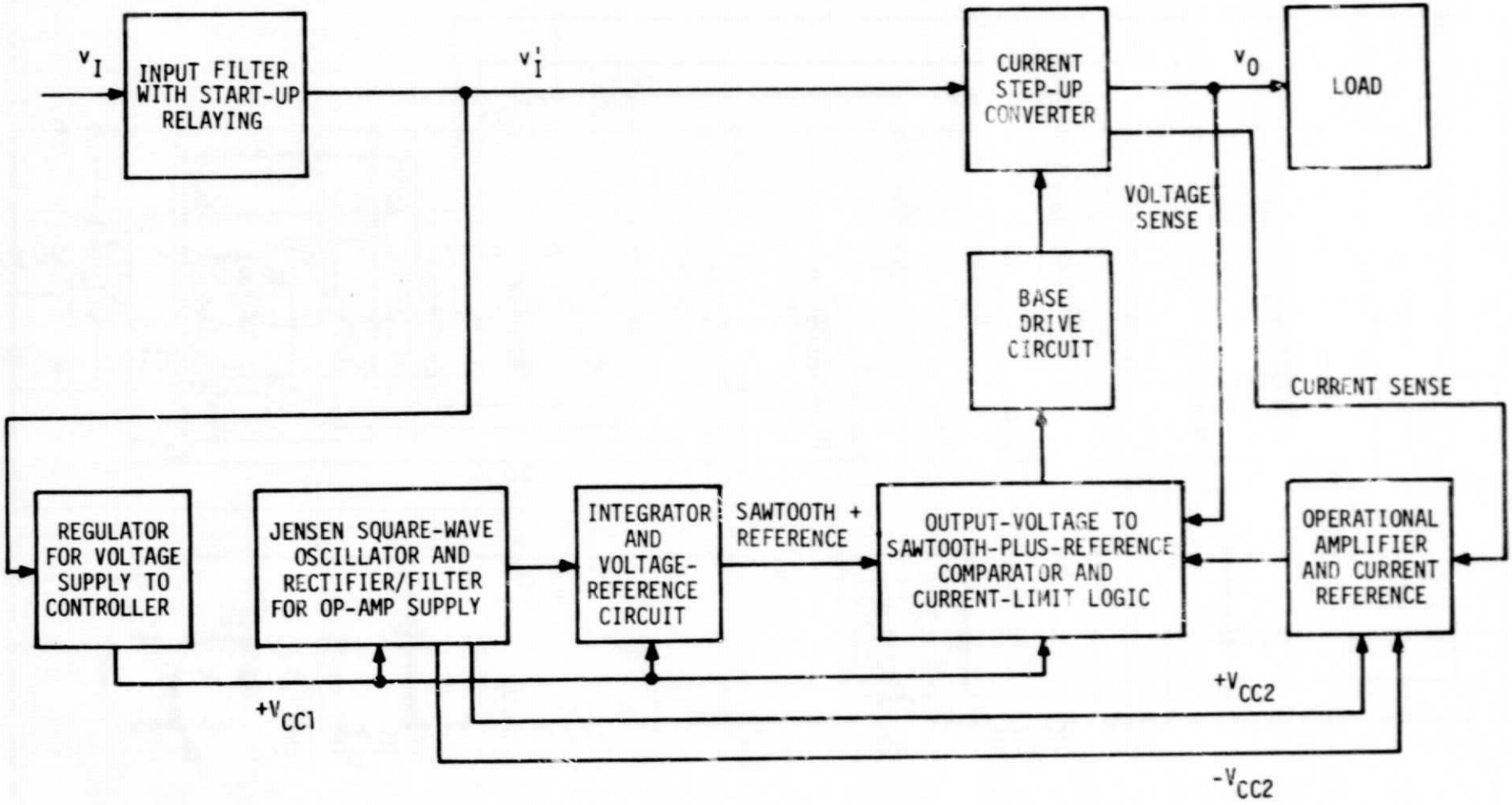


Figure 2. Block diagram of the preregulator for the A2 X-ray experiment on the High Energy Astronomy Observatory Satellite (HEAO).

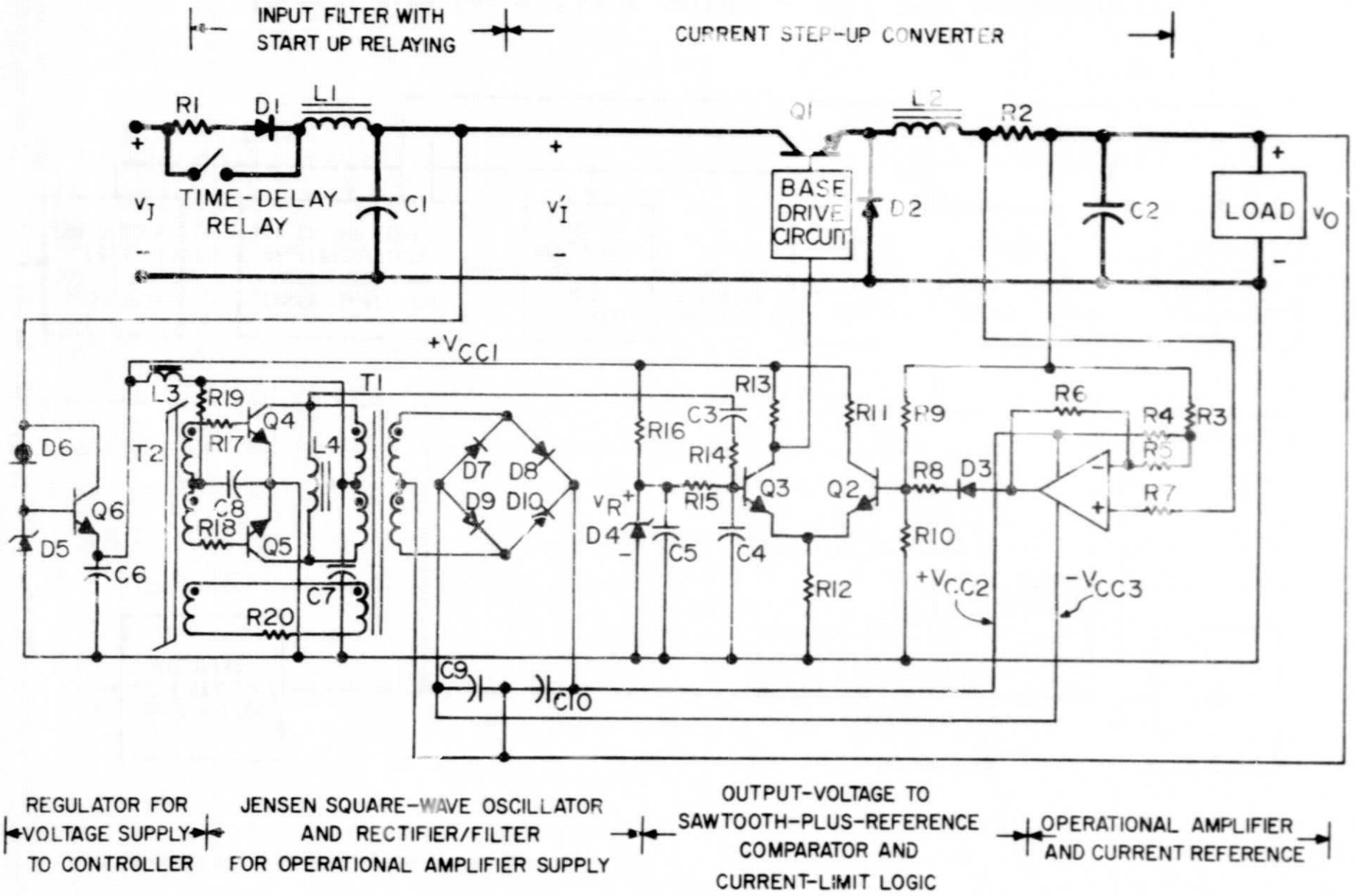


Figure 3. Simplified circuit diagram of HEAO-A2 X-ray experiment preregulator.

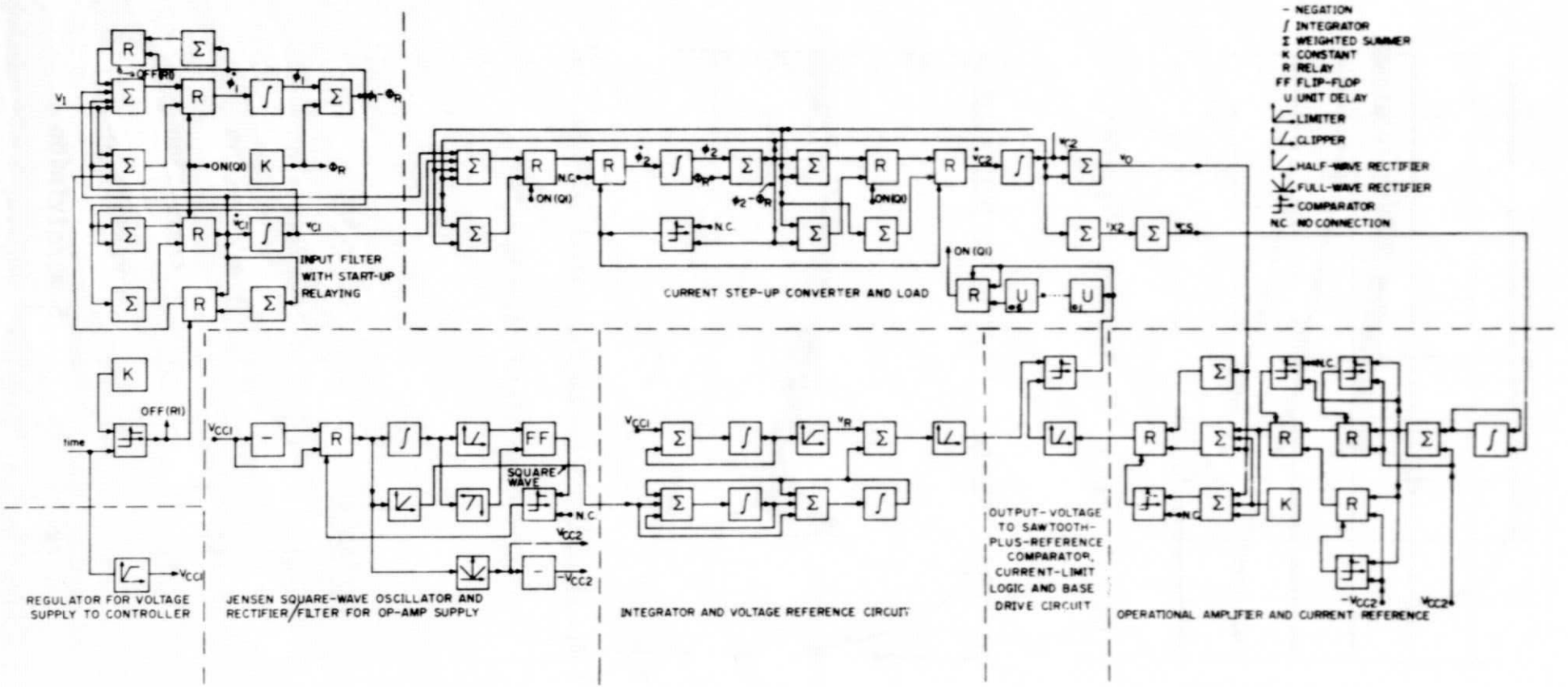
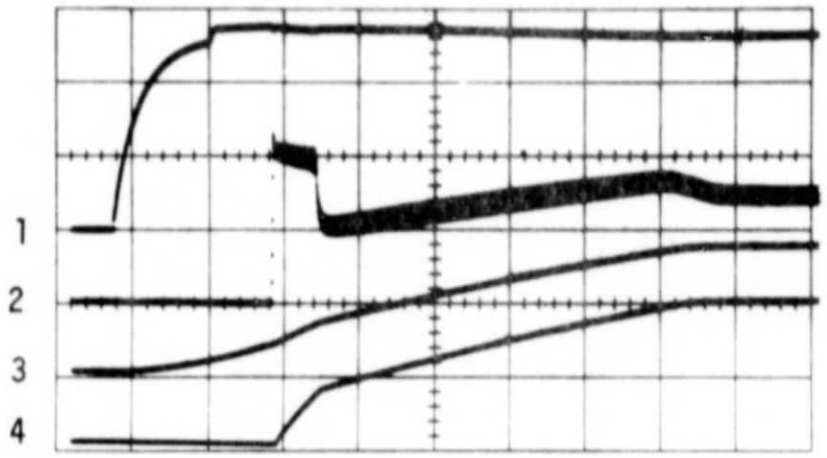
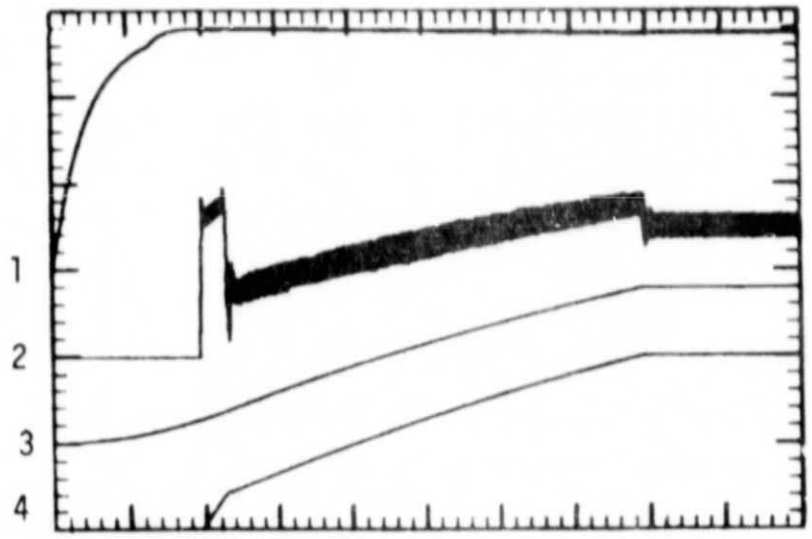


Figure 4. Block diagram for simulating HEAO-A2 X-ray experiment preregulator.



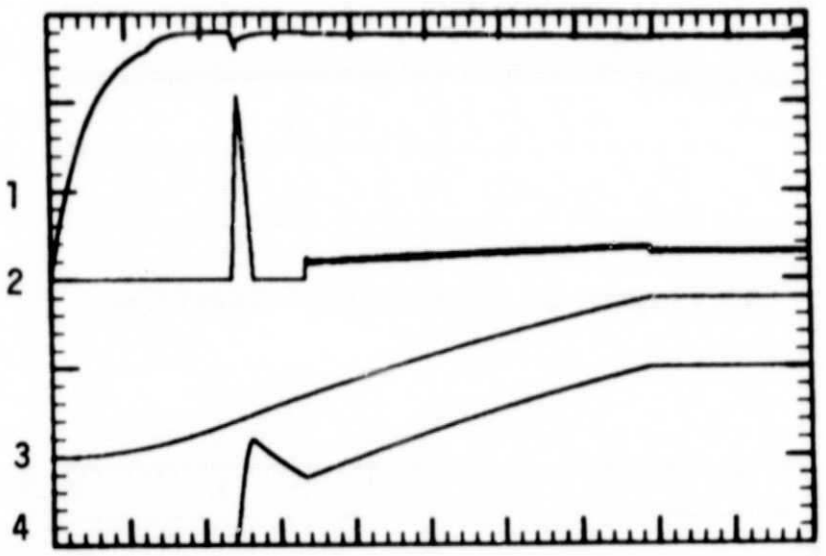
Oscillogram of Experimental Waveforms



Computer Simulation Waveforms

Waveform	Variable	Scale	Range
1	v_I'	10 V/division	-30 to +30 V
2	i_{X2}	1 A/division	-2 to +4 A
3	v_R	5 V/division	-5 to +25 V
4	v_O	10 V/division	0 to +60V
	Time	5 ms/division	0 to 50 ms

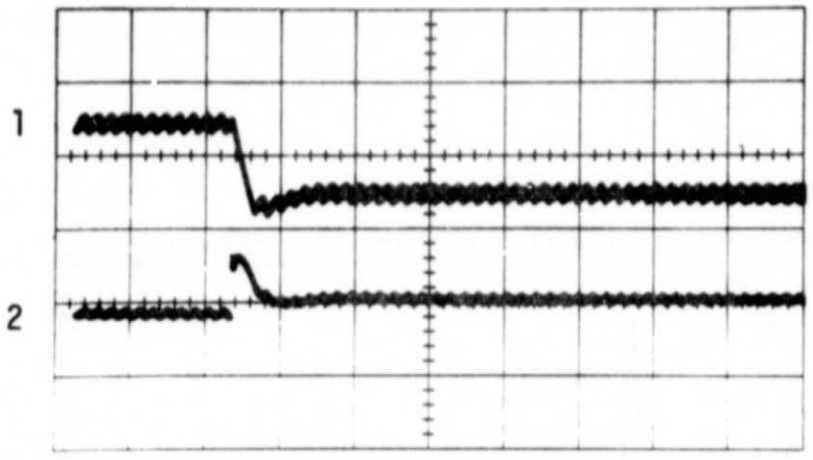
Figure 5. Start-up transients in HEAO-A2 preregulator.



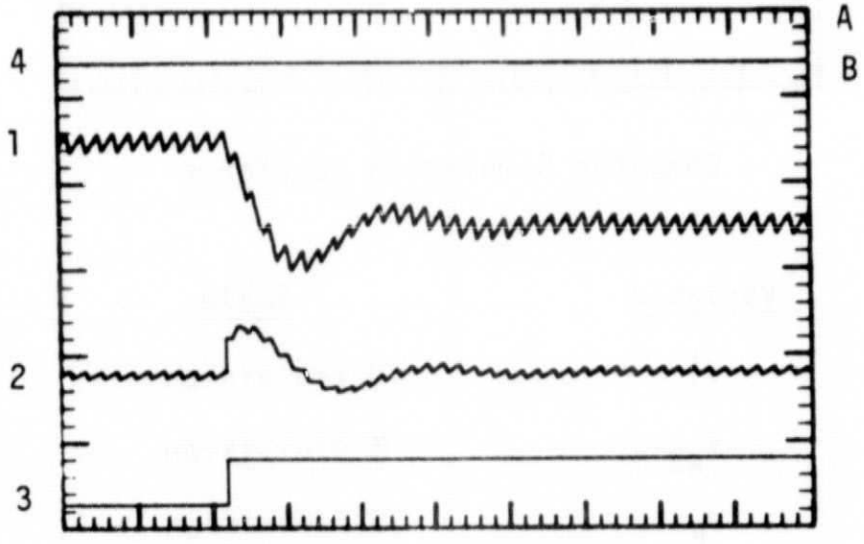
Computer Simulation Waveforms

Waveform	Variable	Scale	Range
1	v_I'	10 V/division	-30 to +30 V
2	i_{X2}	5 A/division	-15 to +15 A
3	v_R	5 V/division	-5 to +25 V
4	v_C	10 V/division	0 to +60V
	Time	5 ms/division	0 to 50 ms

Figure 6. Start-up Transients in HEAO-A2 preregulator with current-limit feature disabled.



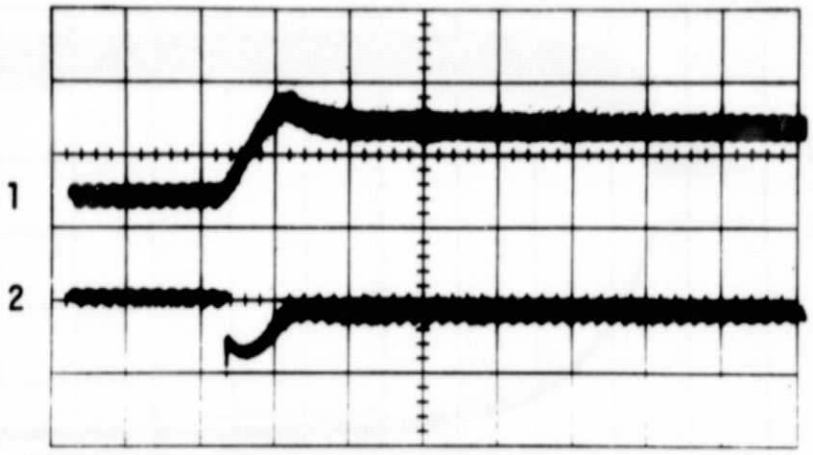
Oscillogram of Experimental Waveforms



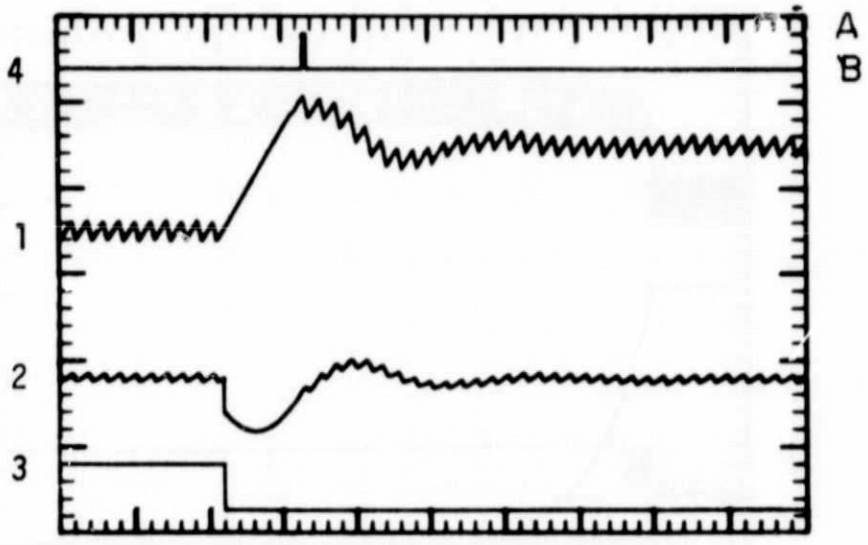
Computer Simulation Waveforms

Waveform	Variable	Scale	Range
1	i_{X2}	1 A/division	-3 to +3 A
2	V_O	.2 V/division	+19.6 to +20.8 V
3	R_L	50 Ω/division	0 to 300 Ω
4	Current-limit mode	Position: A - in; B - out	
	Time	200 μs/division	

Figure 7. Transients in HEAO-A2 preregulator due to 30-watt to 10-watt load change.



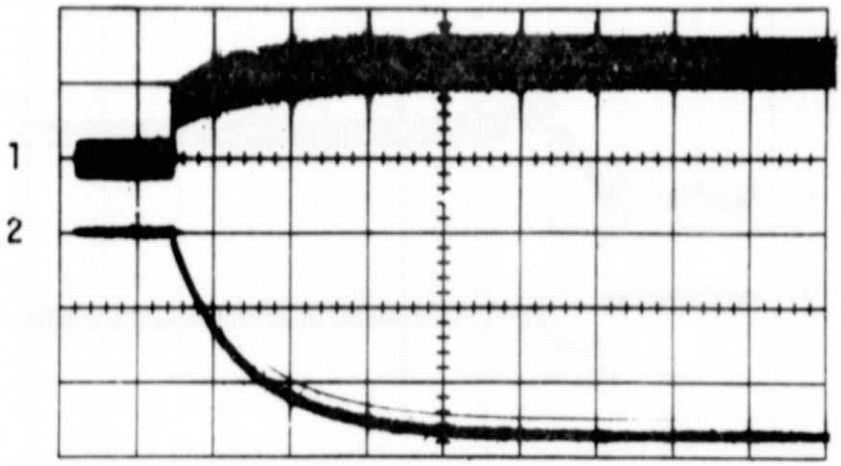
Oscillogram of Experimental Waveforms



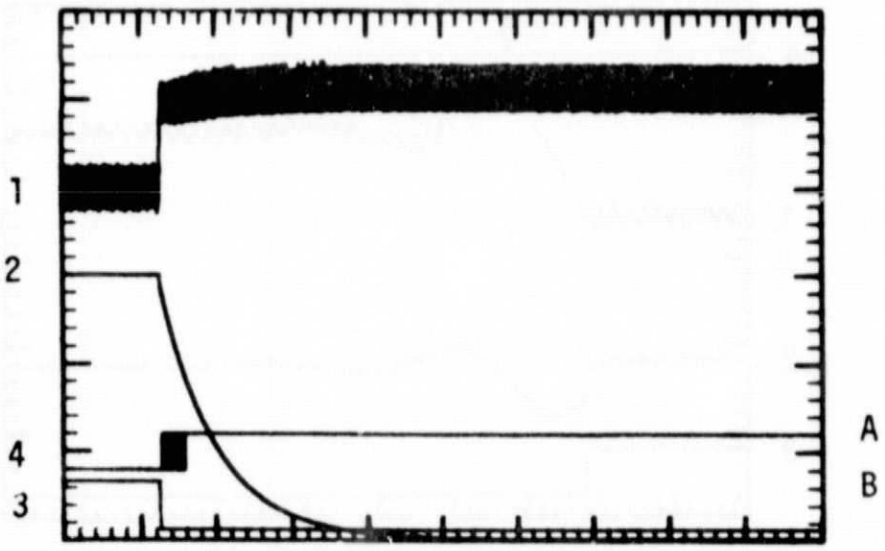
Computer Simulation Waveforms

Waveform	Variable	Scale	Range
1	i_{X2}	1 A/division	-3 to +3 A
2	v_O	.2 V/division	+19.6 to +20.8 V
3	R_L	50 Ω/division	0 to 300 Ω
4	Current-limit mode	Position: A - in; B - out	
	Time	200 μs/division	

Figure 8. Transients in HEAO-A2 preregulator due to 10-watt to 30-watt change.



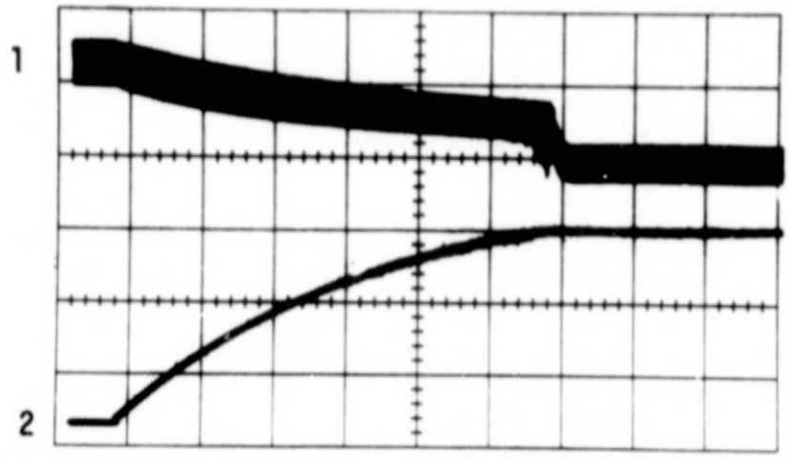
Oscillogram of Experimental Waveforms



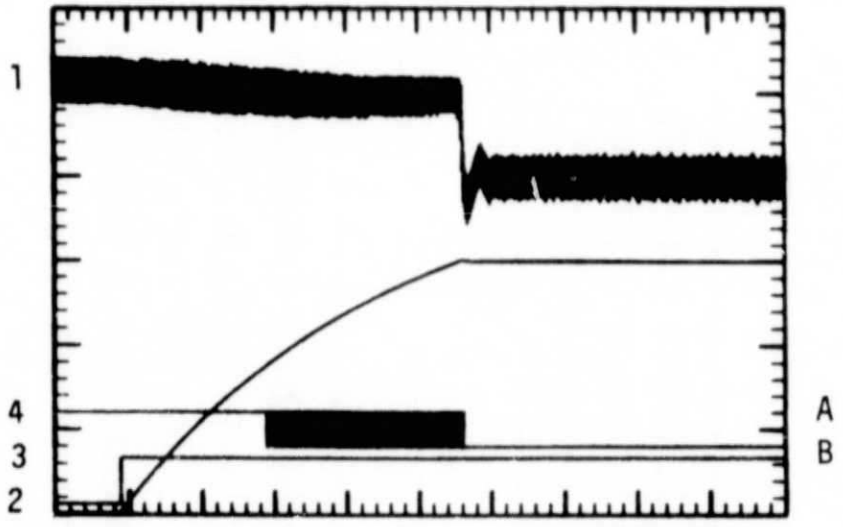
Computer Simulation Waveforms

Waveform	Variable	Scale	Range
1	i_{X2}	.5 A/division	-.5 to +2.5 A
2	v_0	5 V/division	+5 to +35 V
3	R_L	20 Ω/division	0 to 120 Ω
4	Current-limit mode	Position: A - in: B - out	
	Time	2 μs/division	

Figure 9. Transients in HEAO-A2 preregulator due to application of 3-ohm fault in parallel with 13.33 ohm load resistance.



Oscillogram of Experimental Waveforms



Computer Simulation Waveforms

Waveform	Variable	Scale	Range
1	i_{X2}	.5 A/division	-.5 to +2.5 A
2	v_O	5 V/division	+5 to +35 V
3	R_L	20 Ω/division	0 to 120 Ω
4	Current-limit mode	Position: A - in; B - out	
	Time	2 μs/division	

Figure 10. Transients in HEAO-A2 preregulator due to removal of 3-ohm fault in parallel with 13.33 ohm load resistance.

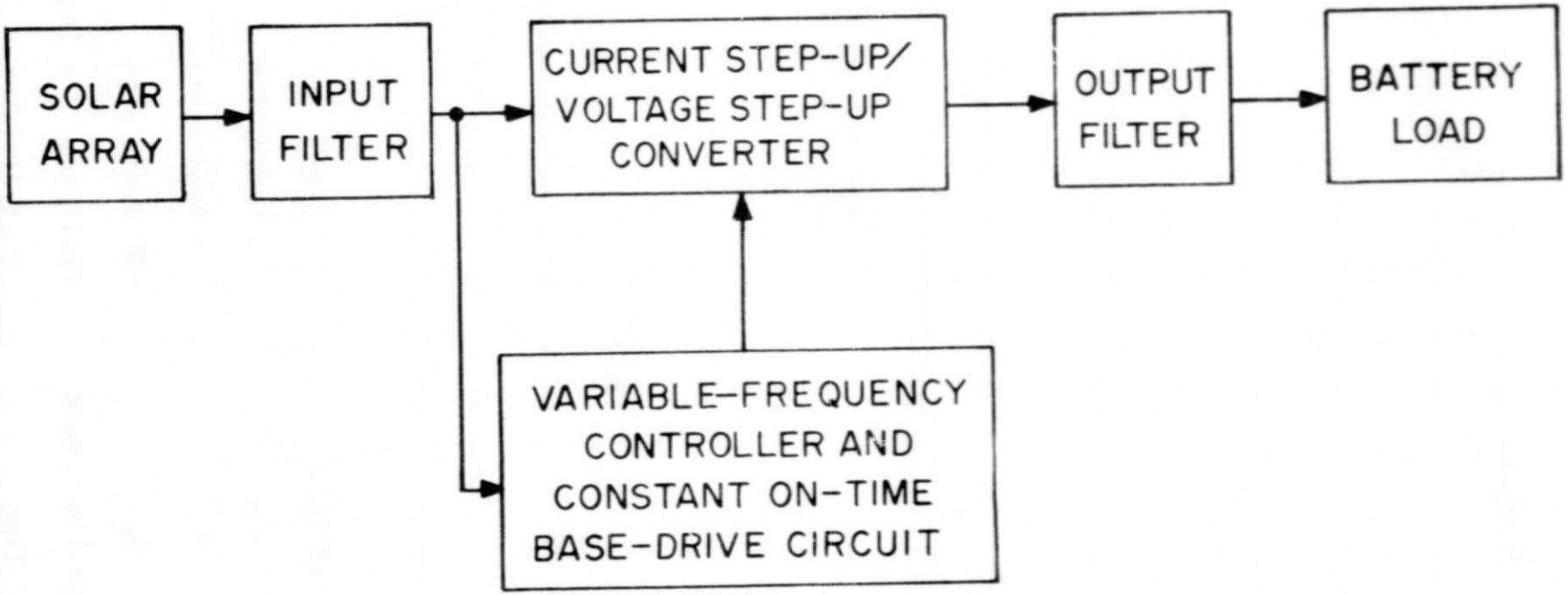


Figure 11. AE-B Battery-charger block diagram.

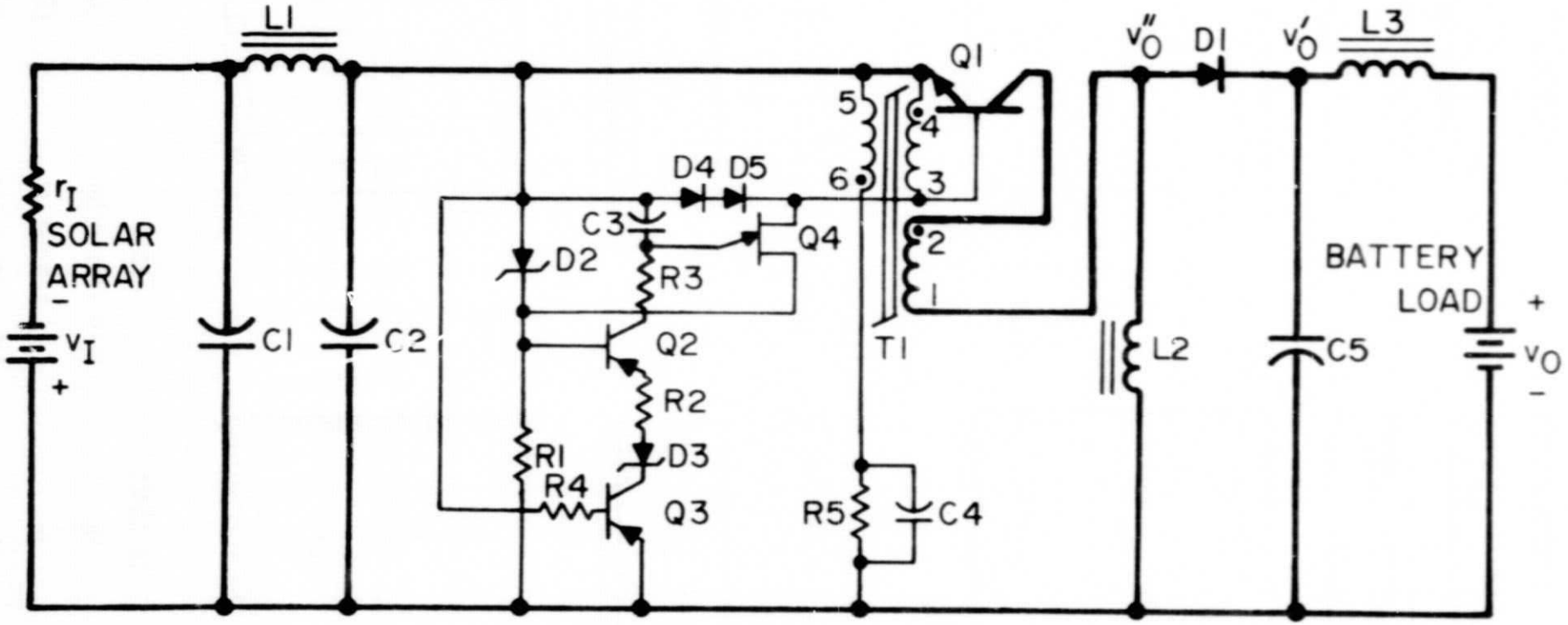
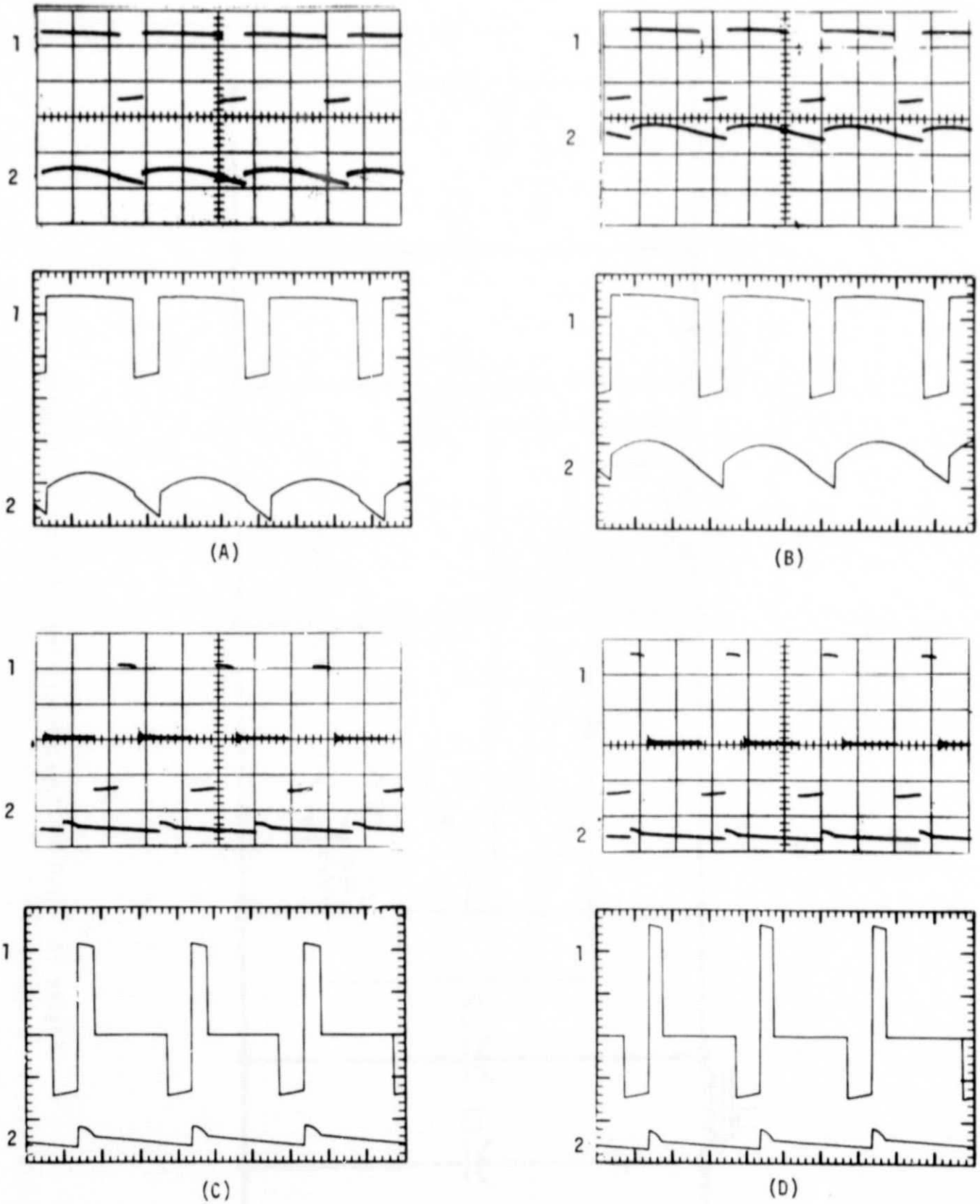


Figure 12. AE-B Battery-charger simplified circuit diagram.



Waveform	Variable	Scale	Battery Load
1	v''_0	10 V/division	(A) 3 V (B) 4 V
2	v'_0	1 V/division	(C) 20 V (D) 25 V
	Time	50 μs/division	Input power 9.1 W

Figure 13. AE-B Battery-charger Oscillographic and Simulation waveforms for input power of 9.1 watts and four different battery loads.