Digital Control For Power Factor Correction

Manjing Xie

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Dr. Fred C. Lee, Chair
Dr. Alex Q. Huang
Dr. Thomas L. Martin

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ABSTRACT

This thesis focuses on the study, implementation and improvement of a digital controller for a power factor correction (PFC) converter.

The development of the telecommunications industry and the Internet demands reliable, cost-effective and intelligent power. Nowadays, the telecommunication power systems have output current of up to several kiloamperes, consisting of tens of modules. The high-end server system, which holds over 100 CPUs, consumes tens of kilowatts of power. For mission-critical applications, communication between modules and system controllers is critical for reliability. Information about temperature, current, and the total harmonic distortion (THD) of each module will enable the availability of functions such as dynamic temperature control, fault diagnosis and removal, and adaptive control, and will enhance functions such as current sharing and fault protection. The dominance of analog control at the modular level limits system-module communications. Digital control is well recognized for its communication ability. Digital control will provide the solution to system-module communication for the DC power supply.

The PFC converter is an important stage for the distributed power system (DPS). Its controller is among the most complex with its three-loop structure and multiplier/divider. This thesis studies the design method, implementation and cost effectiveness of digital control for both a PFC converter and for an advanced PFC converter. Also discussed is the influence of digital delay on PFC performance. A cost-effective solution that achieves good performance is provided. The effectiveness of the solution is verified by simulation.

The three level PFC with range switch is well recognized for its high efficiency. The range switch changes the circuit topology according to the input voltage level. Research literature has discussed the optimal control for both range-switch-off and range-switch-on topologies. Realizing optimal analog control requires a complex structure. Until now optimal control for the three-level PFC with analog control has not been achieved. Another disadvantage of the three-level PFC is the output capacitor voltage imbalance. This thesis proposes an active balancing solution to solve this problem.

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1 INTRODUCTION

Power supplies for the computer and telecommunications industry have become more and more important in our society.

The greatest concern is power supply availability or redundancy. Not just because downtime can cause millions of dollars of lost in revenue for large corporations such as banks, insurance companies and e-business companies [1], as shown in Table 1 [4], but also because it is intolerable for mission-critical applications in which systems handle real-time commands and human lives. Thus, power electronics and related power processing technologies are called “enabling infrastructure technology” [2]. High redundancy, for example the N+1 technology, has been widely adopted to secure availability.

Table 1 Cost of Power outage [4]

Industry	Average Cost of Downtime ($/hour)
Cellular communications	41,000
Telephone ticket sales	72,000
Credit card operations	2,580,000
Brokerage operations	6,480,000

The problem with the current power supply system is the difficulty in system-module communication, which at present is confined to on/off signals. When there is a failure, the system controller can give only “on/off” instructions to the individual module. With large amounts of consumable and finite-life components, the power supply can fail and trip occasionally. At present, diagnosis and repair are left to technicians, which adds to the redundancy and maintenance cost. Failure diagnosis, repair on the module level, and system-level dynamic control

will prevent sudden power outages. This intelligence relies on the implementation of digital control of power supplies on both the module level and the system level.

With expanding functions and storage, power consumption keeps increasing. No one can predict the ultimate limit. The product life span of telecom equipment is just 18 to 24 months [1]. While power supply technology is not evolving so quickly, reusing the previous design could be cost effective [1]. Reusing the power supply product for the next generation of products makes flexibility a must.

Digital control is well recognized for its communication ability, flexibility and capability in implementation of nonlinear control. The advances of the IC industry provide the possibility for a capable and cost effective digital signal processor. Different from many occasions in which the computing speed of the digital signal processor is the most critical feature, the selection of the DSP may depend more on availability of special on-chip hardware features, for example pulse width modulation (PWM) and an analog-to-digital converter (ADC). Trade-off exists between cost and performance. The higher cost of the DSP can even be compensated by the reduction of the parts count, which can enable mass production of control board instead of customized manufacture. Nonetheless, cost effectiveness is always the goal of industry and academic research.

1.1 Brief Review of DC Power Supply System

As early as 1978, the first International Telecommunications Energy Conference (Intelec) addressed the energy issue generated by the emerging digital, optical and wireless systems, and the need for energy-efficient and cost-effective power systems and architectures to assure the expected high reliability and dependability of the public switched telephone network [3]. Over the years, the exploding growth of the Internet and data communications has impacted power in two ways. First, it has increased the demand for higher-capacity central office power plants. High-power plants (3,000 to 10,000 Amps) are expected to grow at 20% to 25% annually for several years. Secondly, the growth has also energized

the debate over the preferred powering for telecommunications: non-stop DC power system or UPS-protected AC power systems [3]. Telecom 48V DC power systems are at least 20 times more reliable than AC UPS systems for typical datacom applications [3]. More users and operators of the Internet are starting to expect the non-stop DC power supply systems. As the trend continues, more and more electric power will be processed by distributed power systems (DPSs). System functions of DPS will soon become an important research topic.

The DPS architecture can better address the increasing concerns regarding fault tolerance, improved reliability, serviceability and redundancy without a significant added cost [6]. But as the DC power system grows, current sharing, fault diagnosis and health monitoring will become more difficult.

Figure 1 shows a typical DPS [8]. Each front-end converter adopts a conventional two-stage approach. The first stage achieves the power factor correction from universal single-phase input line voltage (90-264V). The second stage provides isolation and the tightly regulated DC bus voltage. Normally, a conventional single-switch continuous-conduction-mode (CCM) boost converter is used in the first stage. The output DC voltage of the PFC must be higher than 375 for universal-line applications. In this thesis, the output voltage of PFC is set to 400V. The DC/DC converter converts 400V DC into 48V DC output.

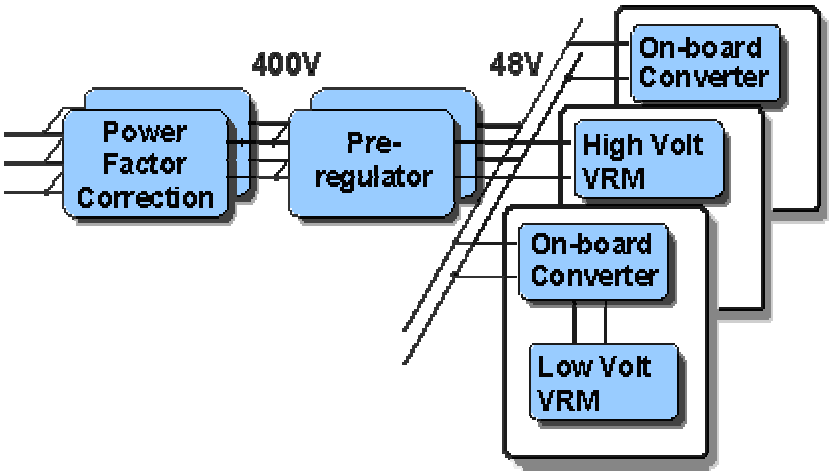


Figure 1 Structure of the distributed power system.

The roadmap for the CPU industry suggests that the CPU of tomorrow will operate with high di/dt, consuming more current and requiring a tighter voltage transient response [1,4]. Reliability requirement will become stricter. System functions such as impedance matching analysis, system-aging prediction, dynamic thermal control and fault self-removal will greatly increase DC power system-level reliability. Realization of these functions requires better communication between the module and the system controller and a smarter modular controller.

1.2 Brief Review of the Digital Signal Processor

Digital signal processing is widely used in the motor control, inverter, converter and many embedded systems because of its ability to handle deterministic operation and deal with interruptions, and its strong computation ability, which is required by space vector calculation.

As the technology advances, the cost continues to drop, as shown in Table 2. In 1982, a 50,000-transistor DSP offered 5 MIPS for $150. A decade later, in 1992, a 500,000-transistor DSP capable of 40 MIPS cost $15. Current projections by Texas Instruments are a 5-million-transistor DSP that provides 5,000 MIPS will be priced at just $1.50 [5]. As the process technology advances the trend will continue.

Table 2 Two decades of DSP market integration (typical DSP figures)

	1982	1992	2002
Die Size (mm)	50	50	50
Technology Size (Microns)	3	0.8	0.18
MIPS	5	40	5,000
MHz	20	80	500
RAM (Words)	144	1,000	16,000
ROM (Words)	1,500	4,000	64,000
Transistors	50,000	500,000	5 million
Price (dollars)	150	15	1.50

At the same time, more and more analog functionality has been integrated. Analog-to-digital converter (ADC) and pulse-width-modulation (PWM) are standard for most motor control-oriented DSPs. The speed of on-chip ADC has already reached 20MHz.

Adoption of digital control will sooner or later become a trend in the large DC power supply industry.

1.3 Goal of Thesis

The goal of this thesis is to study both the performance and cost effectiveness of digital control for a PFC converter and the possibility of implementing a reliable, high-efficiency, universal-line-input, three-level PFC converter with digital control.

1.4 Task Description

Because of the slow response speed and the complexity of the control structure, digital control for PFC is the first task for the work on the whole system. This thesis describes the design, implementation and improvement of digital control for PFC. Based on the experimental and simulation results, cost effectiveness is examined.

1.5 Thesis Organization

Chapter 1 is the introduction to this thesis, and provides a summary of the background of this work. Task descriptions and thesis organization are also given.

Chapter 2 surveys the current literature in the field of digital control for power supply systems.

Chapter 3 describes the PFC converter. The function is described, and the control structure of the converter is explained. Detailed control requirements are explained. Finally digital controllers are designed and implemented. The current loop feed forward method is proposed for improve power factor correction performance.

Chapter 4 describes the design and implementation of digital control for a three level PFC converter. Optimal control and operation of the three-level PFC is specified. The solution to output capacitor balancing is proposed.

2 REVIEW OF LITERATURE

With the development of the DC power supply, attention began to be paid to digital control for PFC, DC/DC converters, and voltage regulation modules (VRMs). To apply digital control to PFC, it is imperative to learn the previous work and understand the challenges.

The boost converter and boost-buck (flyback) converter are both suitable for PFC. The boost converter is widely used in two stage DPS for its smaller EMI filter and lower voltage stress [2,8]. This thesis focuses on digital control for boost-type PFC.

2.1 Challenges of Digital Control for PFC

The three-loop control scheme for PFC is widely adopted in industry. Commercial IC chips such as UC3854 and ML4824 have been available for a long time. The current compensator is the most important. To faithfully track the semi-sinusoidal current reference, the current loop must be fast [6]. The integral, phase-lead average current compensator is widely used for the analog compensator for PFC current loop. L. Dixon (1990) and C. Zhou (1992) discussed the design and design trade-offs in their own papers [17, 7]. The voltage loop bandwidth is much slower than twice the line frequency because the existence of the second harmonic in the output voltage [6].

When digital control is applied, it is inevitable that sample-and-hold and computation delays will be introduced, resulting in phase lag (C.L. Phillips, 1984) [10]. For a given delay, the higher the bandwidth, the more phase lag is introduced at the crossover frequency. For current loop, which has a wide bandwidth, when designing a digital current compensator, one must consider the phase lag caused by digital delays. Bibian (2001) pointed out that digital control for PFC suffers from reduced performance due to computation delay and sample-and-hold delays [35].

One can either increase DSP speed to reduce digital delay or lower the current loop bandwidth to alleviate the influence of digital delay. However, increasing DSP speed would increase the cost while a lower current loop bandwidth would compromise performance. Selecting the crossover frequency of current loop becomes a trade-off between performance and cost.

2.2 Realization of Digital Control

2.2.1 Digital Signal Processor (DSP) Realization of Digital Controller

Because of the availability of DSPs, many DSP controllers have been proposed and implemented [13, 21-24, 29, 35]. Most of these DSPs are motor control-oriented. However, PFC has its own requirement: high frequency and low cost. Two factors influence the selection of DSP frequency. First, DSP realization is sequential, which means instructions are executed one after another, thus accumulating computation delay. To achieve a small delay, a high frequency DSP will be used. Second, most DSPs have system clock based PWM units; in order to obtain high-resolution digital PWM (DPWM), a fast DSP must be used. The DSP solution is not cost-effective for future digital control of PFC [28].

2.2.2 Concurrent Realization of Digital Controller

Concurrent realizations have also been discussed. Field-programmable-gate-array (FPGA) and mix-signal Application-specific-integrated-circuit (ASIC) are two concurrent realizations of the digital controller for PFC.

P. Zumel, et al. in [27] noted that when a complex controller is implemented, FPGA requires more resources. The same law applies to ASIC realization. R. Zane, et al. pointed out that digital control for the current loop requires high-speed ADC and it may also suffer from possible stability problems if PWM

resolution is not high enough [34]. The current compensator and PWM resolution become bottlenecks when low cost digital controller is implemented for PFC.

Whatever realization method is adopted, current compensator complexity, current loop gain and loop bandwidth is closely related to cost and performance of the digital controller. When it comes to cost effectiveness it is necessary for us to find out the relation between current loop gain and performance and explore the possibility of using simple compensator to achieve the desired performance.

2.3 Small-Signal Model for the Low-Frequency Range

This thesis implies that the power factor is also affected by input voltage. To understand the relation between current compensator and power factor, a small-signal model for the frequency range (twice line frequency ~ 1kHz) is necessary. While a quasi-static small signal model is not valid for frequency range around line frequency. A. Huliehel, et al. derived a small-signal model for this frequency range [38]. For low frequency range, the relation between current compensator and input voltage might be explained by this model.

3 DESIGN AND IMPLEMENTATION OF SINGLE SWITCH PFC CONVERTER

3.1 State-of-the-art controller for PFC Converter

3.1.1 PFC Converter

3.1.1.1 Power Factor

A detailed definition of power factor is given in [6]. Power factor (PF) is the ratio of average power to apparent power at an AC terminal.

$$PF = \frac{Average \quad power}{Apparent \quad power} = \frac{avg[v(t) \cdot i(t)]}{V_{rms} \cdot I_{rms}} \qquad \text{Eq. 3-1}$$

Assuming an ideal sinusoidal input voltage source, PF can be expressed as the product of two factors: the displacement factor k_θ and the distortion factor k_d. The displacement factor k_θ is the cosine of the displacement angle between the fundamental input current and the input voltage. The distortion factor k_d is the ratio of the root-mean-square (RMS) of the fundamental input current to the total RMS of input current. These relationships are given as follows:

$$PF = \frac{V_{rms} I_{rms(1)} \cos\theta}{V_{rms} I_{rms}} = \frac{I_{rms(1)} \cos\theta}{I_{rms}} = k_d k_\theta \qquad \text{Eq. 3-2}$$

where: V_{rms} is the voltage total RMS value,

I_{rms} is the current total RMS value,

$I_{rms(1)}$ is the current fundamental harmonic RMS value,

θ is the displacement angle between the voltage and current fundamental harmonics,

$k_\theta = \cos\theta$ is the displacement factor,

$k_d = \frac{I_{rms(1)}}{I_{rms}}$ is the distortion factor.

In Figure 2, examples of different current shapes show the different distortion factors and displacement factors [6].

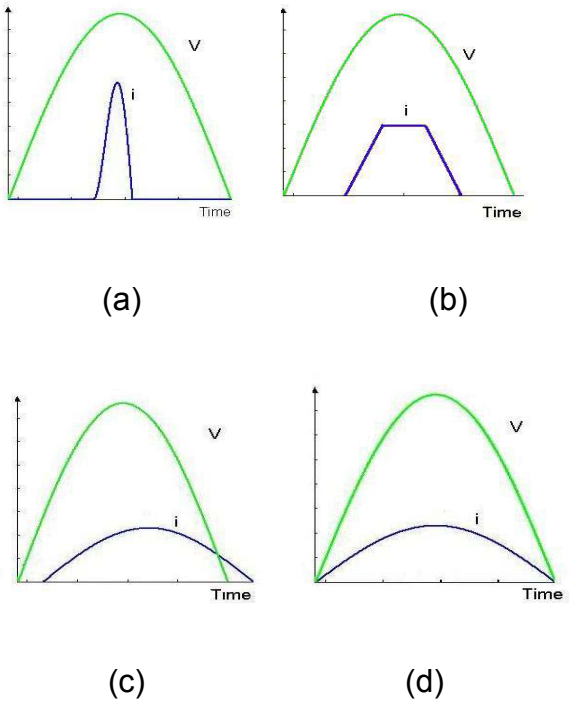


Figure 2 Illustration of PF relationship between current and voltage:
(a) $k_\theta < 1, k_d < 1$, **(b)** $k_\theta = 1, k_d < 1$, **(c)** $k_\theta < 1, k_d = 1$, **(d)** $k_\theta = 1, k_d = 1$

In the first case, a smaller k_θ means a larger apparent current for the same load. As we know, current causes more losses in a supply and distribution system. Utility companies regulate customers' k_θ. In the second case, a small k_d means a large amount of harmonics in the current, which pollutes the utility power source and affects other users. All the power supplies have to meet PF standards, for

example, the IEC 61000-3-2. Converting AC to DC, the conventional diode-rectifiers always produce large amounts of harmonic current. Nowadays, the most advanced solution is to add PFC converter.

3.1.1.2 PFC Boost Converter

Among the three basic power converters—buck, boost, buck-boost—the boost converter is the most suitable for use in implementing PFC. Because the boost inductor is in series with the line input terminal, the inductor will achieve smaller current ripple and it is easier to implement average current mode control. Buck converter has discontinuous input current and would lose control when input voltage is lower than the output voltage. The buck-boost converter can achieve average input line current, but it has higher voltage and current stress, so it is usually used for low-power application [8]. The power stage adopted in this thesis is boost converter operating in continuous conduction mode. Figure 3 shows the circuit diagram of the boost PFC converter [8].

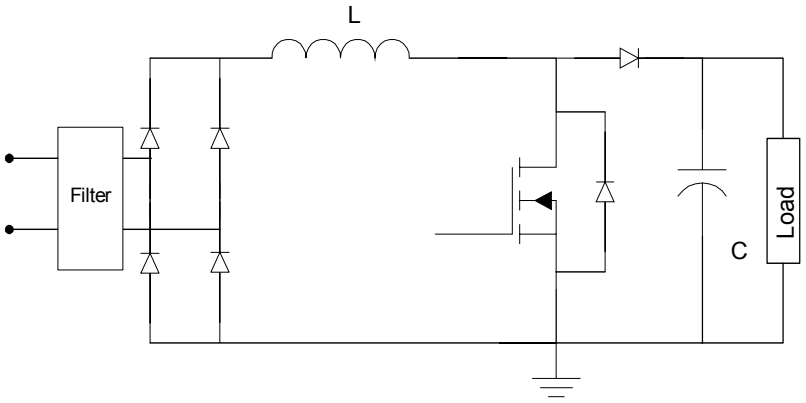
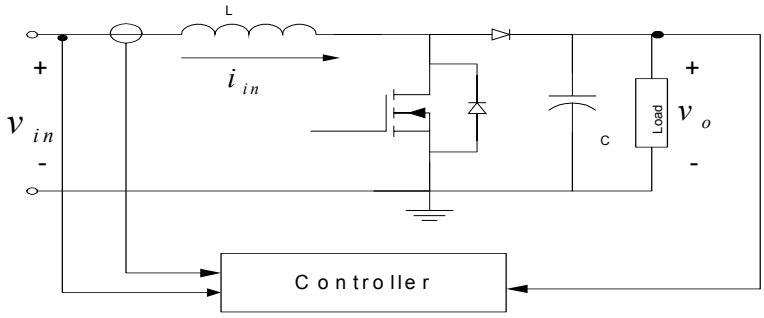


Figure 3 Boost Power Factor Correction converter

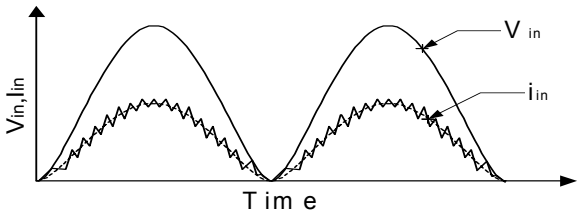
3.1.2 Review of Control Structure for PFC

As shown in Figure 4, the controller has two tasks:

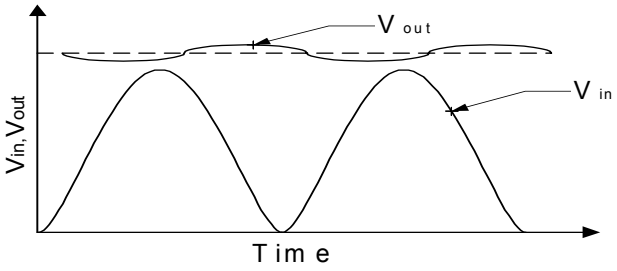
1. Current tracking forces the average inductor current to track the current reference so that it has the same shape as the input voltage, as shown in Figure 4 (b). This task gives the input a unity PF.
2. Voltage regulation regulates the output voltage keeping the output voltage equal to 400V, which is higher than the input voltage as shown in Figure 4 (c).



(a)



(b)



(c)

Figure 4 Boost PFC converter controller: (a) Boost PFC with controller, (b) Waveforms of input voltage and inductor current, (c) Waveforms of input voltage and output voltage.

The analog controller for PFC is often achieved by a current-mode PFC control chip such as the Unitrode UC3854 [19]. The analog control structure for a single switch CCM PFC boost converter is illustrated in Figure 5. The PFC converter has a three-loop control structure. The fast current loop keeps the input current the shape of the input voltage, which renders the unity PF [6-7]. The input voltage feed-forward loop is to compensate the input voltage variation [6]. The voltage loop keeps the output voltage at 380~400V [6-7]. The voltage loop is very slow to avoid introducing 2nd harmonic ripple into the current reference [6, 7].

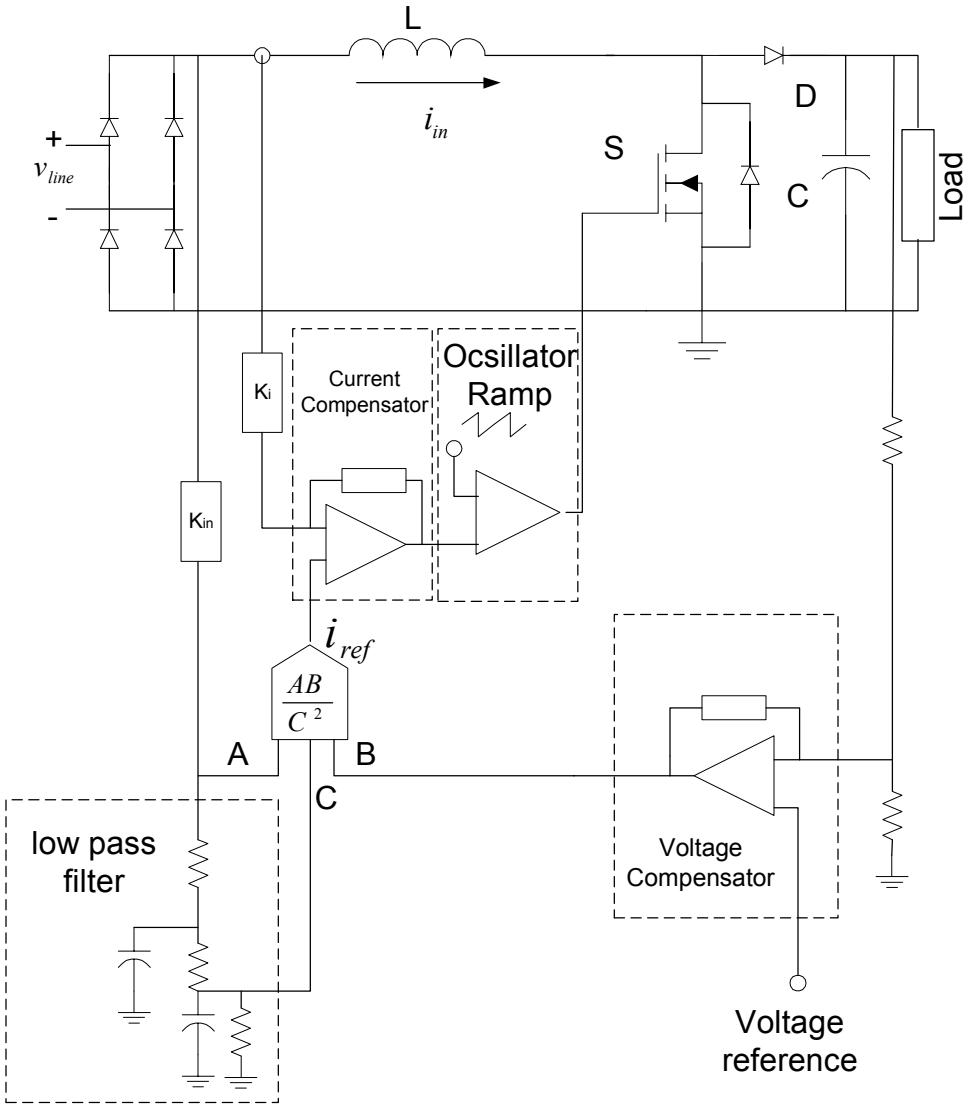


Figure 5 Analog average current control For boost-type PFC

3.1.2.1 Current loop Compensation

The function of the current compensator is to force the current to track the current reference that is given by the multiplier and which has the same shape as the input voltage. So the current loop bandwidth must be higher than the reference bandwidth. For faithfully tracking a semi-sinusoidal waveform of 120 or 100Hz, the bandwidth of the current loop is usually set to 2-10KHz [6].

Using the three terminal average models, a small-signal equivalent circuit of the current loop is shown in Figure 6.

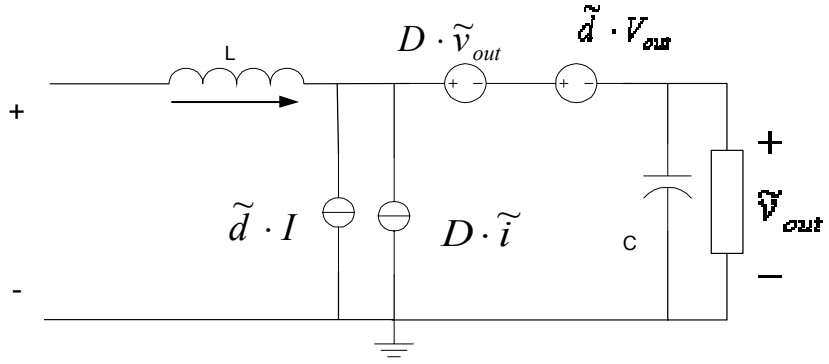


Figure 6 Small-signal model of current loop

The power stage small-signal duty-to-current transfer function is derived as follows [6]:

$$G_{id}(s) = \frac{\tilde{i}}{\tilde{d}} = \frac{2V_{out}}{R_L(1-D)^2} \cdot \frac{1+\frac{sR_LC}{2}}{1+\frac{sL}{R_L(1-D)^2}+\frac{s^2LC}{(1-D)^2}}. \qquad \text{Eq. 3-3}$$

For $s = j\omega$, when ω is large enough, the high frequency approximation can be derived:

$$G_{id}(s) = \frac{\tilde{i}}{\tilde{d}} \approx \frac{V_{out}}{Ls}. \qquad \text{Eq. 3-4}$$

Figure 7 shows Bode plots for duty-to-current transfer function for different input voltages and the high frequency approximation.

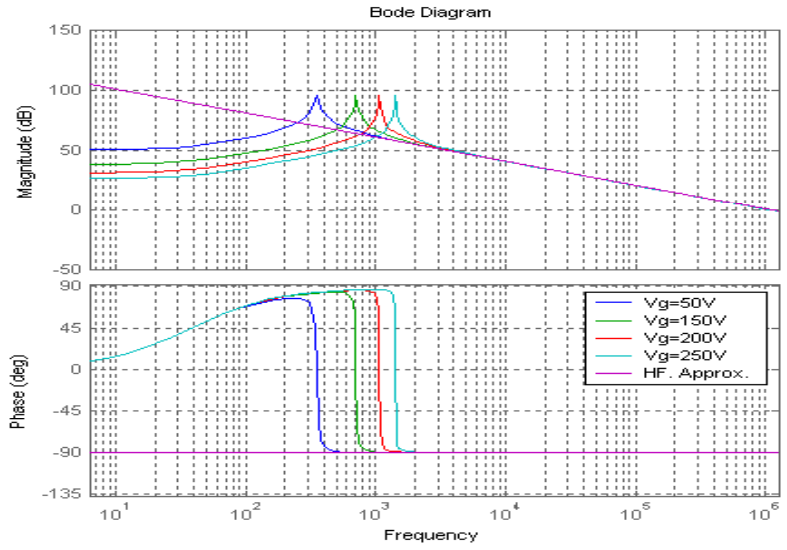


Figure 7 Small-signal duty-to-current transfer functions

Integral and lead-lag compensation is usually employed in average-current-model control. Figure 8 shows Bode plots of $G_{id}(s)$ and the current open loop gain T_c of 8kHz crossover frequency and 45° phase margin.

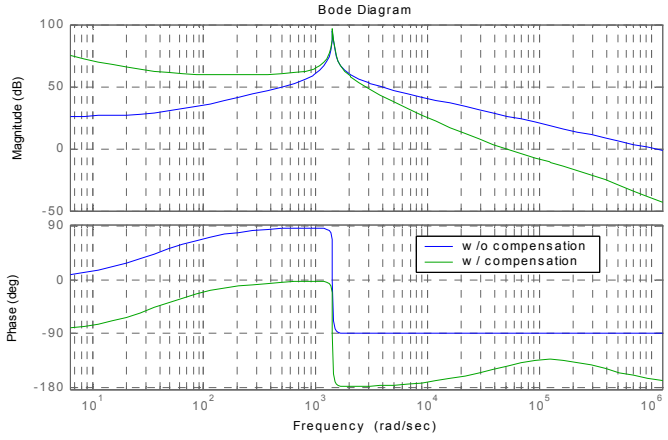


Figure 8 Duty-to-current transfer function and current open loop gain example

3.1.2.2 Feed-forward Loop Compensation

The current reference is given by:

$$i_{ref} = \frac{AB}{C^2}, \qquad \text{Eq. 3-5}$$

where $A = K_{in} \cdot v_{in}$ (K_{in}: Input voltage gain), $B = v_c$ (v_c: Voltage compensator output) and $C = K_{ff} \cdot v_{in\_rms}$ (K_{ff}: Input voltage feed forward gain).

Assume the inductor current tracks the reference perfectly. The input current is proportional to the input voltage, which means the voltage loop can be affected by input voltage variation. The feed-forward loop is inserted to compensate the line voltage variation [6]. C is in proportion to the input-voltage RMS value. It is derived from a second order low-pass filter (as shown in Figure 9).

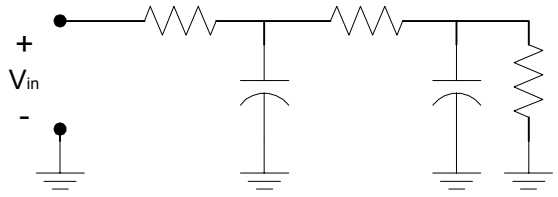


Figure 9 Second order filter in feed forward loop

Because both the input voltage and output voltage contain 2nd harmonic component, there are ripples in B and C. The ripples in components B and C are passed into the current reference. From Equation 3-5, it is derived that:

$$\frac{\Delta i_{ref}}{i_{ref}} = \frac{\Delta B}{B} - 2\frac{\Delta C}{C}. \qquad \text{Eq. 3-6}$$

Although the phases of ΔB and ΔC are unknown, the worst case occurs when they have a 180° phase shift:

$$\left|\frac{\Delta i_{ref}}{i_{ref}}\right|_{worst} = \left|\frac{\Delta B}{B}\right| + \left|2\frac{\Delta C}{C}\right|. \qquad \text{Eq. 3-7}$$

If given a maximum acceptable THD of 1.5%, Equation 3-7 means that the distortion of C should be smaller than 0.5%, and the total distortion of B should be smaller than 0.5%. Selecting the cut-off frequency of the feed-forward low - pass filter and voltage compensator gain should be based on this criterion.

3.1.2.3 Voltage Loop Compensation

Assume the input current is perfectly controlled and tracks the input voltage. Equation 3-5 can be written as $i_{in} = kv_{in}v_c$, where $k = \frac{k_{in}}{(k_{ff}v_{in\_rms})^2}$. For $P_{in} = P_{out}$ we have the following equations:

$$i_{in}v_{in} = i_o v_{out}, \text{ and} \qquad \text{Eq. 3-8}$$

$$kv_{in}^2 v_c = i_o v_{out}. \qquad \text{Eq. 3-9}$$

Using small-signal perturbation method [6], the linearized equation is obtained:

$$\tilde{i}_o = \frac{2kV_c V_{in}}{V_{out}}\tilde{v}_{in} + \frac{kV_{in}^2}{V_{out}}\tilde{v}_c - \frac{kV_{in}^2 V_C}{V_{out}^2}\tilde{v}_{out} \qquad \text{Eq. 3-10}$$

where V_C, V_{in}, V_{out} are steady state values, and $\tilde{v}_C, \tilde{v}_{in}, \tilde{v}_{out}$ are small signal perturbations.

Then, a low-frequency small-signal model is developed to design voltage compensator, as shown in Figure 10.

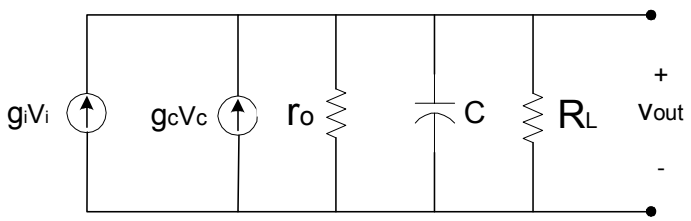


Figure 10 low-frequency Small-Signal Model for voltage loop

In Figure 10, $g_c = k\frac{V_{in\_rms}^2}{V_{out}}$, $g_i = k\frac{2V_{in}V_C}{V_{out}}$, and $r_0 = \frac{V_{out}}{I_{out}}$. For a constant power load, we have $R_L = -\frac{V_{out}}{I_{out}}$ [6]. From the small-signal model, the control to output voltage transfer function is derived as follows:

$$G_v = \frac{\tilde{v}_{out}}{\tilde{v}_c} = \frac{g_c}{Cs}. \qquad \text{Eq. 3-11}$$

For a constant power load, a voltage compensation of 45° phase margin is adopted [6]. Figure 11 shows the Bode plots for the control-to-output transfer function G_v, compensator or error amplifier transfer function G_{EA}, and the voltage open loop gain $T_v = G_v \cdot G_{EA}$.

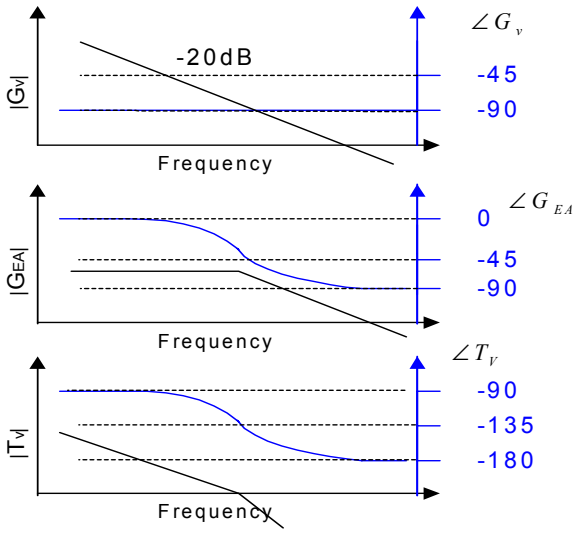


Figure 11 Voltage loop compensation with 45° phase margin

3.1.2.4 Voltage Loop Bandwidth Selection

As we have discussed in section 3.1.2.2, the ripple in B will be passed on to the current reference. The amplitude of this ripple is calculated below. Assuming that input voltage is $v_{in} = \sqrt{2}V_{in}\left|\sin\omega_L t\right|$, that the input current is $i_{in} = \sqrt{2}I_{in}\left|\sin\omega_L t\right|$ and that $\omega_L = 2\pi f_L$, where f_L is the line frequency:

$$P_o = P_{in} = v_{in}\cdot i_{in} = V_{in}\cdot I_{in}(1-\cos 2\omega_L t)\,. \qquad \text{Eq. 3-12}$$

Assume that the output voltage varies small enough to be constant. Then the output current, as shown in Figure 4 is:

$$i_o = \frac{P_o}{V_{out}} = \frac{V_{in}I_{in}}{V_{out}}(1-\cos 2\omega_L t)\,. \qquad \text{Eq. 3-13}$$

Equation 3-9 indicates that the output current consists of a large 2nd harmonic component, as shown in Figure 12(c), which is given by:

$$i_{ripple} = -\frac{V_{in}I_{in}}{V_{out}}\cos 2\omega_L t\,. \qquad \text{Eq. 3-14}$$

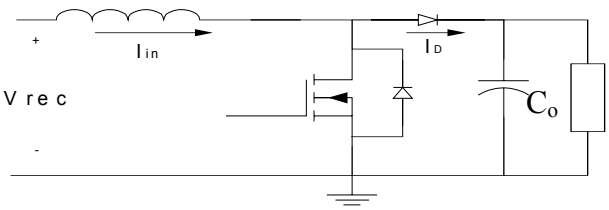
This current ripple charges and discharges the output capacitor, leading to the 2nd harmonic ripple at the output voltage, such that:

$$v_{ripple} = \frac{V_{in}I_{in}}{2V_{out}\omega_L C_o}\sin(2\omega_L t+\pi) \qquad \text{Eq. 3-15}$$

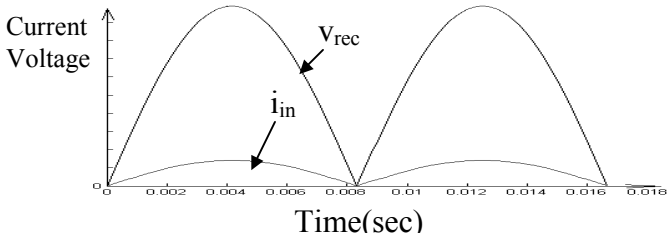
The amplitude of the ripple is:

$$V_o^{rip} = \frac{V_{in}I_{in}}{2V_{out}\omega_L C_o}\,. \qquad \text{Eq. 3-16}$$

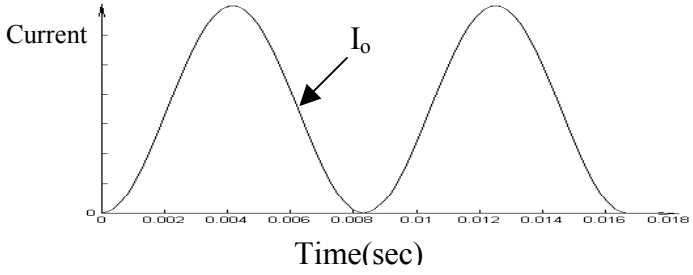
To avoid large distortion, the voltage loop compensation should have a bandwidth much smaller than 120Hz.



(a)



(b)



(c)

Figure 12 (a) Boost PFC circuit, (b) Input voltage and current waveform, (c) Average Diode forward current waveform

The 2nd harmonic in the output voltage produces a fundamental component and 3rd harmonic distortions in the line current [6]. The amplitude of the 3rd harmonic equals to half of 2nd harmonic amplitude at the voltage compensator output [6].

Another bandwidth selection of the voltage loop is based on the total allowable 3rd harmonic distortions [6]. For known maximum allowed third harmonic at voltage loop, the required attenuation of output ripple (2nd harmonic) through the voltage compensator is

$$G_{EA}(120Hz) = \frac{2(3^{rd})_{HAR}^{EA}}{V_o^{rip}} \quad \text{Eq. 3-17}$$

Since the voltage compensator gain at low frequencies is flat, the crossover frequency of voltage loop can be determined from

$$G_{EA}(120Hz) = G_{EA}(f_c) \quad \text{Eq. 3-18}$$

$$G_{EA}(120Hz) \cdot G_v(f_c) = 1 \quad \text{Eq. 3-19}$$

Thus, the bandwidth of the voltage loop is chosen to be 10~20Hz.

3.2 Digital Controller for PFC

3.2.1 Issues surrounding Digital Control

To implement digital control on a continuous system, we need an ADC, sample-and-hold circuits and a digital-to-analog converter (DAC) for digital and analog signal interface. Because the ADC and digital PWM quantize signals, the speed and resolution of ADC and PWM are critical in this application.

Different from analog control, in which the compensator is realized by operational amplifiers, the control law in digital control system is realized by binary calculation. As a result, delay is inevitable and depends on the speed of the digital controller. The presence of a signal of frequency higher than half of the sampling frequency can affect the controller by the aliasing effect. This can be relieved by low pass filter or by selecting a higher sampling frequency.

3.2.1.1 Resolution of ADC and PWM

When digital control is implemented, continuous signals are converted into discrete signals at the input of the controller while the controller output is converted back into a continuous signal that is the duty cycle or gate-drive signal for switch-mode power converters. ADC truncates input signal and DAC or PWM truncates the output signal to their least-significant-bit (LSB). The process is equal to quantization that introduces disturbance and noise into the control system producing undesired oscillation or distortion at output. The effect is illustrated in Figure 13.

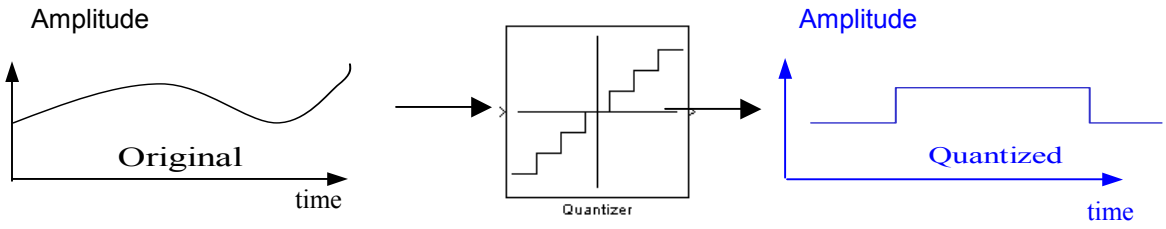


Figure 13 Quantization effect.

The difference between the quantized signal and the original signal can be modeled by an error introduced into the system. The equivalent of the quantizer is shown in Figure 14.

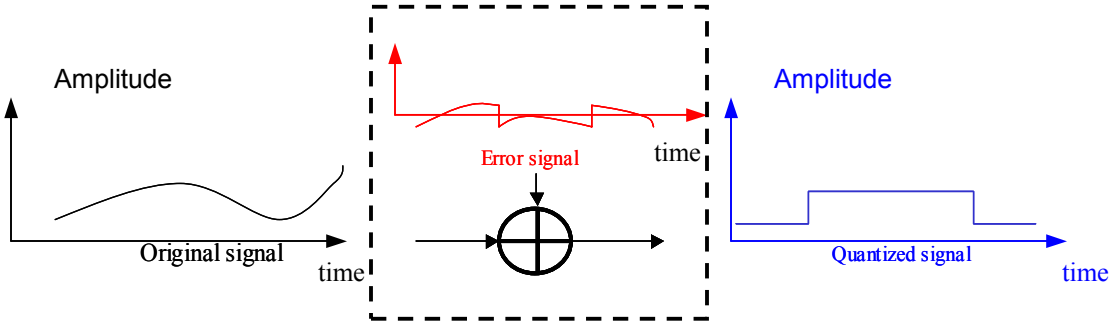


Figure 14 Equivalents for quantization effect

Although it is difficult to predict the frequency and shape of the error signal, which varies under different conditions, we can find out its maximum amplitude, as shown in Figure 15, where R equals one quantization step.

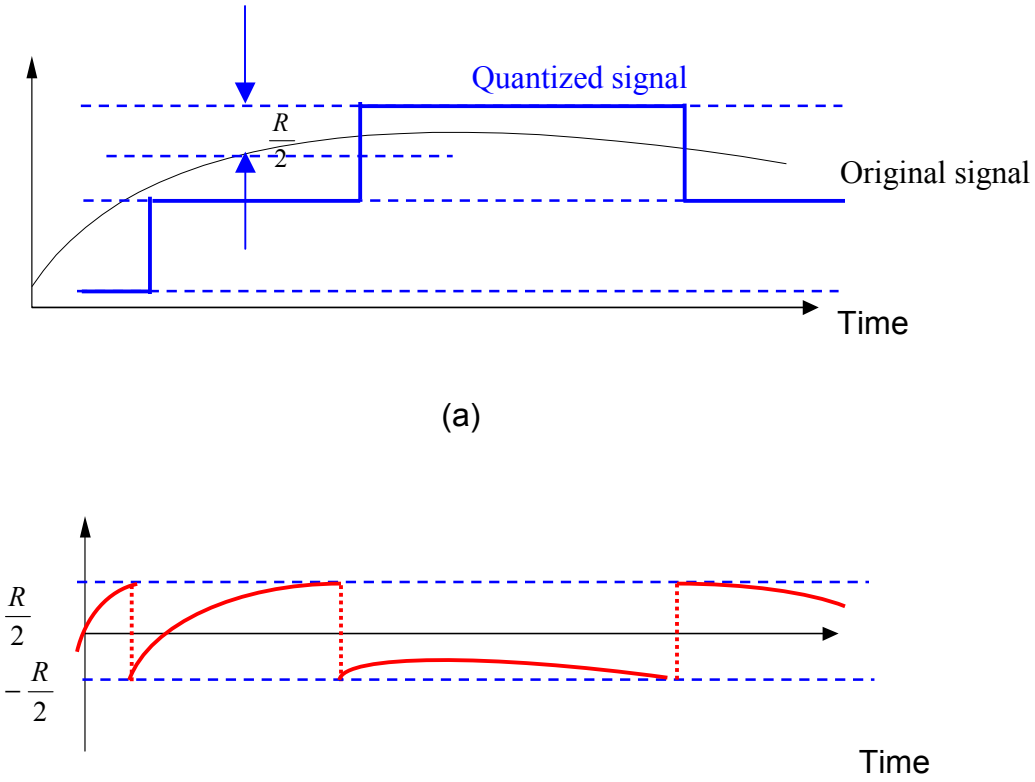


Figure 15 Noise and disturbance amplitude (a) Original signal and quantized signal, (b) Error signal introduced into system.

By substituting the quantizer with the error model, the digital control system for the current loop can be represented by Figure 16. As shown in Equation 3-20, because the harmonic produced by quantization should not exceed the maximum permissible harmonic standard, we need to determine the resolution requirement for ADC and PWM. One objective of this thesis is to quantify these ADC and PWM resolutions, as required to meet the harmonic standard.

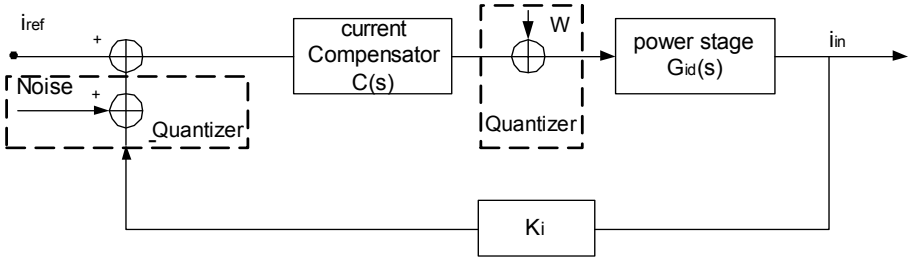


Figure 16 complete control systems for the PFC current loop

The inductor current is:

$$i_{in}(s) = i_{ref}(s)\frac{C(s)G_{id}(s)}{1+T_C(s)} + n_{ADC}(s)\frac{C(s)G_{id}(s)}{1+T_C(s)} + w_{PWM}(s)\frac{G_{id}(s)}{1+T_C(s)} \qquad \text{Eq. 3-20}$$

where: $i_{in}(s)$ is the Laplace transformation of inductor current,

$n_{ADC}(s)$ is the Laplace transformation of ADC quantization noise,

$w_{PWM}(s)$ is the Laplace transformation of PWM quantization error,

$C(s)$ is the current compensator transfer function,

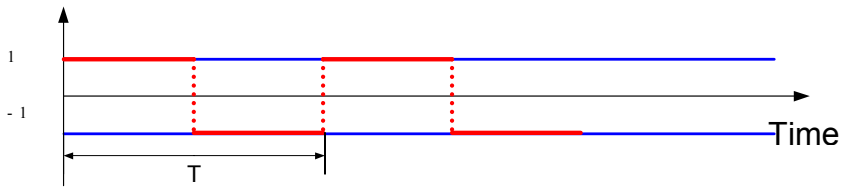
$G_{id}(s)$ is the duty-to-current transfer function,

$T_C(s) = K_i C(s) G_{id}(s)$ is the current open loop gain transfer function and

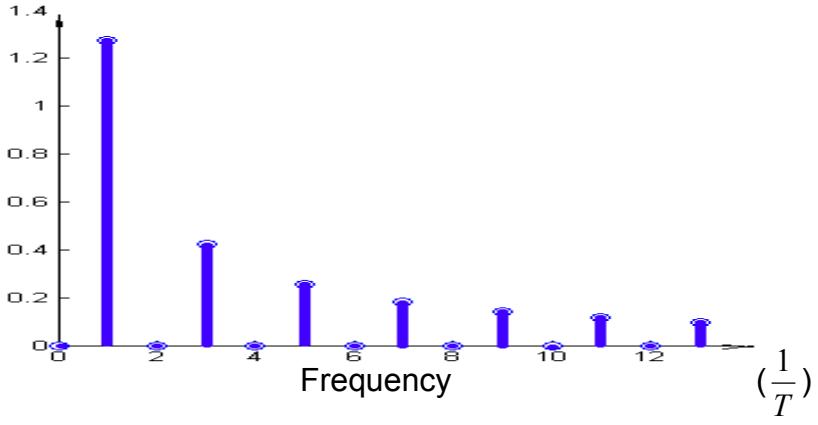
K_i is the current sensor gain.

In order to determine the level of introduced harmonics, the error signal is represented by a regular shape waveform. And the fundamental component of this regular shape waveform is used to calculate the resolution (see Appendix I). Two regular shapes are demonstrated here.

1. Square waveform



(a)



(b)

Figure 17 (a) square waveform and (b) harmonic components

For a square waveform of frequency f, the harmonic component values are as follows:

$$a_n = \begin{cases} \frac{4}{\pi n}, n = 2k+1 (k = 0,1,2\cdots) \\ 0, n = 2k (k = 0,1,2\cdots) \end{cases}, \qquad \text{Eq. 3-21}$$

where a_n is the amplitude of harmonic components and n is the harmonic order.

2. Saw tooth waveform

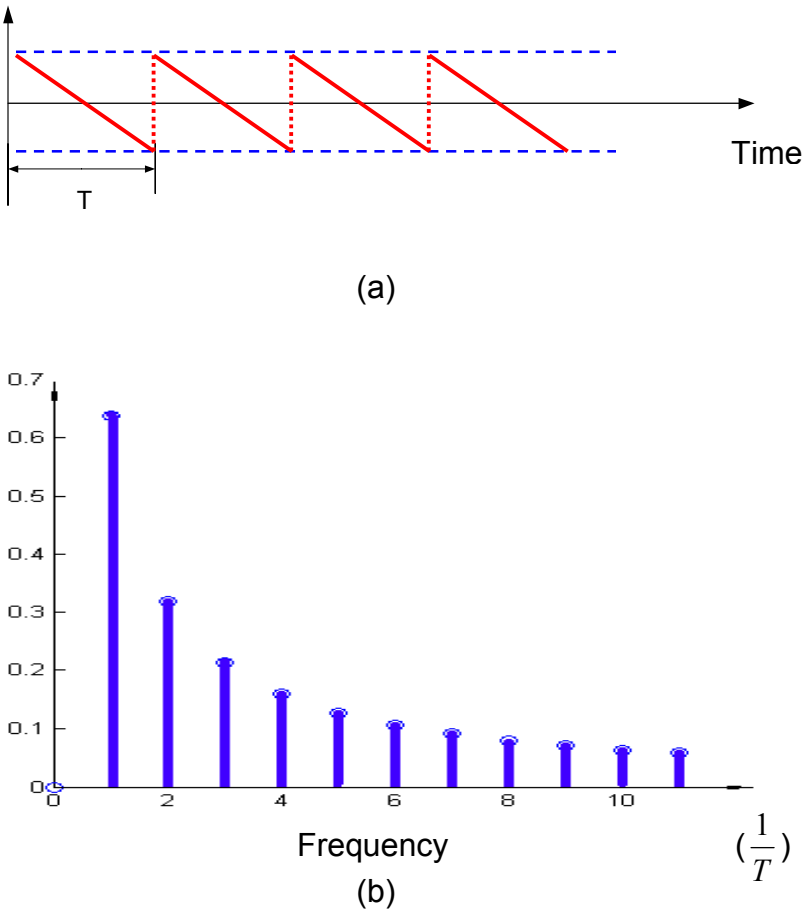


Figure 18 Saw tooth waveform and (b) harmonic components

For a saw tooth waveform of frequency f, the harmonic component values are as follows:

$$a_n = \frac{2}{\pi n}, (n = 1,2,3\cdots), \qquad \text{Eq. 3-22}$$

where a_n is the amplitude of harmonic components and n is the harmonic order

Square wave is admitted for the worst-case design (see Appendix I).

$$|n_{ADC}(j\omega)|_{\max} \approx \frac{Resolution}{2} \cdot \frac{4}{\pi} \qquad \text{Eq. 3-23}$$

$$|w_{PWM}(j\omega)|_{\max} \approx \frac{Resolution}{2} \cdot \frac{4}{\pi} \qquad \text{Eq. 3-24}$$

Based on this approximation and some specific conditions in a certain control system, adequate resolution can be calculated.

3.2.1.2 Digital Delay

The sample and hold of continuous signals and the non-zero computation time cause delay in a digital control system. Delay in a system usually causes phase lag that leads to reduction of the phase margin.

3.2.1.2.1 Sample-and-Hold delay

When a signal $e(t)$ is sampled and held at interval T_s, the output $e^*(t)$ is given by:

$$\begin{aligned} e^*(t) = {} & e(0)[u(t) - u(t - T_s)] + e(T)[u(t) - u(t - T_s)] \\ & + e(2T)[u(t) - u(t - T_s)] + \cdots \end{aligned} \qquad \text{Eq. 3-25}$$

Here $u(t)$ is the unit step function. The Laplace transformation of Equation 3-25 is:

$$E^*(s) = [\sum_{n=0}^{\infty} e(nT)e^{-nT_s}] \frac{1 - e^{-T_s s}}{s} \qquad \text{Eq. 3-26}$$

Note that the first part of Equation 3-26 is a function of the input signal and sampling period while the second factor is independent of the input. The effect of the sample-and-hold function [10] can be described as:

$$G_H(s) = \frac{1 - e^{T_s \cdot s}}{s}. \qquad \text{Eq. 3-27}$$

The frequency response is shown in Figure 19.

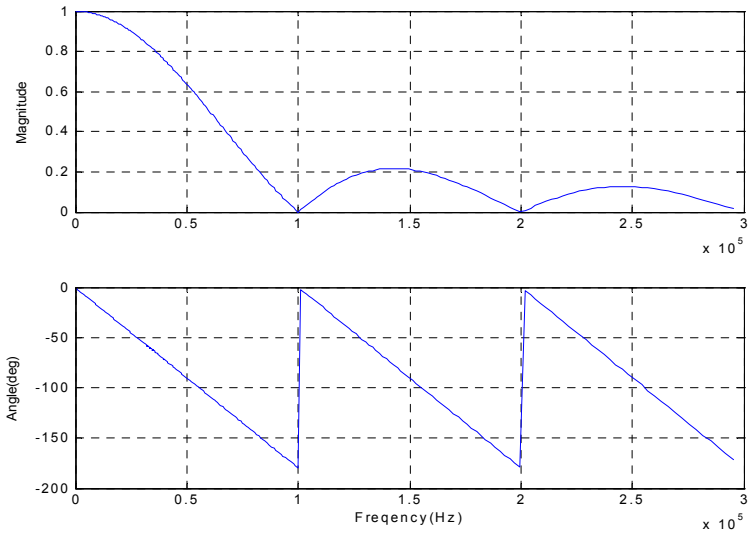


Figure 19 Frequency response of sample-and-hold function with 100KHz sampling frequency.

3.2.1.2.2 Computation Delay

The computation delay can be expressed as

$$D_{delay} = e^{s \cdot T_{delay}}. \qquad \text{Eq. 3-28}$$

Because in a PFC converter the fastest loop is the current loop, the digital delay affects the current loop most. Assuming the controller has one switching cycle or 10us delay for ADC, PWM and computation, there is 29^o phase shift reducing the phase margin by the same volume (shown in Figure 20). This delay has to be compensated to stabilize the system. It is predictable that compensating this delay will result in a poor current compensator performance. Its exact influence and compensation will be further discussed in chapter 3.

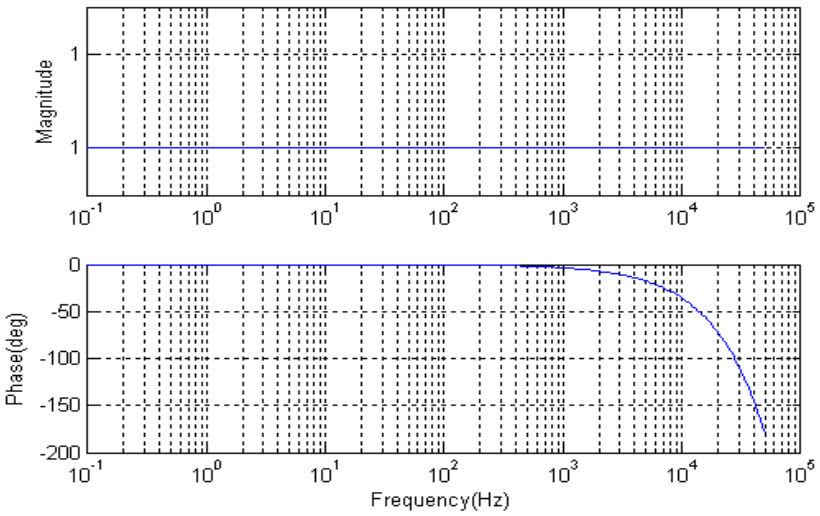


Figure 20 Effect of digital delay

3.2.1.3 Aliasing Effect

Aliasing is a phenomenon associated with any device or process where the data are divided into individual samples, i.e., a continuous signal is sampled at intervals as shown in Figure 21. Any frequency above half of the sampling frequency can cause aliasing.

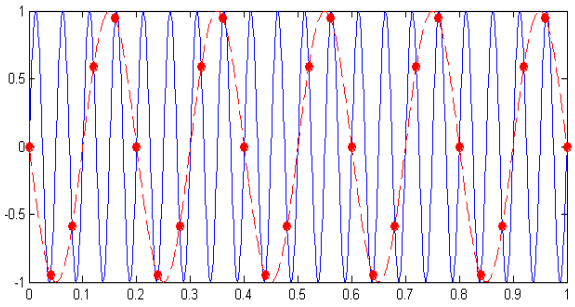


Figure 21 Sampling a 20Hz sinusoidal wave at 25 Hz sampling frequency

From a frequency domain standpoint, frequency component above half of f_s is wrapped around appearing as a lower frequency component, as shown in Figure 22.

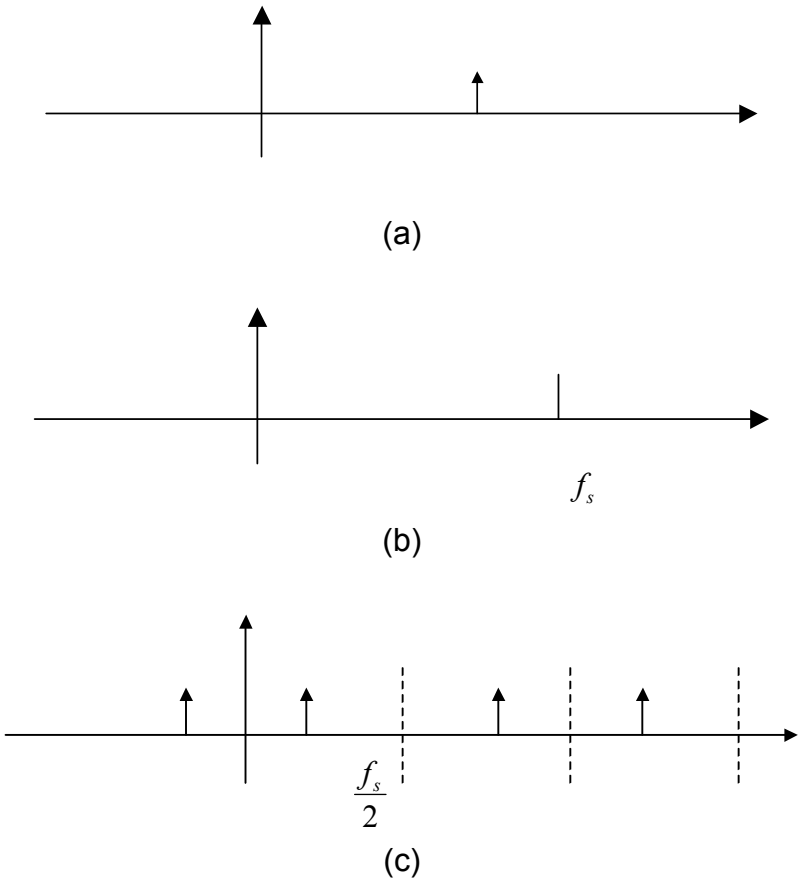


Figure 22 Illustration of the aliasing effect in frequency domain (a) Signal spectrum, (b) Sampling frequency and (c) Wrap around spectrum

The aliasing effect can cause confusion and serious error. When the sampling frequency is fixed, the system can use a low-pass filter to reduce the aliasing effect. If the signal processed has a wide bandwidth, the sampling frequency should be high enough. Switching noise and switching ripple is common phenomenon in all switching mode power supplies. Avoiding the aliasing effect is very important for reliability and performance.

3.2.2 Requirements

3.2.2.1 ADC Resolution

In PFC circuit, three signals are sampled: inductor current, input voltage and output voltage. Since the bandwidths of the signals are different, so are the

resolution requirements. It is also necessary to pay attention to the range of the sampled signal. For example, the inductor current has a large range because a universal-line PFC converter is to be applied to large input voltage range variation (90V~264V) and load ranges.

3.2.2.1.1 Inductor Current ADC Resolution

In PFC converter, the current tracks the input voltage, which has a semi-sinusoidal waveform. To guarantee a high power factor, the ADC resolution must be high enough to reduce the sensing noise (Figure 23).

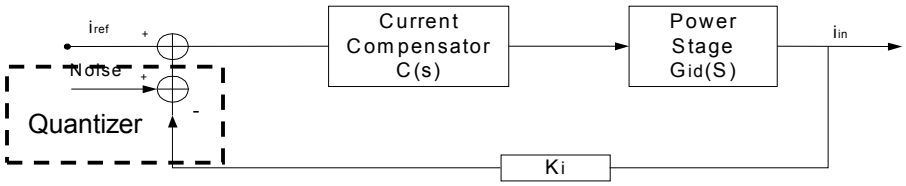


Figure 23 Noise introduced by ADC

From Figure 23, the relationship between noise and input current is derived:

$$i_{in} = n \left. \frac{CG_{id}}{1 + CG_{id}K_i} \right|_{i_{ref}=0} . \qquad \text{Eq. 3-29}$$

Though the amplitude and frequency of the noise introduced by ADC varies under different conditions, |n| has a maximum amplitude as Equation 3-23, and $\left| \frac{CG_{id}}{1 + CG_{id}K_i} \right| \approx \frac{1}{K_i}$ at low frequency range $f << f_c$. We have:

$$|n|_{\max} \cdot \left| \frac{CG_{id}}{1 + CG_{id}K_i} \right| \approx \frac{R}{2} \cdot \frac{4}{\pi} \cdot \frac{1}{K_i}, f << f_c . \qquad \text{Eq. 3-30}$$

Table 3 limits for Class A equipment in IEC61000-3-2

Harmonic order (n)	Maximum Permissible harmonics current (A)
Odd harmonics	
3	2.3
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
15<=n<40	0.15*15/n
Even harmonics	
2	1.08
4	0.43
6	0.30
8<=n<=40	0.23*8/n

Referring to the IEC 61000-3-2 Class A requirement (Table 3), the lowest limit of current harmonic RMS value is 0.046A (when n=40 in Table 3).

$$\frac{R}{2}\cdot\frac{4}{\pi}\cdot\frac{1}{K_i}\le 0.046\sqrt{2}$$

For example, if K_i=0.0725, the minimum ratio of noise to reference is 0.74%. This is equivalent to 8-bit resolution.

3.2.2.1.2 Input Voltage ADC Resolution

The input voltage is sampled for two purposes: giving the shape of the current reference and as input of the feed-forward low-pass filter.

Figure 24 shows the relation of ADC resolution and power factor of a rectified signal of a 60Hz sinusoidal waveform. Sampling frequency is 100KHz, which is well above the cross over frequency of current loop.

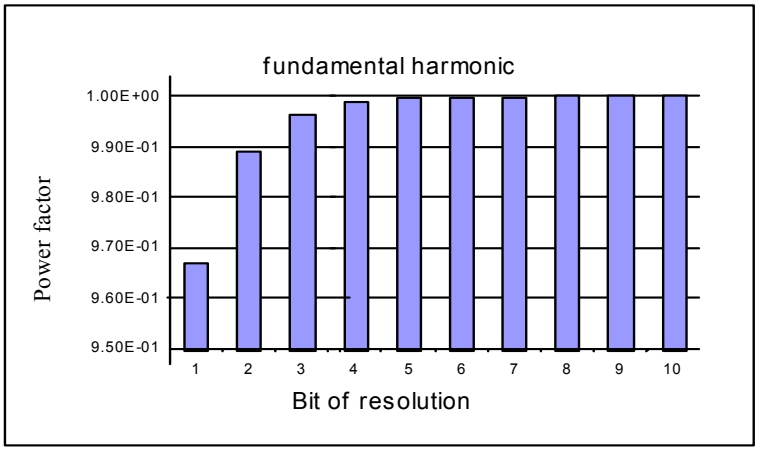


Figure 24 Fundamental harmonic and ADC resolution.

Figure 24 shows that five-bit resolution ADC is required to have a 99.9% PF reference. It is noticed that PFC has a large input voltage range (90V~264V) in which the high-line voltage is 3 times of the low-line voltage. If the five-bit resolution is required for 90V, the seven-bit resolution is needed for covering the whole range.

3.2.2.1.3 Output Voltage ADC Resolution

The output voltage is 400V DC. For 1% resolution, seven-bit ADC resolution is required.

3.2.2.2 Sampling Frequency

The sampling frequency for current loop is 100KHz, which is well above the current loop bandwidth (2~10KHz). The sampling frequency is the same as the switching frequency. It is costly to have high frequency ADC. The best way to avoid the aliasing effect is to insert low-pass filter before the ADC, which can filter out the switching noise.

For the feed-forward low-pass filter, although the bandwidth is very low, the existence of high order harmonic can still cause the aliasing effect. Furthermore, the input voltage waveform serves as the current reference waveform; high-order harmonics should be preserved [6]. Therefore, the input voltage sampling frequency should be high enough to avoid these high order harmonic components being wrapped into low frequencies.

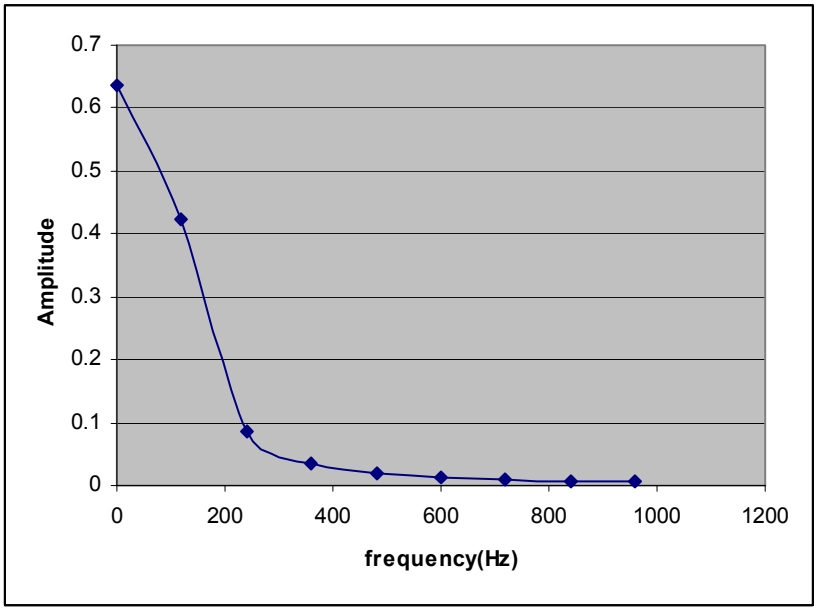


Figure 25 harmonic ratios for semi sinusoidal wave

Figure 25 shows that to keep these harmonics within half of the sampling frequency, the input voltage sampling frequency should be larger than 2KHz. A 5kHz sampling frequency is adopted.

3.2.2.3 Pulse Width Modulation Resolution

Digital PWM resolution is closely related to the system clock. For a digital PWM whose operation is based on the system clock, the resolution is $R = \frac{f_{switch}}{f_{clock}}$. For a given switching frequency, the higher the resolution, the higher the system clock, which means the higher the cost.

The current-loop diagram with the equivalent quantizer is shown in Figure 26. Although digital controller is different from analog control, the frequency response of digital and analog controllers are similar in the frequency range specified in IEC61000-3-2, which is far below the current loop crossover frequency. For convenience analog compensator is used to represent the digital compensator and related delays.

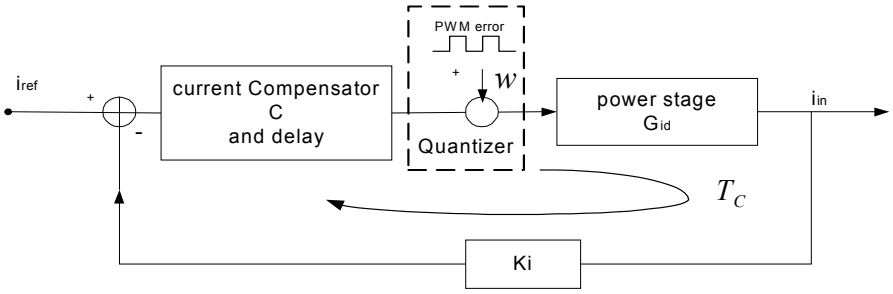


Figure 26 Illustration of disturbance introduced by digital PWM

From Figure 26, following relationship between PWM error w and input current is found:

$$i_{in} = w\frac{G_{id}}{1+T_C}\bigg|_{i_{ref}=0}, \qquad \text{Eq. 3-31}$$

where T_C is the current open loop gain.

A method similar to that described in section *3.2.2.1.1* is used to determine PWM resolution:

$$|\, w\frac{G_{id}}{1+T_C}| \leq 0.046\cdot\sqrt{2}\ . \qquad \text{Eq. 3-32}$$

For $f << f_c$, the current open loop gain $|T_C|$ is large enough that the magnitude can be approximated as follows:

$$\left|\frac{G_{id}}{1+T_C}\right| = \left|\frac{G_{id}}{1+CG_{id}K_i}\right| \approx \left|\frac{1}{CK_i}\right|. \qquad \text{Eq. 3-33}$$

Since the zero is not effective at this frequency range, the behavior of the current compensator is a simple integral, and the effect of digital delay can be ignored.

$C(s) = \dfrac{\omega_i(1+\dfrac{s}{\omega_z})}{s(1+\dfrac{s}{\omega_p})} \approx \dfrac{\omega_i}{s}$. Thus:

$$\left|\frac{G_{id}}{1+T_C}\right| \approx \left|\frac{1}{CK_i}\right| = \left|\frac{s}{\omega_i K_i}\right| \propto f. \qquad \text{Eq. 3-34}$$

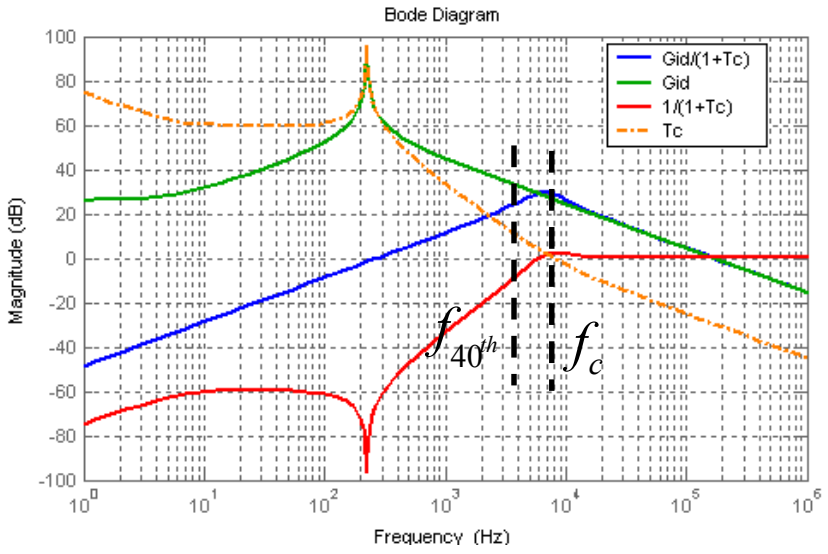


Figure 27 Bode plot for $\dfrac{G_{id}}{1+CG_{id}K_i}$

As shown in Figure 27, $\left|\dfrac{G_{id}}{1+T_C}\right|_{\max}$ in the range $f_{1^{st}} \le f \le f_{40^{th}}$ occurs at the fortieth harmonic frequency. Hence:

$$|w|_{\max} \cdot \left| \frac{G_{id}}{1+CG_{id}K_i} \right|_{\max} \approx \left| \frac{R}{2} \cdot \frac{4}{\pi} \right| \cdot \left| \frac{2\pi f_{40th}}{\omega_i K_i} \right| \leq 0.046\sqrt{2} \qquad \text{Eq. 3-35}$$

For the case L=380uH, Vout = 400V and crossover frequency $f_c = 8kHz$, we have $R \geq 0.0108$, which is equivalent to seven-bit resolution. Because digital current compensator has a smaller ω_i with the same phase margin and cross over frequency. We choose eight-bit DPWM resolution.

When the DPWM clock is the DSP system clock, the clock must meet this requirement:

$$\frac{f_{clock}}{f_{switch}} \geq 2^8 \qquad \text{Eq. 3-36}$$

For a 100KHz switching frequency, eight-bit PWM resolution requires the system clock to be 26MHz.

3.2.3 Designing the Digital Controller for PFC

The requirement on the resolution of ADC, PWM and system clock is summarized in Table 4.

Table 4 Summary on digital controller firmware requirement

System clock (MHz)	26
ADC channels (n)	3
ADC resolution (Bit)	8
PWM resolution (Bit)	8

According to the requirements listed above, general purpose DSP ADMC401 from Analog Device is chosen for the implementation.

The main specifications of ADMC401 are listed in Table 5.

Table 5 Specification of DSP ADMC401 [40]

System clock (MHz)	26
ADC Channels (n)	8
ADC Resolution (Bit)	12
PWM Resolution (Bit)	8
On-Chip Data ROM and RAM (Word)	1K
On-Chip Program ROM and RAM (Word)	4K

Figure 28 shows the control structure of the digital controller for a single-switch PFC converter.

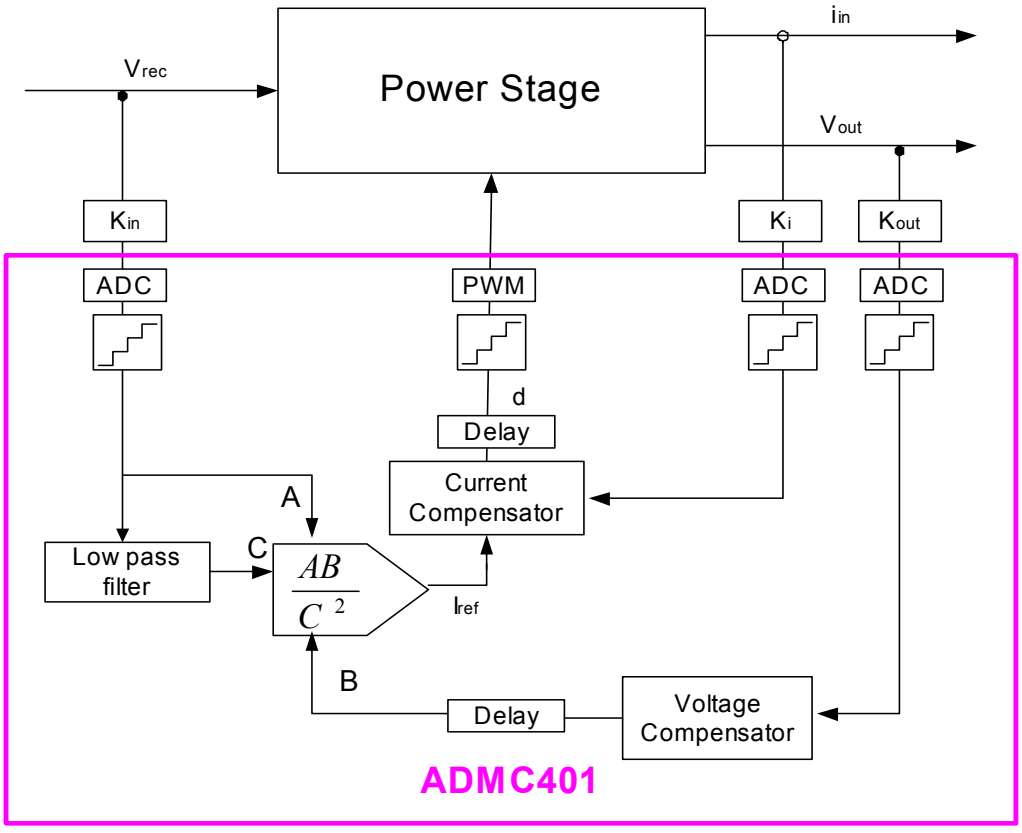


Figure 28 Digital control structure of single-switch PFC

3.2.3.1 Power Stage Parameters

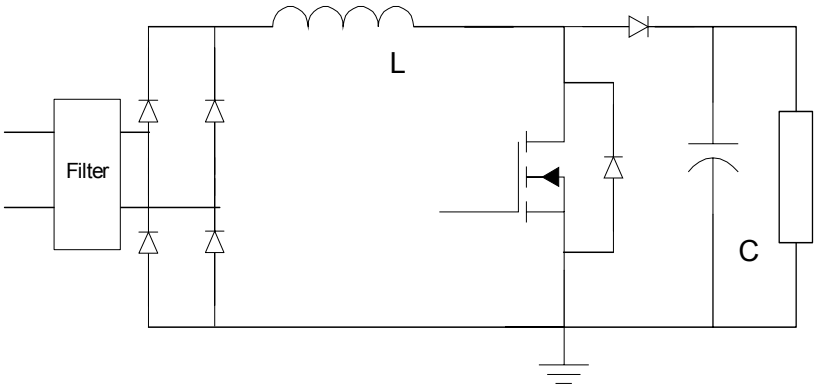


Figure 29 Power stage of Boost PFC

3.2.3.1.1 Parameters

1. Boost inductance: 380μH
2. Output capacitor: 330μF

3.2.3.1.2 Specifications

1. Input voltage: 90 ~ 265V_{ac} single phase
2. Output voltage: 400V
3. Output power: 1,000W between 150 ~ 265V; 600W between 90 ~ 150V
4. Switching frequency: 100KHz
5. THD: ≤1.5%

3.2.3.1.3 Interface Coefficient

The ADC of the ADMC401 has input range of (-2~2V). The interface gains should keep the signals from overflowing at input of the ADC under normal operation conditions. The result of ADC is Q-15 formatted (shown in Figure 30). In the Q-15 format, there is one sign bit (the most significant bit). Specifically, the maximum value, 0111,1111,1111,1111 (binary) is normalized as +1, which implies the ADC has a gain of 0.5.

Below are examples of Q-15 numbers and their decimal equivalents.

Q-15 Number (HEX)	Decimal Equivalent
0x0001	0.000031
0x7FFF	0.999969
0xFFFF	-0.000031
0x8000	-1.000000

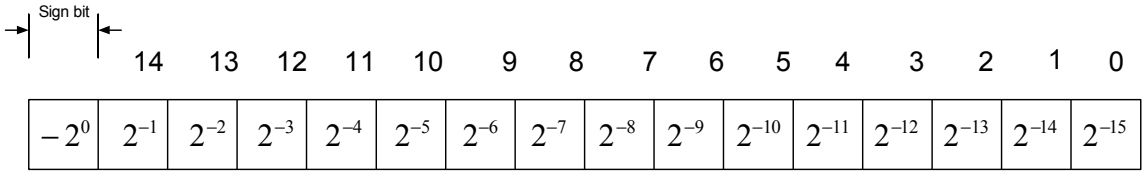


Figure 30 Bit weighting for Q-15 Format [40].

With voltage dividers and sensing resistor, the following parameters exist.

Input voltage gain: $K_{in} = g_{divider1} \cdot g_{ADC} = 0.2426 \cdot 10^{-2}$

Current gain: $K_i = g_{interface} \cdot g_{ADC} = 0.0725$

Output voltage gain: $K_{out} = g_{divider2} \cdot g_{ADC} = 0.2 \cdot 10^{-2}$

3.2.3.2 Direct Design in the Z-Domain

The simplest method to implement digital control is to convert an analog compensator into a digital controller. There are many conversion methods, such as “backward integral,” “Tustin” and “zero and pole matching [10].” However, it is difficult to model sample and hold, $G_H(s)$ and computation delay $e^{-Tdelay}$ in s-domain. Designing an analog compensator may not be accurate. Even with an

accurate analog controller, converting it into a discrete form may compromise its performance.

Alternatively, we design the digital controller directly in z-domain employing the relation of z variable and s variable:

$$z = e^{sT_s}, \qquad \text{Eq. 3-37}$$

where T_s is the sampling cycle.

The frequency response of a digital system $G(z) = k\frac{(z-\xi_1)\cdots(z-\xi_m)}{(z-\rho_1)\cdots(z-\rho_n)}$ can be represented by $G(e^{j\omega T_s}) = k\frac{(e^{j\omega T_s}-\xi_1)\cdots(e^{j\omega T_s}-\xi_m)}{(e^{j\omega T_s}-\rho_1)\cdots(e^{j\omega T_s}-\rho_n)}$.

The magnitude response is

$$\left|G(e^{j\omega T_s})\right| = k\frac{\prod_{i=1}^{m}\left|e^{j\omega T_s}-\xi_i\right|}{\prod_{j=1}^{n}\left|e^{j\omega T_s}-\rho_j\right|}. \qquad \text{Eq. 3-38}$$

The phase response is

$$\angle G(e^{j\omega T_s}) = \sum_{i=1}^{m}\angle(e^{j\omega T_s}-\xi_i) - \sum_{j=1}^{n}\angle(e^{j\omega T_s}-\rho_j). \qquad \text{Eq. 3-39}$$

These responses are directly related to the position of zeros and poles on the z-plain as shown in Figure 31. Particularly, the computation delay $e^{-T_{delay}s}$ can be mapped into the origin as $z^{-\frac{T_{delay}}{T_s}}$.

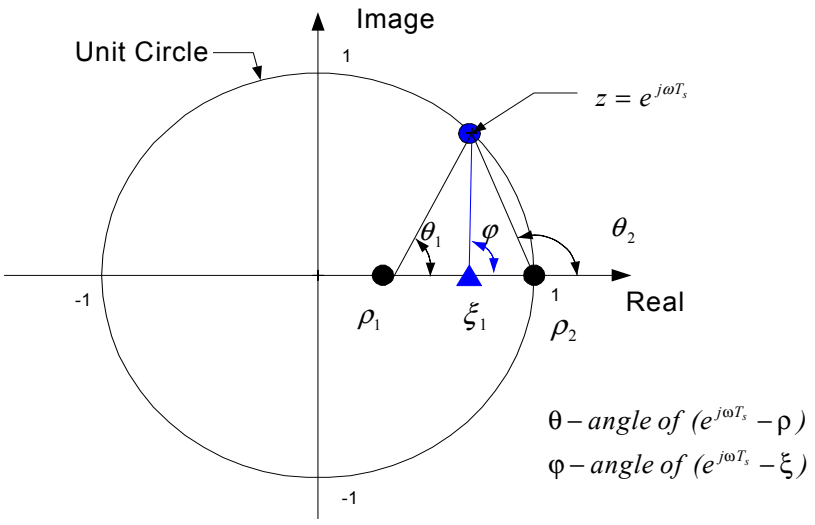


Figure 31 Poles and zeros in the z-plane.

In this approach the compensator is designed by placing the poles and zeros in z-plane to stablize the converter and achieve the power factor correction. Before the compensator is designed, proper model of power stage must be obtained.

3.2.3.3 Discrete Time Model of Power Stage with Sample-and-Hold

As discussed in section 3.2.1.2, sample-and-hold function in digital control actually modifies magnitude and phase response [10]. This effect must be included in the power stage model.

If $e(t)$ is the impulse response of system G, the Laplace transformation of a sampled signal, $e^*(t)$, is as follows:

$$E^*(s) = \sum_{n=0}^{\infty} e(nT)e^{-nT_s} = \sum_{poles}[residue\ of\ E(\lambda)\frac{1}{1-e^{-T_s(s-\lambda)}}], \qquad \text{Eq. 3-40}$$

where: $E^*(s)$ is the Laplace transformation of $e^*(t)$.

Combined with the sample-and-hold function [10], we can have:

$$E^*(s) = [\sum_{n=0}^{\infty} e(nT)e^{-nT_s}]\frac{1-e^{-T_s s}}{s}$$
$$= \sum_{poles}[residue\ of\ E(\lambda)\frac{1}{1-e^{-T_s(s-\lambda)}} \cdot \frac{(1-e^{-T_s\lambda})}{\lambda}] \quad \text{Eq. 3-41}$$

Utilizing Equation 3.37, $E^*(s) = E^*(\frac{\ln z}{T_s})$ [10].

The power stage can be digitized using the zero-order-hold method with sampling frequency of 100KHz, as shown in Figure 32.

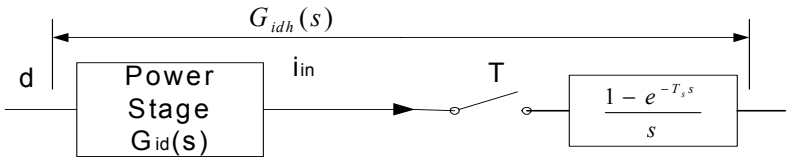


Figure 32 Power stage with sample and hold

From Figure 32, discrete duty to current transfer function is derived:

$$G_{idz}(z) = \frac{V_{out}}{L} \cdot \frac{T_s}{(z-1)}, \quad \text{Eq. 3-42}$$

where $T_s = 10^{-5}$ second.

Figure 33 shows the discrete transfer function in the z-plane.

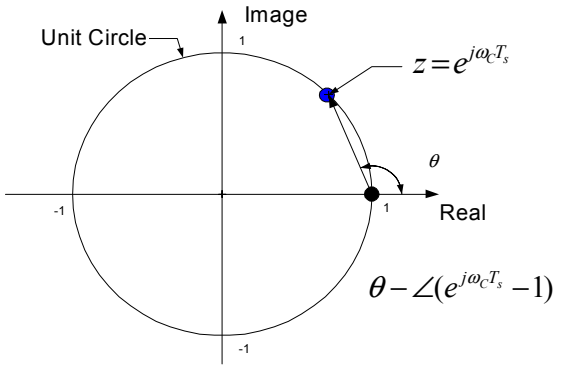


Figure 33 Duty to current transfer function mapped into z-plane

Figure 34 shows that below half of the sampling frequency, the discrete model gives nearly the same frequency response with the continuous model with sample-and-hold.

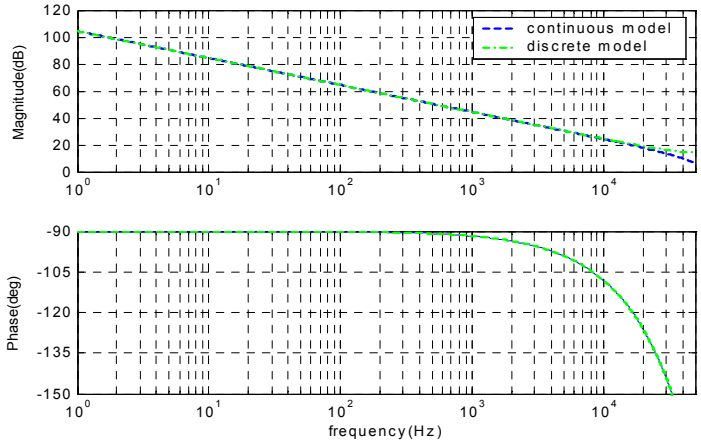


Figure 34 Comparison of the discrete model and continuous model

The same method is used to derive discrete control to output transfer function:

$$G_{vz}(z) = \frac{g_c}{C} \cdot \frac{T_s}{(z-1)}, \qquad \text{Eq. 3-43}$$

where $T_s = 2 \cdot 10^{-4}$ second.

3.2.3.4 Current Loop Compensator

As mentioned before analog low-pass filters with cutoff frequency equal to half of the switching frequency are inserted in the current and voltage feedback loops in order to reduce the aliasing effect. As a result, only the frequency range below half of the switching frequency is of concern in digital controller design and the transfer function of the low pass filter is ignored.

When we are designing the current compensator, the influence of slow voltage loop can be ignored. The current loop with digital compensator is illustrated in Figure 35.

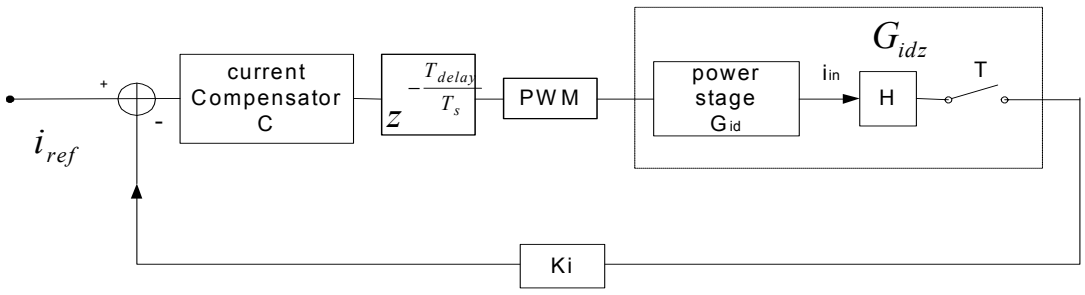


Figure 35 Current loop with digital compensator

The design target is similar to that of the analog compensator. For robustness, the phase margin is set to 45°. For a faithful tracking of the semi sinusoidal waveform, the bandwidth is 8KHz.

To compensate the digital delay, there are two approaches: the one-zero approach, in which the zero is moved toward the origin, and the two-zero approach, in which a second zero is added.

3.2.3.4.1 One-Zero Approach

The current compensator is $C(z) = K_P \frac{(z-\xi)}{z-1}$. The current loop gain is:

$$\begin{aligned} T_C(z) &= G_{idz}(z) \cdot C(z) \cdot Ki \cdot z^{-\frac{T_{delay}}{T_s}} \\ &= \frac{V_{out} \cdot T_s}{L(z-1)} \cdot \frac{K_P(z-\xi)}{z-1} \cdot K_i \cdot z^{-\frac{T_{delay}}{T_s}} \cdot \end{aligned} \qquad \text{Eq. 3-44}$$

The two design targets, crossover frequency and phase margin are used to determine two unknown variables, gain K_P and zero ξ, as follows:

$$\begin{cases} \left|T_C(e^{j\omega_c T_s})\right| = 1 \\ \angle T_C(e^{j\omega_c T_s}) = -180^0 + 45^0 \end{cases} \qquad \text{Eq. 3-45}$$

From Equation 3-45, we have derived:

$$\begin{cases} \dfrac{V_{out}\cdot T_s}{L\,|\,e^{j\omega_c T_s}-1\,|}\cdot\dfrac{K_P\,|\,e^{j\omega_c T_s}-\xi\,|}{|\,e^{j\omega_c T_s}-1\,|}\cdot K_i = 1 \\ \angle(e^{j\omega_c T_s}-\xi)-\angle(e^{j\omega_c T_s}-1)-\angle(e^{j\omega_c T_s}-1)-\omega_C T_{delay}\cdot\dfrac{180^o}{\pi} = -180^0+45^0 \end{cases} \quad \text{Eq. 3-46}$$

where $\omega_C = 2\pi f_C = 2\pi\cdot 8krad/\sec, V_{out} = 400V, L = 380\mu H, K_i = 0.0725, T_{delay} = 10\mu s$ and $T_s = 10\mu s$.

By solving Equation 3-46, the value of gain K_P and zero ξ are determined as follows:

$$\begin{cases} K_P = 0.6567 \\ \xi = 0.984 \end{cases}.$$

Hence, the compensator transfer function is $C(z) = 0.6567\dfrac{(z-0.984)}{z(z-1)}$ and its Bode plot is shown in Figure 36.

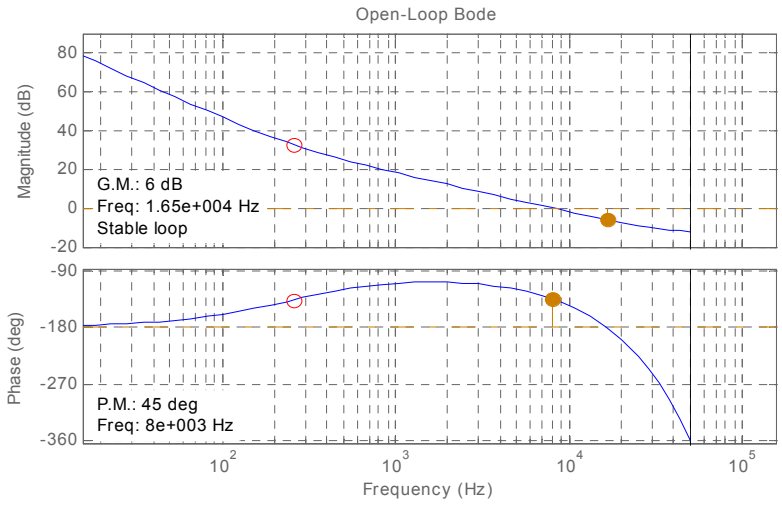


Figure 36 Bode plot for current open loop gain with one zero compensation

Compared with the analog current compensator, this digital compensator results in a much smaller current loop gain. Simulation results show a large zero-cross distortion and great displacement angle as well.

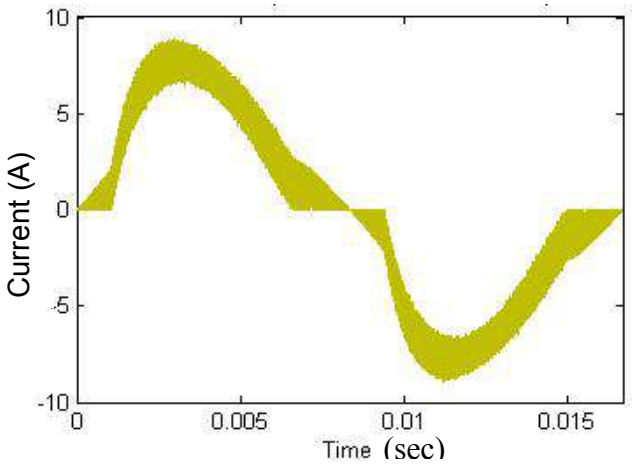


Figure 37 Input current waveform with one-zero digital current compensator.

3.2.3.4.2 Two-Zero Design

In this approach, the compensator transfer function is $C(z) = K_P \frac{(z-\xi)^2}{z(z-1)}$.

$$\begin{cases} \frac{V_{out} \cdot T_s}{L|e^{j\omega_c T_s} - 1|} \cdot \frac{K_P |e^{j\omega_c T_s} - \xi|^2}{|e^{j\omega_c T_s} - 1|} \cdot K_i = 1 \\ 2 \cdot \angle(e^{j\omega_c T_s} - \xi) - \angle(e^{j\omega_c T_s} - 1) - \angle(e^{j\omega_c T_s} - 1) - \omega_C T_{delay} \cdot \frac{180^o}{\pi} - \omega_c T_s \cdot \frac{180^o}{\pi} = -180^0 + 45^0 \end{cases} \quad \text{Eq. 3-47}$$

where $\omega_C = 2\pi f_C = 2\pi \cdot 8krad/\sec, V_{out} = 400V, L = 380\mu H, K_i = 0.0725, T_{delay} = 10\mu s$ and $T_s = 10\mu s$.

By solving Equation 3-47, the value of gain K_P and zero ξ are obtained:

$$\begin{cases} K_P = 1.162 \\ \xi = 0.6588 \end{cases}$$

The compensator transfer function is $C(z) = 1.162\frac{(z-0.6588)^2}{z(z-1)}$ and its Bode plot is shown in Figure 37.

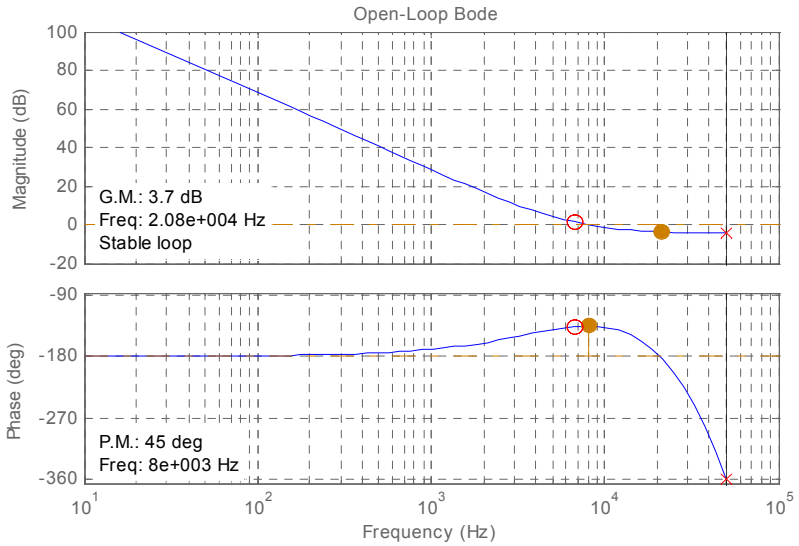


Figure 38 Current Open loop Bode plot with two zeros compensation

The two zero method can obtain a higher current open loop gain. But it also lowers the gain margin. The digital delay, which is inevitable, has limited the current loop bandwidth. Otherwise we must make trade-off between bandwidth and stability. As we know, current loop bandwidth is directly related to PF. In the first step, a digital control is implemented with the two-zero compensator. Later, a solution is proposed to improve the power factor with a low current loop bandwidth.

3.2.3.4.3 Realization:

The simplest way to realize a digital compensator is to convert it directly into differential equation:

$$y(k) = y(k-1) + 1.162e(k) - 1.5311e(k-1) + 0.5043e(k-2)\,. \qquad \text{Eq. 3-48}$$

But on some occasions these coefficients are too sensitive [10] and implementation requires more memories. The better method is to use state equations:

$$\begin{aligned} x(k) &= A \cdot x(k-1) + B \cdot e(k) \\ y(k) &= C \cdot x(k) + D \cdot e(k) \end{aligned} \qquad \text{Eq. 3-49}$$

From $C(z) = 1.162\dfrac{(z-0.6588)^2}{z(z-1)}$ the state equations are derived as follows:

$$\begin{bmatrix} x_1(k) \\ x_2(k) \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ -0.6588 & 1 \end{bmatrix} \cdot \begin{bmatrix} x_1(k-1) \\ x_2(k-1) \end{bmatrix} + \begin{bmatrix} 1.162 \\ 1.162 \end{bmatrix} e(k) + \begin{bmatrix} -0.6588 \\ -0.6588 \end{bmatrix} e(k-1) \qquad \text{Eq. 3-50}$$
$$\text{and } d(k) = x_2(k)$$

The state equation method needs to store only one coefficient and three variables ($x_1(k-1), x_2(k-1), e(k-1)$) while the direct approach needs to store three coefficients (the value of 1 doesn't have to be stored) and three variables ($y(k-1), e(k-1), e(k-2)$).

3.2.3.5 Feed-forward loop-low pass filter

The feed-forward loop is shown in Figure 39. A second-order low-pass filter is used to filter out the average value of the input voltage. Assuming that the input signal is an ideal semi-sinusoidal with unity amplitude, the DC component of input signal a_0 is $\dfrac{2}{\pi}$ and the second harmonic component amplitude a_2 is $\dfrac{4}{3\pi}$. The ratio of 2nd harmonic component to the DC component is $2/3$.

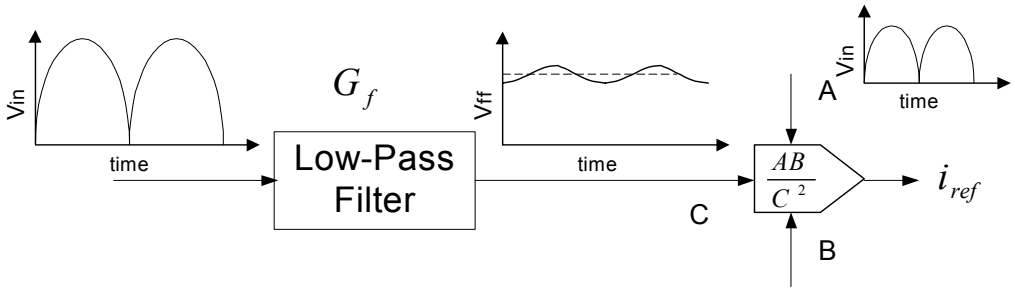


Figure 39 Feed forward loop.

The simplified Bode plot of the low pass filter is shown in Figure 40.

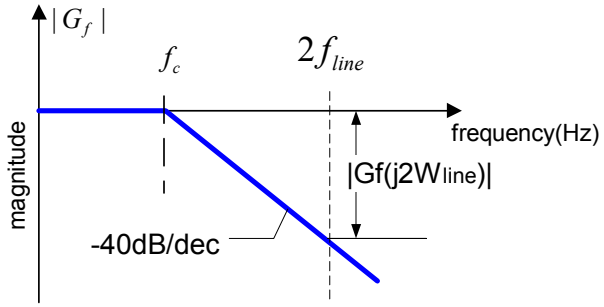


Figure 40 Bode plot of the low-pass filter

From Figure 40, the cut-off frequency, f_c is derived:

$$f_c = 2f_{line} \cdot 10^{\frac{|G_f(j2\omega_{line})|(dB)}{40}} \quad . \qquad \text{Eq. 3-51}$$

To meet the C distortion requirement, Equation 3-52 must be satisfied:

$$\left|\frac{a_2}{a_0}\right| \cdot \left|G_f(j2\omega_{line})\right| \le \left|\frac{\Delta C}{C}\right|_{\max} \quad . \qquad \text{Eq. 3-52}$$

For the requirement given in section *3.1.2.2,* $\left|\frac{\Delta C}{C}\right| \le 0.5\%$, so:

$$\left|G_f(j2\omega_{line})\right| \le \left|\frac{\Delta C}{C}\right|_{\max} \cdot \left|\frac{a_0}{a_2}\right| = 0.0075 = -42.5dB\,. \qquad \text{Eq. 3-53}$$

The corresponding cut-off frequency is:

$$f_c = 2f_{line} \cdot 10^{\frac{\left|G_f(j2\omega_{line})\right|(dB)}{40}} \le 2f_{line} \cdot 10^{\frac{-42.5}{40}} = 2f_{line} \cdot 0.0866\,, \qquad \text{Eq. 3-54}$$

for the case $f_{line} = 50Hz$, $f_c \le 8.6Hz$.

Butterworth or Chebyshev filters are widely used to realize digital filter. For example, the discrete state equation of a second-order Butterworth filter can be expressed as:

$$\begin{aligned} x(k) &= A \cdot x(k-1) + B \cdot e(k) \text{ and} \\ y(k) &= C \cdot x(k) + D \cdot e(k) \end{aligned} \qquad \text{Eq. 3-55}$$

The coefficients are as follows:

$$A = \begin{bmatrix} 0.98477 & -0.01072 \\ 0.01072 & 0.99994 \end{bmatrix}, \qquad B = \begin{bmatrix} 0.015167 \\ 8.2 \cdot 10^{-5} \end{bmatrix}, \qquad C = [0.003792, 0.707086] \qquad \text{and}$$

$D = 2.8977 \cdot 10^{-5}$.

However, this implementation has some disadvantages. First, some of the coefficients are too small and sensitive, which may cause problems when the Q-15 format truncates a number between (-1,1) to its LSB, i.e. the number has a resolution of $1/2^{15}$ or $3.05 \cdot 10^{-5}$. Second, these coefficients cost much memory resource. Therefore another method is used to implement the low-pass filter.

In this method, an analog second-order low-pass filter is designed first, such that:

$$G_{fs}(s) = \frac{{\omega_o}^2}{s^2 + 2 \cdot \sqrt{2} \cdot \omega_o \cdot s + {\omega_o}^2}\,, \qquad \text{Eq. 3-56}$$

where $\omega_o = 2\pi f_c$ is the cut-off frequency.

The two poles $p_{1,2} = \sqrt{2}\omega_o(-1 \pm j)$ are mapped into the z–plane with the relation $z = e^{sT_s}$, which gives two discrete poles $z_{p_{1,2}} = e^{\sqrt{2}\omega_o(-1\pm j)T_s} = 0.9924 \pm j0.0076$. Then the discrete state equations are derived:

$$\begin{aligned} x(k) &= A \cdot x(k-1) + B \cdot e(k) \ \ and \\ y(k) &= C \cdot x(k) + D \cdot e(k) \end{aligned},$$

where $A = \begin{bmatrix} 0.9924 & -0.0076 \\ 0.0076 & 0.9924 \end{bmatrix}, B = \begin{bmatrix} 0.0152 \\ 0 \end{bmatrix}, C = [0,1], D = 0$.

The low-pass filter described above has a DC gain of 1. But for a semi-sinusoidal waveform, the ratio of RMS value to average value is 1.1. The matrix B should be replaced by $\begin{bmatrix} 0.0152 \\ 0 \end{bmatrix} \cdot 1.1 = \begin{bmatrix} 0.0167 \\ 0 \end{bmatrix}$.

Finally, the filter has a DC gain of 0.818dB and a gain of -41.8dB at 100Hz. Attenuation at 100Hz is -42.6dB. The Bode plot is shown in Figure 41.

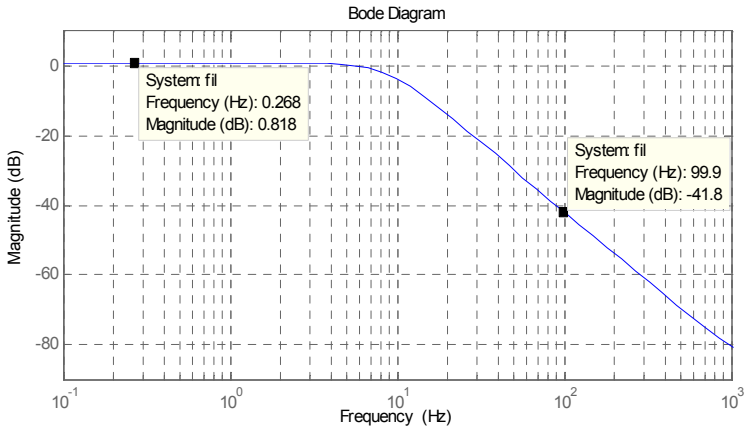


Figure 41 Bode plot for low-pass filter.

The feed forward gain K_{ff} is determined by input voltage gain and the low-pass filter gain: $K_{ff} = K_{in} \approx 0.2624 \cdot 10^{-2}$.

3.2.3.6 Voltage loop Compensator

The voltage loop is shown in Figure 42. The discrete transfer function of the voltage compensator can be expressed as $G_{EAZ}(z) = \frac{K_p}{z - \rho}$.

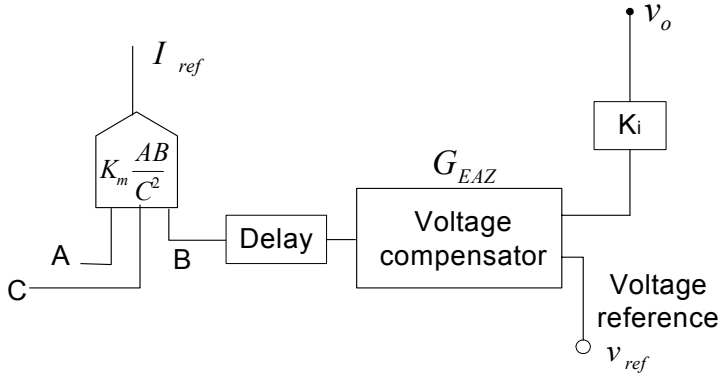


Figure 42 Outer voltage loop

The following equations are derived:

$$i_{in} = \frac{1}{K_i}(K_{in} \cdot v_{in}) \cdot v_c \cdot K_m \cdot \frac{1}{(k_{ff} \cdot v_{in\_rms})^2} \quad , \qquad \text{Eq. 3-57}$$

$$k = \frac{i_{in}}{v_{in} v_c} = \frac{1}{K_i} K_{in} \cdot K_m \cdot \frac{1}{(k_{ff} \cdot v_{in\_rms})^2} \text{ and} \qquad \text{Eq. 3-58}$$

$$g_c = k \frac{V_{in\_rms}^2}{V_{out}} = \frac{K_{in} K_m}{K_i V_{out} K_{ff}^2}, \qquad \text{Eq. 3-59}$$

where $K_i = 0.0725$, (current feed back gain), $K_m = 0.25$ (multiplier gain), $K_{in} = 0.002624$ (input voltage gain) and $K_{ff} = 0.002624$ (feed-forward gain).

From the given parameters, we can calculate that $g_c = 2.93$. Hence the discrete control-to-voltage transfer function is:

$$G_{vz} = \frac{g_c}{C} \cdot \frac{T_s}{z-1} = \frac{0.1776}{z-1}. \qquad \text{Eq. 3-60}$$

For the requirement given in section *3.1.2.2,* $\left|\frac{\Delta B}{B}\right| \le 0.5\%$, the B distortion requirement is obtained:

$$|\Delta B| \le 0.5\%|B|_{\max} = 0.5\%\frac{I_{o\max}}{g_c} = 0.00427 \qquad \text{Eq. 3-61}$$

Furthermore:

$$\Delta B = V_0^{ripp} \cdot K_{out} \cdot |G_{EA}(j2\omega_{line})|, \qquad \text{Eq. 3-62}$$

where $V_o^{rip} = \frac{V_{in} I_{in}}{2V_{out}\omega_L C_o}$ (Equation 3-16) and $K_{out} = 0.2 \cdot 10^{-2}$ (output voltage sensing gain).

To satisfy Equation 3-61, the voltage compensator gain at $2f_{line}$ should have $|G_{EA}(j2\omega_{line})| \le \frac{\Delta B_{\max}}{V_0^{ripp} \cdot K_{out}}$.

The voltage open loop gain is

$$T_v = G_{vz} \cdot K_{out} \cdot G_{EA} \cdot z^{-\frac{Tdelay}{T_s}} = \frac{g_c T_s}{C(z-1)} \cdot K_{out} \cdot \frac{K_p}{z-\rho} \qquad \text{Eq. 3-63}$$

Thus we have three variables: the crossover frequency for voltage loop f_c, the poles for voltage compensator ρ, and the gain of voltage compensator K_p, so

$$\begin{cases} \left|G_{EA}(e^{-j2\omega_{line}T_s})\right| = \left|\dfrac{K_p}{e^{-j2\omega_{line}T_s}-\rho}\right| = \dfrac{\Delta B}{V_0^{ripp}\cdot K_{out}} \\ \angle T_v(e^{-j\omega_c T_s}) = -180^o + 45^o \\ \left|T_v(e^{-j\omega_c T_s})\right| = 1 \end{cases}, \qquad \text{Eq. 3-64}$$

where $T_{delay} = 10us, T_s = 200us, g_c = 2.93, K_{out} = 0.002, C = 330uF$.

From Equation 3-64, voltage compensator parameters are found:

$$\begin{cases} \omega_c = 37.4 rad/\sec \\ K_p = 0.0222 \\ \rho = 0.9924 \end{cases}$$

The voltage compensator transfer function is $G_{EAZ}(z) = \dfrac{K_p}{z-\rho} = \dfrac{0.00222}{z-0.9924}$.

The state equation is:

$$x(k) = 0.9924 \cdot x(k-1) + 0.00222 \cdot e(k) \qquad \text{Eq. 3-65}$$

The Bode plot of voltage loop gain in Figure 43 shows the voltage loop has a bandwidth of 6Hz and phase margin of 45°.

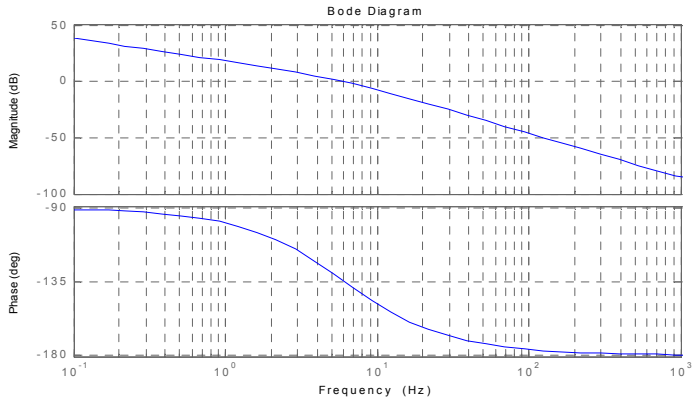


Figure 43 Bode plot for voltage open loop gain

3.3 Implementation

The complete digital control scheme includes one low-pass filter and two compensators. Three subprograms are established to fulfill them. For current compensator, which has a sampling frequency equal to the switching frequency, the compensation subprogram is executed per switching cycle. For feed-forward low-pass filter and voltage compensator, whose sampling frequency is 5kHz, subprograms are executed once per 20 switching cycles. A software counter is installed to organize the timing. Executions of subprograms are synchronized by an on-chip PWM timer, which generates two PWM synchronous interrupt signals per switching cycle. The PWM synchronous interrupts also serves as the start signal of ADC.

3.3.1 Flowchart

3.3.1.1 Main Program

The flowchart of main program is shown in Figure 44. The task of main program is to keep DSP in operation. The condition for halting main program is the power down or PWM trip interrupt, which can be used for fault protection.

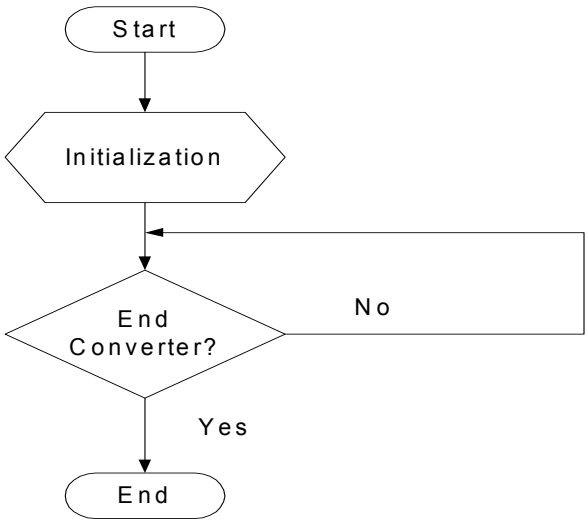


Figure 44 Flowchart of main program

3.3.1.2 Interrupt Service Routine Program

The two PWM interrupt signals (PWMsyn1 and PWMsyn2) are generated separately at the beginning and the middle of one switching cycle. Both of them can start the interrupt service routine. To identify them the status register is read. The interrupt service routine is separated into two parts: one for signal PWMsyn1, the other for signal PWMsyn2. The flowchart of the interrupt service routine is shown in Figure 45.

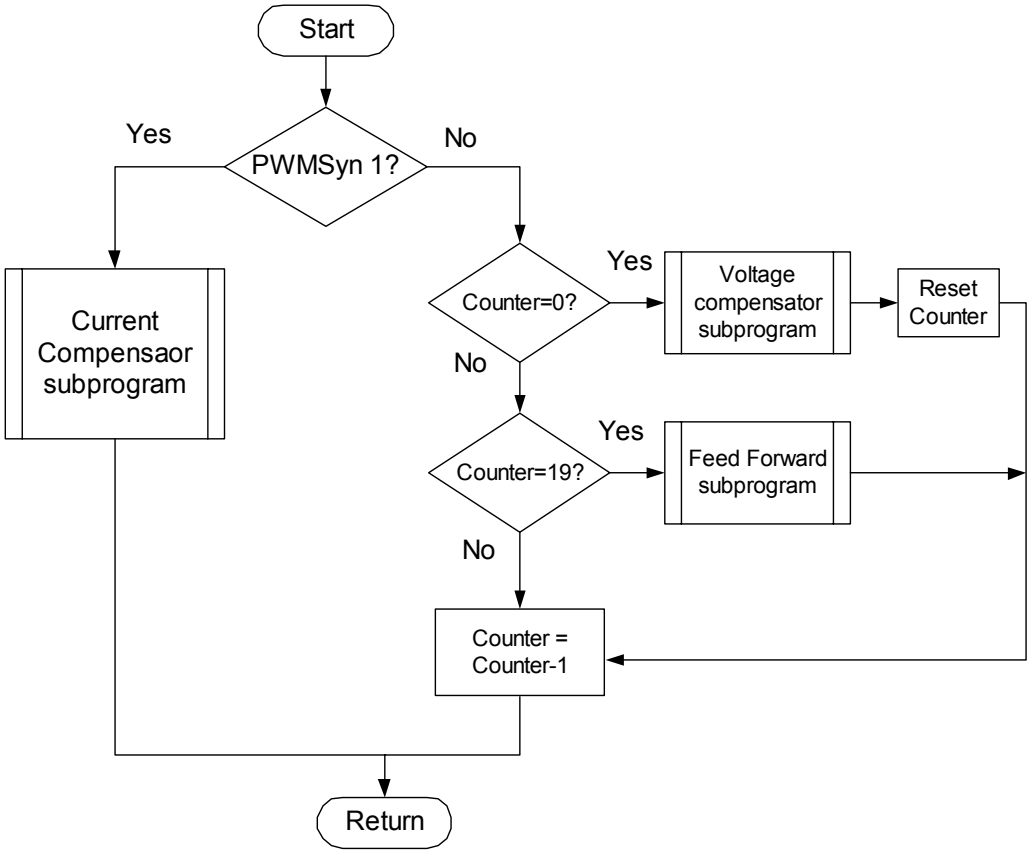


Figure 45 Flowchart for interrupt service routine program

3.3.1.3 Subprograms

3.3.1.3.1 Current compensator Subprogram

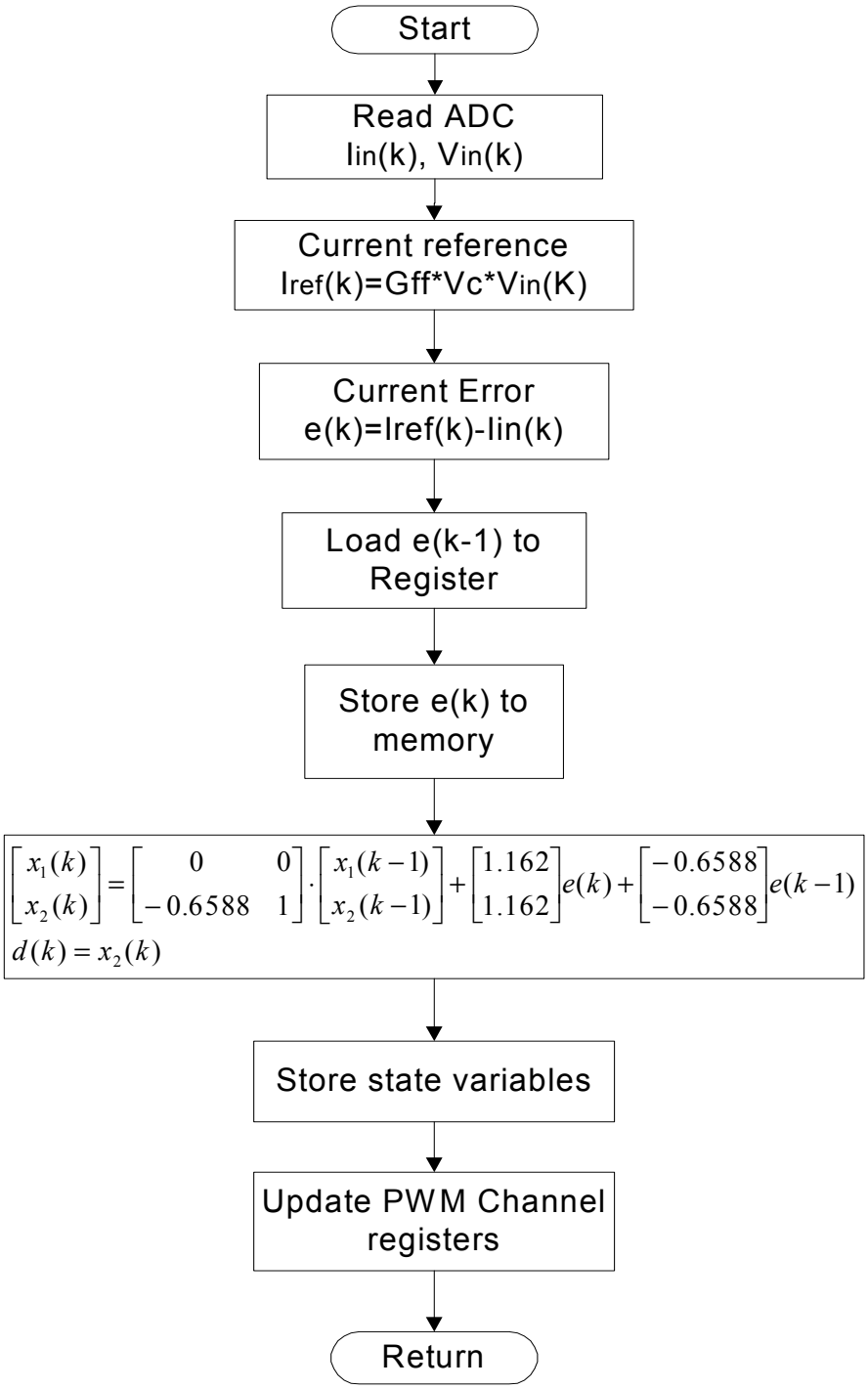


Figure 46 Flowchart for current compensator subprogram

3.3.1.3.2 Voltage Compensator Subprogram:

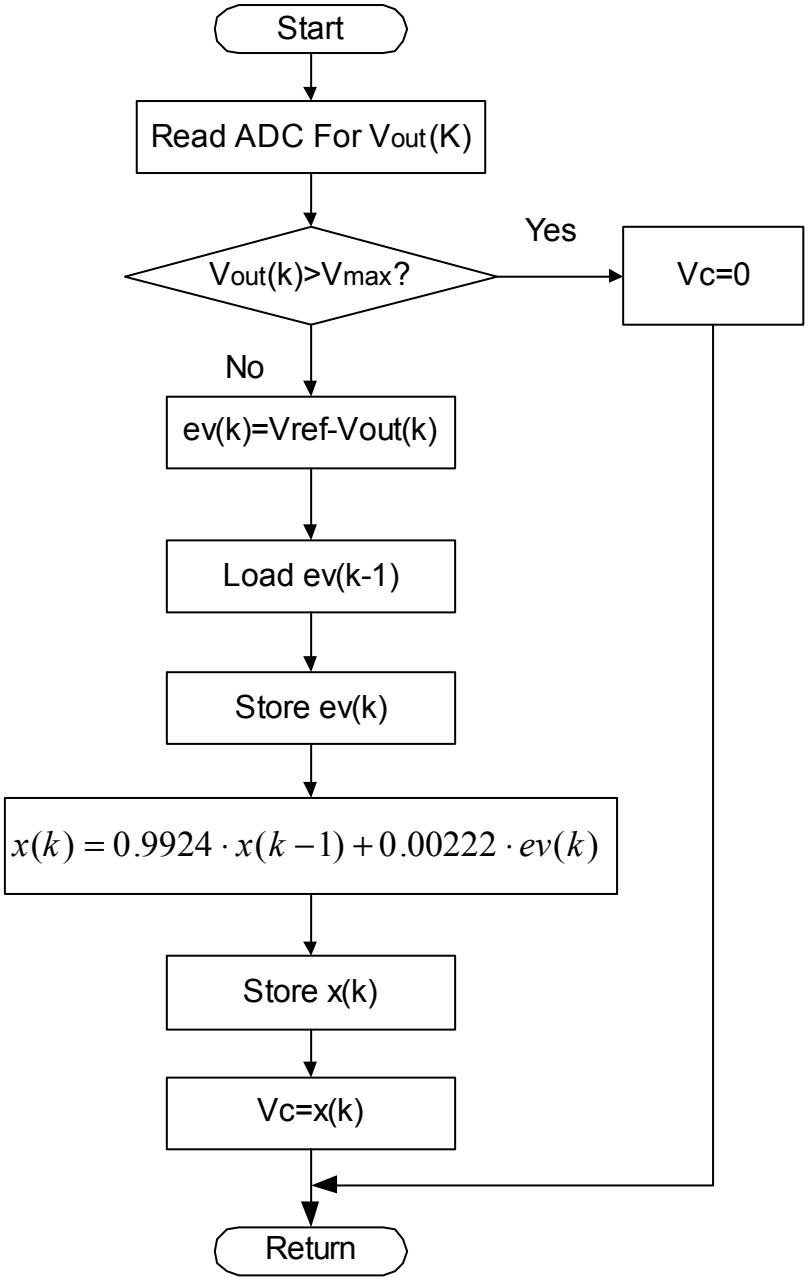


Figure 47 Flowchart for voltage compensator subprogram

3.3.1.3.3 Feed Forward Subprogram:

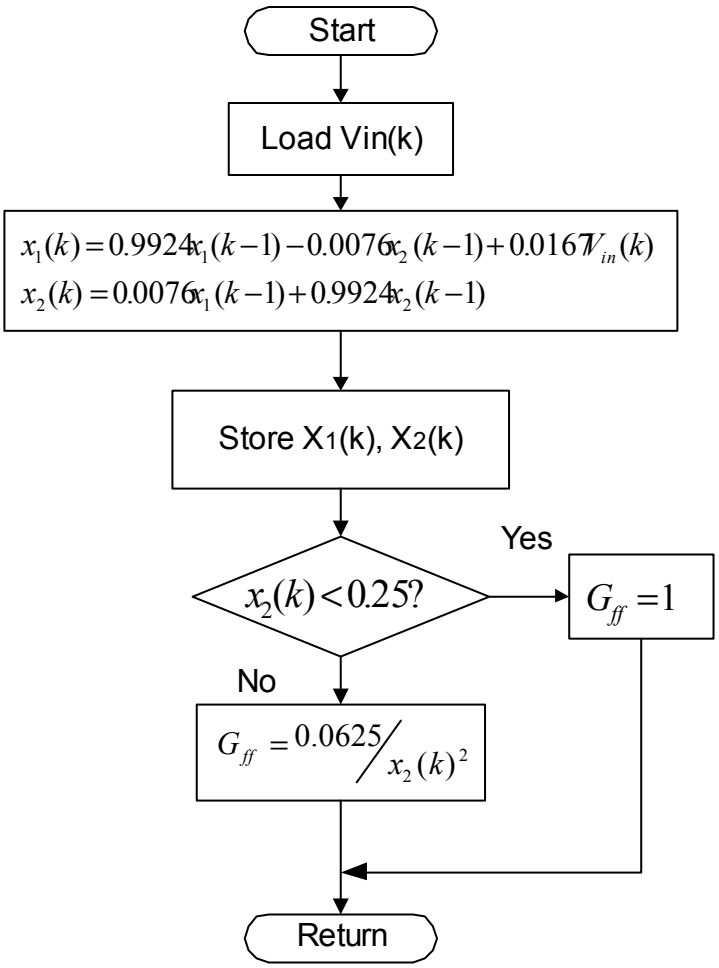


Figure 48 Flowchart for feed forward loop subprogram

3.3.2 Experimental Results

ADMC401 is used to implement digital control for the 1kW PFC converter.

Resource occupation:

Memory for state variables, input signals and temporary results: 20 words

Memory for control coefficients: 10 words

Maximum instructions per PWM cycle: 180

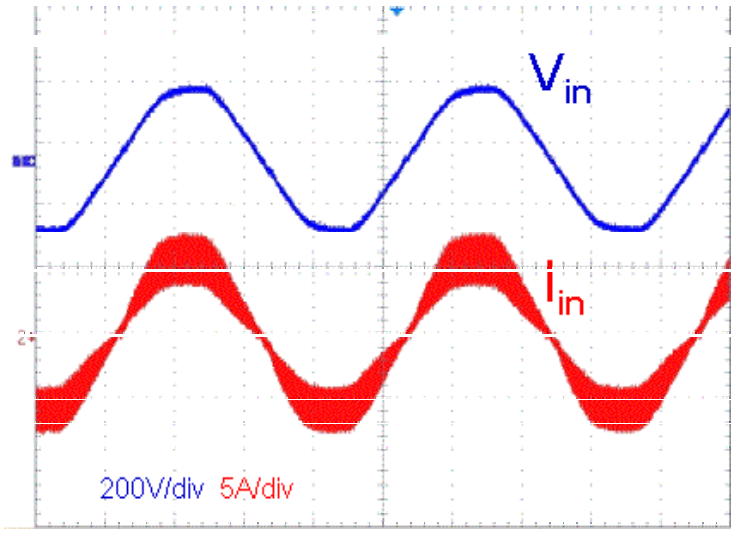


Figure 49 Input Current waveform w/o EMI filter

A PF of 99.7% is achieved by digital controlled 1kW PFC with 100kHz switch frequency.

3.4 Current-Loop Feed-Forward Compensation

As we discussed before, the digital delay limits the current loop bandwidth and jeopardizes its stability. The reason for the high bandwidth current loop gain is not just for faithful tracking of the semi-sinusoidal reference but also for achieving a high disturbance rejection. The largest disturbance injected into the power stage is the input voltage, as shown in Figure 50.

The input voltage contains large amounts of harmonics. As we discussed before, even-order harmonics in inductor current generate fundamental and odd-order harmonics in line current. If the resulting fundamental current harmonic has a large phase displacement between the input voltage, it can significantly reduce the displacement factor k_θ. Moreover, the odd-order harmonics can reduce the distortion factor k_d. Both lead to a smaller PF. In this section, the influence of input voltage on line current and the relation with current compensation will be studied. Current-loop Feed-Forward (CFF) Compensation is proposed to reduce this influence. The benefit and trade-off of inserting CFF compensation is also studied in the following sections.

Despite the difference in frequency response at high frequency ($f \geq f_c$), the digital and analog compensators have a similar frequency response at low frequency ($f << f_c$). For the purpose of convenience, the compensator frequency response is represented by that of an analog compensator in the following studies. For the frequency less than 2kHz, the digital delay is smaller than 8^o. The effect of digital delay is ignored for this frequency range. For frequency that is much smaller than half of the switching frequency, PWM is considered as a gain of 1 in the following sections.

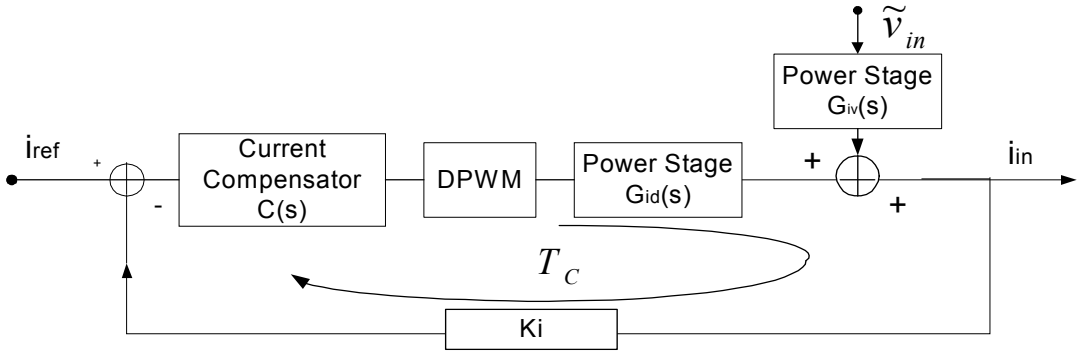


Figure 50 Simplified current loop system with input voltage influence.

The inductor current is:

$$i_{in}(s) = i_{ref}(s)\frac{CG_{id}}{1+T_C} + v_g(s)\frac{G_{iv}}{1+T_c} \qquad \text{Eq. 3-66}$$

3.4.1 Input voltage harmonics

The input voltage consists of a large amount of harmonic components. Table 6 gives two examples.

Table 6 Examples of harmonic components in input voltage

Harmonic Order (n) / V_{rms}(V)	2	4	6	8	10	12
90	54	10.8	4.63	2.6	1.64	1.13
264	158	31.7	13.6	7.5	4.8	3.32

The higher the line voltage the more the line current is influenced.

3.4.2 Influence of input voltage

The DC component of the rectified voltage does not influence the current loop because the current compensator always has an infinite DC gain because of the

integrator. However the large amount of even order harmonics influences the current loops and increase THD and the displacement angle.

The open loop voltage-to-current transfer function is:

$$G_{iv}(s)=\frac{\widetilde{i}_{in}}{\widetilde{v}_g}=\frac{1}{R_L(1-D)^2}\cdot\frac{1+sR_LC}{1+\frac{sL}{R_L(1-D)^2}+\frac{s^2LC}{(1-D)^2}}. \qquad \text{Eq. 3-67}$$

As shown in Figure 50, the voltage-to-current transfer function with current loop closed is:

$$G_{ivclose}(s)=\frac{G_{iv}(s)}{1+T_C(s)}, \qquad \text{Eq. 3-68}$$

where $T_c=K_iG_{id}C$ is the current open-loop gain. Since significant harmonics mainly exist in the range much below the crossover frequency where the magnitude of loop gain is huge, it is proper to approximate $\frac{1}{1+T_C}$ with $\frac{1}{T_C}$. Thus, $G_{ivclose}$ can be simplified as:

$$G_{ivclose}(s)=\frac{G_{iv}(s)}{1+T_C(s)}\approx\frac{G_{iv}(s)}{K_iG_{id}(s)C(s)}. \qquad \text{Eq. 3-69}$$

And we can further simplify Equation 3-69 with the following approximation:

$$\frac{G_{iv}(s)}{G_{id}(s)}=\frac{1}{2V_o}\cdot\frac{1+sR_LC}{1+\frac{sR_LC}{2}}\approx\frac{1}{V_o},\ f>>\frac{2}{2\pi R_LC} \qquad \text{Eq. 3-70}$$

The output capacitor C is very large. It is appropriate to assume that the frequency $2f_{line}$ is much larger than $\frac{1}{2\pi R_L C}$ and $\frac{2}{2\pi R_L C}$. For frequency domain of interest, $\frac{G_{iv}(s)}{G_{id}(s)} \approx \frac{1}{V_o}$. We have $G_{ivclose}(S) \approx \frac{1}{V_o K_i C(S)}$.

A conventional average-current-mode compensator is:

$$C(s) = \frac{\omega_i(1+\frac{s}{\omega_z})}{s(1+\frac{s}{\omega_p})}. \qquad \text{Eq. 3-71}$$

The pole is placed at half of the switching frequency that is far larger than f_C. For the digital control in this thesis, this function is still realized by analog components with transfer function as $\frac{1}{1+\frac{s}{\omega_p}}$. The effect of $\frac{1}{1+\frac{s}{\omega_p}}$ in the frequency range of interest can be ignored. As we discussed before, the digital compensator response in the frequency range of interest can be approximated by $\frac{\omega_i(1+\frac{s}{\omega_z})}{s}$. For frequency much smaller than $f_z = \frac{\omega_z}{2\pi}$, current compensator can be simplified as

$$C(s) \approx \frac{\omega_i}{s}, (f << f_z) \qquad \text{Eq. 3-72}$$

Therefore the voltage-to-current transfer function is further simplified:

$$G_{ivclose} \approx \frac{G_{iv}}{K_i G_{id} C} \approx \frac{1}{K_i} \cdot \frac{1}{V_o} \cdot \frac{s}{\omega_i}, (f << f_z) \qquad \text{Eq. 3-73}$$

Therefore the magnitude of $G_{ivclose}$ is related to the current open-loop gain. Figure 51 shows Bode plots of $G_{ivclose}$ with the same 45° phase margin and different bandwidth.

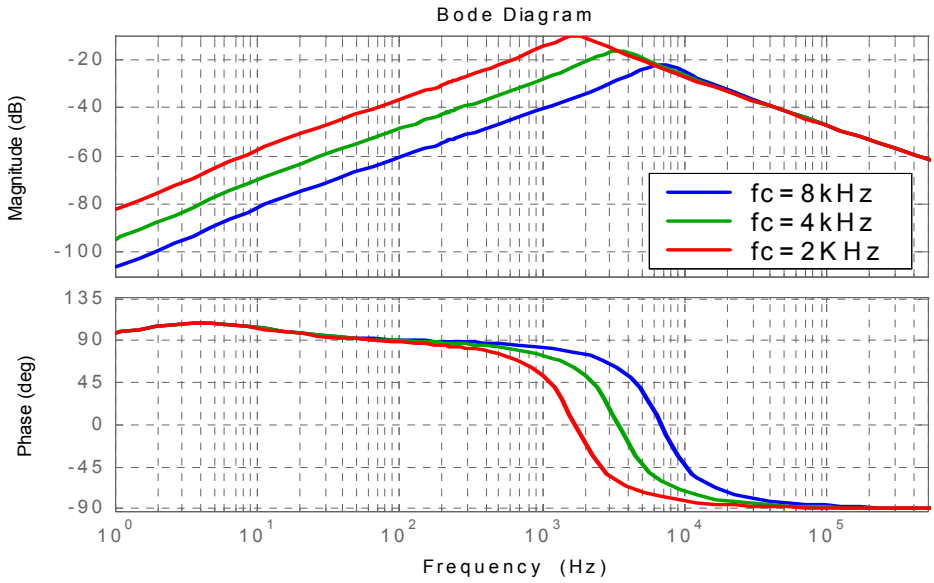


Figure 51 Bode plots of $G_{ivclose}$ with different current compensator

When the one-zero digital current compensator is put into simulation, great distortion is observed at zero crossing. One of the reasons is the lower current loop gain. The digital compensator has a lower frequency zero to compensate the phase lag caused by digital delay, resulting in a lower ω_i.

To fully understand how this input voltage influences PF, we can analyze the even order voltage harmonics. From Equation 3-73, the harmonic of the input voltage will create a 90° lead corresponding harmonic at the inductor current. The relation is shown in Figure 52. For convenience, 2nd order harmonic is used to represent all even-order harmonics in the inductor current.

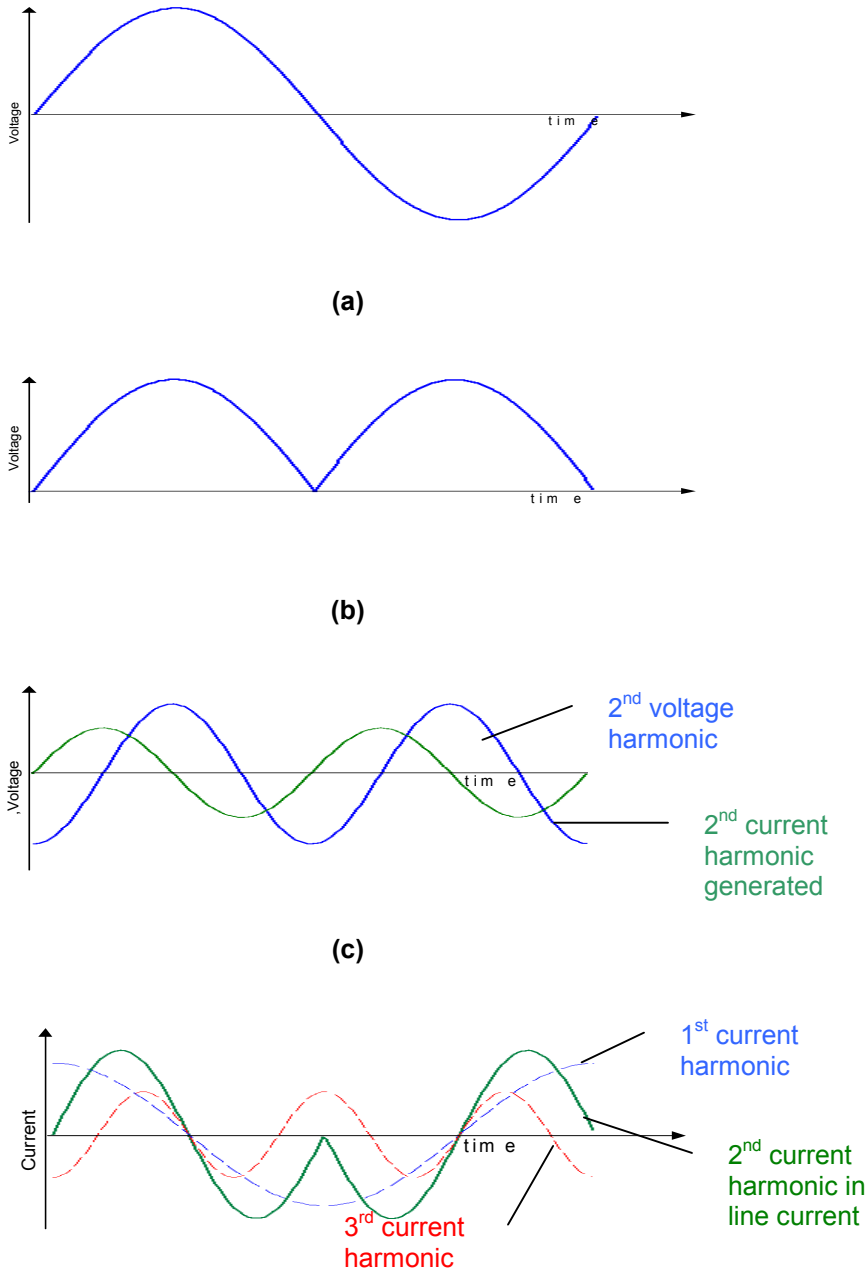


Figure 52 Relationship between voltage 2nd harmonic and line current: (a) line voltage, (b) boost converter input voltage, (c) 2nd harmonic voltage and 2nd harmonic current and (d) fundamental and 3rd harmonics generated

The 2nd-order harmonic component value is:

$$V_{2n\_rms} = \frac{4}{(4n^2-1)\pi} V_{in\_rms}$$ Eq. 3-74

The inductor current generated by this voltage harmonic is:

$$I_{2n\_rms} = V_{2nd\_rms} \cdot G_{ivclose}(j2n \cdot \omega_{line})$$ Eq. 3-75

The fundamental line current generated by this inductor current is:

$$I_{1st\_rms} = I_{2n\_rms} \cdot \frac{8n}{(4n^2-1)\pi}$$ Eq. 3-76

This fundamental line current is 90° ahead of the line voltage. It is expressed as $I_{\perp}$ for convenience.

As shown in Figure 53, the fundamental current generated is 90° ahead of the input voltage vector, increasing the displacement angle between input current and input voltage.

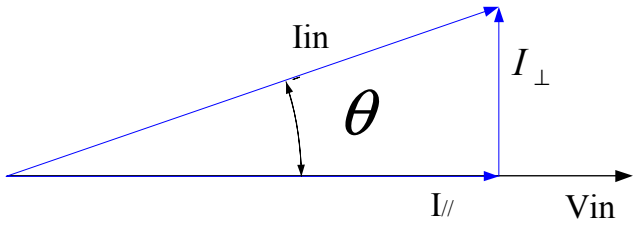


Figure 53 Current vectors and voltage vector

Assuming the converter has an efficiency of 0.9, we can calculate the current vector parallel to the input voltage.

$$I_{//} = \frac{P_{out}}{\eta \cdot V_{in\_rms}}$$ Eq. 3-77

Displacement angle θ is:

$$\theta = \arctan(\frac{I_{\perp}}{I_{//}})$$ Eq. 3-78

The input voltage can be treated as a disturbance whose attenuation is defined as $\frac{\tilde{v}_{in}}{\tilde{i}_{in}}$. To have a large disturbance attenuation requires a large current open loop gain.

The third order harmonic line current generated by 2nd order inductor current is:

$$I_{3\_rms} = I_{2n\_rms} \cdot \frac{8n}{(4n^2-9)\pi}$$ Eq. 3-79

Because low frequency zero is used to compensate the phase lag caused by digital delay. The simple one-zero compensator will result in a low current loop gain at the frequency range of interest, while the two-zero compensator has a small gain margin and complex structure that increases cost.

Following is a solution to achieve good PF with simple one-zero compensator.

3.4.3 Current Loop Feed Forward

Thus Current-loop Feed-Forward (shown in Figure 54) is a solution to achieve high PF even with a low bandwidth current compensator.

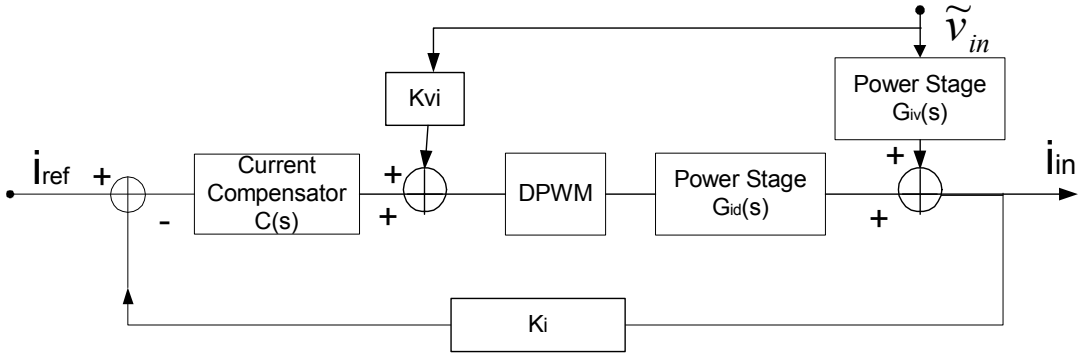


Figure 54 Illustration of current-loop feed-forward

Assuming the CFF gain is K_{vi}, a new voltage-to-current transfer function is obtained:

$$G_{ivclose} = G_{iv}\frac{1+K_{vi}\cdot\frac{G_{id}}{G_{iv}}}{1+T_C}. \qquad \text{Eq. 3-80}$$

The aim of CFF compensation is to reduce the magnitude of $G_{ivclose}$ in the frequency range of interest. It is noticed in Equation 3-70 that $\frac{G_{iv}}{G_{id}} \approx \frac{1}{V_o}$ for $(\frac{2}{2\pi R_L C} < 2f_{line} < f << f_c)$. If $K_{vi} = -\frac{1}{V_o}$, the magnitude of $G_{ivclose}$ is greatly decreased. A normalized coefficient k_{vi} is applied, $k_{vi} = -K_{vi}\cdot V_0$.

Figure 55 shows how the value of k_{vi} affects the magnitude of voltage-to-current transfer function. The current loop has a bandwidth of 4kHz. It is observed that the closer k_{vi} is to 1, and the smaller is $|G_{ivclose}|$.

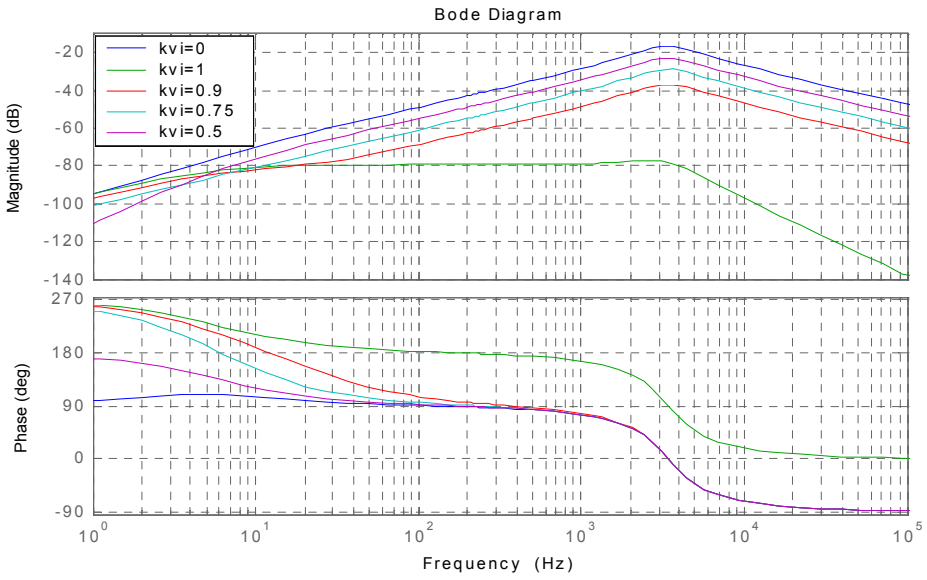


Figure 55 Effect of different CFF gain k_{vi}

3.4.4 Simulation Results

As we mentioned before, input voltage harmonics can influence both the displacement factor and distortion factor. Comparisons of both of these factors are made. Following simulations are run at V_{in_rms}=220V.

3.4.4.1 Displacement Factor Comparison

Simulations are run in Simulink to verify the effectiveness of CFF comparison. First analog current compensator with an 8KHz bandwidth is used as the base line. PFs are tested under full load condition. The output power is 1,000W.

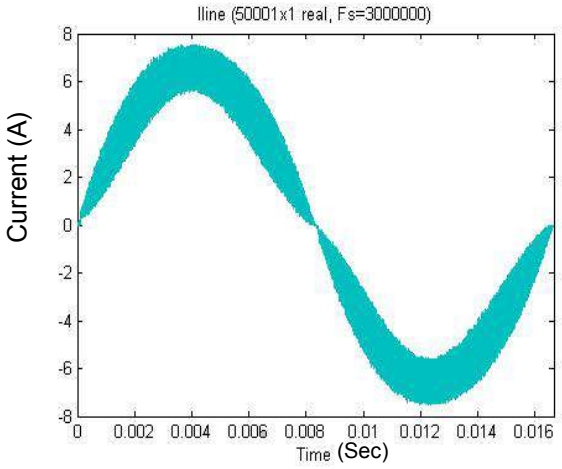


Figure 56 Line current of PFC w/o EMI filter (f_c =8KHz).

Fourier analysis is used to calculate the fundamental component of the line current. For the fundamental component: $I_{//} = 4.5964A, \text{and } I_{\perp} = 0.149A$.

The displacement angle θ is 1.86° ahead. The displacement factor without EMI filter is $K_{\theta} = \cos 1.86^{o} = 0.9995$.

Then an analog current compensator with a 4 KHz bandwidth is used to verify the relationship between the current compensator and the displacement factor.

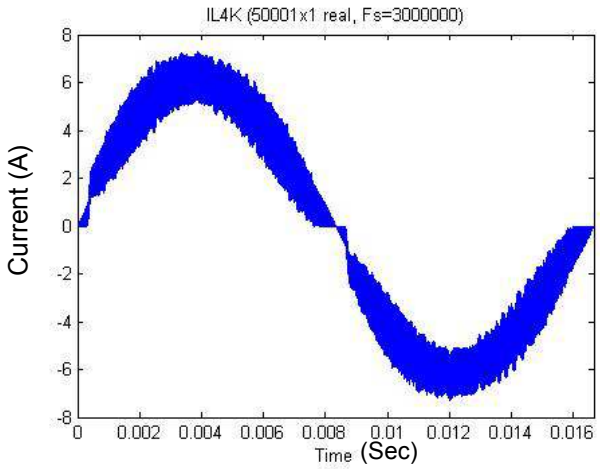


Figure 57 Line current of PFC w/o EMI filter (f_c =4KHz)

Fourier analysis is used to calculate the fundamental component of the line current. For the fundamental component: $I_{//} = 4.2748A$ and $I_{\perp} = 0.4418A$.

The displacement angle θ is 5.9^o ahead. The displacement factor without EMI filter is $K_\theta = \cos 5.9^o = 0.9947$.

A 4 KHz bandwidth current compensator with CFF compensation is used to verify the effectiveness of CFF.

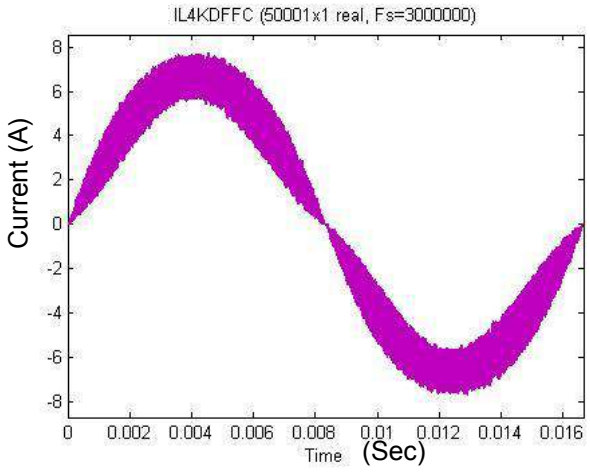


Figure 58 Line current of PFC w/o EMI filter (f_c =4KHz, w/ $k_{vi} = 0.9$)

Fourier analysis is used to calculate the fundamental component of the line current. For the fundamental component: $I_{//} = 4.6984A$ and $I_{\perp} = 0.069A$.

The displacement angle θ is 0.84°. The displacement factor without EMI filter is $K_{\theta} = \cos 0.84^{o} = 0.9999$. The CFF compensation is effective to improve the displacement factor.

3.4.4.2 Harmonic Distortion Comparisons

The FFT method is used to calculate line-current harmonics. Figure 59 is the line-current harmonics of current loop bandwidth 8kHz and 4kHz. In the frequency range (120Hz~2,400Hz), i.e., harmonic order from 2 to 40, 8kHz bandwidth design shows lower level of harmonics current than that of the 4kHz bandwidth.

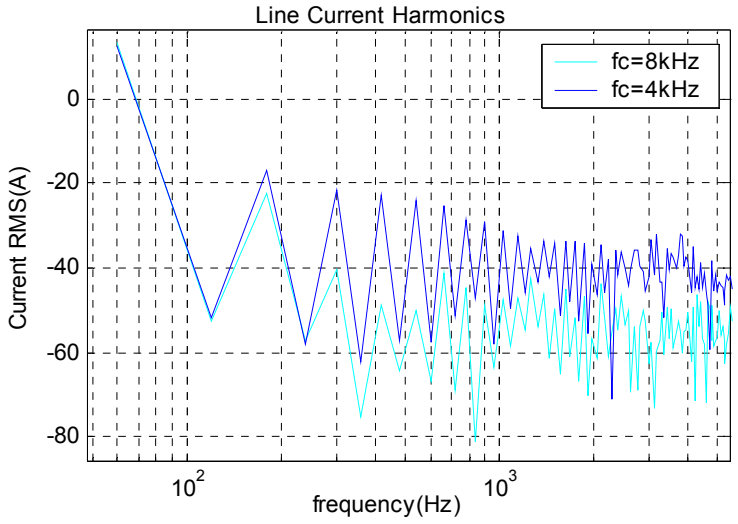


Figure 59 Comparison of line-current harmonics with different current loop bandwidths.

Comparison is also made between line current harmonics with and without CFF. Figure 60 shows that with the same current compensator, the one with CFF shows lower level of current harmonics.

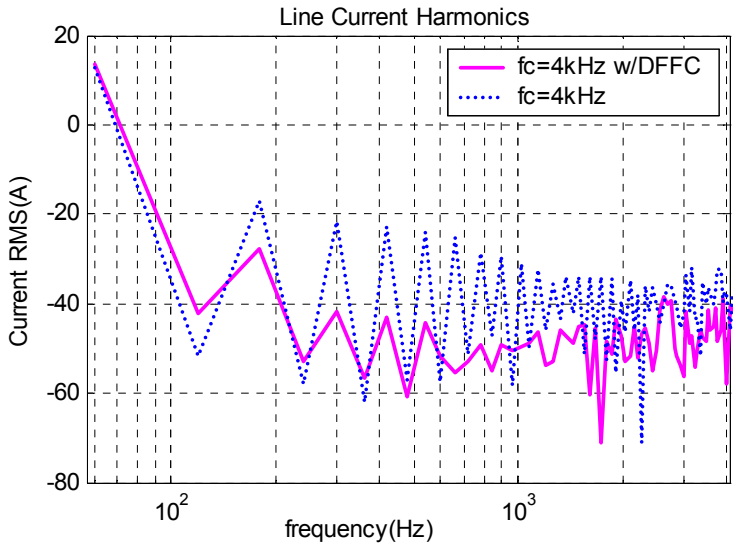


Figure 60 Comparison of line current harmonics with and without CFF

Figure 61 shows the maximum permissible harmonic values and the three examples. All of them can meet the requirement.

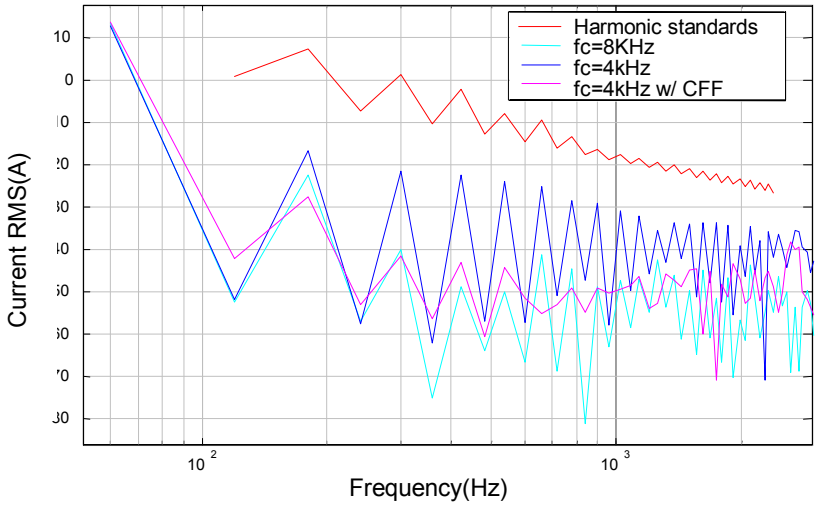


Figure 61 harmonic comparisons

Not only high frequency harmonics are reduced, but 3rd order harmonic is reduced as well, which indicates that CFF is effective at low frequencies. As we

know, the quasi-static model is only valid for frequencies much higher than $2f_{line}$. However A. Huliehel pointed out that despite the large input voltage variation at low frequencies and nonlinearity, it is still possible to derive small-signal model for low frequencies [39]. This small-signal model in [39] differs from the quasi-static model just in operation point. If so, CFF is effective for low frequencies.

3.4.4.3 Influence of CFF Gain K_{vi}

It is noted that there is no perfect sensor. K_{vi} is subject to deviation. Furthermore, implementing CFF with K_{vi}=1 will require extra multiplication and storage of result and coefficients. It is necessary to study the influence of K_{vi}. From section 3.4.3, we have

$$\left.\begin{aligned} G_{ivclose} = G_{iv}\frac{1+K_{vi}\cdot\dfrac{G_{id}}{G_{iv}}}{1+T_C} \approx G_{iv}\frac{1+K_{vi}\cdot V_{out}}{1+T_C} \\ k_{vi} = -K_{vi}\cdot V_{out} \end{aligned}\right\} \Rightarrow G_{ivclose} = \frac{G_{iv}}{1+T_C}(1-k_{vi}) \text{, Eq. 3-81}$$

where k_{vi} is the normalized CFF gain. To have:

$$\left|G_{ivclose}\right| = \left|\frac{G_{iv}}{1+T_C}(1-k_{vi})\right| < \left|\frac{G_{iv}}{1+T_C}\right|, \qquad \text{Eq. 3-82}$$

we should have

$$\left|1-k_{vi}\right| < 1 \Rightarrow 0 < k_{vi} < 2\,. \qquad \text{Eq. 3-83}$$

From Equation 3-73, $\frac{G_{iv}}{1+T_C} \approx \frac{G_{iv}}{K_i G_{id} C} \approx \frac{1}{K_i}\cdot\frac{1}{V_o}\cdot\frac{s}{\omega_i}, (f << f_c)$. Then when $k_{vi} < 1$, $\frac{1}{K_i}\cdot\frac{1}{V_o}\cdot\frac{1}{\omega_i}\cdot(1-k_{vi}) > 0$. The input voltage harmonics generate 90° lead input current harmonics. Figure 62 gives several Bode plots with different $k_{vi} \subset (0,1)$.

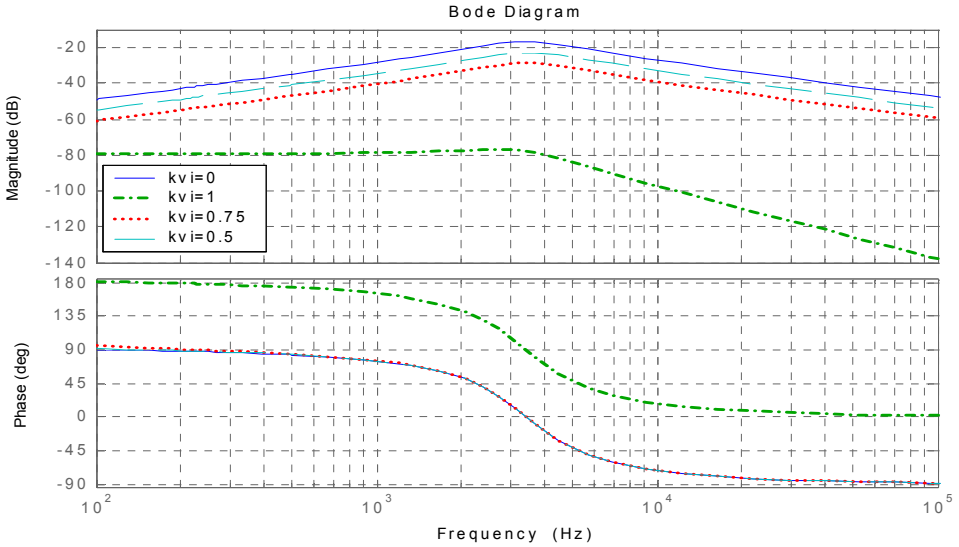


Figure 62 Bode plots for $k_{vi} \subset (0,1)$

When $1 < k_{vi}$, $\frac{1}{K_i V_o \omega_i}(1-k_{vi}) < 0$. Then input voltage harmonics generate 90° lag input current harmonic. Figure 63 gives several Bode plots with different $k_{vi} \subset$ (1,2).

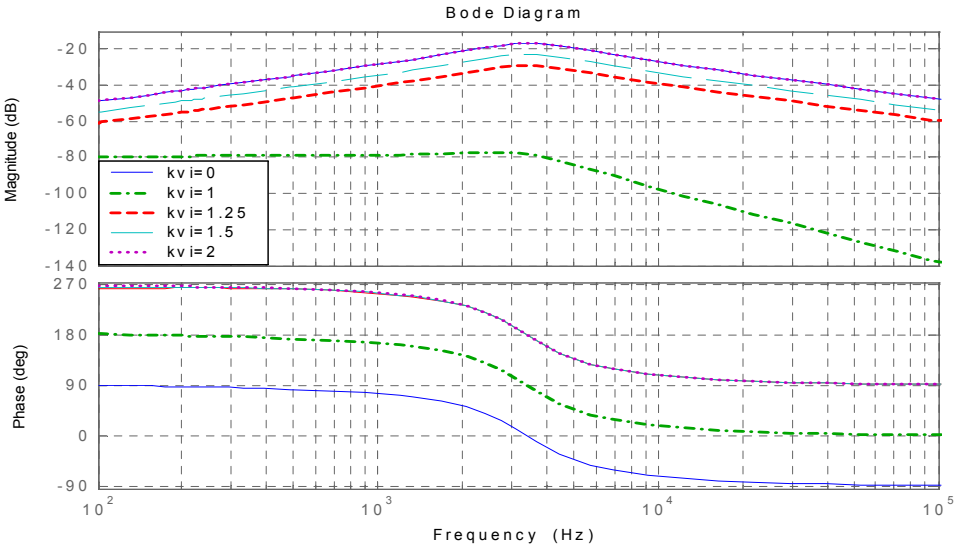


Figure 63 Bode plots for $k_{vi} \subset (1,2)$

Simulations with different k_{vi} are run in Simulink. FFT analysis and Fourier analysis are given to each case. Figure 64 compares the results with different k_{vi}.

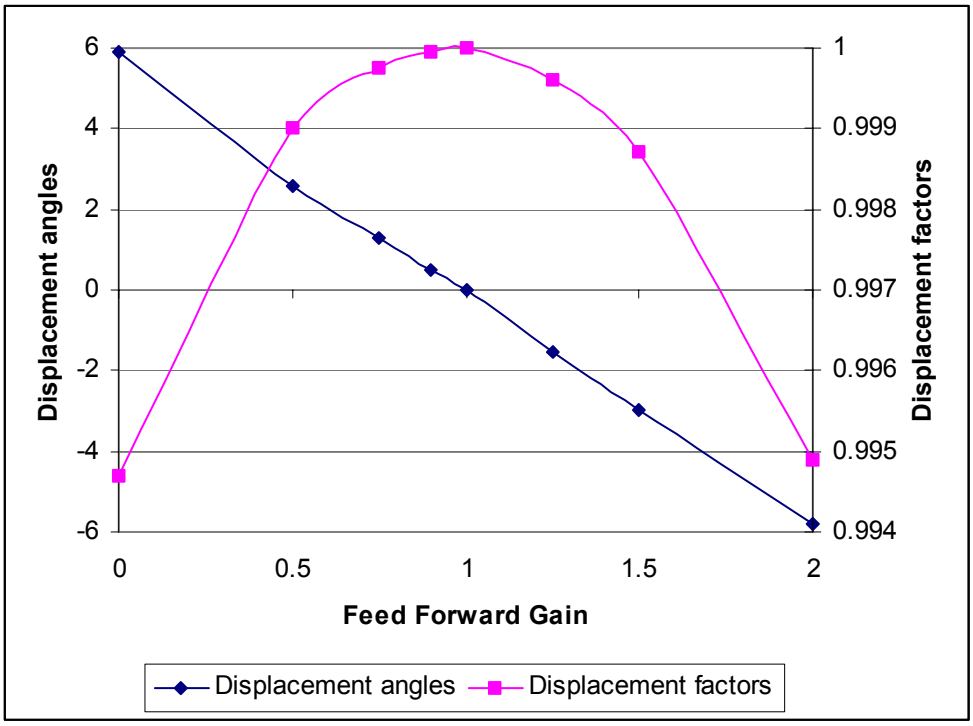


Figure 64 Comparison of displacement angles (degree) and displacement factors with different CFF gain.

3.4.4.4 Digital Controller with CFF Compensation

The previous study of CFF carried out is with analog controllers. Digital controller performance is compromised by digital delay. Thus the effectiveness has to be proved for digital controller. A digital current compensator is designed to achieve 4kHz current loop bandwidth.

3.4.4.4.1 Displacement Factor Comparison:

Simulation result of digital current compensator without CFF compensation is shown in Figure 65.

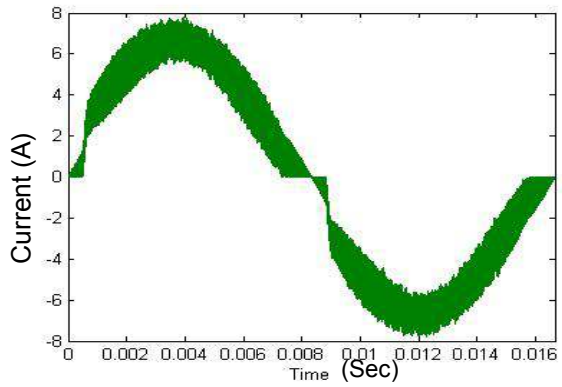


Figure 65 Line current w/o EMI filter (f_c =4KHz, w/o CFF)

Fourier analysis is used to calculate the fundamental component of the line current. For the fundamental component: $I_{//} = 4.6975A$ and $I_{\perp} = 0.67A$.

The displacement angle θ is 8.23°. Then displacement factor without EMI filter is $K_{\theta} = \cos 8.23^{o} = 0.9895$.

A CFF compensation with $k_{vi} = 0.9$ is applied.

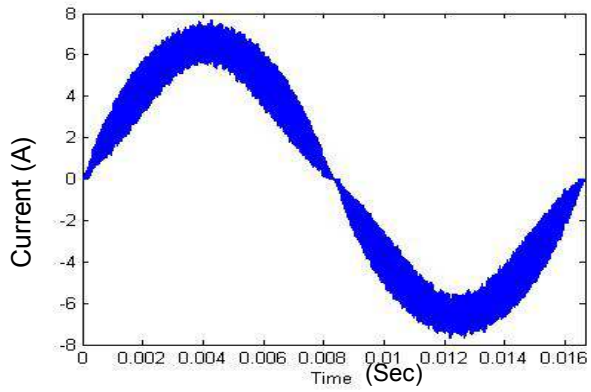


Figure 66 Line current w/o EMI filter (f_c =4KHz, w/ CFF $k_{vi} = 0.9$)

Fourier analysis is used to calculate the fundamental component of the line current. For the fundamental component: $I_{//} = 4.6966A$ and $I_{\perp} = 0.0825A$.

The displacement angle θ is 1.04°. The displacement factor without EMI filter is $K_\theta = \cos 1.04^o = 0.9998$. Significant improvement is observed.

3.4.4.4.2 Harmonic Distortion Comparison:

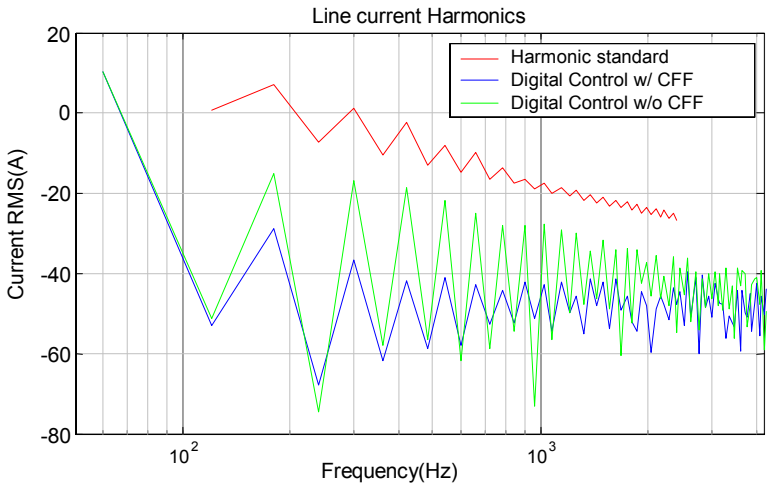


Figure 67 Line Current Harmonics Comparison

It is observed Digital Controller w/ CFF compensation has greatly reduced the line current harmonics.

4 DIGITAL CONTROL FOR THE THREE-LEVEL PFC

Increasing power density is one of the goals of research in DC power supply. Conventional single switch PFC has larger power loss at low line than at high line. It is common that universal-line PFC always has power derating at 90~150 V_{ac}. An advanced PFC was proposed to solve this problem. This three-level PFC (3-LPFC) has high efficiency at low line, which indicates it can achieve higher power density than single switch PFC under the same power rating. However, problems such as control of range switch, complex optimal control structure and output capacitor imbalance are to be solved before wide application of 3-L PFC. Digital control can provide logic operation, which may provide simple solutions. It is necessary to study digital control for 3-L PFC.

4.1 Three-Level PFC Converter

When the input voltage of the PFC decreases, the input current will increase accordingly, which means larger power loss in the converter. This generates a great stress on thermal management. To solve this problem, the three-level PFC w/ Range Switch (3-LPFC w/ RS) was proposed, as shown in Figure 68. The range switch (RS) turns on when input voltage is 90~140V, when the circuit is referred as working in Rson mode. The RS turns off when input voltage is 140~264V, when the circuit is referred as working in Rsoff mode. The most significant feature of this converter is its high efficiency at Rson mode.

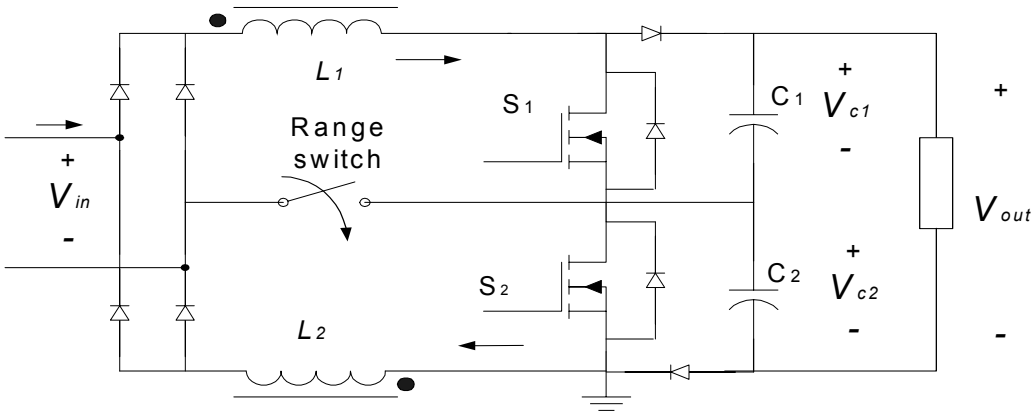


Figure 68 Power stage of 3-LPFC w/ RS

The reasons for high efficiency at Rson mode are:

1. Lower conduction loss: The input current flows through one of the rectifier diodes instead of two of them. Thus, lower diode bridge conduction loss is achieved.

2. Lower switching loss: For MOSFETs, V_{ds} is half of the output voltage, and lower rating MOSFETs can be used. Each switch is working half of the time. Thus, lower switching loss is achieved.

Implementation of optimal operation for the Rson and Rsoff modes and reliable balancing of output capacitor voltages can greatly enhance the 3-LPFC's competitiveness.

4.2 Literature Review and Previous works

Y. Jiang with VPEC proposed a 3-LPFC without RS [39]. The paper proposed the 180^{o} phase shift PWM for the two switches, which reduced the inductor current ripple amplitude to a quarter of the original one. However, this topology has not been widely adapted. The PWM operation proposed is the optimal method for the 3-LPFC at its Rsoff mode.

In 1995, Dr. Erickson from the University of Colorado applied the concept of RS to the 3-LPFC. The paper proved the high efficiency of 3-LPFC at low line. However, the 3-LPFC at Rsoff mode had the same control and operation with the 3-LPFC at Rson mode. The output capacitor voltage was balanced passively [33].

In 2000, Bing Lu with CPES at Virginia Tech built an analog-controlled 1kW 3-LPFC with RS prototype. The control schemes are the same for RS on/off. Experimental results show that its performance is compromised at Rsoff mode because it is not working with optimal operation. The efficiency chart shows that the worst case of Rsoff is only slightly higher than the worst case of Rson. If heat distribution is taken into consideration, it is possible that the thermal management worst case occurs at Rsoff.

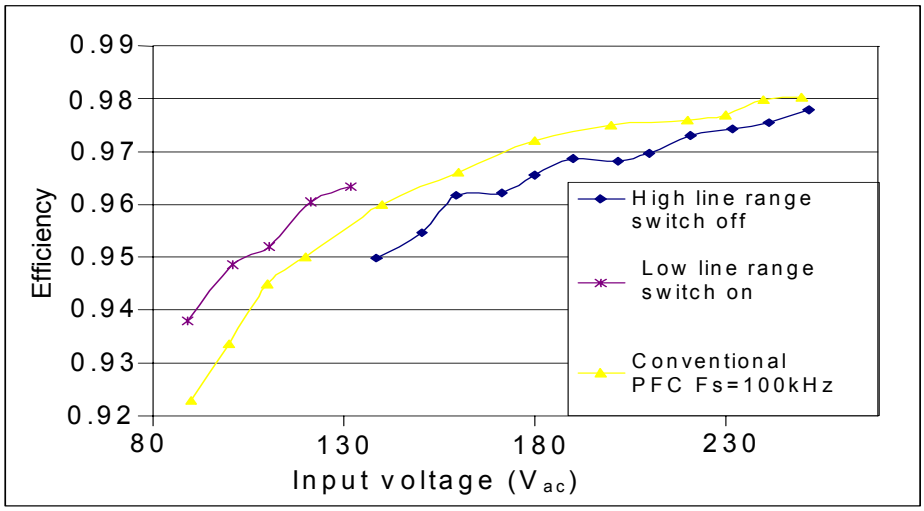


Figure 69 Efficiency comparisons between conventional Single-switch PFC and analog controlled 3-LPFC.

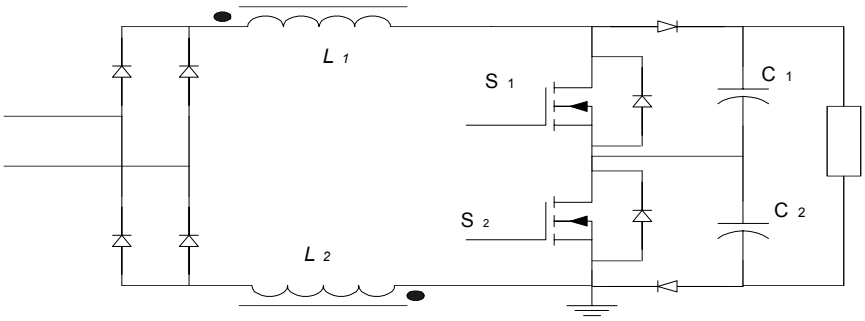
4.3 Review of 3-LPFC with RS: Operation and Control

4.3.1 Topology at Rsoff mode

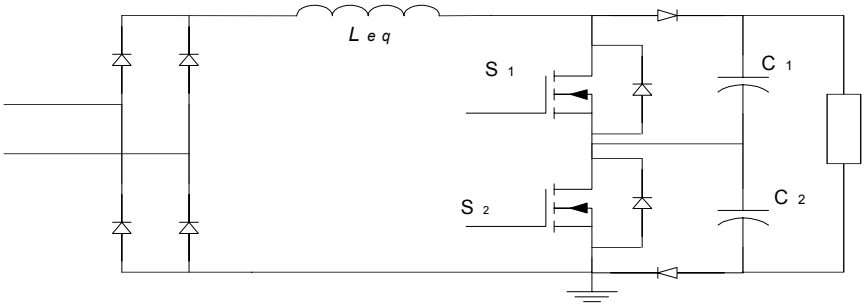
When the range switch is turned off the two well coupled inductors are in series (Figure 70 (a)). They equal to one inductor with inductance of

$$L_{eq} = L_1 + L_2 + 2\sqrt{L_1 L_2}$$

The simplified circuit is equivalent to the circuit proposed by Jiang [39]. When $L_1 = L_2 = L$, we have $L_{eq} = 4L$.



(a)



(b)

Figure 70 Converter topology at Rsoff mode: (a) Original topology and (b) simplified topology

The switching frequency is half of the frequency of the inductor current ripples [39]. With the optimal operation proposed in [39], the switching frequency is just half of the switching frequency used by Erickson [33] and B. Lu (2000). This would help to reduce the switching loss at Rsoff mode. However, balancing the output capacitor is a challenge.

4.3.1.1 Output Capacitor Imbalance

Output capacitor imbalance can be caused by driver mismatching, device mismatching and unequal capacitor leakage currents. Previous work used balancing resistors to balance the output capacitor voltage shown in Figure 71.

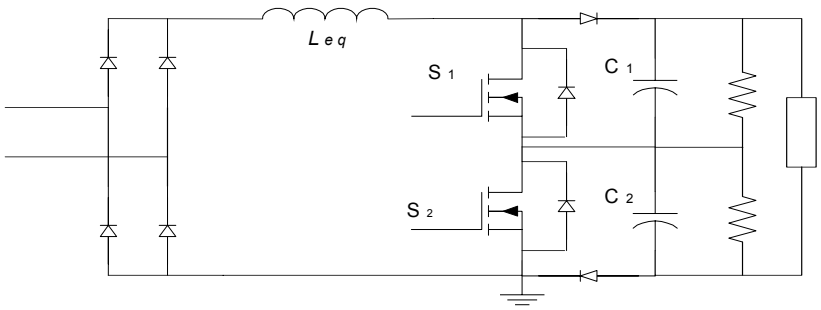


Figure 71 Passive balancing with balancing resistors.

It is difficult to predict either the mismatching of devices or drivers or the leakage current for each capacitor. Concerns exist pertaining to under-design of balancing resistors.

4.3.1.2 Power Stage Modeling

To find out the opportunity to actively balance output capacitor voltage, it is necessary to find out the exact power stage model.

Different from conventional single-switch PFC, the 3-LPFC has two capacitors and one inductor. Two three-terminal average models are used to find out the small-signal model. Here the two switches are independent. The duty cycle is defined separately as d_1 and d_2.

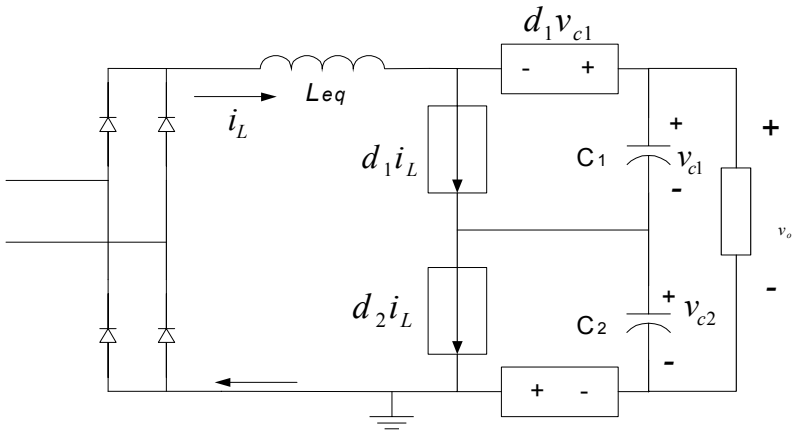


Figure 72 Average model of 3-LPFC at Rsoff mode.

Using the perturbation and linearization method, the small-signal model is derived.

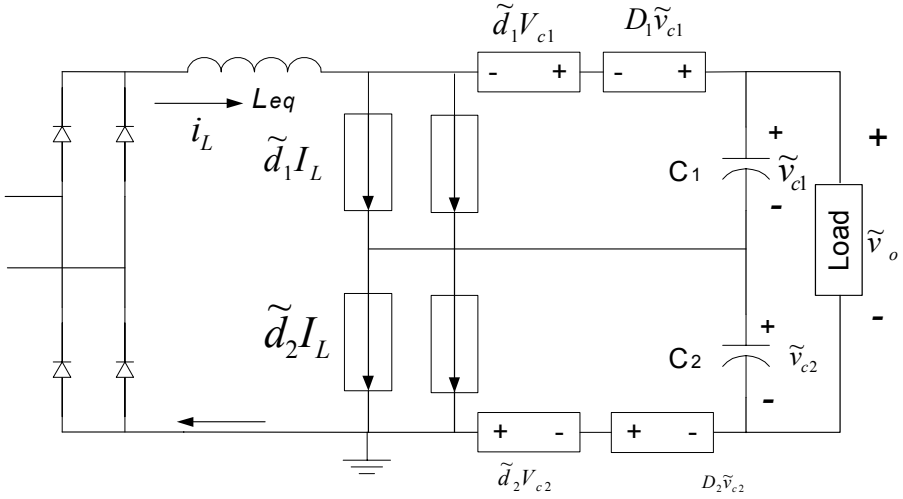


Figure 73 Small-signal model of 3-LPFC at Rsoff mode.

The state equations for the topology shown in Figure 73 are

$$\frac{d\tilde{x}}{dt}=\begin{bmatrix} 0 & -\frac{1-D_1}{L_{eq}} & -\frac{1-D_2}{L_{eq}} \\ \frac{1-D_1}{C_1} & -\frac{1}{C_1R} & -\frac{1}{C_1R} \\ \frac{1-D_2}{C_2} & -\frac{1}{C_2R} & -\frac{1}{C_2R} \end{bmatrix}\cdot\tilde{x}+\begin{bmatrix} \frac{1}{L_{eq}} & \frac{V_{c1}}{L} & \frac{V_{c2}}{L} \\ 0 & \frac{-I}{C_1} & 0 \\ 0 & 0 & -\frac{I}{C_2} \end{bmatrix}\cdot\begin{bmatrix} \tilde{v}_g \\ \tilde{d}_1 \\ \tilde{d}_2 \end{bmatrix}, \qquad \text{Eq. 4-1}$$

where D_1 is the steady state value of duty cycle d_1, D_2 is the steady state value of duty cycle d_2, and $\tilde{x}$ are the state variables for 3_LPFC circuit, $\tilde{x}=\begin{bmatrix} \tilde{i}_L \\ \tilde{v}_{c1} \\ \tilde{v}_{c2} \end{bmatrix}$.

To better understand the relationship, we define the average of two duty cycles as $\tilde{d}_s$:

$$\tilde{d}_s = \frac{\tilde{d}_1 + \tilde{d}_2}{2}. \qquad \text{Eq. 4-2}$$

Deviation of the two duty cycle as Δd yields:

$$\Delta\tilde{d} = \tilde{d}_1 - \tilde{d}_2. \qquad \text{Eq. 4-3}$$

From Equations 4-2 and 4-3, we find that:

$$\begin{bmatrix} \tilde{v}_g \\ \tilde{d}_1 \\ \tilde{d}_2 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & \frac{1}{2} \\ 0 & 1 & \frac{-1}{2} \end{bmatrix} \begin{bmatrix} \tilde{v}_g \\ \tilde{d}_s \\ \Delta\tilde{d} \end{bmatrix}. \qquad \text{Eq. 4-4}$$

Applying this transformation to Equation 4-1 yields:

$$\frac{d\tilde{x}}{dt} = \begin{bmatrix} 0 & -\frac{1-D_1}{L_{eq}} & -\frac{1-D_2}{L_{eq}} \\ \frac{1-D_1}{C_1} & -\frac{1}{C_1 R} & -\frac{1}{C_1 R} \\ \frac{1-D_2}{C_2} & -\frac{1}{C_2 R} & -\frac{1}{C_2 R} \end{bmatrix} \cdot \tilde{x} + \begin{bmatrix} \frac{1}{L_{eq}} & \frac{V_{c1}+V_{c2}}{L_{eq}} & \frac{V_{c1}-V_{c2}}{L_{eq}} \\ 0 & \frac{-I}{C_1} & \frac{-I}{2C_1} \\ 0 & \frac{-I}{C_2} & \frac{I}{2C_2} \end{bmatrix} \cdot \begin{bmatrix} \tilde{v}_g \\ \tilde{d}_s \\ \Delta\tilde{d} \end{bmatrix}. \qquad \text{Eq. 4-5}$$

The two most important transfer functions are derived from this state equation.

The $\tilde{d}_s$-to-$\tilde{i}_L$ transfer function is:

$$\frac{\tilde{i}_L}{\tilde{d}_s} = \frac{2(\frac{sRC_1C_2}{2(C_1+C_2)}+1)(V_{c1}+V_{c2})}{(1-D_s)^2 \cdot R \cdot \left[\frac{s^2 L_{eq} \frac{C_1 C_2}{C_1+C_2}}{(1-D_s)^s} + \frac{L_{eq}}{R(1-D_s)^2} + 1 \right]}. \qquad \text{Eq. 4-6}$$

Because D_1=D_2, the system is reduced to a second-order system. Equation 4-6 shows that $\widetilde{d}_s$-to-$\widetilde{i}_L$ transfer function is similar to duty-to-current transfer function for a single-switch PFC. The current compensator of a conventional single switch PFC can therefore be adopted.

The high frequency approximation can be expressed as:

$$\frac{\widetilde{i}_L}{\widetilde{d}_s} = \frac{V_{c1} + V_{c2}}{L_{eq} s}. \qquad \text{Eq. 4-7}$$

Because $L_{eq} = 4L$ and $V_{c1} + V_{c2} = V_o$, $\frac{\widetilde{i}_L}{\widetilde{d}_s} \approx \frac{V_o}{4Ls}$.

The $\Delta\widetilde{d}$-to-$(\widetilde{v}_{c1} - \widetilde{v}_{c2})$ transfer function is:

$$\frac{\widetilde{v}_{c1} - \widetilde{v}_{c2}}{\Delta\widetilde{d}} = \frac{-1}{2s} \cdot \frac{\frac{s(C_1 - C_2)\cdot(V_{c1} - V_{c2})}{1 - D_s} + 4I \cdot \left[\frac{s^2 L(C_1 + C_2)}{4(1 - D_s)^s} + \frac{Ls}{R(1 - D_s)^2} + 1 \right]}{(C_1 + C_2) \cdot \left[\frac{s^2 L \frac{C_1 C_2}{C_1 + C_2}}{(1 - D_s)^s} + \frac{Ls}{R(1 - D_s)^2} + 1 \right]}. \qquad \text{Eq. 4-8}$$

The low frequency approximation of the $\Delta\widetilde{d}$-to-$\widetilde{v}_{c1} - \widetilde{v}_{c2}$ transfer function is:

$$\frac{\widetilde{v}_{c1} - \widetilde{v}_{c2}}{\Delta\widetilde{d}} \approx \frac{-2}{s} \frac{I}{(C_1 + C_2)}, \text{for } f << \frac{1 - D_s}{\sqrt{L \frac{C_1 C_2}{C_1 + C_2}}} \qquad \text{Eq. 4-9}$$

An active balance loop can be formed based on this relationship.

One could raise the concern as to whether or not the deviation of duty cycle would affect the inductor current. Another transfer function is derived from Equation 4-5.

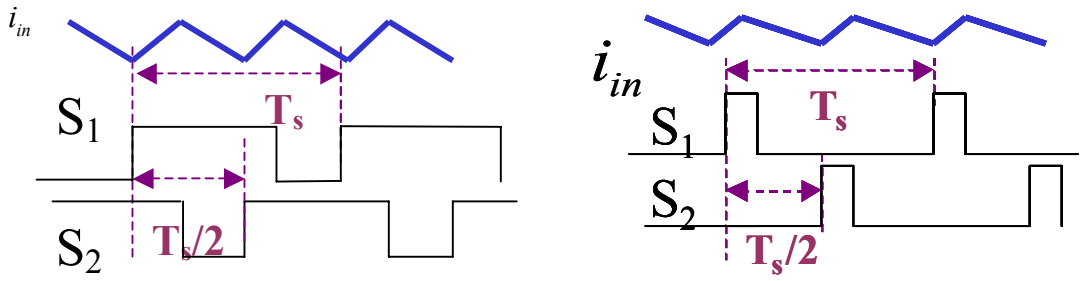
$\Delta\tilde{d}$ -to- $\tilde{i}_L$ transfer function is:

$$\frac{\tilde{i}_L}{\Delta\tilde{d}} = \frac{(sR\frac{C_1C_2}{C_1+C_2}+1)\cdot(V_{c1}-V_{c2})+\frac{1}{2}(V_{c1}+V_{c2})\frac{C_1-C_2}{C_1C_2}}{(1-D_s)^2\cdot R\cdot\left[\frac{s^2L\frac{C_1C_2}{C_1+C_2}}{(1-D_s)^s}+\frac{L}{R(1-D_s)^2}+1\right]} \quad \text{Eq. 4-10}$$

When 5% capacitors are used, we can say that $\frac{C_1-C_2}{C_1C_2}\approx 0$. If the output capacitors are well balanced, we can say that $V_{c1}-V_{c2}\approx 0$. Then, $\frac{\tilde{i}_L}{\Delta\tilde{d}}\approx 0$, which means that deviation of duty cycles does not affect the inductor current.

4.3.1.3 PWM Pattern

The voltage across the inductor $v_L = v_{in} - v_{am} - v_{mb}$, where v_{am} and v_{mb} are pulsating voltages with similar duty cycles. Inductor current is the integration of $v_{in} - v_{am} - v_{mb}$. To decrease the current ripple, interleaving technology is applied [39]. The switches are 180° phase-shifted (see Figure 74).



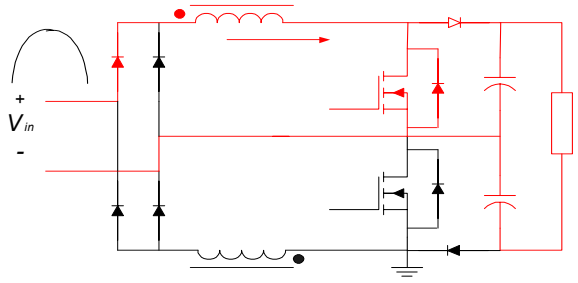
(a) (b)

Figure 74 PWM operation in Rsoff mode: (a) Duty cycle >50% and (b) Duty cycle <50%.

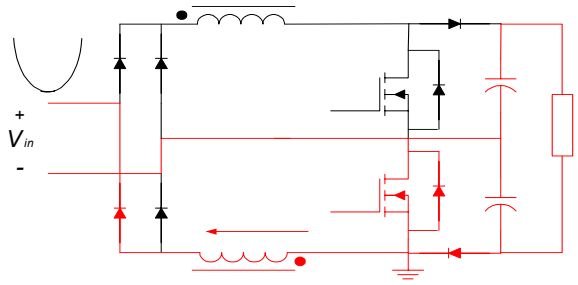
With the 180^o phase-shifted PWM, switching frequency can be reduced to half of the original one while maintaining very small current ripple amplitude. Lowering the switching frequency can increase efficiency.

4.3.2 Topology at Rson Mode

When the RS is turned on, we assume that $V_{c1} = V_{c2} = \frac{V_{out}}{2}$.



(a)



(b)

Figure 75 Operation of 3-LPFC at Rson mode: (a) Active parts at positive half cycle and (b) Active parts at negative half cycle.

Figure 75 shows that for each half cycle, only half of the circuit is active. For each half cycle, the equivalent circuit is shown in Figure 76. Applying the three-terminal averaging techniques, we can obtain the average model and derive the small-signal model (Figure 77).

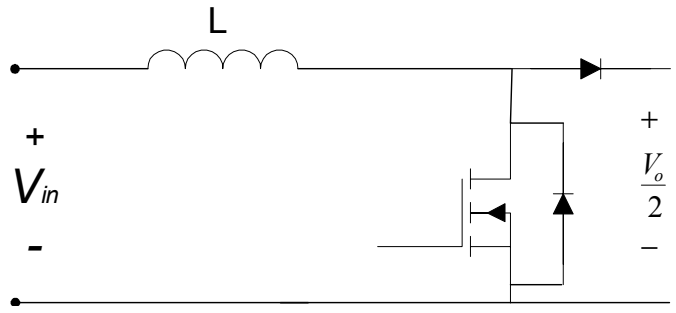


Figure 76 Equivalent high-frequency model 3-LPFC at Rson mode

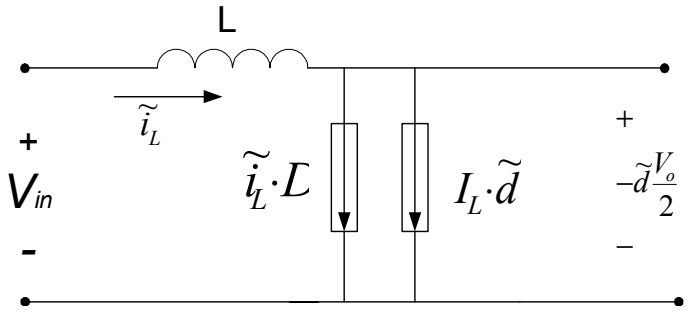


Figure 77 Small-signal model for Equivalent circuit at Rson mode

The high frequency approximation of duty-to-current transfer function is:

$$\frac{\tilde{i}_L}{\tilde{d}} = \frac{V_o}{2Ls}. \qquad \text{Eq. 4-11}$$

4.4 Control Parameters for Rsoff and Rson modes

The PWM patterns and switching frequency differ at Rsoff and Rson modes. As discussed in section 4.3 with the change of power stage topology, control parameters changes accordingly.

4.4.1 Current Loop Difference and Compensation

The duty-to-current transfer function in Rsoff mode is: $\frac{\tilde{i}}{\tilde{d}_s} = \frac{V_o}{4Ls}$.

The duty-to-current transfer function in Rson mode is: $\frac{\tilde{i}}{\tilde{d}} = \frac{V_o}{2Ls}$.

Two current sensors are installed in the 3-LPFC as shown in Figure 78. For the two modes, current sensor gain is different, as follows:

$$\frac{K_{iRsoff}}{K_{iRson}} = 2 . \qquad \text{Eq. 4-12}$$

We have $\frac{V_{out}}{4Ls} \cdot K_{iRsoff} = \frac{V_{out}}{2Ls} \cdot K_{iRson}$. The current compensator is the same for both Rsoff and Rson modes.

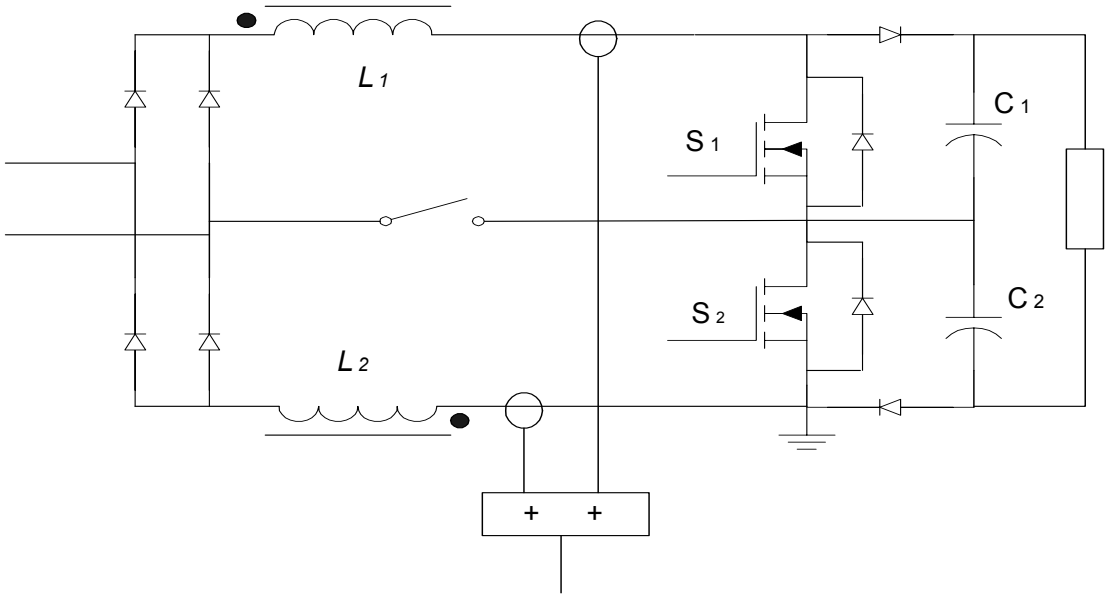


Figure 78 Current sensors for 3-LPFC with RS

4.4.2 Voltage Loop Difference and Compensation

In Chapter 3, we discussed the control-to-output voltage transfer function: $G_v = \frac{g_c}{Cs}$, where $g_c = k\frac{V_{in\_rms}^2}{V_{out}} = \frac{K_{in}K_m}{K_i V_{out} K_{ff}^2}$. As we discussed in 4.4.1, K_i is different for the two different mode, which results in different g_c, so

$$\frac{g_{cRsoff}}{g_{cRson}} = \frac{K_{iRson}}{K_{iRson}} = \frac{1}{2}, \qquad \text{Eq. 4-13}$$

where g_{cRsoff} is the value of g_c at Rsoff mode and g_{cRson} is the value of g_c at Rson mode.

The difference in voltage loop is compensated by software. When the converter is started, the initialization program sets up the control parameters accordingly.

4.5 Control structure of 3-LPFC Converter

Figure 79 shows the digital control structure of for 3-LPFC w/ RS. The structure includes three compensators and one low pass filter. The design method is the same with single switch PFC.

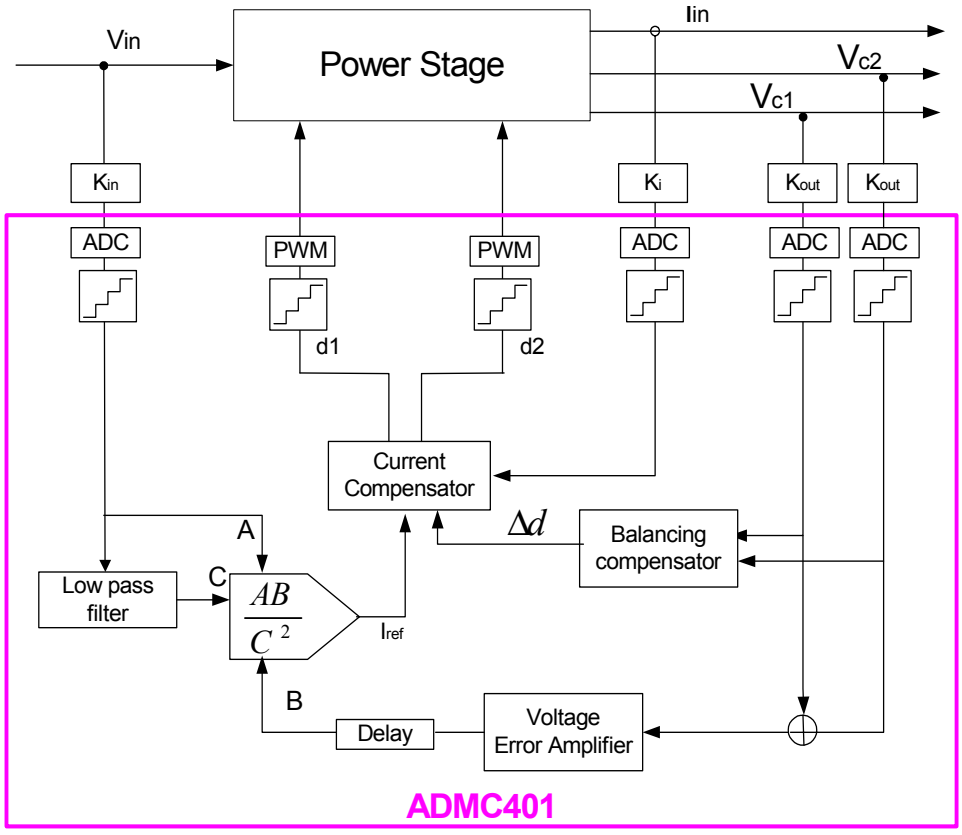


Figure 79 Digital Control structure for 3-LPFC with RS

4.6 Experimental Results

Figure 80 shows experimental results in Rsoff mode. Input power factor is over 99%. Middle point voltage is about half of output voltage, which means active balance is effective.

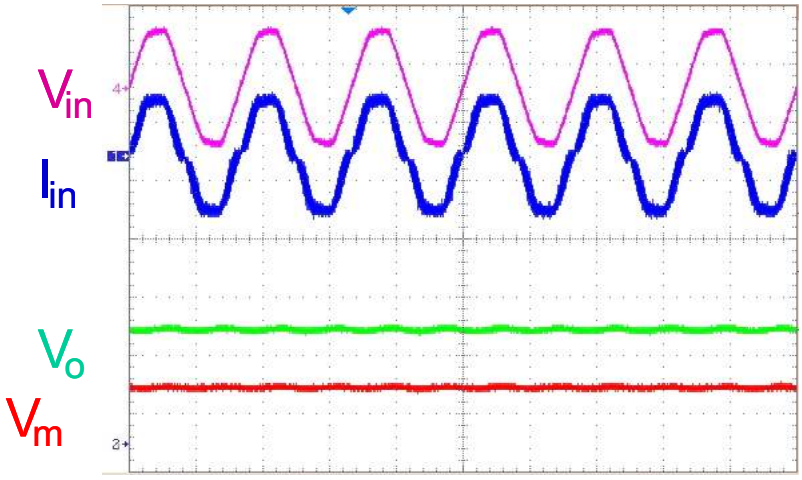


Figure 80 Input current (w/o EMI filter), input voltage, output voltage and midpoint voltage waveforms

Figure 81 shows the improved efficiency in Rsoff mode with digital control.

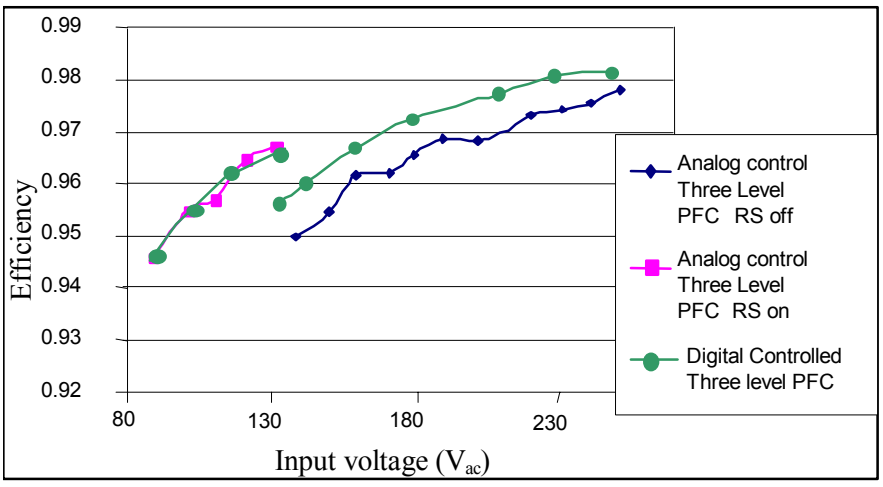


Figure 81 Efficiency comparison between analog controlled 3-LPFC and digital controlled 3-LPFC

5 CONCLUSION AND DISCUSSION

5.1 Conclusions

Digital control is the trend for tomorrow's DC power supply systems. Despite the merits of communication ability, noise immunity and capability to implement complex control methods. Digital control has its disadvantages. DPWM resolution and digital delay is the bottleneck in implementing digital control for PFC. It is necessary to know the requirement for ADC resolution, DPWM resolution and the system clock.

This thesis presents a generalized analysis of sampling frequency, DPWM resolution and ADC resolution requirements. The design experience and implementation of a digital controller for PFC are discussed. The experimental result is presented. Then, the effect of digital delay and how it influences the performance of PFC are studied. The CFF compensation method is proposed to improve PF with low current loop gain design. Simulation results are presented to prove the effectiveness of this solution.

Chapter 4 discusses optimal control for 3-LPFC with RS circuit. The PWM operation at Rsoff mode, and the difference in power stage model and control parameters are studied. Optimal controls for the two distinct modes are implemented using a digital controller.

Previous works show that analog control compromises performance in Rsoff mode. When analog control is applied, implementing optimal control requires much more extra analog components for 3-LPFC. Digital control implements optimal control without extra components. Experimental results demonstrate improved efficiency at Rsoff mode.

Although the passive balancing method can balance the output capacitor voltage, there are concerns as far as the underdesign of balance resistors. The active

balancing method is introduced. Studies in Chapter 4 show that changing the two switch duty cycles can not only influence inductor current but also change the output capacitor voltages. The frequency responses are derived in Chapter 4. The active balancing method is developed. Experimental results prove the effectiveness of the active balancing method.

5.2 Future Work

This thesis gives a general study of DPWM resolution. In reality, frequency and shape of the PWM error are related to input voltage, current reference and current loop gain and bandwidth. The exact effect of the PWM error may be tested in simulation or experiment. More accurate models may be established for study.

Digital delay is another factor for digital control. Currently, most digital control for PFC is realized by a DSP. The sequential execution of DSP is the main source of computation delay. Thus ASIC design is not only a low cost approach, but also helps to reduce digital delay and improve performance. However the huge amount of calculation required by PFC controller may result in a complex structure, which might require several adders and dividers. Mixed-signal design is also possible. Further research is required for cost effectiveness of digital control.

One of the goals of research in PFC is to achieve higher power density. One of the methods pushes switching frequency up to reduce the bulky boost inductor. Studies included in this thesis shows that pushing the switching frequency may increase the DPWM resolution requirements. Even with the promise of hybrid PWM and development of IC industry [32], this will remain the most challenging aspect for implementing digital control for DPS.

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APPENDIX I

Following are theorems we will use in this appendix.

A.1a Theorem. If $f(t)$ is integrable on $\{a \le t \le b\}$, and c is an intermediate point, then

$$\int_a^b f(t)dt = \int_a^c f(t)dt + \int_c^b f(t)dt \ .$$

A.1b Theorem. If $f(t)$ is integrable on $\{a \le t \le b\}$, and if c is a constant, then $cf(t)$ is integrable there and

$$\int_a^b cf(t)dt = c\int_a^b f(t)dt \ .$$

A.1c Theorem. If $f(t)$ and $g(t)$ are integrable on $\{a \le t \le b\}$, and if $f(t) \ge g(t)$ there, then

$$\int_a^b f(t)dt \ge \int_a^b g(t)dt \ .$$

A.1d Theorem. If $f(t)$ is integrable on $\{a \le t \le b\}$, then so is $|f(t)|$, and

$$\left|\int_a^b f(t)dt\right| \ge \int_a^b |f(t)|dt \ .$$

Before we proceed to the next conclusion, it is convenient to set up some notation. Given a function $f(t)$, we define the corresponding functions $f^+(t)$ and $f^-(t)$ by

$$f^+(t) = \begin{cases} f(t), & f(t) \ge 0 \\ 0, & f(t) < 0 \end{cases},$$

and

$$f^-(t)=\begin{cases}0, & f(t)\geq 0\\ -f(t), & f(t)<0\end{cases}.$$

Then, we have

$$f(t)=f^+(t)-f^-(t),$$

and

$$|f(t)|=f^+(t)+f^-(t).$$

Then, we have

$$\begin{aligned}\left|\int_a^b f(t)dt\right| &= \left|\int_a^b f^+(t)dt-\int_a^b f^-(t)dt\right| \\ &= \begin{cases}\int_a^b f^+(t)dt-\int_a^b f^-(t)dt, & \int_a^b f(t)dt\geq 0\\ \int_a^b f^-(t)dt-\int_a^b f^+(t)dt, & \int_a^b f(t)dt<0\end{cases},\end{aligned}$$

and

$$\int_a^b|f(t)|dt=\int_a^b f^+(t)dt+\int_a^b f^-(t)dt.$$

To have $\left|\int_a^b f(t)dt\right|=\int_a^b|f(t)|dt$, we have

$$\begin{aligned}&\int_a^b f^+(t)dt-\int_a^b f^-(t)dt=\int_a^b f^+(t)dt+\int_a^b f^-(t)dt, \quad \int_a^b f(t)dt\geq 0\\ &\Rightarrow\int_a^b f^-(t)dt=0\end{aligned}.$$

Because $f^-(t)\geq 0$, we have $f^-(t)=0, t\subset[a,b]$ which means $f(t)\geq 0, t\subset[a,b]$

Or, we have

$$\int_a^b f^-(t)dt - \int_a^b f^+(t)dt = \int_a^b f^+(t)dt + \int_a^b f^-(t)dt, \quad \int_a^b f(t)dt < 0$$
$$\Rightarrow \int_a^b f^+(t)dt = 0$$

.

Because $f^+(t) \geq 0$, we have $f^+(t) = 0, t \subset [a,b]$, which means $f(t) \leq 0, t \subset [a,b]$.

Assuming the periodic function is $f(t) = f(t+T)$, the amplitude of the waveform is M (M>0). Then we have $|f(t)| \leq M$. For any periodic function, we can have its Fourier series:

$$f(t) = \frac{C_0}{2} + \sum_{n=1}^{\infty} C_n \cos(n\omega t + \delta_n), \qquad \text{Eq. A1-1}$$

where $$C_1 = \frac{2}{T}\int_0^T f(t)\cos(\omega t + \delta_1)dt. \qquad \text{Eq. A1-2}$$

Function $f(t)\cos(\omega t + \delta_1)$ is periodic with a period of T so:

$$\begin{aligned} C_1 &= \frac{2}{T}\int_0^T f(t)\cos(\omega t + \delta_1)dt \\ &= \frac{2}{T}\int_{\frac{-T}{4}}^{\frac{3T}{4}} f(t - \frac{\delta_1}{\omega})\cos(\omega t)dt \end{aligned} \quad . \qquad \text{Eq. A1-3}$$

We have

$$|C_1| = \frac{2}{T}\left|\int_{\frac{-T}{4}}^{\frac{3T}{4}} f(t - \frac{\delta_1}{\omega})\cos(\omega t)dt\right|. \qquad \text{Eq. A1-4}$$

For $\left|\int_{\frac{-T}{4}}^{\frac{3T}{4}} f(t - \frac{\delta_1}{\omega})\cos(\omega t)dt\right|$, we have (see Theorem A1.c):

$$\left|\int_{\frac{-T}{4}}^{\frac{3T}{4}} f(t-\frac{\delta_1}{\omega})\cos(\omega t)dt\right| \le \int_{\frac{-T}{4}}^{\frac{3T}{4}}\left|f(t-\frac{\delta_1}{\omega})\cos(\omega t)\right|dt$$
$$= \int_{\frac{-T}{4}}^{\frac{3T}{4}}\left|f(t-\frac{\delta_1}{\omega})\right|\cdot\left|\cos(\omega t)\right|dt \quad . \qquad \text{Eq. A1-5}$$

Because $|f(t)| \le M$, $\left|f(t-\frac{\delta_1}{\omega})\right|\cdot|\cos(\omega t)| \le M|\cos(\omega t)|$.

With Equation A1-5, we have

$$\left|\int_{\frac{-T}{4}}^{\frac{3T}{4}} f(t-\frac{\delta_1}{\omega})\cos(\omega t)dt\right| \le \int_{\frac{-T}{4}}^{\frac{3T}{4}}\left|f(t-\frac{\delta_1}{\omega})\right|\cdot|\cos(\omega t)|dt$$
$$\le \int_{\frac{-T}{4}}^{\frac{3T}{4}} M\cdot|\cos(\omega t)|dt \quad . \qquad \text{Eq. A1-6}$$

With Eq. A1-6, we have

$$|C_1| \le \frac{2}{T}\left|\int_{\frac{-T}{4}}^{\frac{3T}{4}} f(t-\frac{\delta_1}{\omega})\cos(\omega t)dt\right|$$
$$\le \frac{2M}{T}\left|\int_{\frac{-T}{4}}^{\frac{3T}{4}}|\cos(\omega t)|dt\right| \quad . \qquad \text{Eq. A1-7}$$
$$= \frac{4M}{\pi}$$

For any periodic function $f(t)$, which has amplitude of M (M>0), the fundamental component amplitude is less than or equal to $\frac{4M}{\pi}$.

From Eq. A1-6, to have $\int_{\frac{-T}{4}}^{\frac{3T}{4}}\left|f(t-\frac{\delta_1}{\omega})\cos(\omega t)\right|dt = \int_{\frac{-T}{4}}^{\frac{3T}{4}} M\cdot|\cos(\omega t)|dt$, we must have $\left|f(t-\frac{\delta_1}{\omega})\right| = M$.

As we discussed before, to have $\left|\int_{\frac{-T}{4}}^{\frac{3T}{4}} f(t-\frac{\delta_1}{\omega})\cos(\omega t)dt\right| = \int_{\frac{-T}{4}}^{\frac{3T}{4}} \left|f(t-\frac{\delta_1}{\omega})\right| \cdot \left|\cos(\omega t)\right| dt$, we must have $f(t-\frac{\delta_1}{\omega})\cos(\omega t) \geq 0, t \subset [\frac{-T}{4}, \frac{3T}{4})$ or $f(t-\frac{\delta_1}{\omega})\cos(\omega t) \leq 0, t \subset [\frac{-T}{4}, \frac{3T}{4})$. We know $\begin{cases} \cos\ \omega t \geq 0, t \subset [\frac{-T}{4}, \frac{T}{4}) \\ \cos\ \omega t < 0, t \subset [\frac{T}{4}, \frac{3T}{4}) \end{cases}$.

If $f(t-\frac{\delta_1}{\omega})\cos(\omega t) \geq 0, t \subset [\frac{-T}{4}, \frac{3T}{4})$, then we have $\begin{cases} f(t-\frac{\delta_1}{\omega}) = M, & t \subset [\frac{-T}{4}, \frac{T}{4}) \\ f(t-\frac{\delta_1}{\omega}) = -M, & t \subset [\frac{T}{4}, \frac{3T}{4}) \end{cases}$. If $f(t-\frac{\delta_1}{\omega})\cos(\omega t) \leq 0, t \subset [\frac{-T}{4}, \frac{3T}{4})$, then we have $\begin{cases} f(t-\frac{\delta_1}{\omega}) = -M, & t \subset [\frac{-T}{4}, \frac{T}{4}) \\ f(t-\frac{\delta_1}{\omega}) = +M, & t \subset [\frac{T}{4}, \frac{3T}{4}) \end{cases}$. In both case, the periodic function results in a square waveform.

VITA

Manjing Xie was born on March 11, 1978, in Guangzhou, Guangdong, People's Republic of China. She received a B.S. degree in Electrical Engineering from Tsinghua University in 2001, in Beijing, P.R. China. In the fall of 2001, she entered the Center for Power Electronics System (CPES) at Virginia Tech to pursue her Master's degree. Her research interests include switch-mode power supplies and digital control for DC power supplies.