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Digital Control of a High Voltage (2.5 kV) Bidirectional DC-DC Flyback Converter for Driving a Capacitive Incremental Actuator

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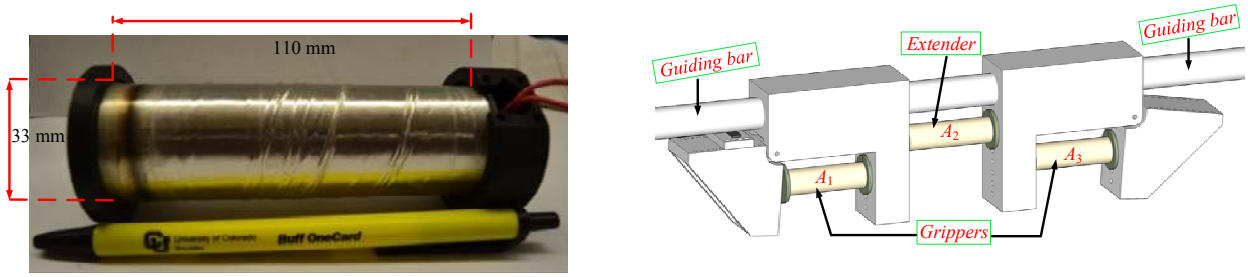
Abstract — **This paper presents a digital control technique to achieve valley switching in a bidirectional flyback converter used to drive a dielectric electro-active polymer based capacitive incremental actuator. The paper also provides the design of a low input voltage (24 V) and variable high output voltage (0-2.5 kV) bidirectional dc-dc flyback converter for driving a capacitive incremental actuator. The incremental actuator consists of three electrically isolated, mechanically connected capacitive actuators. It requires three high voltage (2-2.5 kV) bidirectional dc-dc converters, to accomplish the incremental motion by charging and discharging the capacitive actuators. The bidirectional flyback converter employs a digital controller to improve efficiency and charge/discharge speed using the valley switching technique during both charge and discharge processes, without the need to sense signals on the output high-voltage (HV) side. Experimental results verifying the bidirectional operation of a high voltage flyback converter are presented, using a 3 kV polypropylene film capacitor as the load. The energy loss distributions of the converter when 4 kV and 4.5 kV HV MOSFETs are used on HV side are presented. The flyback prototype with a 4 kV MOSFET demonstrated 89% charge energy efficiency to charge the capacitive load from 0 V to 2.5 kV, and 84% discharge energy efficiency to discharge it from 2.5 kV to 0 V, respectively.**

Index Terms — **switch-mode power converters, high voltage dc-dc converters, digital control, energy efficiency, actuator**

I. INTRODUCTION

Dielectric electro-active polymer (DEAP) is an evolving smart material that has experienced substantial development and has gained growing attention over the last decade [1]-[3]. DEAPs, when used as linear actuators, have the potential to be an effective replacement for many conventional (e.g., piezo, pneumatic and hydraulic) linear actuators because of their unique properties, including light weight, low noise operation, high flexibility, large strain, and autonomous capability. The DEAP actuator, shown in Fig. 1(a), is ideally equivalent to a pure capacitive load [4]. The DEAP incremental actuator concept, proposed in [5], consists of two grippers at both ends (to enable gripping operation) and an extender (to move the grippers), as shown in Fig. 1(b). These grippers connect with the extender using mechanical structures. The grippers A_1 and A_3 and the extender A_2 are similar to the DEAP actuator shown in Fig. 1(a). For moving the incremental actuator with a given speed and direction, the three DEAP actuators (which behave as electrically isolated capacitive loads) need to be driven with a specific sequence of signals. Details of the DEAP incremental actuator operation can be found in [5].



a) b)

Fig. 1. a) DEAP actuator; b) DEAP incremental actuator.

To drive a DEAP incremental actuator, high voltage (HV) bidirectional DC-DC converters are required. The typical driving voltage range is 2-2.5 kV, which is needed to generate sufficient mechanical force and displacement from each gripper and extender [5]. Bidirectional operation is needed for the converters, to discharge the high-voltage across the actuators, also to transfer a part of the energy stored in the actuators to the source. High voltage drivers for a DEAP incremental actuator can be implemented using a piezo or magnetic transformer based DC-DC converters. Piezoelectric transformer (PT) based high voltage (HV) unidirectional and bidirectional DC-DC converters for driving a capacitive DEAP actuator are implemented in [6] and [7], respectively. The bidirectional PT based converters suffers from the disadvantages of high design and control complexity, and low energy efficiency [7]. The magnetic transformer based flyback converter is suitable for high voltage (2.5 kV) and low power (< 150 W) DC-DC applications due to its simple structure and low component count [8]. High voltage unidirectional flyback converters for charging the capacitive loads have been implemented in [9], [10]. The flyback converter

proposed in [9] has split secondary HV windings, to reduce the transformer self-capacitance. The topology proposed in [9] cannot discharge the high-voltage across the capacitive actuator, and the high-voltage across the capacitive load in [10] was discharged through a resistor. The bidirectional flyback based DC-DC converter topologies are proposed in [11]-[13] to transfer the power in both directions. However, those topologies cannot be directly used for charging and discharging a capacitive load at high voltage (2.5 kV). A modified bidirectional flyback converter to drive a capacitive DEAP actuator is implemented in [14], which utilized the control IC LT3751 [15] to achieve the charge and discharge operations, with boundary conduction mode (BCM) and discontinuous conduction mode (DCM) control, respectively. In [14], the converter is not optimized in terms of power density or efficiency. The schematic of the HV bidirectional flyback converter is shown in Fig. 2. The output voltage and load current waveforms across the load for one charge and discharge cycle are provided in Fig. 3. In Fig. 3(a), T_{ch}, T_{delay} and T_{dch} are the charge time, delay between the charge and discharge processes, and discharge time, respectively. In Fig. 3(b), I_{ppkC}, I_{spkC}, I_{ppkD}, I_{spkD} are the primary and secondary peak currents during charge process, primary and secondary peak currents during during discharge process, respectively.

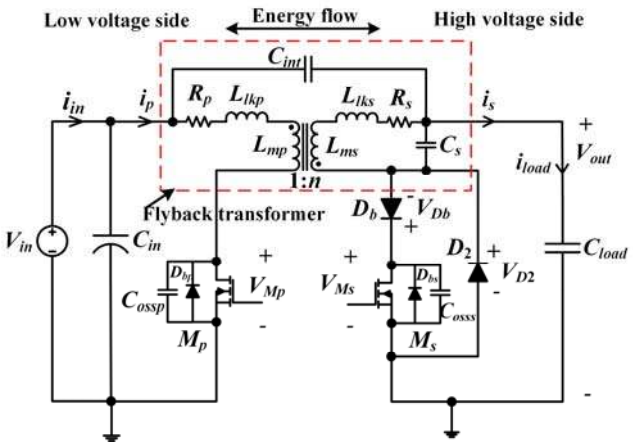


Fig. 2. Schematic of the high voltage bidirectional flyback converter for driving a capacitive load.

The flyback transformer is the most critical component in the HV flyback converter. Selecting a best transformer winding architecture (TWA) and optimizing the HV transformer using it, would lead to an improved energy efficiency. Several TWAs for HV capacitor charge and discharge applications, have been investigated and implemented in [16], with turns ratios 10 and 20, respectively. In [17] an efficiency optimization technique is proposed for a bidirectional flyback converter used to a drive a HV capacitor load. However, the discharge energy efficiency of the converter in [17] is lower compared to the charge energy efficiency, due to the capacitive switching losses during DCM operation. In the HV capacitor charging and discharging applications, even though the best transformer is designed, the capacitive switching losses due to the equivalent lumped

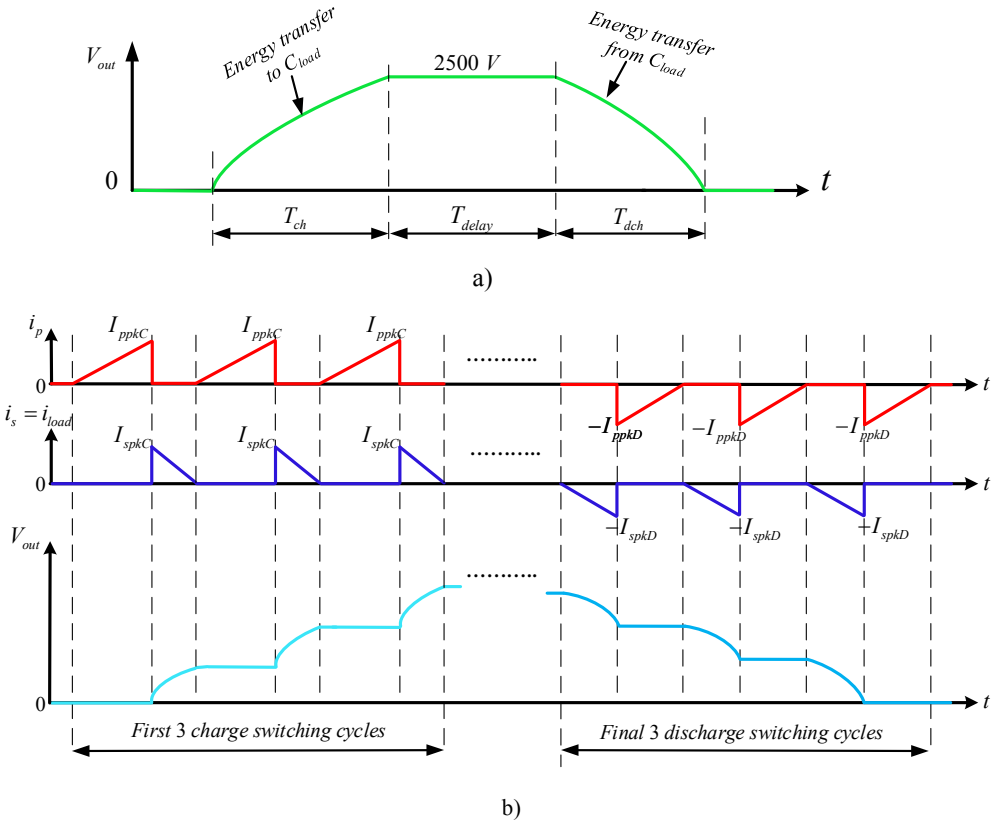


Fig. 3. Ideal switching waveforms of a HV bidirectional flyback converter operating in boundary conduction mode (BCM) during both charge and discharge modes, a) output voltage variation in the complete charge and discharge processes, b) Primary and secondary currents, and output voltage during charge and discharge processes.

capacitance [18] and [19], at the drain node of primary MOSFET during charge process, and at the drain node of secondary HV MOSFET during discharge process dominates the total losses in the converter, especially, when proper control scheme is not implemented.

Control algorithms for optimal-flyback charging of a capacitive load have been proposed in [20], which focuses mainly on minimizing the conduction losses in the converter. The soft switching in the flyback converter can be accomplished by operating the converter in the critical conduction mode, i.e., at the CCM/DCM boundary. The operation at the CCM/DCM boundary requires a variable-frequency control. Valley switching or quasi-resonant (QR) control has been used, to improve the efficiency of the switch-mode power supplies by reducing the capacitive turn-on/switching losses, also to reduce electromagnetic interference (EMI) problems. Efficiency and performance improvement control techniques, for flyback converters driving resistive loads have been widely investigated. An efficiency optimization technique has been proposed for a flyback converter in [18], which employs the valley switching control. Under lightload or high-input voltage condition, the

switching frequency of QR Flyback may be too high, which will cause high EMI noise and challenge the EMI filter design. The maximum switching frequency was limited by setting a minimum off-time for the switching period or for the switch turn off-time [21], [22].

Digital control techniques for flyback converters have been widely investigated. A digital primary-side sensing control technique is proposed in [23], for the output voltage/current regulation by employing an auxiliary winding. An adaptive blanking time control scheme to overcome the frequency hopping issue in a conventional QR control flyback converter with maximum frequency clamp is presented in [24]. Compared with conventional closed-loop control scheme with secondary-side feedback, the primary-side regulation (PSR) [25]–[27] can control both output voltage and output current without opto-coupler, which decreases design difficulty and production cost and minimizes PCB layout size. A digitally controlled soft valley change (SVC) technique is proposed in [28], to minimize the audible noise caused by a sudden change in switching frequency during valley change. It changes the turn-on instant among valleys gradationally during several switching cycles under any transient situation. To achieve a high efficiency flyback converter with minimized external components, a dynamic frequency selector (DFS) technique is proposed in [29], which dynamically chooses one suitable valley voltage in the resonance to extend the switching period. In addition, valley switching with valley skip (VS) control is developed to reduce the turn-on switching loss under the light load condition. An improved synchronous rectifier (SR) driving strategy focusing on the quasi-resonant primary-side regulation (QR-PSR) flyback converter, to prevent reverse energy flowing in light-load/standby mode is proposed in [30]. A primary side peak current measurement strategy (PCMS) for the high precision constant output current converter is proposed in [31]. However, for HV capacitor charge and discharge applications, due to the very high voltage (~2.5 kV) on the output HV side, the control schemes described above cannot be directly used to achieve the ZVS operation in both charge and discharge operations, without sensing HV signals.

Consequently, the approach followed in this paper is to reduce the capacitive switching losses by implementing the valley switching control without sensing HV side signals, for charging as well as discharging the capacitive load. The proposed valley switching technique [32] requires only sensing of the low voltage side voltages (input supply voltage and drain voltage of low-voltage MOSFET) without the need to sense any HV side signals. The discharge energy efficiency in [17] is not as high as charge energy efficiency due to the DCM control with fixed switching frequency during the discharge operation, which also increases the discharge time. The increased discharge time decreases the speed of incremental actuator.

The main objective of this paper is to implement the valley switching technique using a digital controller, during both charge and discharge operations, in order to improve efficiency and charge/discharge speed, as well as to reduce electromagnetic interference (EMI). Furthermore, another objective is to eliminate the need to sense any signal (voltage or

current) on the HV side. This paper is organized as follows: following the introduction, Section II describes the converter design considerations. Section III presents the theoretical analysis of the HV flyback converter in DCM, for achieving the valley switching during both charge and discharge modes. Section IV discusses the proposed valley switching control technique. Section V provides the experimental and energy loss distribution results, followed by the conclusions in Section VI.

II. Bidirectional DC-DC Flyback Converter Design Considerations

The converter design considerations [33] are discussed in this section. Specifications of the converter and power stage components used are provided in Tables I and II, respectively. For the primary low-voltage side a 250V MOSFET was selected. For the secondary HV side, the only available MOSFETs in the market are 4 kV and 4.5 kV from IXYS. A 5 kV HV diode from VMI has been selected as both freewheeling and blocking diodes.

TABLE I
SPECIFICATIONS OF BIDIRECTIONAL FLYBACK CONVERTER

Parameter	Value
Input voltage V_{in}	24 V
Output voltage V_{out}	0-2.5 kV ($V_{o,max}$=2.5 kV)
Capacitance of the load C_{load}	400 nF
On time of primary MOSFET during charge process t_{onC}	9 μs
Target charging time T_{ch}	50 ms

TABLE II
POWER STAGE COMPONENTS USED IN THE CONVERTER

Component	Value
Primary low-voltage MOSFET M_p	250V, 25A [IPD600N25N3 G]
Secondary HV MOSFET M_s	4.5 kV, 200 mA, 750 Ω [IXTA02N450HV] / 4 kV, 300 mA, 290 Ω [IXTV03N400S]
Secondary HV diode D_b / D_2	5 kV, 150 mA [SXF6525]

A. Choice of turns ratio of the flyback transformer

For the capacitor charging application, the turns ratio n is selected ~~based~~ depending on the required maximum charging voltage of the capacitive load $V_{o,max}$. The typical voltage stress waveforms across primary MOSFET M_p, secondary HV MOSFET M_s, and HV diode D_2 are shown in Figs. ~~3(a), 3(b) and 3(c)~~, 4(a), 4(b) and 4(c), respectively.

1) Charge process: The maximum and minimum turns ratios, from secondary to primary of the flyback transformer during charge process can be calculated to meet the devices breakdown voltage constraints.

The voltage stress across the primary MOSFET M_p when turned off, should be less than its breakdown voltage V_{BVM1} (Fig. ~~3(a)~~ 4(a)), so

$$\left[V_{in} + \frac{\left[V_{o,max} + V_{onD2} \right]}{n} + V_{leakP} \right] < \beta_{M1} V_{BVM1} \tag{1}$$

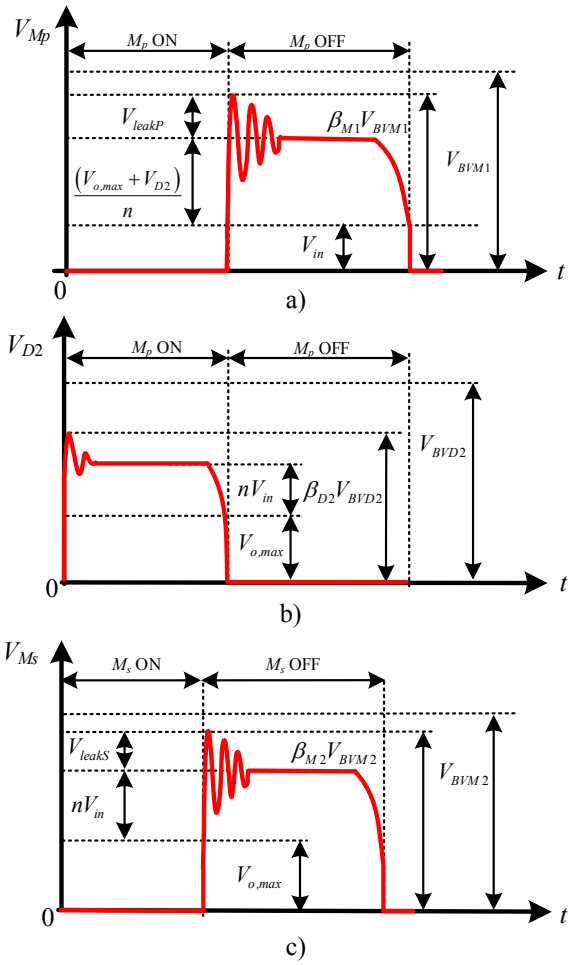
where V_{in} and V_{onD2} are the input voltage and voltage drop of HV diode D_2, respectively, V_{leakP} is the increase in the drain voltage of primary MOSFET due to the leakage inductance L_{lkP}, and β_{M1} is the margin factor (< 1) for primary MOSFET breakdown voltage V_{BVM1}.

From (1), the transformer turns ratio

$$n > n_{min} \tag{2}$$

where n_{min} is the minimum turns ratio needed, to charge the capacitive load to $V_{o,max}$ and is given by

$$n_{min} = \frac{\left[V_{o,max} + V_{onD2} \right]}{\left[\left(\beta_{M1} V_{BVM1} \right) - V_{in} - V_{leakP} \right]} \tag{3}$$



~~Fig. 3~~. Fig. 4. Voltage stress when target output voltage ($V_{o,max}$) is reached across, a) M_p during charge process (BCM), b) D_2 during charge process (BCM), c) M_s during discharge process (BCM); BCM: Boundary Conduction Mode.

For the given input specifications provided in Table I, by choosing V_{leakP}=70 V (this design value can be changed depending on the ~~possible~~ estimated value of the leakage inductance referred to primary L_{lkP}), and choosing a margin factor of β_{M1}=0.9 for a 250 V primary MOSFET (see Table II), with a ~~high voltage~~ HV diode drop of V_{onD2}=7 V, the minimum turns ratio becomes n_{min}=20.

The voltage stress across the ~~high voltage~~ HV diode D_2 when M_p is turned on should be less than its breakdown voltage V_{BVD2} (Fig. ~~3(b)~~ 4(b)), so

$$\left[V_{o,max} + nV_{in}\right] < \beta_{D2} V_{BVD2} \tag{4}$$

where β_{D2} is the margin factor for HV diode breakdown voltage V_{BVD2}.

From (4), the transformer turns ratio

$$n < n_{maxC} \tag{5}$$

where n_{maxC} is the maximum turns ratio needed for the charge process, and is given by

$$n_{maxC} = \left\lfloor \frac{\beta_{D2} V_{BVD2} - V_{o,max}}{V_{in}} \right\rfloor \tag{6}$$

By choosing a margin factor of β_{D2}=0.8 for a 5 kV HV diode D_2, the maximum turns ratio becomes n_{maxC}=62.

2) Discharge process: The maximum allowable turns ratio of the flyback transformer during discharge process can be calculated from the breakdown voltage of the secondary MOSFET M_s. The voltage stress across M_s when turned off should be less than its breakdown voltage V_{BVM2} (Fig. ~~3(c)~~ 4(c)), so

$$\left[V_{o,max} + nV_{in} + V_{leakS}\right] < \beta_{M2} V_{BVM2} \tag{7}$$

where V_{leakS} is the increase in the drain voltage of HV MOSFET due to the leakage inductance L_{lkS} and β_{M2} is the margin factor for secondary MOSFET breakdown voltage V_{BVM2}.

From (7), the transformer turns ratio

$$n < n_{maxD} \tag{8}$$

where n_{maxD} is the maximum turns ratio needed for the discharge process, and is given by

$$n_{maxD} = \left\lfloor \frac{\beta_{M2} V_{BVM2} - V_{o,max} - V_{leakS}}{V_{in}} \right\rfloor \tag{9}$$

By choosing V_{leakS}=650 V, and for a margin factor of β_{M2}=0.95, the maximum turns ratios become 47 and 27 for 4.5 kV and 4 kV MOSFETs, respectively.

From (2), (5) and (8) the transformer turns ratio n must satisfy:

$$n \Rightarrow \begin{cases} n_{min} < n < n_{maxC}, \text{ if } V_{BVD2} < V_{BVM2} \\ n_{min} < n < n_{maxD}, \text{ if } V_{BVD2} > V_{BVM2} \end{cases} \tag{10}$$

From the power stage components shown in Table II, $V_{BVM2}<V_{BVD2}$, hence the turns ratio n should satisfy $20<n<47$, for a 4.5 kV HV MOSFET, and $20<n<27$, for a 4 kV HV MOSFET, respectively. The turns ratio n for the practical implementation is selected as 25. Nevertheless, the designer for this application, can choose a different turns ratio by satisfying (10).

B. Selection of peak currents during charge and discharge processes

1) Charge process: The expression for primary peak current I_{ppkC} to charge the HV capacitive load from 0 V to $V_{o,max}$ in time T_{ch} is ~~[8], [10]~~ [15], [20]

$$I_{ppkC} = \frac{\left(2nV_{in} + V_{o,max}\right) C_{load} V_{o,max}}{\eta V_{in} \left(T_{ch} - T_{delay}\right)} \tag{11}$$

where C_{load} is the capacitance of the load or actuator, η is the power efficiency of the converter, and T_{ch} and T_{delay} are the charge time to reach the target output voltage and total propagation delay time in the whole charge process, respectively.

For the given input specifications, for a turns ratio of n=25, by choosing a power efficiency η=0.8, and for a chosen delay time of T_{delay}=5 ms, the approximate value of primary peak current is I_{ppkC}=4.28 A.

The expression for maximum secondary peak current $I_{spkC,max}$ to charge the HV capacitive load through HV diode D_2, when the converter is operating in BCM is

$$I_{spkC,max} < \frac{2I_{D2}}{\left(1 - D_{onC,min}\right)} < \frac{2I_{D2}}{D_{offC,max}} \tag{12}$$

where I_{D2}, $D_{onC,min}$ and $D_{offC,max}$ are the rated average current of HV diode D_2, minimum on-time duty cycle of M_p and maximum off-time duty cycle of M_p, respectively.

Equation (12) is derived based on the average current expression across HV diode D_2 during the charge process. The maximum secondary peak charging current, when a 5 kV HV diode, with a rated current of I_{D2}=150 mA is used, and for a maximum off-duty cycle during charge process of $D_{offC,max}$=0.9 is $I_{spkC,max}$=333 mA. This corresponds to a maximum primary peak charging current of 8.3 A, for n=25.

2) Discharge process: During the discharge process, since the output voltage decreases in each switching cycle, to discharge the load with constant peak current I_{spkD}, the on-time of HV MOSFET t_{onD} should increase in each switching cycle. The expression for maximum secondary peak current $I_{spkD,max}$, to discharge the HV capacitive load, through the series combination of ~~high voltage~~ HV blocking diode D_b and ~~high voltage~~ HV MOSFET M_s (see Fig. 2) is

$$I_{spkD,max} < \frac{2I_{sD}}{D_{onD,max}} \tag{13}$$

where $D_{onD,max}$ is the maximum on-time duty cycle of M_s, and I_{sD} is the average current in the secondary HV side during discharge process, and is given by:

$$I_{sD} = \begin{cases} I_{Db}, \text{ if } I_{Db} < I_{Ms} \\ I_{Ms}, \text{ if } I_{Db} > I_{Ms} \end{cases} \tag{14}$$

where I_{Db} and I_{Ms} are the rated average current of HV diode D_b and MOSFET M_s, respectively. Since average current of D_b is less than that of M_s, i.e., $I_{Db}<I_{Ms}$ (see Table II), the average current in the secondary side $I_{sD}=I_{Db.}$ The maximum secondary peak discharging current, for a maximum discharge on-time duty cycle $D_{onD,max}$=0.8 is $I_{spkD,max}$=375 mA. This corresponds to a maximum primary peak discharging current of 9.37 A, for n=25. From (12)-(14), the secondary peak discharge current should be less than 333 mA. The peak secondary current during discharge process is selected as I_{spkD}=170 mA, the value is equal to $\frac{I_{ppkC}}{n}$.

C. Design of primary and secondary turns

The design methodologies for transformers and coupled inductors used in conventional switch-mode power supplies are well documented ~~[9], [25] [27]~~ [8], [34]-[36]. In the HV bidirectional flyback converter, the primary and secondary turns are selected to avoid the saturation of the core during both charge and discharge modes. The converter operates with valley switching/BCM control during both charge and discharge processes ~~[23]~~ [32].

1) Charge process: The number of primary turns N_p needed during charge process is

$$N_p = \frac{V_{in}\ t_{onC}}{B_{maxC} A_c} \tag{15}$$

where t_{onC} is the on-time during the charge mode, B_{maxC} and A_c are the maximum flux density during charge process and the area of cross-section of the magnetic core, respectively.

The number of secondary turns needed during charge operation is

$$N_{sC} = N_p n \tag{16}$$

By choosing a PQ 20/20 core with A_c=62 mm^2, for a maximum flux density of B_{maxC}=0.3 T, and for the specifications shown in Table I, the primary and the secondary turns become N_p=12 and N_{sC}=300.

2) Discharge process: The number of secondary turns needed during discharge process is

$$N_{sD} = \frac{V_{outD}\ t_{onD}}{B_{max\,D} A_c} = \frac{n\left(V_{in} + \Delta V_{inD}\right) t_{offD}}{B_{max\,D} A_c} \tag{17}$$

where t_{onD} and t_{offD} are the on-time and off-time of M_s during the discharge mode, respectively, and B_{maxD} is the maximum flux density of the core during discharge process, respectively.

The same secondary turns ($N_s = N_{sC} = N_{sD}$) should meet both (16) and (17). The input capacitance of C_{in}=30 mF is chosen, such that the input voltage increment during the discharge process ΔV_{inD} <2 V.

D. Design of primary magnetizing inductance

1) Charge process: When the converter operates in BCM during charge process, selecting fixed on-time t_{onC} ensures constant peak current. In this case, the duty cycle and the switching frequency are maximum at the final switching cycle (where the output voltage is close to the maximum target output voltage ($V_{o,max}$)), and minimum in the first switching cycle (where the output voltage is minimum or 0 V). The expression for the primary magnetizing inductance L_{mpC} needed during charge process is

$$L_{mpC} = \frac{V_{in} t_{onC}}{I_{ppkC}} \tag{18}$$

For V_{in}=24 V, t_{onC}=9 μs, and I_{ppkC}=4.28 A, the primary magnetizing inductance becomes L_{mpC}=50.5 μH.

2) Discharge process: When the converter operates in BCM during discharge process, selecting variable on-time t_{onD} (as the output voltage decreases) ensures constant peak current. In this case, the duty cycle and the switching frequency are maximum at the first switching cycle (where the output voltage is close to the maximum target output voltage ($V_{o,max}$)), and minimum in the final switching cycle (where the output voltage is close to minimum discharge voltage or 0 V). When the capacitive load transfers the energy back to the source, the input voltage slightly increases by ΔV_{inD}. The magnitude of ΔV_{inD} depends on the value of the input capacitance C_{in} used. The expression for the primary magnetizing inductance L_{mpD} during discharge process is

$$L_{mpD} = \frac{\left(V_{in} + \Delta V_{inD}\right) t_{offD}}{I_{ppkD}} \tag{19}$$

The same primary magnetizing inductance ($L_{mp} = L_{mpC} = L_{mpD}$) should meet both (18) and (19).

From (15)-(19), it can be concluded that, if the number of secondary turns $N_s = N_{sC} = N_{sD}$ and the magnetizing inductance $L_{mp} = L_{mpC} = L_{mpD}$ then, the peak discharge flux density B_{maxD} interms of peak charge flux density B_{maxC} is given by

$$B_{max\,D} = \frac{I_{ppkD}}{I_{ppkC}} B_{max\,C} = \frac{nI_{spkD}}{I_{ppkC}} B_{max\,C} \tag{20}$$

The secondary discharge peak current I_{spkD} in any switching cycle limits the peak flux density B_{maxD} during the discharge process. Hence, from (20) suppose if a secondary discharge peak current of I_{spkD}=200 mA is chosen, then the flux density during discharge process becomes (for n=25, I_{ppkC}=4.28 A, B_{maxC}=0.3 T) B_{maxD}=0.35 T. Hence, the secondary discharge peak current I_{spkD} value needs be selected to avoid the core saturation during the discharging process.

E. HV flyback transformer winding design

The flyback transformer is designed using an automatic winding layout (AWL) technique proposed in [17], to minimize mainly the total energy loss due to the transformer paracitics. The parameters of the designed HV transformer measured using the impedance analyzer are provided in Table III. The proper insulation between the low-voltage (primary) and high-voltage (secondary) windings is achieved by using a triple insulated (TEX-E) [37] solid wire for primary winding. Due to large number of secondary turns, single insulated wire is used for secondary winding. The 300 secondary turns are wounded with 4 secondary layers and the 12 primary turns are wounded in a single primary layer. The self-capacitance of the HV winding has been significantly reduced by providing an insulation layer (using Kapton tape) between the secondary layers. Figure 5 shows the practical implementation of the flyback transformer. The secondary turns are wounded on the bobbin first, followed by the primary. The Z-type winding scheme [36] is implemented for the secondary layers, which further reduces the self-capacitance. The calculated core and winding losses of the transformer as a function of the output voltage are shown in Fig. 6, and the temperature rise of flyback transformer with PQ 20/20 core, which has a thermal resistance of 18 ºC/W is shown in Fig. 7. The temperature rise distribution as a function of output voltage justifies the chosen PQ 20/20 core.

TABLE III
PRACTICAL FLYBACK TRANSFORMER PARAMETERS

Parameter	Value
Core used / material used	PQ 20/20 / P type
Primary N_p / secondary turns N_s	12 / 300
Primary L_{mp} / secondary magnetizing inductance L_{ms}	47.5 μH / 30 mH
Leakage inductance referred to primary L_{lkp} / secondary L_{lks}	990 nH / 620 μH
Self-capacitance of secondary winding C_s	6 pF
Diameter of primary / secondary winding	0.5 mm (TEX-E) / 0.11 mm
DC resistance of primary R_p / secondary R_s	62 mΩ / 14 Ω
Number of layers of transformer primary / secondary	1 / 4
Thickness of insulation between secondary layers $d_{\text{insulation}}$	0.9 mm

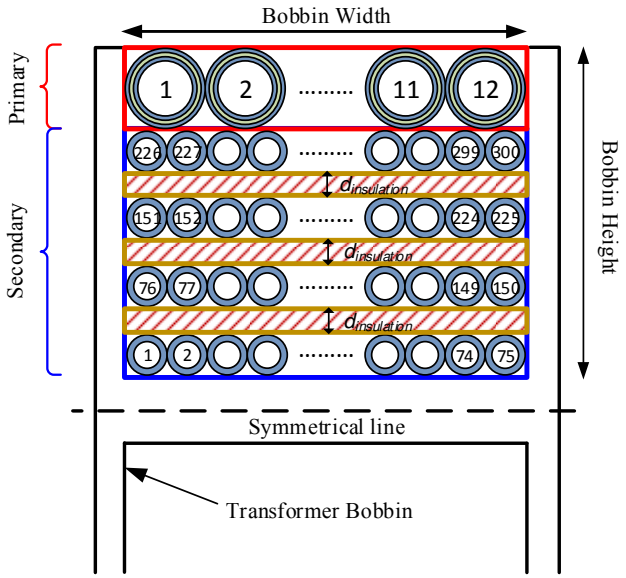


Fig. 5. Practical HV transformer implementation.

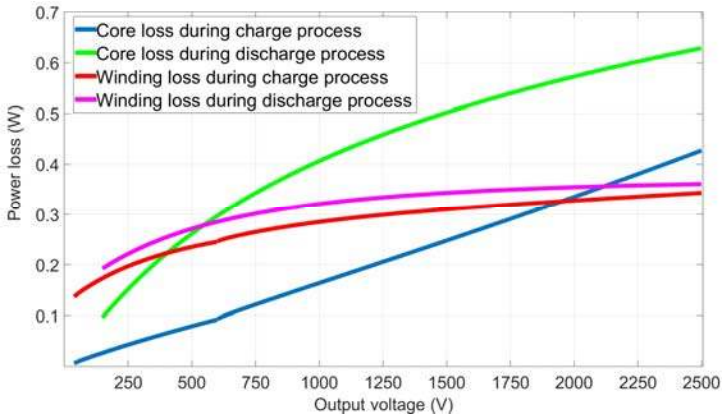


Fig. 6. Estimated core and winding losses during charge and discharge modes.

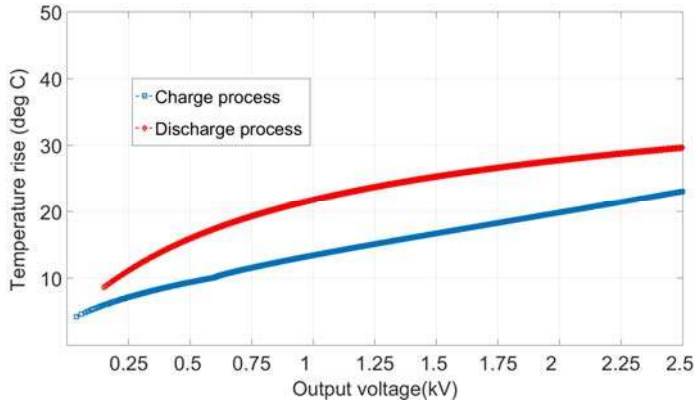


Fig. 7. Temperature rise in the transformer with PQ 20/20 core during charge and discharge modes.

III. QUASI RESONANT (QR) / VALLEY SWITCHING CONTROL

The schematic of the HV bidirectional flyback converter for charging and discharging a capacitive actuator/load is shown in Fig. 2. This section provides the theoretical analysis for detectecting the valley points in the drain voltage of low-voltage and high-voltage MOSFETs, in a bidirectional flyback converter. The assumption made in the analysis is that the load capacitance C_{load} is much greater than the self-capacitance C_s of the transformer (C_{load}>>C_s).

A. ~~Analysis~~ Valley switching during charge process

1) Analysis

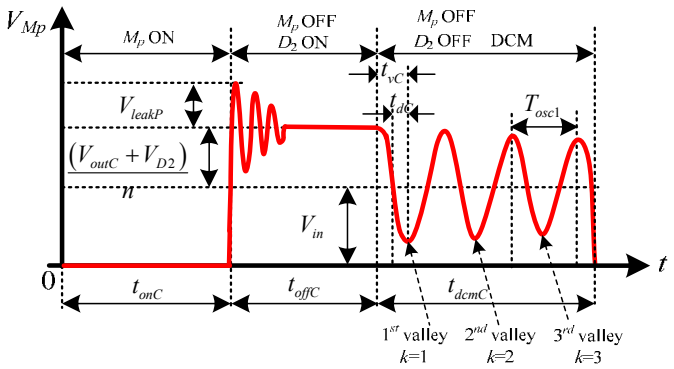
~~Figure 4~~ Figure 8 shows the drain-to-source voltage of the primary MOSFET M_p during charge process, when the converter operates in DCM. The drain to source voltage V_{Mp} when the output voltage during charge process V_{outC} is less than nV_{in}, i.e., V_{outC}<nV_{in} in DCM is given by ~~[22]~~ [19]

$$V_{Mp}(t) = V_{in} + \left[\frac{V_{outC} + V_{onD2}}{n}\right] \cdot e^{-\left[\frac{R_p}{2(L_{mp}+L_{lkp})}\right]t} \cos(w_{r1}t) \tag{21}$$

where V_{outC} is the output voltage during the charge process at a given switching cycle, V_{onD2} is the on-state voltage drop of 5 kV diode D_2, R_p and L_{lkp} are the primary DC resistance and leakage inductance referred to primary, respectively. V_{leakP} is the voltage increment in drain-to-source voltage of M_p due to leakage inductance referred to primary L_{lkp} and is given by $V_{leakP} \approx I_{ppk}\sqrt{\frac{L_{lkp}}{C_{lumpP}}}$.

The ringing frequency f_{r1} (or the oscillation period T_{osc1}) in DCM is given by

$$f_{r1} = \frac{w_{r1}}{2\pi} = \frac{1}{2\pi\sqrt{(L_{mp}+L_{lkp})C_{lumpP}}} = \frac{1}{T_{osc1}} \tag{22}$$



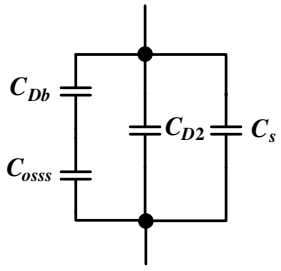
~~Fig. 4.~~ Fig. 8. Voltage across low voltage MOSFET M_p in DCM, during charge process when V_{outC}<nV_{in}.

where R_p and L_{lkp} are the primary DC resistance and leakage inductance referred to primary, respectively. In Fig. 8, t_{onC}, t_{offC}, t_{dcmC}, t_{vC}, and t_{dC} are the on-time, off-time of M_p, total DCM time duration, time to reach the valley point in the drain voltage from the instant when M_p is switched-off, and delay time needed to reach the valley point, from the instant when V_{Mp}=V_{in}, respectively.

From ~~Fig. 5~~ Fig. 9, the lumped capacitance C_{lumpP} in terms of different capacitances in the converter is given by

$$C_{lumpP} = C_{ossp} + n^2\left(C_s + C_{D2} + \frac{C_{Db}C_{osss}}{C_{Db} + C_{osss}}\right) \tag{23}$$

where C_{ossp}, C_{osss}, C_{D2}, and C_{Db}, are the output capacitances of MOSFETs M_p and M_s, junction capacitance of HV diodes D_2 and D_b, respectively.



~~Fig. 5.~~ Fig. 9. Equivalent circuit on the secondary HV side to calculate the lumped capacitance referred to primary or secondary.

The output capacitance of the primary MOSFET as a function of its drain-to-source voltage V_{Mp} is given by

$$C_{ossp}\left(V_{Mp}\right) \approx C_{Mp0}\sqrt{\frac{V_{Mp0}}{V_{Mp}}} \tag{24}$$

where C_{Mp0} is the MOSFET output capacitance when V_{Mp}=V_{Mp0}. For 250 V MOSFET, C_{Mp0}=101 pF at V_{Mp0}=100 V.

Similarly, the output capacitance of the secondary HV MOSFET as a function of its drain-to-source voltage V_{Ms} is given by

$$C_{osss}\left(V_{Ms}\right) \approx C_{Ms0}\sqrt{\frac{V_{Ms0}}{V_{Ms}}} \tag{25}$$

where C_{Ms0} is the MOSFET output capacitance for V_{Ms}=V_{Ms0}. For both 4 kV and 4.5 kV MOSFETs, C_{Ms0}=19 pF at V_{Ms0}=25 V.

If the controller employs valley switching in DCM, the switching-node voltage V_{Mp} at k^{th} valley point is given by

$$V_{Mp}\big|_k = V_{in} - \left[\frac{V_{outC} + V_{onD2}}{n}\right] \cdot e^{-\left[\frac{R_p}{2\left(L_{mp}+L_{lkp}\right)}(2k-1)\frac{T_{osc1}}{2}\right]} \tag{26}$$

The maximum number of valley points in the drain-voltage, in terms of DCM period t_{dcmC} is given by ~~[13]~~ [18]

$$k_{max} = round\left(\frac{t_{dcmC}}{T_{osc1}}\right) \tag{27}$$

The switching frequency at k^{th} valley point when the controller employs valley switching in DCM during charge process, is given by

$$f_{swC}\big|_k = \frac{1}{t_{onC} + t_{offC} + (2k-1)\frac{T_{osc1}}{2}} = \frac{1}{\frac{L_{mp} I_{ppkC}}{V_{in}} + \frac{L_{mp} I_{ppkC} \cdot n}{V_{outC}} + (2k-1)\frac{T_{osc1}}{2}} \tag{28}$$

At the end of each switching period, the energy stored in the non-linear lumped capacitance C_{lumpP} is dissipated when the MOSFET M_p is turned on ~~[17], [22]~~ [18], [19]. This paper considers achieving valley switching for M_p and M_s at first valley point. However, it is possible to optimize the switching loss in the converter by switching at other valley points. The switching loss P_{swC} due the lumped capacitance at the drain node, when the converter employs the valley switching at the first valley point (k=1) is

$$P_{swC}\big|_{k=1} = \frac{1}{2} C_{lumpP} \left[V_{Mp}\big|_{k=1} \right]^2 \left[f_{swC}\big|_{k=1} \right] \tag{29}$$

~~Table III~~ Table IV provides the comparison of different operating modes such as, continuous conduction mode (CCM), DCM without valley switching, and DCM with valley switching, during charge process, in terms of switching frequency and drain-to-source voltage. When $V_{outC} > nV_{in}$ zero voltage switching (ZVS) of M_p occurs, and there is no energy loss due to the lumped capacitance, hence ~~(27)~~ (29) is equal to 0 W.

~~TABLE III~~ TABLE IV
COMPARISON OF DIFFERENT OPERATING MODES IN A FLYBACK CONVERTER DURING CHARGE PROCESS

Operating Mode	**Switching frequency during charge process f_{swC}**	**Drain-to-source voltage of M_p (V_{Mp}) at the beginning of next switching cycle during charge process**
CCM	$\frac{1}{\left[t_{onC} + t_{offC} \right]}$	$V_{in} + \frac{V_{TC}}{n}$, where $V_{TC} = V_{outC} + V_{onD2}$
DCM (without valley switching)	$\frac{1}{\left[t_{onC} + t_{offC} + t_{dcmC} \right]}$	$V_{in} + \frac{V_{TC}}{n} \cdot e^{-\Delta_1} \cos(w_{r1} t_{dcmC})$ where $\Delta_1 = \left[\frac{R_p}{2L_{Tp}} t_{dcmC} \right]$ and $L_{Tp} = L_{mp} + L_{lkp}$
DCM (with valley switching at k^{th} valley point)	$\frac{1}{\left[t_{onC} + t_{offC} + (2k-1)\frac{T_{osc1}}{2} \right]}$	$\begin{cases} V_{in} - \frac{V_{TC}}{n} e^{-\Delta_2}, \text{ if } V_{outC} < nV_{in} \\ 0 \Rightarrow \text{ZVS}, \text{ if } V_{outC} > nV_{in} \end{cases}$ where $\Delta_2 = \left[\frac{R_p}{2L_{Tp}} (2k-1) \frac{T_{osc1}}{2} \right]$

2) An example to calculate the capacitive switching loss at a given charging voltage

Table V provides the calculated switching losses in different operating modes. The following specifications are used to calculate the switching losses during the charge mode: V_{in}=24 V, C_{lumpP}=9 nF, V_{onD2}=7 V, n=25, L_{mp}=50 µH, I_{ppkC}=4.28 A, R_p=60 mΩ, f_{r1}=240 kHz. In CCM operation, as the output voltage increases, the switching loss increases. Since the on-time is fixed, the switching frequency also increases (from 33 kHz to 90 kHz) with output voltage. When the converter operates in DCM without valley switching, the switching loss increases, as the converter charges the load to high-voltage. However, the loss magnitude in DCM is less compared to that during CCM operation. Two cases are shown for DCM, one with t_{dcmC}=10 µs and the other with t_{dcmC}=50 µs. In the first case, the switching frequency increases from 24 kHz to 47 kHz, and in the second case, the switching frequency increases only from 12 kHz to 16 kHz. Therefore, the swithing loss for the second case is less. Nevertheless, if the switching frequency is too low, the converter charging time increases, and the difference between the target and the actual charging time will be very high. When the converter operates in DCM with valley switching, the switching frequency increases, as the output voltage increases. The switching frequency decreases as the value of k increases (from eq. (28)). However, if the converter switches at k^{th} valley point, the charging time to charge the load to 2.5 kV increases. This will reduce the speed of the incremental motor. Hence, it is recommended to switch at first valley point for achieving maximum incremental motor speed. With valley switching control the switching loss P_{swC} when $V_{outC} > nV_{in}$ is 0 W.

TABLE V
SWITCHING LOSS IN DIFFERENT OPERATING MODES DURING CHARGE PROCESS: AN EXAMPLE

Output voltage V_{outC} (V)	**In CCM**		**In DCM (without valley switching)**				**In DCM (with valley switching at k^{th} valley point)**			
			t_{dcmC}=10 µs		**t_{dcmC}=50 µs**		**Switching loss (W)**		**Switching frequency (kHz)**	
	Switching loss (W)	**Switching frequency (kHz) [When $V_{out} = V_{outC}$]**	**Switching loss (W)**	**Switching frequency (kHz)**	**Switching loss (W)**	**Switching frequency (kHz)**	***k*=1**	***k*=5**	***k*=1**	***k*=5**
250	0.175	33.1	0.125	24.87	0.024	12.47	0.03	0.018	30.9	20.42
500	0.45	51	0.278	33.78	0.012	14.37	0.003	0.002	46	26.07
1000	1.3	70	0.69	41.1	0.008	15.5	0	0	61	30.25
1500	2.55	79.8	1.26	44.38	0.001	15.99	0	0	68.4	31.96
2000	4.2	85.84	2	46.19	0.001	16.22	0	0	72.8	32.89
2500	6.25	89.92	2.89	47.34	0.005	16.36	0	0	75.7	33.48

B. ~~Analysis~~ Valley switching during discharge process

1) Analysis

~~Figure 6~~ Figure 10 shows the voltage across HV diode D_2, drain-to-source voltages of the primary and HV MOSFETs during

discharge process, when the converter operates in DCM. All equations given below are derived with an assumption of $V_{outD}>nV_{in}$. The drain-to-source voltage across the primary MOSFET M_p in DCM is given by

$$V_{Mp}(t) = V_{in} - V_{in} \cdot e^{-\left[\frac{R_s}{2(L_{ms}+L_{lks})}\right]t} \cos(w_{r2}t) \tag{30}$$

where R_s and L_{lks} are the secondary DC resistance and leakage inductance referred to secondary, respectively.

The voltage across freewheeling HV diode D_2 in DCM is

$$V_{D2}(t) = (V_{outD} - V_{onDb}) + nV_{in} \cdot e^{-\left[\frac{R_s}{2(L_{ms}+L_{lks})}\right]t} \cos(w_{r2}t) \tag{31}$$

where V_{outD} is the output voltage during the discharge process at a given switching cycle.

The voltage across blocking HV diode D_b in DCM is

$$V_{Db}(t) = \left[\delta \cdot V_{leakD} + \delta \cdot nV_{in}\left\{1 - e^{-\left[\frac{R_s}{2(L_{ms}+L_{lks})}\right]t} \cos(w_{r2}t)\right\}\right] \tag{32}$$

V_{leakS} is the voltage increment in drain-to-source voltage of M_s due to leakage inductance referred to secondary L_{lks} and is given by $V_{leakS} \approx I_{spkD}\sqrt{\frac{L_{lks}}{C_{lumpS}}}$ and $\delta = \frac{C_{osss}}{C_{osss}+C_{Db}}$.

In Fig. 10, t_{onD}, t_{offD} , t_{dcmD} , t_{vD} , and t_{dD} are the on-time, off-time of M_s, total DCM time duration, time to reach the valley point in the drain voltage from the instant when M_s is switched-off, and delay time needed to reach the valley point, from the instant when $V_{D2}=V_{outD}-V_{onDb}$, respectively.

The voltage across HV MOSFET M_s in DCM is

$$V_{Ms}(t) = \left[(V_{outD} - V_{onDb}) + \delta \cdot V_{leakD} + \delta \cdot nV_{in} + nV_{in}(1-\delta) \cdot e^{-\left[\frac{R_s}{2(L_{ms}+L_{lks})}\right]t} \cos(w_{r2}t)\right] \tag{33}$$

where V_{onDb} is the forward voltage drop of HV diode D_b.

The ringing frequency f_{r2} (or the oscillation period T_{osc2}) in DCM is given by

$$f_{r2} = \frac{w_{r2}}{2\pi} = \frac{1}{2\pi\sqrt{(L_{ms}+L_{lks})C_{lumpS}}} = \frac{1}{T_{osc2}} \tag{34}$$

The lumped capacitance C_{lumpS} in terms of different capacitances in the converter is given by

$$C_{lumpS} = \left(C_s + C_{D2} + \frac{C_{Db} \cdot C_{osss}}{C_{Db} + C_{osss}}\right) \tag{35}$$

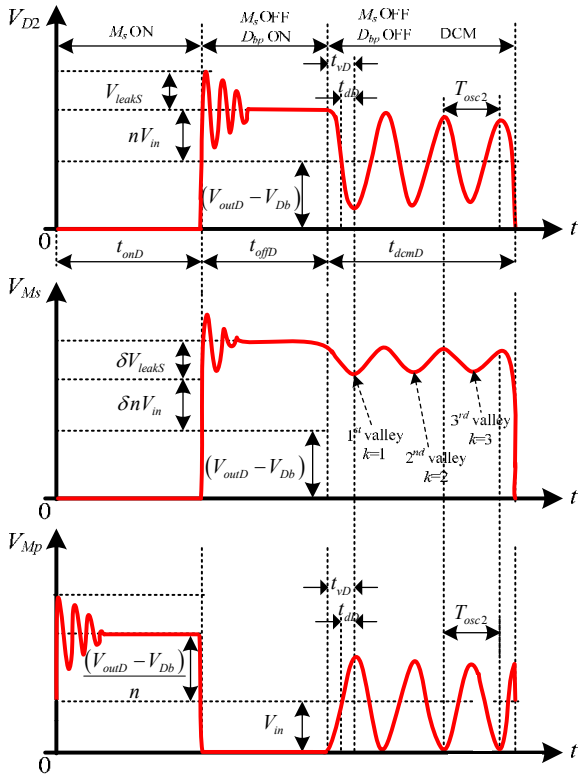
If the controller employs valley switching in DCM during discharge process, the switching-node voltage V_{Ms} at k^{th} valley point is given by

$$V_{Ms}\big|_k = \left[\left(V_{outD} - V_{onDb}\right) + \delta \cdot V_{leakD} + \delta \cdot nV_{in} + nV_{in}\left(1-\delta\right) \cdot e^{-\left[\frac{R_s}{2\left(L_{ms}+L_{lks}\right)}\left(2k-1\right)\frac{T_{osc2}}{2}\right]} \right] \tag{36}$$

The switching frequency at k^{th} valley point when the controller employs valley switching in DCM during discharge process, is given by

$$\begin{aligned} f_{swD}\big|_k &= \frac{1}{t_{onD} + t_{offD} + \left(2k-1\right)\dfrac{T_{osc2}}{2}} \\ &= \frac{1}{\dfrac{L_{ms} I_{spkD}}{V_{outD}} + \dfrac{L_{mp} I_{spkD} n}{\left(V_{in} + \Delta V_{in}\right)} + \left(2k-1\right)\dfrac{T_{osc2}}{2}} \end{aligned} \tag{37}$$

~~Table IV~~ Table VI provides the comparison of different operating modes during discharge process, in terms of switching frequency and drain-to-source voltage. At the end of each switching period, the stored energies in the non-linear output capacitance C_{osss} of the MOSFET M_s, the self-capacitance C_s of the transformer, and junction capacitance C_{D2} of the HV diode



~~Fig. 6.~~ Fig. 10. Voltages across D_2, M_s and M_p in DCM, during discharge process when $V_{outD}>nV_{in}$.

~~TABLE IV~~ TABLE VI
COMPARISON OF DIFFERENT OPERATING MODES IN A FLYBACK CONVERTER DURING DISCHARGE PROCESS

Operating Mode	Switching frequency during charge process f_{swD}	Drain-to-source voltage of M_s (V_{Ms}) at the beginning of the next switching cycle during the discharge process
CCM	$\frac{1}{\left[t_{onD}+t_{offD}\right]}$	$V_{TD}+\delta\cdot V_{leakD}+\delta\cdot nV_{in}$ where $V_{TD}=V_{outD}-V_{onDb}$
DCM (without valley switching)	$\frac{1}{\left[t_{onD}+t_{offD}+t_{dcmD}\right]}$	$\left[V_{TD}+\delta\cdot V_{leakD}+\delta\cdot nV_{in}+nV_{in}\left(1-\delta\right)e^{-\Delta_3}\cos\left(w_{r2}t_{dcmD}\right)\right]$ where $\Delta_3=\left[\frac{R_s}{2L_{Ts}}t_{dcmD}\right]$ and $L_{Ts}=L_{ms}+L_{lks}$
DCM (with valley switching at k^{th} valley point)	$\frac{1}{\left[t_{onD}+t_{offD}+\left(2k-1\right)\frac{T_{osc2}}{2}\right]}$	$\begin{cases}\left[V_{TD}+\delta\cdot V_{leakD}+\delta\cdot nV_{in}-nV_{in}\left(1-\delta\right)e^{-\Delta_4}\right], & \text{if } V_{outD}>nV_{in}\\ \left[\delta\cdot V_{TD}+\delta\cdot V_{leakD}+\delta\cdot nV_{in}\right], & \text{if } V_{outD}<nV_{in}\end{cases}$ where $\Delta_4=\left[\frac{R_s}{2L_{Ts}}\left(2k-1\right)\frac{T_{osc2}}{2}\right]$
DCM (with valley switching at k^{th} valley point, when blocking diode D_b is not used on HV side)	$\frac{1}{\left[t_{onD}+t_{offD}+\left(2k-1\right)\frac{T_{osc2}}{2}\right]}$	$\begin{cases}V_{TD}-nV_{in}e^{-\Delta_4}, & \text{if } V_{outD}>nV_{in}\\ 0 \Rightarrow \text{ZVS}, & \text{if } V_{outD}<nV_{in}\end{cases}$

D_2 are dissipated when the switch M_s is turned-on. Valley switching at the first valley point is employed during the discharge process, to improve the efficiency and to increase the driving frequency of the incremental motor, by reducing the discharging time.

The switching loss at the drain node of HV MOSFET M_s, when the converter employs the valley switching at the first valley point (k=1) is given by

$$P_{swD}\big|_{k=1}=\frac{1}{2}\left[C_s+C_{D2}+C_{osss}\right]\cdot\left[V_{Ms}\big|_{k=1}\right]^2\cdot\left[f_{swD}\big|_{k=1}\right] \tag{38}$$

2) An example to calculate the capacitive switching loss at a given discharging voltage

Table VII provides the calculated switching losses in different operating modes. The following values are used to calculate the switching losses in different modes: V_{in}=24 V, ΔV_{inD}=2 V, C_{lumpS}=14 pF, V_{onDb}=7 V, n=25, L_{ms}=31 mH, I_{ppkD}=170 mA, R_s=14 Ω, L_{lkS}=620 µH, f_{r2}=240 kHz, C_s=6 pF, C_{D2}= 0.7 pF. In CCM operation, as the output voltage decreases, the switching loss decreases. The switching frequency also decreases (from 97 kHz to 34 kHz) as the converter discharges. When the converter operates in DCM without valley switching, the switching loss decreases, as the converter discharges the load. However, the loss magnitude in DCM is less compared to that during CCM operation. Two cases are shown for DCM, one with t_{dcmC}=10 µs and the other with t_{dcmC}=50 µs. In the first case, the switching frequency decreases from 49 kHz to 25 kHz, and in the second case, the switching frequency decreases only from 16 kHz to 12 kHz. Therefore, the swithing loss for the second case is less. Nevertheless, if the switching frequency is too low, the converter discharging time increases. When the

converter operates in DCM with valley switching, the swithing frequency decreases, as the output voltage decreases. The switching loss in DCM (without valley switching) is slightly less compared to that in DCM valley switching. However, the total discharging time will be lower in the later case than the former one.

The switching frequency decreases as the value of k increases (from eq. (37)). However, if the converter switches at k^{th} valley point, the discharging time to discharge the load from 2.5 kV to 0 V increases, as the value of k increases. This will reduce the speed of the incremental motor. With valley switching control, the switching loss P_{swD} during discharge process when $V_{outD} < nV_{in}$ should be 0 W (see last row in Table VI). This happens only when there is no blocking diode D_b on HV side. The presence of a HV blocking diode D_b in series with HV MOSFET M_s on the secondary HV side, increases the capacitive switching loss. This is one of the reasons for lower discharge energy efficiency during the discharge operation, which will be explained in Section V.

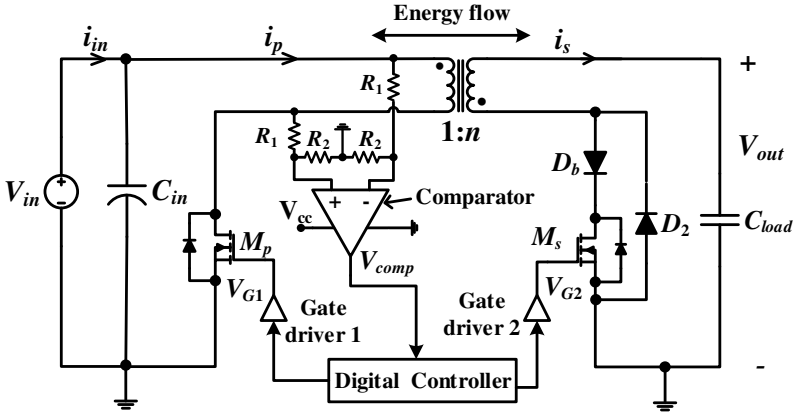
TABLE VII
SWITCHING LOSS IN DIFFERENT OPERATING MODES DURING DISCHARGE PROCESS: AN EXAMPLE

Output voltage V_{outD} (V)	**In CCM**		**In DCM (without valley switching)**				**In DCM (with valley switching)**			
	Switching loss (W)	**Switching frequency (kHz) [When $V_{out} = V_{outD}$]**	**t_{dcmD}=10 µs**		**t_{dcmD}=50 µs**		**Switching loss (W)**		**Switching frequency (kHz)**	
			Switching loss (W)	**Switching frequency (kHz)**	**Switching loss (W)**	**Switching frequency (kHz)**	***k*=1**	***k*=5**	***k*=1**	***k*=5**
2500	5.6	97.1	3.09	49.26	0.93	16.58	4.23	1.42	80.77	34.42
2000	4.14	92.34	2.36	48	0.71	16.44	3.12	1.37	77.44	33.8
1500	2.87	85.36	1.71	46.05	0.53	16.2	2.18	0.987	72.47	32.8
1000	1.8	74.15	1.15	42.58	0.42	14.97	1.38	0.667	64.23	31
500	0.88	53.19	0.65	34.72	0.23	14.53	0.71	0.398	47.89	26.6
250	0.46	33.98	0.38	25.36	0.16	12.59	0.4	0.266	31.74	20

IV. PROPOSED VALLEY SWITCHING CONTROL

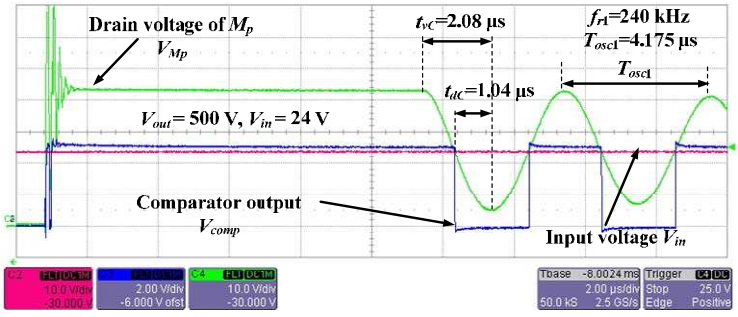
A. Charge process

The bidirectional flyback converter with the control circuit to achieve the valley switching during charge and discharge processes is shown in ~~Fig. 7~~ Fig. 11. The input voltage and the drain voltage of primary MOSFET M_p, each scaled by a resistor divider network (R_1=90 kΩ and R_2=3 kΩ), are compared using a high speed comparator TLV3501A. The comparator output becomes low (V_{comp}=0), when the drain voltage of M_p is lower than the input voltage V_{in}. The output signal of the comparator V_{comp} is sent to the 16-bit microcontroller (PIC18F45K22) which detects the comparator output change, and produces a fixed on-time pulse to enable the gate driver 1 which drives the MOSFET M_p.

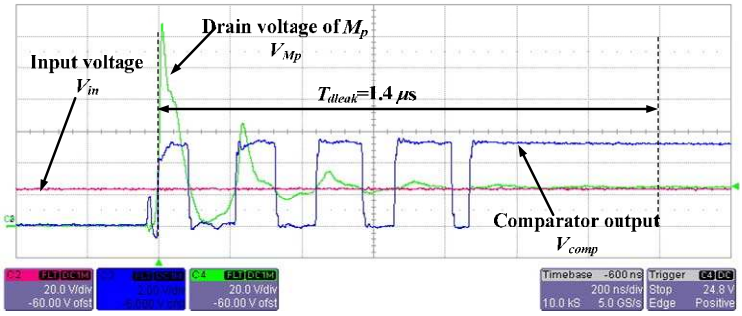


~~Fig. 7~~ Fig. 11. Schematic of the bidirectional flyback converter with the control circuit to achieve valley switching.

To introduce the control approach, ~~Figs. 8-10~~ Figs. 12-14 provide experimental results in the flyback converter during charge process, in the case when the converter is driven at a fixed frequency without valley switching. From ~~Fig. 8~~ Fig. 12, it can be observed that there is a delay time t_{dC} (~1.04 μs) between the time when the comparator output goes low and the first valley point (at which the next switching cycle should start to achieve valley switching), in the drain voltage V_{Mp} of M_p. The



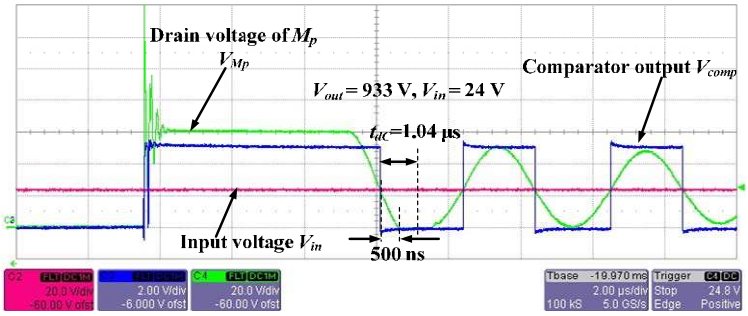
~~Fig. 8.~~ Fig. 12. Experimental results when M_p is driven with fixed frequency (V_{out}<600 V) during charge process; CH2: V_{in}; CH3: V_{comp}; CH4: V_{Mp}.



~~Fig. 9~~ Fig. 13. A zoomed view of Fig. 12 immediately after M_p is turned-off.

microcontroller provides the delay time t_{dC} such that the next turn-on cycle of M_p starts at the first valley point. The delay time t_{dC} can be calculated from the ringing frequency of V_{Mp} in DCM. The delay time t_{dC} is half of the time to reach first valley point t_{vC} (k=1) when $V_{outC}<nV_{in}$ (see ~~Fig. 4~~ Fig. 8). The expression for t_{dC} in terms of DCM ringing frequency f_{r1} is given by

$$t_{dC} = \frac{t_{vC}}{2} = \frac{1}{4f_{r1}} = \frac{\pi}{2}\sqrt{\left(L_{mp} + L_{lkp}\right)C_{lumpP}} \tag{39}$$

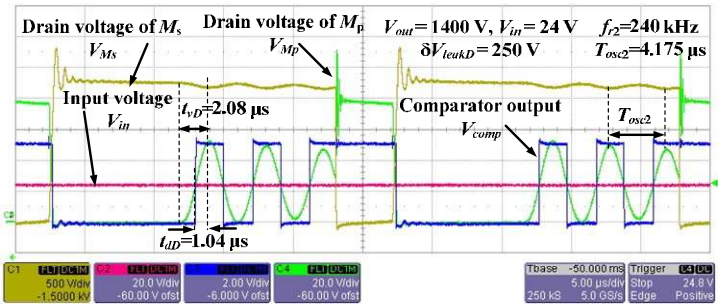


~~Fig. 10~~ Fig. 14. Experimental results when M_p is driven with fixed frequency (V_{out}>600 V) during charge process; CH2: V_{in}; CH3: V_{comp}; CH4: V_{Mp}.

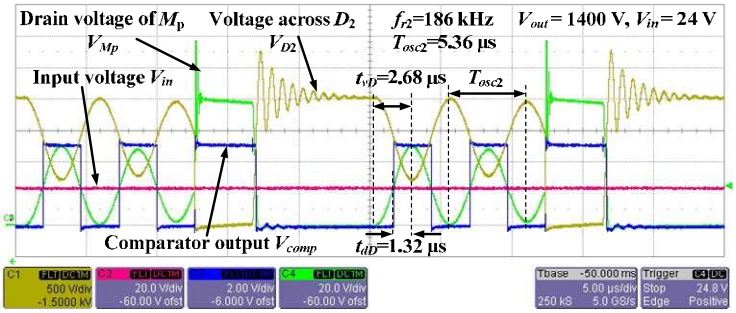
As mentioned before, M_p is turned-on whenever the comparator output becomes low (V_{comp}=0), but the operation can be corrupted by the high frequency ringing due to the leakage inductance L_{lkp}, which can also make the comparator output low (see ~~Fig. 9~~ Fig. 13). So, another delay time t_{dleak} (~1.5-2 μs) is provided by the microcontroller to disable the switching of M_p during this interval. When the output voltage $V_{outC}>nV_{in}$ the drain voltage V_{Mp} reaches 0 V (within 500 ns) before the delay time t_{dC}, which ensures zero voltage turn-on, as shown in ~~Fig. 10~~ Fig. 14. Hence, there is no capacitive switching loss during charge process when the output voltage $V_{outC}>nV_{in}$ (see ~~Table III~~ Table IV).

B. Discharge process

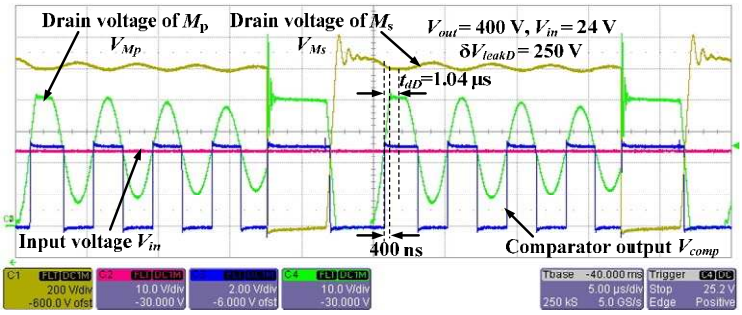
To achieve valley switching of HV MOSFET M_s during discharge process, only the information of the comparator output V_{comp} is used, without sensing any HV signal. The comparator output becomes high (V_{comp}=5 V), when the drain voltage of M_s is higher than the input voltage V_{in}. Similar to the charge process, the output signal of the comparator is sent to the microcontroller which produces fixed on-time pulses in steps, to enable the gate driver 2, which drives the MOSFET M_s. To discharge the capacitor load with constant secondary discharge peak current I_{spkD}, the on-time t_{onD} of M_s should be increased, as the output voltage decreases. ~~Figures 11-14~~ Figures 15-18 provide experimental results in the flyback converter during discharge process, in the case when the converter is driven at a fixed frequency without valley switching. From ~~Fig. 11~~ Fig. 15, it can be observed that there is a delay time t_{dD} (~1.04 μs) between the time when the comparator output goes high and the first



~~Fig. 11~~ Fig. 15. Experimental results when M_s is driven with fixed frequency (V_{out}>600 V) during discharge process; CH1: V_{Ms}; CH2: V_{in}; CH3: V_{comp}; CH4: V_{Mp}.



~~Fig. 12~~ Fig. 16. Experimental results when M_s is driven with fixed frequency (V_{out}>600 V) during discharge process; CH1: V_{D2}; CH2: V_{in}; CH3: V_{comp}; CH4: V_{Mp}.

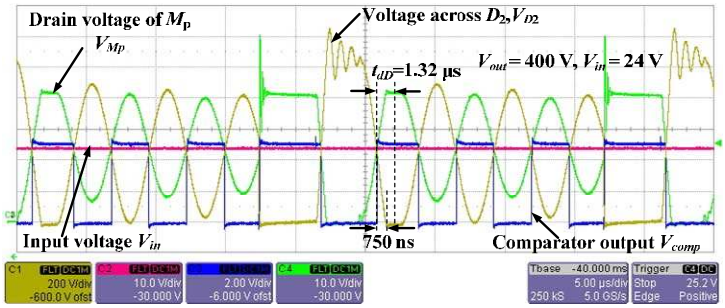


~~Fig. 13~~ Fig. 17. Experimental results when M_s is driven with fixed frequency (V_{out}<600 V) during discharge process; CH1: V_{Ms}; CH2: V_{in}; CH3: V_{comp}; CH4: V_{Mp}.

valley point (at which the next switching cycle should start to achieve valley switching), in the drain voltage V_{Ms} of M_s. The microcontroller provides the delay time t_{dD} such that the next turn-on cycle of M_s starts at the first valley point, and it can be calculated from the ringing frequency of V_{Ms} in DCM. The delay time t_{dD} is half of the time to reach first valley point t_{vD} (k=1) when V_{outD}>nV_{in} (see ~~Fig. 6~~ Fig. 10). The expression for t_{dD} in terms of DCM ringing frequency f_{r2} is given by

$$t_{dD} = \frac{t_{vD}}{2} = \frac{1}{4 f_{r2}} = \frac{\pi}{2}\sqrt{\left(L_{ms} + L_{lks}\right) C_{lumpS}} \tag{40}$$

When the HV probe is placed across HV diode D_2, the equivalent lumped capacitance C_{lumpS} is increased by ~9-10 pF due to the capacitance $C_{HVprobe}$ of the HV probe (Lecroy PPE 4 kV). Due to this, ringing frequency f_{r2} shown in ~~Figs. 11 and 12~~ Figs. 15 and 16 are different. When the HV probe is placed across M_s, the capacitance C_{lumpS} remains unchanged, due to the series combination of D_b and M_s. When $V_{outD}<nV_{in}$ the drain voltage V_{Ms} reaches a voltage of $\delta \cdot V_{TD} + \delta \cdot V_{leakD} + \delta \cdot nV_{in}$ (see Table VI), whereas the voltage across D_2 becomes 0 V before the delay time t_{dD}, as shown ~~Figs. 13 and 14~~ Figs. 17 and 18, respectively.



~~Fig. 14~~ Fig. 18. Experimental results when M_s is driven with fixed frequency (V_{out}<600 V) during discharge process; CH1: V_{D2}; CH2: V_{in}; CH3: V_{comp}; CH4: V_{Mp}.

C. *Sensitivity*

1) *In calculation of t_{dC}*

For L_{mp}=47.5 µH, L_{lkp}=920 nH, and C_{lumpP}=9 nF, the calculated time t_{dC} using (39) is 1.04 µs. For a 5% variation in each parameter L_{mp}, L_{lkp} and C_{lumpP}, then t_{dC} becomes 1.09 µs. For 10%, 20%, 30%, 40% and 50%, variations all parameters, t_{dC} turn out to be 1.14 µs, 1.24 µs, 1.35 µs, 1.45 µs and 1.55 µs, respectively. From Fig. 12, it is clear that the duration for which the first valley voltage of M_p is almost constant is approximately 400 ns. Hence, the maximum allowable tolerance for all parameters L_{mp}, L_{lkp} and C_{lumpP} could be 30%.

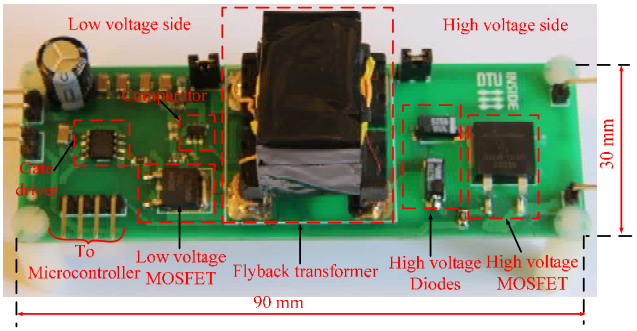
2) *In calculation of t_{dD}*

For L_{ms}=30 mH, L_{lks}=620 µH, and C_{lumpS}=14 pF, the calculated time t_{dD} using (40) is 1.03 µs. For 5%, 10%, 20%, 30%, 40% and 50%, variations in each parameter, t_{dD} become 1.08 µs, 1.13 µs, 1.23 µs, 1.34 µs, 1.44 µs and 1.54 µs, respectively. From Fig. 15, it is clear that the duration for which the first valley voltage of M_s is almost constant is approximately 450 ns. Therefore, the maximum allowable tolerance for all parameters L_{ms}, L_{lks} and C_{lumpS} is 30%.

V. VALLEY SWITCHING EXPERIMENTAL RESULTS

A. Experimental results

The experimental prototype of the HV bidirectional flyback converter is shown in ~~Fig. 15~~ Fig. 19. Tables VIII and IX provide the converter and controller specifications, components used in the conver**r**ter, and flyback transformer parameters, respectively. The experimental results in the converter, tested with a film capacitive load of 400 nF, to validate the proposed valley switching technique are shown in ~~Figs. 16-19~~ Figs. 20-24. In ~~Figs. 16 and 17~~ Figs. 20 and 21, successful valley-switching operation at different output voltages during the charge process is shown. From ~~Fig. 17~~ Fig. 21, it is clear that the converter operates with zero voltage switching (ZVS) turn-on, and the primary current is negative before the switch is turned-on. In ~~Fig. 18~~ Fig. 22, successful valley-switching operation during discharge process is shown. As explained in Section III, the first valley voltage in the drain to-source voltage of M_s is not very low, compared to the first valley voltage in HV diode voltage V_{D2} (due to the series combination of D_b and M_s). The capacitive switching loss is directly proportional to the voltage across the HV MOSFET when it is turned-on. This could lead to the low energy efficiency during the discharge process.



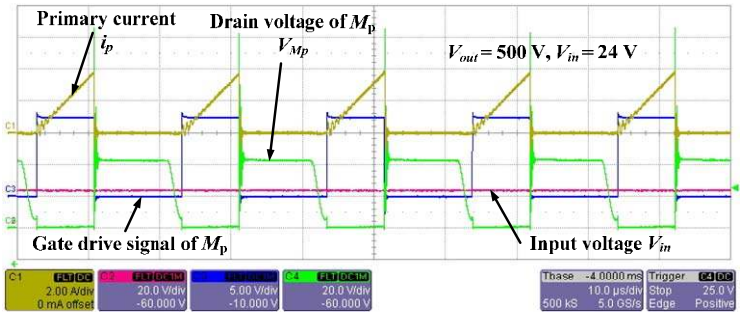
~~Fig. 15~~ Fig. 19. Experimental prototype of the HV bidirectional flyback converter with a 4.5 kV MOSFET on the HV side.

TABLE VIII
SPECIFICATIONS OF THE DIGITAL CONTROLLER

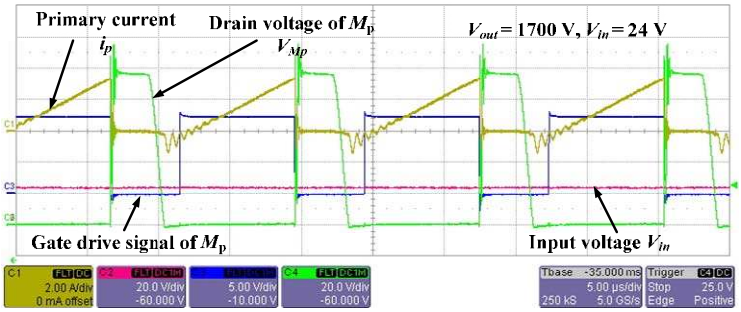
Parameter	Value
On time of low voltage MOSFET M_p during charge process t_{onC}	9 μs
On times of HV MOSFET M_s during discharge process t_{onD}	[2 μs, 3 μs, 5 μs, 10 μs, 20 μs, 150 μs, 200 μs]

TABLE IX
COMPONENTS USED IN THE HV CONVERTER

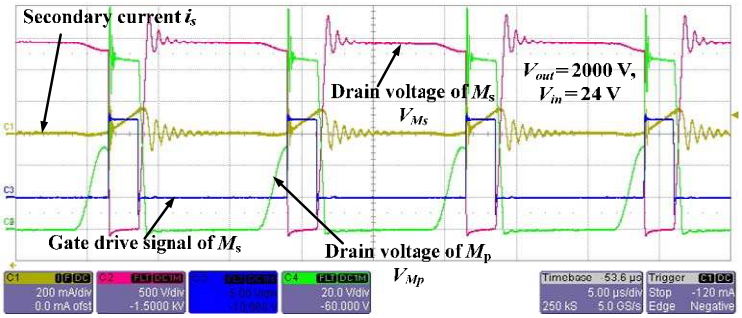
Component	Value
Gate driver	EL7104
Comparator	4.5 ns Rail-to-Rail, TLV3501A
Film capacitive load	400 nF, 3 kV Polypropelene [WIMA]



~~Fig. 16~~ Fig. 20. Experimental results when the converter is operated with valley switching during charge process; CH1: i_p; CH2: V_{in}; CH3: V_{G1}; CH4: V_{Mp}.

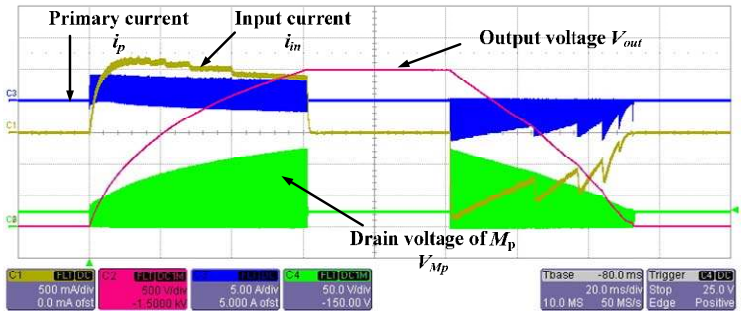


~~Fig. 17~~ Fig. 21. Experimental results with valley switching operation during the charge process; CH1: i_p; CH2: V_{in}; CH3: V_{G1}; CH4: V_{Mp}.



~~Fig. 18~~ Fig. 22. Experimental results with valley switching operation during discharge process; CH1: i_s; CH2: V_{Ms}; CH3: V_{G2}; CH4: V_{Mp}.

The bidirectional operation of the HV converter at 2.5 kV output voltage is shown in the ~~Fig. 19~~ Fig. 23. As shown in ~~Table V~~ Table VIII, due to constant turn on-time t_{onC} for M_p during charge process, the primary current I_{ppkC} is constant. The secondary current (load current) when the converter is driven at 2.42 kV is shown in Fig. 24. During the discharge process, employing variable turn on-time t_{onD} for M_s makes the secondary current (hence the primary current) I_{spkC} almost constant. This can be observed from Figs. 23 and 24. The set of on-times of M_s used in the digital controller when the converter was driven at 2.42 kV, as shown in Fig. 24, are slightly different than the corresponding specifications provided in Table VIII.



~~Fig. 19~~ Fig. 23. Experimental waveforms showing the bidirectional operation at 2.5 kV output voltage. CH1: i_{in}; CH2: V_{out}; CH3: i_p; CH4: V_{Mp}.

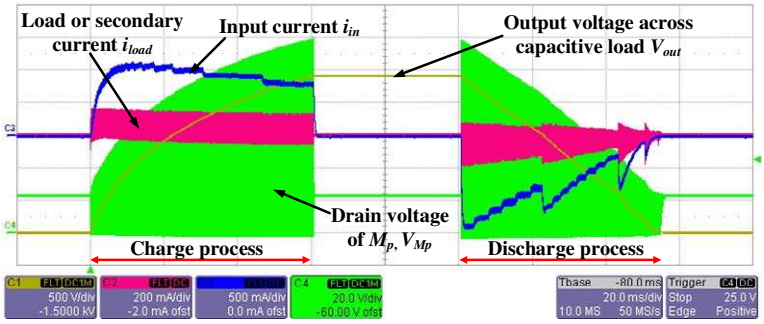
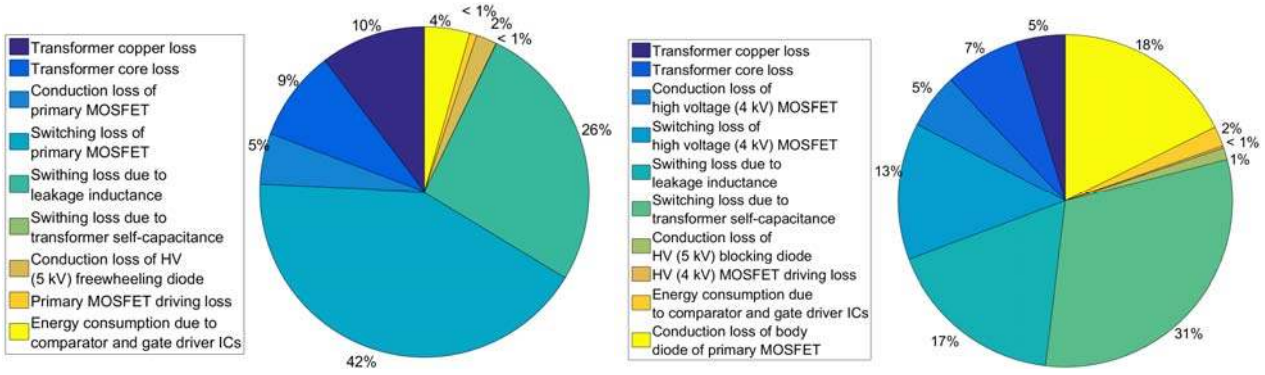


Fig. 24. Experimental waveforms showing the bidirectional operation at 2.42 kV output voltage. CH1: V_{out}; CH2: i_{load}; CH3: i_{in}; CH4: V_{Mp}.

B. Loss modelling of HV bidirectional flyback converter

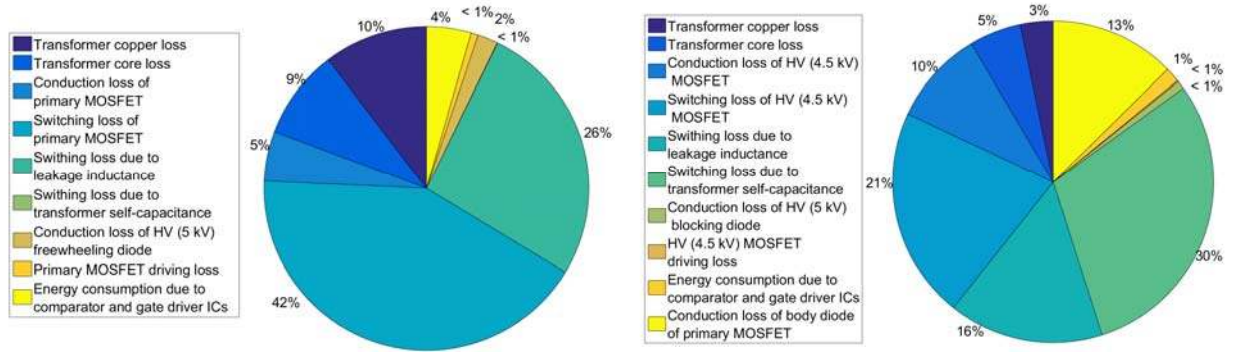
In order to investigate the bidirectional flyback converter efficiency, it is necessary to calculate the losses associated with each circuit component in the converter. The loss model is a function of transformer parasitics. Different losses in the bidirectional flyback converter are calculated in MATLAB software. The charge and discharge energy loss distributions when 4 kV MOSFET [38] and 4.5 kV MOSFET [39] are used in HV side are provided in Figs. 25 and 26, respectively. The energy loss at an output voltage of 2.5 kV is the loss occurred in a given component of the converter, for charging the capacitive load from 0 V to 2.5 kV. Similarly, the energy loss at an output voltage of 2.5 kV is the loss occurred in a given component of the converter, for discharging the capacitive load from 2.5 kV to 0 V. From Figs. 25(a) and 26(a), the major loss contributors during charge operation are the switching loss of the primary low-voltage MOSFET and the switching loss (snubber loss) due to the leakage inductance. As explained in the previous sections, the switching loss due to the self-capacitance during charge process is very low, due to the valley switching control. From Figs. 25(b) and 26(b), the major losses during discharge operation with 4 kV and 4.5 kV MOSFETs on HV side, occurs due to the conduction and switching loss of HV MOSFET, switching loss due to the leakage inductance, switching loss due to the self-capacitance, and the conduction loss of the body

diode of the primary MOSFET. By comparing the discharge loss distributions of 4 kV and 4.5 kV MOSFETs, the 4.5 kV MOSFET has higher conduction and switching losses. This significantly reduced the discharge energy efficiency.



a) b)

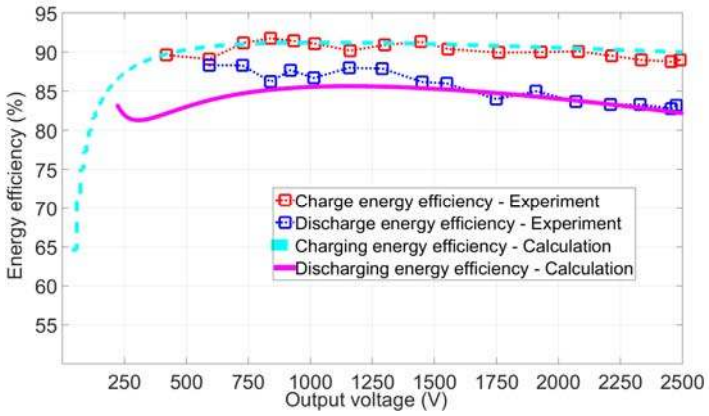
Fig. 25. Energy loss distribution during a) charge process, b) discharge process for a single charge and discharge switching cycle when 4 kV MOSFET is used on HV side.



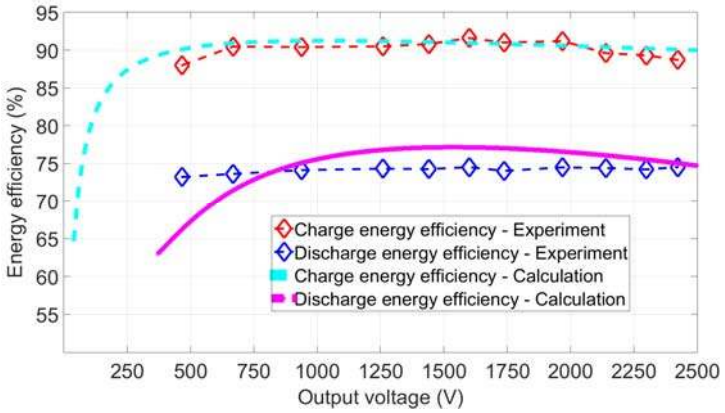
a) b)

Fig. 26. Energy loss distribution during a) charge process, b) discharge process for a single charge and discharge switching cycle when 4.5 kV MOSFET is used on HV side.

The junction capacitance of HV diode D_b [40] is 0.7 pF, the measured output capacitance of the HV MOSFET from the measured from ringing frequencies f_{r1} and f_{r2} is 10-12 pF. The lumped capacitances from the measurements are C_{lumpP}=9 nF and C_{lumpS}=14 pF, respectively. The calculated and measured energy efficiencies during charge and discharge processes ~~[7]~~ [14] with 4 kV and 4.5 kV MOSFETs on the HV side are compared in ~~Fig. 20~~ Figs. 27 and 28, respectively. The measured charge energy efficiency for both 4 kV and 4.5 kV MOSFETs is above 90%, for the output voltage range 750 V<V_{out}<2.2 kV, with a maximum efficiency of 92%. The charge energy efficiency for the output voltage range 2.2 kV<V_{out}<2.5 kV is between 88-90%. As explained earlier, the discharge energy efficiency for 4 kV MOSFET is lower than the charge energy efficiency due to the fact that valley voltage in drain-to-source voltage V_{Ms} of MOSFET M_s is not equal to valley voltage in V_{D2} during DCM.



~~Fig. 20~~ Fig. 27. Energy efficiency comparisons of flyback converter at different output voltages when a 4 kV MOSFET is used on secondary HV side.



~~Fig. 20~~ Fig. 28. Energy efficiency comparisons of flyback converter at different output voltages when a 4.5 kV MOSFET is used on secondary HV side.

C. Discussion

The charge energy efficiency η_C at a given output voltage was calculated using the following expression

$$\eta_C\left(V_{outC}\right)=\frac{0.5C_{load}V_{outC}^2}{0.5C_{load}V_{outC}^2+\sum_{i=1}^{N_C}E_{TotallossC}\left(i\right)} \tag{41}$$

where $E_{TotallossC}\left(i\right)$ and N_C are the total energy loss during the charge process in i^{th} switching cycle and the number of switching cycles required to charge the capacitor load from 0 V to a voltage V_{outC}.

The discharge energy efficiency η_D at a given output voltage was calculated using the following expression

$$\eta_D\left(V_{outD}\right)=\frac{0.5C_{load}V_{outD}^2-\sum_{j=1}^{N_D}E_{TotallossD}\left(j\right)}{0.5C_{load}V_{outD}^2} \tag{42}$$

where $E_{TotallossD}(j)$ and N_D are the total energy loss during the discharge operation in j^{th} switching cycle and the number of switching cycles required to discharge the capacitor load from a voltage V_{outD} to 0 V.

With the valley switching control during both charge and discharge operations, the bidirectional flyback converter should achieve very high energy efficiency. Nevertheless, the practical efficiency measurements and the loss modelling results confirmed that the charge efficiency at 2.5 kV output voltage was high (89%), but the discharge efficiency was low, mainly due to the capacitive switching losses. The capacitive switching loss (see Table VI and Eq. (38)) during discharge operation is directly proportional to the equivalent capacitance, leakage inductance and switching frequency. The equivalent capacitance is the sum of drain-to-source capacitance of HV MOSFET and the self-capacitance of the transformer. Since, the MOSFET capacitance cannot be eliminated, the only way to reduce the capacitive switching loss is by reducing both the leakage inductance and self-capacitance of the transformer. In [16], several transformer winding architectures (TWAs) are proposed especially for HV capacitor charge and discharge application. The TWA can be selected depending on the application where the actuator is used. With valley switching control, the switching frequency will have some variation, however, this is not the major reason for the energy loss in the converter. The proposed valley control with variable switching frequency control during both charge and discharge modes, reduces the charge and discharge times of the capacitive actuator, which improves the speed of the incremental actuator. It has been identified that the HV blocking diode in series with HV MOSFET prevents the efficient valley switching operation. The capacitive switching loss has been increased due to an increase in the drain-to-source voltage of the HV MOSFET, which is a function of the leakage inductance of the transformer. The 4.5 kV MOSFET has very low (75%) discharge efficiency at 2.5 kV output voltage due to its very high conduction loss, which has an on-resistance of 750 Ω. A setup to demonstrate the incremental motion using the DEAP based incremental actuator is shown in Fig. 29. Three DEAP actuators are connected through mechanical connections. Each actuator needs to be driven by a HV bidirectional dc-dc converter to achieve the incremental motion.

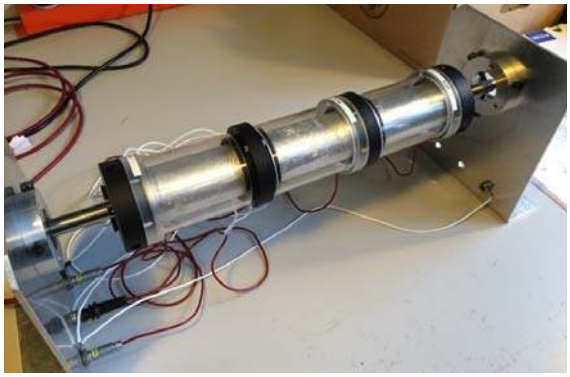


Fig. 29. Setup of the DEAP incremental actuator.

VI. Conclusions

A digital control technique to achieve the valley switching operation in a bidirectional flyback converter used to drive a dielectric electro-active polymer (DEAP) based capacitive actuator is presented. The power stage design of a high voltage bidirectional flyback converter for driving a capacitive actuator is described. The design of high-voltage transformer is provided. Detailed mathematical analysis when both the primary low-voltage and secondary high-voltage MOSFETs switch at the valley of drain voltage ringing are provided. The capacitive switching loss of the converter in different modes (CCM, DCM, BCM/valley mode) are discussed, for both charge and discharge operations, and an example is provided to compare all three modes.

The proposed valley switching technique has been implemented on a high-voltage bidirectional flyback converter, using a 16-bit microcontroller. The experiments are conducted on a 3 kV film capacitor load instead of a capacitive actuator. Experimental results demonstrating the valley switching operation during both the charge and discharge operations are provided. Using the proposed simple valley switching technique, the flyback converter was able to charge and discharge the capacitor load in minimum time. Hence, using the proposed control scheme incremental actuator could be driven with the maximum speed, for a given converter design. The energy loss distribution of the converter is provided during both charge and discharge modes. To charge the capacitive load to 2.5 kV and discharge it from 2.5 kV output voltage, using a 4 kV MOSFET, the flyback converter has achieved a charge and discharge energy efficiencies of 89% and 84%, respectively. Similarly, energy efficiencies to charge the capacitive load to 2.5 kV and discharge it from 2.5 kV output voltage, using a 4.5 kV MOSFET are 89% and 75%, respectively.

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