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CHAPTER 1

CONTINUOUS-TIME AVERAGED MODELING OF DC–DC CONVERTERS

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Converter systems rely on feedback loops to achieve the desired regulation performance. For example, in a typical dc–dc converter application, the objective is to maintain tight regulation of the output voltage in the presence of input voltage or load current variations. An accurate small-signal description of the converter control-to-output dynamics is the starting point for feedback loop design techniques based on frequency-domain concepts of loop gain, crossover frequency, phase margin, and gain margin.

The most successful and widespread modeling technique for switched-mode converters is based on *averaged small-signal modeling* [1, 118–120]. This technique is based on first averaging the converter behavior over a switching period with the purpose of smoothing the discontinuous, time-varying nature of the converter into a continuous, time-invariant nonlinear system model. A successive linearization step yields a linear, time-invariant model that can be treated using standard tools of linear system theory. The converter is described by a *continuous-time linear system*, often presented in the form of a linear equivalent circuit model, a natural representation in the context of analog control design.

The averaging approach is currently the most widely accepted way of *understanding* dynamics of switched-mode power converters. In addition to the relative simplicity and straightforwardness, popularity of the averaging approach has been reinforced by the success of innumerable practical designs supported by robust and easy-to-use integrated circuits for analog converter control.

The main purpose of this chapter is to revisit the main aspects of analysis and modeling techniques for switched-mode power converters. Averaged small-signal modeling, in particular, is reviewed in detail, highlighting the main assumptions behind the approach. This prepares the background necessary to understand the limitations of the averaged small-signal modeling in the context of digital control design and to allow subsequent developments of discrete-time models where these limitations are removed.

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A brief review of pulse width modulated (PWM) dc–dc converters is presented in Section 1.1, followed by a summary of steady-state analysis and modeling techniques in Section 1.2. Section 1.3 explains the need for dynamic modeling in the design of control loops around switched-mode power converters and introduces the small-signal averaged modeling approach. The method of state-space averaging [119, 120], a general approach to modeling switched-mode power converters, is summarized in Section 1.4. Analog control design examples are presented in Section 1.5. In the subsequent chapters, these examples are revisited to illustrate modeling and digital control design principles. To complete the background necessary to engage in developments of analysis, modeling and control techniques in the context of digitally controlled PWM converters, a discussion related to the nature of duty cycle, the control variable in PWM converters, is presented in Section 1.6. The key points are summarized in Section 1.7.

1.1 PULSE WIDTH MODULATED CONVERTERS

The focus of this book is on *PWM* converters, which are operated so as to alternate between two or more distinct subtopologies in a periodic fashion, with a fundamental *switching period* T_s. The Boost converter depicted in Fig. 1.1, for instance, operates with the switch in position 1 for a fraction DT_s of the switching period and with the switch in position 0 for the remaining fraction $D'T_s \triangleq (1-D)T_s$. The quantity $0 \leq D \leq 1$ is the *duty cycle*, which determines the fraction of a switching period the switch is kept in position 1. In PWM converters, D is the *control input* for the system, which is adjusted by a controller in order to regulate a converter voltage or current.

Typical waveforms of a PWM converter are shown in Fig. 1.2, which exemplifies the gate driving signal $c(t)$ and one of the converter state variables, such as the output voltage $v_o(t)$. Assuming that the converter duty cycle is sinusoidally modulated at a frequency $f_m \ll f_s$, the output voltage consists of a low-frequency component $\overline{v}_o(t)$, plus a high-frequency *switching ripple*. The low-frequency component of $v_o(t)$ contains a dc term V_o and a spectral component at the modulation frequency f_m. Using the terminology of modulation theory, $\overline{v}_o(t)$ is the *baseband* component of $v_o(t)$. The high-frequency content, on the other hand, contains the switching frequency f_s and its harmonics, as well as all the modulation sidebands

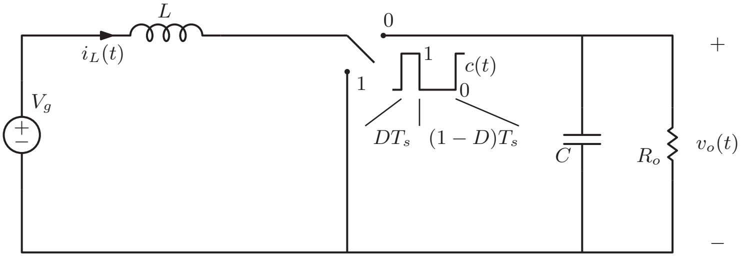


Figure 1.1 Pulse width modulated Boost converter.

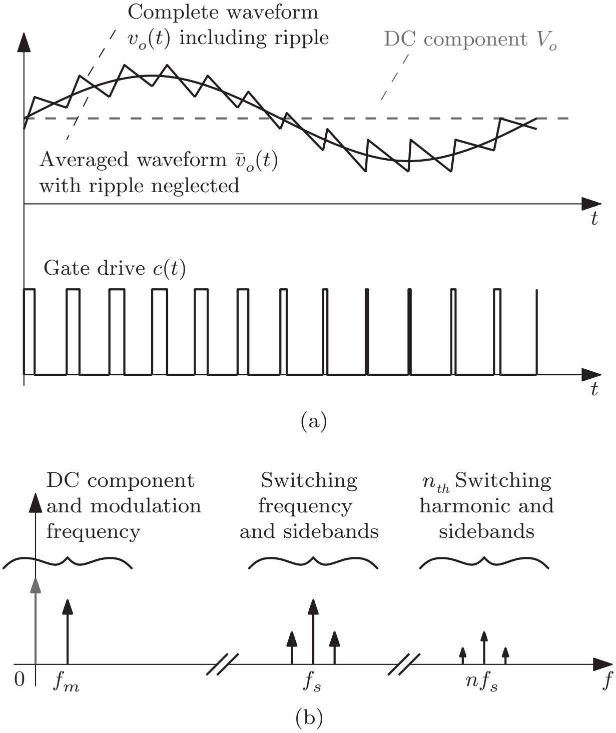

Complete waveform
$v_o(t)$ including ripple
DC component V_o
Averaged waveform $\overline{v}_o(t)$
with ripple neglected
t
Gate drive $c(t)$
t
(a)
DC component
and modulation
frequency
Switching
frequency
and sidebands
n_{th} Switching
harmonic and
sidebands
0
f_m
f_s
nf_s
f
(b)

Figure 1.2 (a) Converter waveforms with duty cycle modulation and (b) qualitative spectrum of a pulse width modulated signal.

originating from nonlinear interactions between f_m and f_s components occurring as a result of the modulation process.

In the context of the averaged modeling approach, the separation between low-frequency and high-frequency portions of the converter signals is of central importance. To be more precise, the *moving average operator* $\langle \cdot \rangle_T$ is introduced,

$$\boxed{\langle x(t) \rangle_T \triangleq \frac{1}{T} \int_{t-T/2}^{t+T/2} x(\tau)\, d\tau}, \tag{1.1}$$

which averages signal $x(t)$ over a period T. With this definition, the low-frequency component $\overline{v}_o(t)$ of $v_o(t)$ illustrated in Fig. 1.2 is defined as its moving average over the switching period T_s,

$$\boxed{\overline{v}_o(t) \triangleq \langle v_o(t) \rangle_{T_s}}. \tag{1.2}$$

The fundamental simplification at the basis of the averaging method consists of describing the small-signal dynamics of $\overline{v}_o(t)$ rather than $v_o(t)$, therefore neglecting high-frequency components of the converter waveforms. Both the power and the limitations of the method reside in the averaging approximation.

1.2 CONVERTERS IN STEADY STATE

When a converter is operating in steady state, every converter state variable—and therefore every voltage and current—is *periodic* in time, with a period equal to the converter switching period T_s. Steady-state operation is reached when all the converter inputs are constant—including the duty cycle—and after all transients are extinguished. In the following text, the basic ideas behind steady-state analysis of PWM converters are summarized. More extensive and detailed treatments can be found in power electronics textbooks [1–5].

Steady-state analysis of switched-mode power converters consists of expressing the dc values of all the voltages and currents in terms of the converter inputs. The analysis is founded on two basic principles, which are direct consequences of the periodicity of the system waveforms:

- *Inductor volt-second balance.* As all the inductor currents are periodic, no net flux variation can occur in any inductor over a switching period,

$$L(i_L(T_s) - i_L(0)) = \int_0^{T_s} v_L(\tau)\, d\tau = 0. \tag{1.3}$$

  This is equivalent to stating that the average inductor voltage over a switching interval is zero,

$$\boxed{\overline{v}_L(t) = 0}. \tag{1.4}$$

- *Capacitor charge (ampere-second) balance.* By a dual argument, as all the capacitor voltages are periodic, no net charge can be absorbed or delivered by any capacitor over a switching period,

$$C(v_C(T_s) - v_C(0)) = \int_0^{T_s} i_C(\tau)\, d\tau = 0. \tag{1.5}$$

  This is equivalent to stating that the average capacitor current over a switching interval is zero,

$$\boxed{\overline{i}_C(t) = 0}. \tag{1.6}$$

The two above-mentioned conditions, combined with conventional circuit analysis, are sufficient to solve the steady-state problem. In practice, the calculations are greatly simplified by introducing the *small-ripple approximation*. By *switching ripple*, one refers to the ac component of a converter voltage or current. In steady state, the switching ripple is a periodic function with a fundamental frequency equal to the converter switching rate. The ripple peak-to-peak amplitudes of a capacitor voltage $v_C(t)$ and an inductor current $i_L(t)$ are denoted as Δv_C and Δi_L, respectively.

The small-ripple approximation states that the dc converter quantities can be approximately determined by neglecting both capacitors voltage ripples and inductors current ripples. This corresponds to considering every capacitor C as an ideal dc voltage source of unknown magnitude V_C and every inductor as a dc current source of unknown magnitude I_L,

$$\boxed{\frac{\Delta v_C}{\overline{v}_C} \ll 1 \Leftrightarrow v_C(t) = V_C = \text{constant}},$$
$$\boxed{\frac{\Delta i_L}{\overline{i}_L} \ll 1 \Leftrightarrow i_L(t) = I_L = \text{constant}}. \tag{1.7}$$

Contrary to the volt-second balance and the ampere-second balance, which follow directly from the characteristics of inductive and capacitive components and the periodicity of the steady-state operation, the small-ripple approximation is simply a convenient assumption that simplifies the steady-state solution and which is often satisfied in practical converter systems. A relaxed version of the small-ripple approximation, known as *linear-ripple approximation*, is also often employed. According to the linear-ripple approximation, ripple components of the $v_C(t)$'s and $i_L(t)$'s are allowed to be triangular waveshapes. It can be shown that the steady-state analysis proceeds as stated earlier for the small-ripple approximation. In practice, the linear-ripple approximation is easier to meet, especially when considering inductor current waveforms. As long as the small-ripple approximation is satisfied for capacitor voltages, in fact, inductor currents retain triangular waveforms even when the peak-to-peak ripple is not negligibly small compared with the dc component.

It is worth mentioning, at this point, that the above discussion is implicitly focused on the converters operating in *continuous conduction mode* (CCM), where the use of the small-ripple or linear-ripple approximation is well justified for *all* the converter state variables. As for converters operating in *discontinuous conduction mode* (DCM), on the other hand, the above-mentioned assumption does not hold and the analysis becomes somewhat more involved. Further details on DCM modeling can be found in [1, 121–123].

1.2.1 Boost Converter Example

As an example, consider the Boost converter depicted in Fig. 1.3. The physical inductor is represented by a series combination of an ideal inductor L and a resistive element r_L, modeling the inductor copper losses. Other converter components are assumed to be ideal.

With the switch in position 1 for an interval DT_s, the voltage across the ideal inductor L is

$$v_L(t) = V_g - r_L I_L, \tag{1.8}$$

where the small-ripple approximation $i_L(t) \approx I_L$ has been employed. In the same topological state and under the small-ripple approximation $v_C(t) \approx V_C$, the output capacitor current is

$$i_C(t) = -\frac{V_C}{R_o}. \tag{1.9}$$

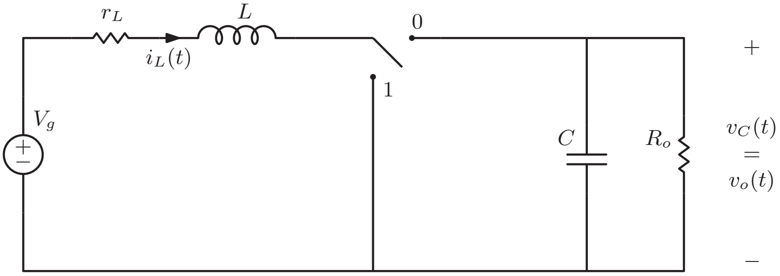


Figure 1.3 Boost converter example.

Similarly, with the switch in position 0 for an interval $D'T_s = (1-D)T_s$, one has

$$\begin{aligned} v_L(t) &= V_g - r_L I_L - V_C, \\ i_C(t) &= I_L - \frac{V_C}{R_o}. \end{aligned} \tag{1.10}$$

Waveforms $v_L(t)$ and $i_C(t)$, including the small-ripple approximation, are shown in Fig. 1.4. Imposing the volt-second balance (1.4) and the charge balance (1.6), one obtains

$$\begin{aligned} \overline{v}_L(t) &= D\big(V_g - r_L I_L\big) + D'\big(V_g - r_L I_L - V_C\big) = 0, \\ \overline{i}_C(t) &= D\left(-\frac{V_C}{R_o}\right) + D'\left(I_L - \frac{V_C}{R_o}\right) = 0, \end{aligned} \tag{1.11}$$

the solution of which is

$$\begin{aligned} I_L &= \frac{V_g}{D'^2 R_o} \frac{1}{1 + \frac{r_L}{D'^2 R_o}}, \\ V_C &= \frac{V_g}{D'} \frac{1}{1 + \frac{r_L}{D'^2 R_o}}. \end{aligned} \tag{1.12}$$

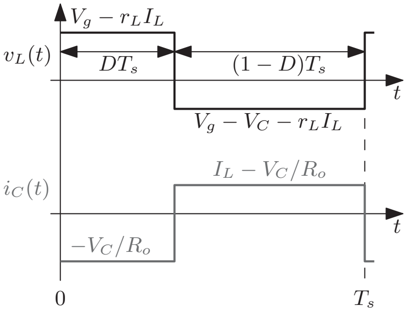


Figure 1.4 Boost converter example: waveforms based on the small-ripple approximation.

The converter *voltage conversion ratio* can be evaluated from the above-mentioned equations as

$$M(D) \triangleq \frac{V_o}{V_g} = \frac{V_C}{V_g} = \frac{1}{D'} \frac{1}{1 + \frac{r_L}{D'^2 R_o}}, \tag{1.13}$$

which reduces to the familiar Boost $M(D) = 1/D'$ for a lossless converter ($r_L = 0$).

1.2.2 Estimation of the Switching Ripple

Once the dc converter quantities are determined, one can go back to the converter topology and estimate both the waveshapes and the amplitudes of the steady-state inductor current and capacitor voltage ripples.

In the Boost converter example, as shown in Fig. 1.4, the inductor voltage waveform $v_L(t)$ is approximately a piecewise-constant signal. The inductor current ripple is therefore a triangular waveform with slopes determined by $v_L(t)$. Neglecting, for simplicity, the inductor series resistance r_L, the peak-to-peak current ripple Δi_L can be determined by integrating $v_L(t)/L$ over either one of the two switching subintervals,

$$\Delta i_L = \frac{1}{L} \int_0^{DT_s} v_L(\tau)\, d\tau = \frac{V_g}{L} DT_s = \frac{T_s}{L} V_g \left(1 - \frac{V_g}{V_o}\right). \tag{1.14}$$

Similarly, one can reconstruct the capacitor voltage ripple waveshape by integration of $i_C(t)$ shown in Fig. 1.4. More accurate results can be obtained by removing the small-ripple approximation and by deriving $i_C(t)$ using, this time, the triangular waveshape $i_L(t)$ determined earlier. The corresponding waveforms are depicted in Fig. 1.5.

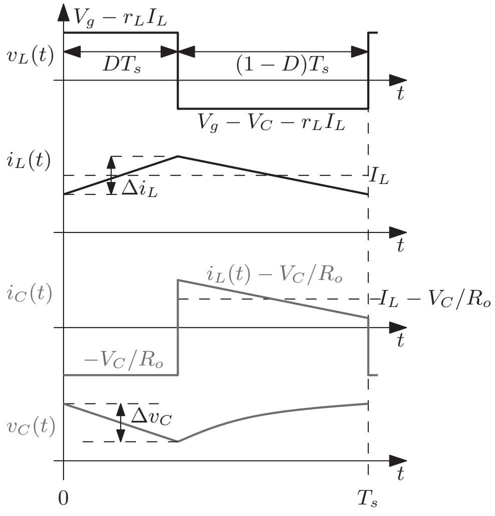


Figure 1.5 Boost converter example: estimation of the ripple waveshapes.

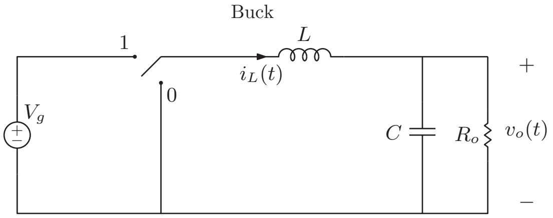
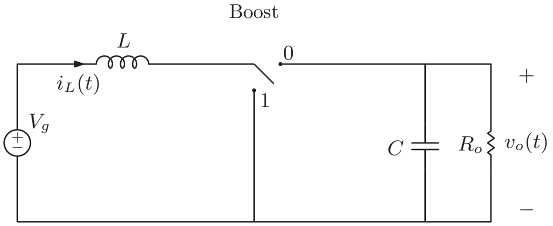
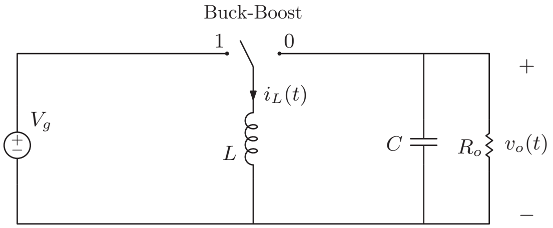
To determine the peak-to-peak output voltage ripple, similar to finding Δi_L, one can directly integrate $i_C(t)/C$ over either one of the two switching subintervals,

$$\Delta v_C = \frac{1}{C}\int_0^{DT_s} |i_C(\tau)|\, d\tau = \frac{V_o}{R_o C} DT_s = \frac{T_s}{R_o C}\left(V_o - V_g\right). \tag{1.15}$$

1.2.3 Voltage Conversion Ratios of Basic Converters

Systematic application of the volt-second and charge balance equations, along with the small-ripple approximation, allows straightforward steady-state analysis of any PWM converter. Table 1.1 reports the CCM conversion ratios of the three basic converter topologies in the ideal (lossless) case.

TABLE 1.1 Ideal Voltage Conversion Ratios of Basic Converters in CCM

Converter	Conversion Ratio
 Buck 1 0 L $i_L(t)$ V_g + − C R_o $v_o(t)$ + −	$M(D) = D$
 Boost L $i_L(t)$ 0 1 V_g + − C R_o $v_o(t)$ + −	$M(D) = \frac{1}{1-D}$
 Buck-Boost 1 0 $i_L(t)$ L V_g + − C R_o $v_o(t)$ + −	$M(D) = -\frac{D}{1-D}$

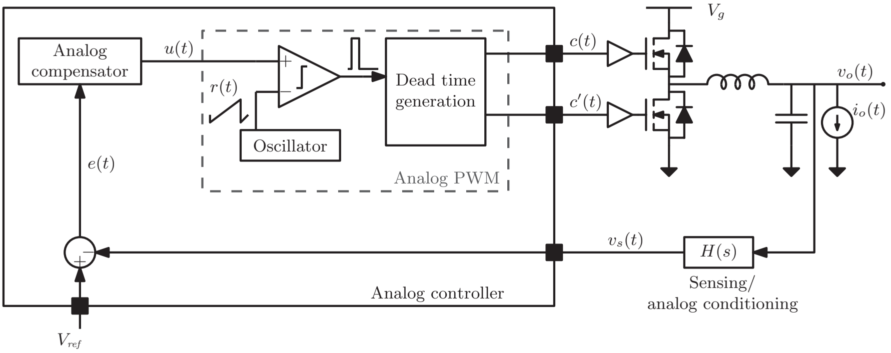


Figure 1.6 Analog voltage-mode control of a synchronous Buck converter.

1.3 CONVERTER DYNAMICS AND CONTROL

The main topic of this chapter—converter averaged small-signal modeling—is now discussed. Consider voltage-mode control of a synchronous Buck converter as a simple case study to review the basic concepts of the approach. A block diagram of the system is illustrated in Fig. 1.6. The term *synchronous* referred to the Buck converter is associated with the implementation of the rectifying, or secondary, switch: instead of the usual free-wheeling diode used as a passive rectifier, the Buck converter of Fig. 1.6 makes use of a *controlled* switch that is driven by the complementary version $c'(t)$ of the PWM signal,

$$c'(t) \triangleq 1 - c(t). \tag{1.16}$$

A primary advantage of synchronous rectification is the smaller voltage drop across the rectifier switch during conduction, as opposed to the diode rectifier, an essential requirement when regulating low output voltages. Furthermore, the rectifier switch becomes *current bidirectional*, therefore guaranteeing CCM operation and converter controllability even at no load.

In Fig. 1.6, the load is represented by an independent current source rather than a resistance. This is an appropriate modeling choice for many digital loads in point-of-load applications, in which the converter output current depends on the load internal activity and is independent of the output voltage.

The converter is feedback-controlled in order to achieve regulation of the output voltage $v_o(t)$ at a constant reference value V_{ref}. To this end, a control error $e(t)$ is found as the difference between the analog setpoint V_{ref} and the sensed signal $v_s(t)$, where $v_s(t)$ is a scaled, filtered version of $v_o(t)$. In Fig. 1.6, sensing, scaling, and analog filtering of $v_o(t)$ are modeled by the transfer function $H(s)$.

The analog continuous-time compensator processes the error signal and outputs a control command $u(t)$. As exemplified in Fig. 1.7, $u(t)$ is then compared with the carrier $r(t)$ of a trailing-edge pulse width modulator, which in turn produces the modulated gate drive signal $c(t)$.

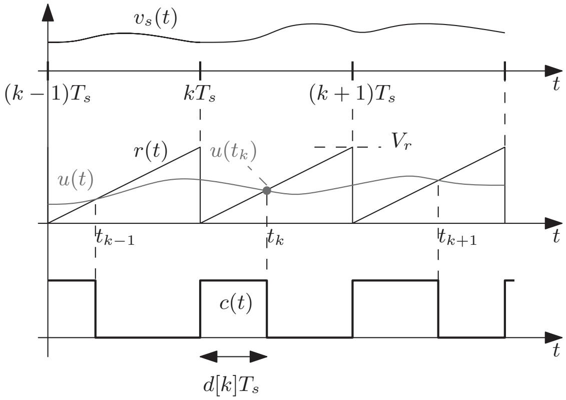


Figure 1.7 Typical analog control waveforms.

The end goal of the modeling step is the derivation of an equivalent small-signal model of the control loop. The process involves, as anticipated, averaging and linearizing the converter behavior around the above steady-state operating point. In the following, notation (1.2) is employed to denote converter quantities averaged over a switching period.

1.3.1 Converter Averaging and Linearization

Referring to the Buck converter shown in Fig. 1.8(a) and applying the moving average operator (1.1) to voltage v_x at the switching node, one has

$$\overline{v}_x(t) \approx d(t)\overline{v}_g(t), \tag{1.17}$$

while the averaged converter input current $\overline{i}_g$ is

$$\overline{i}_g(t) \approx d(t)\overline{i}_L(t). \tag{1.18}$$

These results[1] allow construction of an *averaged equivalent circuit*, as shown in Fig. 1.8(b) [1], which is now time-invariant but still nonlinear.

Perturbation of the circuit equations around the steady-state operating point and successive linearization yields

$$\begin{aligned} \hat{\overline{v}}_x(t) &\approx D\hat{\overline{v}}_g(t) + V_g\hat{d}(t), \\ \hat{\overline{i}}_g(t) &\approx D\hat{\overline{i}}_L(t) + I_L\hat{d}(t), \end{aligned} \tag{1.19}$$

---

[1] Approximation $\langle c(t)x(t)\rangle_{T_s} \approx d(t)\langle x(t)\rangle_{T_s}$ is justified, in general, whenever $x(t)$ has negligible switching content, that is, when it can be regarded as an essentially baseband signal. One exception to this occurs when $x(t)$ has a triangular switching ripple, in which case the approximation is justified even in the presence of a large ripple component. In conclusion, one can safely assume $\langle c(t)x(t)\rangle_{T_s} \approx d(t)\langle x(t)\rangle_{T_s}$ under the small-ripple or linear-ripple approximations already discussed in Section 1.2.

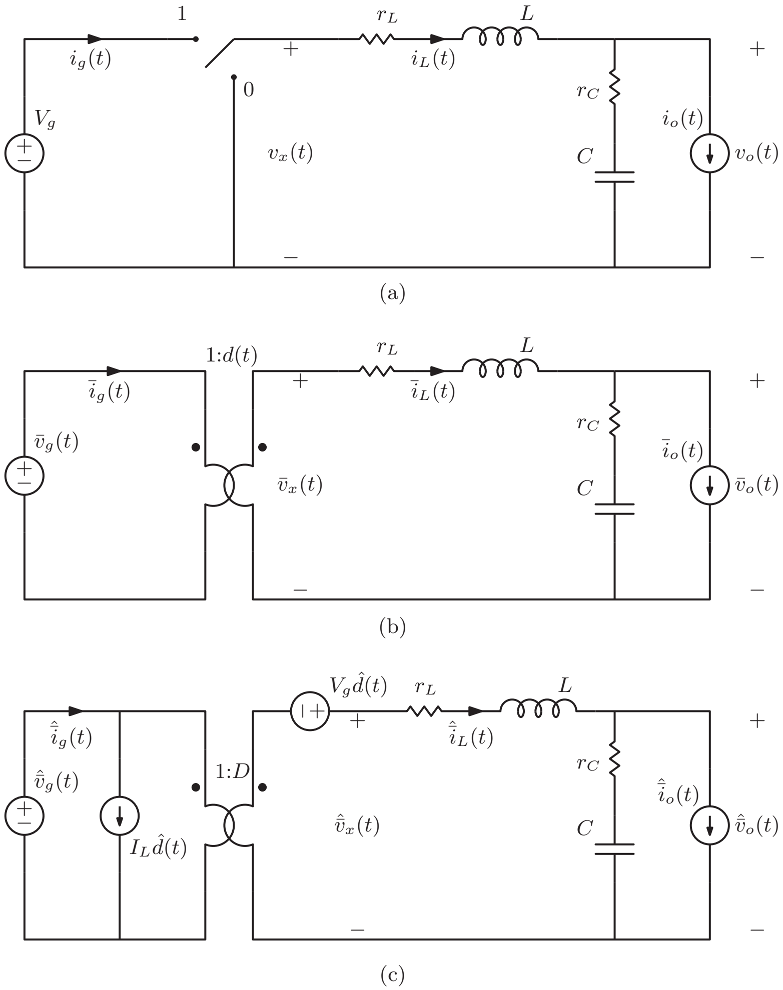

1
0
r_L
L
$i_g(t)$
$i_L(t)$
V_g
$v_x(t)$
r_C
C
$i_o(t)$
$v_o(t)$
+
−
(a)
1:$d(t)$
$\bar{i}_g(t)$
$\bar{v}_g(t)$
$\bar{i}_L(t)$
$\bar{v}_x(t)$
$\bar{i}_o(t)$
$\bar{v}_o(t)$
(b)
$V_g\hat{d}(t)$
$\hat{\bar{i}}_g(t)$
$\hat{\bar{v}}_g(t)$
$I_L\hat{d}(t)$
1:D
$\hat{\bar{i}}_L(t)$
$\hat{\bar{v}}_x(t)$
$\hat{\bar{i}}_o(t)$
$\hat{\bar{v}}_o(t)$
(c)

Figure 1.8 (a) Buck converter and its (b) averaged and (c) small-signal models.

where $\hat{\bar{x}}(t) = \bar{x}(t) - X$ denotes the small-signal component of $\bar{x}(t)$ with respect to the dc component X. Figure 1.8(c) illustrates the averaged, small-signal equivalent circuit of the Buck converter obtained after the linearization process. From the equivalent circuit model, evaluation of the control-to-output transfer function $G_{vd}(s)$ yields

$$\begin{aligned} G_{vd}(s) \triangleq \left.\frac{\hat{\bar{v}}_o(s)}{\hat{d}(s)}\right|_{\hat{\bar{v}}_g=0,\hat{\bar{i}}_o=0} &= V_g\frac{1+sr_CC}{1+s(r_C+r_L)C+s^2LC} \\ &= G_{vd0}\frac{1+\frac{s}{\omega_{ESR}}}{1+\frac{s}{Q\omega_0}+\frac{s^2}{{\omega_0}^2}}, \end{aligned} \tag{1.20}$$

with

$$\begin{aligned} G_{vd0} &\triangleq V_g, \\ \omega_{ESR} &\triangleq \frac{1}{r_C C}, \\ \omega_0 &\triangleq \frac{1}{\sqrt{LC}}, \\ Q &\triangleq \frac{1}{r_C + r_L}\sqrt{\frac{L}{C}}. \end{aligned} \tag{1.21}$$

The converter small-signal behavior is therefore that of a second-order system with resonant frequency and Q-factor (ω_0, Q), and with a real left half-plane (LHP) zero located at $s = -\omega_{ESR}$. The zero originates from the equivalent series resistance (ESR) r_C of the output capacitor.

1.3.2 Modeling of the Pulse Width Modulator

A small-signal model of the pulse width modulator is necessary in order to develop a complete small-signal model of a converter system. This topic is particularly important as there are significant differences in the PWM small-signal dynamics between analog and digital control.

There are two main families of pulse width modulators:

- *Naturally sampled pulse width modulators (NSPWMs)* process a *continuous-time* modulating signal $u(t)$. They are commonly employed in analog controllers.
- *Uniformly sampled pulse width modulators (USPWMs)* are characterized by a *discrete-time modulating* signal $u[k]$, which is updated once every switching period and held constant throughout the entire switching interval during its comparison with the PWM carrier. USPWMs are most commonly employed in digital control loops, where the control signal is inherently discrete in time, as detailed further in the following chapters. It is worth mentioning, however, that it is possible to apply uniformly sampled modulation in analog control: the continuous-time control command $u(t)$ is in this case subject to a *sample & hold* operation, the output of which is then compared with the PWM carrier using an analog comparator.

Consider a naturally sampled PWM employed in analog, continuous-time control loop around a switched-mode converter. As illustrated in Fig. 1.7, the duty cycle $d[k]$ applied to the power converter during the kth switching cycle is equal to

$$d[k] = \frac{u(t_k)}{V_r}, \tag{1.22}$$

where t_k represents the instant at which $u(t)$ intersects the PWM carrier $r(t)$ during the kth switching cycle, while V_r is the PWM carrier amplitude. Duty cycle $d[k]$ during the kth switching cycle therefore corresponds to a *sampled* version of the modulating signal $u(t)$. Sampling occurs as a result of the intersection between u and r and is inherent to the PWM process–this is the main reason why these types of modulator are designated as *naturally sampled*. For small perturbations $\hat{u}$ around a steady-state value U, every sampling instant occurs at the same position in the switching interval, and the equivalent sampling performed by the PWM becomes uniform.

From (1.22), one also has that $d[k]$ is determined by the *instantaneous* value of $u(t)$ at its intersection with the PWM carrier. The absence of any delay between the natural sampling of $u(t)$ operated by the modulator and the generation of the PWM modulated edge justifies, at least on an intuitive level, the common practice in analog control modeling to treat the PWM as a simple *gain* block. Denoting with $\hat{u}$ and $\hat{d}$ the control command and duty cycle small-signal components with respect to their steady-state values, the PWM transfer function is therefore

$$G_{PWM}(s) \triangleq \frac{\hat{d}}{\hat{u}} = \frac{1}{V_r}. \tag{1.23}$$

It should be noted that (1.23) neglects propagation delays in the PWM comparator and in the gate driving circuitry between the pulse width modulator and the power switch. Such delays, however, are usually much shorter than the switching period T_s. It follows that:

Naturally sampled PWMs do not contribute to the small-signal dynamics of the control loop, except for a constant gain factor.

In contrast to the naturally sampled modulators, the uniformly sampled modulators do introduce dynamics in the loop in the form of an equivalent small-signal delay. This important distinction is further justified and explained in Chapter 2.

1.3.3 The System Loop Gain

Figure 1.9 shows a block diagram of the complete small-signal model of a closed-loop regulated converter. In the diagram, $G_c(s)$ represents the compensator transfer function to be designed.

From the block diagram, the system *loop gain* $T(s)$ can be defined by opening the feedback loop as suggested in Fig. 1.10 and by evaluating the resulting transfer

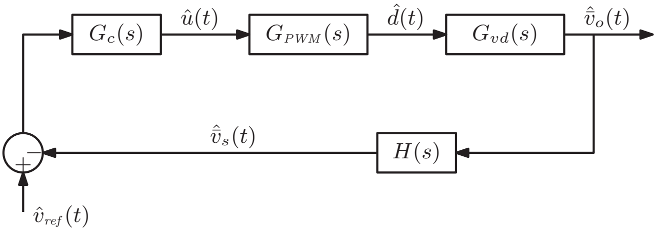


Figure 1.9 Small-signal block diagram of the analog voltage-mode control.

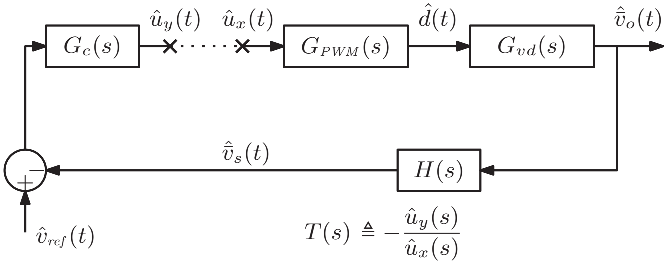


Figure 1.10 Definition of the system loop gain $T(s)$.

function between $\hat{u}_x$ and $\hat{u}_y$,

$$\boxed{T(s) \triangleq -\left.\frac{\hat{u}_y(s)}{\hat{u}_x(s)}\right|_{\hat{v}_{ref}=0} = G_c(s)G_{PWM}(s)G_{vd}(s)H(s)}. \tag{1.24}$$

The *uncompensated loop gain* $T_u(s)$, on the other hand, is defined as the system loop gain when a unity compensation is employed, that is, when $G_c(s) = 1$,

$$\boxed{T_u(s) \triangleq G_{PWM}(s)G_{vd}(s)H(s)}. \tag{1.25}$$

From (1.20), (1.23), and (1.24), one has

$$T_u(s) = \frac{G_{vd0}}{V_r} \frac{1 + \frac{s}{\omega_{ESR}}}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0{}^2}} H(s). \tag{1.26}$$

Result (1.26) represents the starting point for commonly applied frequency-domain compensator design techniques. Analog compensator design proceeds with usual techniques of linear continuous-time control, with the main goals of ensuring sufficient stability margins for the closed-loop system and a control bandwidth adequate for the application.

1.3.4 Averaged Small-Signal Models of Basic Converters

The averaging and linearization steps carried out in Section 1.3.1 can be applied to any converter topology, resulting in a corresponding small-signal equivalent circuit. Figure 1.11 shows the averaged small-signal equivalent circuits of the Buck, Boost, and Buck–Boost converters. In the models, $\hat{\bar{v}}_g(t)$ and $\hat{\bar{i}}_o(t)$ are the small-signal components of the input voltage and output current, respectively, which act as disturbances for the control system. The control input, on the other hand, is represented by the small-signal component of the duty cycle command $\hat{d}$, which acts on the circuit via current and voltage generators having operating point dependent gains. Derivation

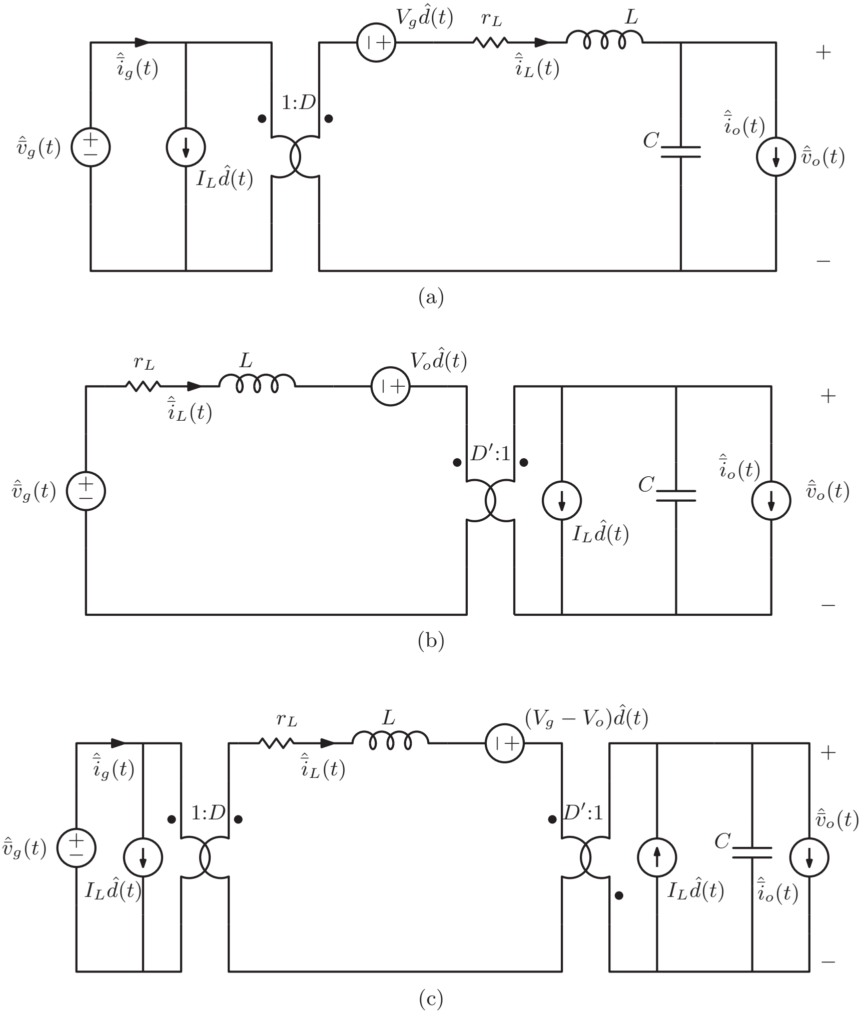

$V_g\hat{d}(t)$
r_L
L
$\hat{i}_g(t)$
$\hat{i}_L(t)$
$1{:}D$
$\hat{v}_g(t)$
$I_L\hat{d}(t)$
C
$\hat{i}_o(t)$
$\hat{v}_o(t)$
+
−
(a)
r_L
L
$V_o\hat{d}(t)$
$\hat{i}_L(t)$
$D'{:}1$
$\hat{v}_g(t)$
$I_L\hat{d}(t)$
C
$\hat{i}_o(t)$
$\hat{v}_o(t)$
+
−
(b)
r_L
L
$(V_g - V_o)\hat{d}(t)$
$\hat{i}_g(t)$
$\hat{i}_L(t)$
$1{:}D$
$D'{:}1$
$\hat{v}_g(t)$
$I_L\hat{d}(t)$
$I_L\hat{d}(t)$
C
$\hat{i}_o(t)$
$\hat{v}_o(t)$
+
−
(c)

Figure 1.11 Averaged small-signal models of the (a) Buck, (b) Boost, and (c) Buck–Boost converters.

of the control-to-output transfer function, or any other input-output transfer function, can be accomplished via straightforward linear circuit analysis. The results and further details can be found in [1]. If needed, dynamic effects of the output capacitor ESR can be included as well, following [124].

Note that the above-mentioned small-signal models depend on the *average* converter operating point (V_g, I_o, D). This fact is compatible with the basic idea behind the averaged modeling approach that low-frequency dynamics are described accurately, while approximations inherent to the method are tolerated in the proximity and above the Nyquist rate. In contrast, as discussed further in Chapter 3, the discrete-time small-signal models depend on the converter waveforms *at a specific point in time*.

1.4 STATE-SPACE AVERAGING

State-space averaging [119, 120] presents a general mathematical formulation for the averaged small-signal modeling approach summarized in Section 1.3.1. In this formulation, the averaged model is derived in a state-space representation form.

Consider the converter operation as alternating between *two* topological states S_0 and S_1, each described by a *linear* set of state-space equations,

$$\begin{aligned} \frac{d\boldsymbol{x}}{dt} &= \boldsymbol{A}_c\boldsymbol{x}(t) + \boldsymbol{B}_c\boldsymbol{v}(t), \\ \boldsymbol{y}(t) &= \boldsymbol{C}_c\boldsymbol{x}(t) + \boldsymbol{E}_c\boldsymbol{v}(t), \end{aligned} \tag{1.27}$$

where $\boldsymbol{x}$, $\boldsymbol{v}$, and $\boldsymbol{y}$ represent the state, input, and output vectors, respectively. Matrices $\boldsymbol{A}_c$, $\boldsymbol{B}_c$, $\boldsymbol{C}_c$, and $\boldsymbol{E}_c$ define the state-space model of the converter for each subtopology, with $c \in \{0, 1\}$ being the PWM signal denoting the topological state.

In general, the converter state-space equations can be written, using the PWM signal $c(t)$ and its complement $c'(t) = 1 - c(t)$, as

$$\begin{aligned} \frac{d\boldsymbol{x}}{dt} &= c(t)\left[\boldsymbol{A}_1\boldsymbol{x}(t) + \boldsymbol{B}_1\boldsymbol{v}(t)\right] + c'(t)\left[\boldsymbol{A}_0\boldsymbol{x}(t) + \boldsymbol{B}_0\boldsymbol{v}(t)\right], \\ \boldsymbol{y}(t) &= c(t)\left[\boldsymbol{C}_1\boldsymbol{x}(t) + \boldsymbol{E}_1\boldsymbol{v}(t)\right] + c'(t)\left[\boldsymbol{C}_0\boldsymbol{x}(t) + \boldsymbol{E}_0\boldsymbol{v}(t)\right]. \end{aligned} \tag{1.28}$$

It is possible now to apply the moving average operator $\langle \cdot \rangle_{T_s}$ to both sides of the foregoing equations. Under the small-ripple or linear-ripple approximations already introduced in Section 1.2, an averaged, large-signal state-space model is obtained,

$$\begin{aligned} \frac{d\overline{\boldsymbol{x}}}{dt} &= \left[d(t)\boldsymbol{A}_1 + d'(t)\boldsymbol{A}_0\right]\overline{\boldsymbol{x}}(t) + \left[d(t)\boldsymbol{B}_1 + d'(t)\boldsymbol{B}_0\right]\overline{\boldsymbol{v}}(t), \\ \overline{\boldsymbol{y}}(t) &= \left[d(t)\boldsymbol{C}_1 + d'(t)\boldsymbol{C}_0\right]\overline{\boldsymbol{x}}(t) + \left[d(t)\boldsymbol{E}_1 + d'(t)\boldsymbol{E}_0\right]\overline{\boldsymbol{v}}(t). \end{aligned} \tag{1.29}$$

As expected, the moving average operator smooths out the time-varying nature of the system, and the system is modeled by a time-invariant, nonlinear set of state-space equations. From this point on, one proceeds with the evaluation of the converter steady-state operating point and with the perturbation/linearization step to obtain the small-signal model.

1.4.1 Converter Steady-State Operating Point

The average steady-state operating point is found from (1.29) by imposing constant inputs $d = D$ and $\overline{\boldsymbol{v}}(t) = \boldsymbol{V}$ and corresponding constant averaged state and output vectors $\overline{\boldsymbol{x}}(t) = \boldsymbol{X}$ and $\overline{\boldsymbol{y}}(t) = \boldsymbol{Y}$,

$$\begin{aligned} 0 &= [D\boldsymbol{A}_1 + D'\boldsymbol{A}_0]\,\boldsymbol{X} + [D\boldsymbol{B}_1 + D'\boldsymbol{B}_0]\,\boldsymbol{V}, \\ \boldsymbol{Y} &= [D\boldsymbol{C}_1 + D'\boldsymbol{C}_0]\,\boldsymbol{X} + [D\boldsymbol{E}_1 + D'\boldsymbol{E}_0]\,\boldsymbol{V}. \end{aligned} \tag{1.30}$$

The first equation, in particular, expresses in a general form the inductor volt-second and capacitor charge balance principles. It corresponds to solving the converter network under the assumptions that $\overline{i}_L(t)$ and $\overline{v}_C(t)$ are *constants* of unknown magnitudes.

With the definitions

$$\begin{aligned} \boldsymbol{A} &\triangleq D\boldsymbol{A}_1 + D'\boldsymbol{A}_0, \\ \boldsymbol{B} &\triangleq D\boldsymbol{B}_1 + D'\boldsymbol{B}_0, \\ \boldsymbol{C} &\triangleq D\boldsymbol{C}_1 + D'\boldsymbol{C}_0, \\ \boldsymbol{E} &\triangleq D\boldsymbol{E}_1 + D'\boldsymbol{E}_0, \end{aligned} \tag{1.31}$$

one finds the steady-state solution for the states and the outputs,

$$\begin{aligned} \boldsymbol{X} &= -\boldsymbol{A}^{-1}\boldsymbol{B}\boldsymbol{V}, \\ \boldsymbol{Y} &= \left[-\boldsymbol{C}\boldsymbol{A}^{-1}\boldsymbol{B} + \boldsymbol{E}\right]\boldsymbol{V}. \end{aligned} \tag{1.32}$$

1.4.2 Averaged Small-Signal State-Space Model

One is now in the position to linearize (1.29) around the converter steady-state operating point $(\boldsymbol{V}, D)$. As usual, all the relevant quantities are expressed in terms of their steady-state value and small-signal ac component as

$$\begin{aligned} \hat{\overline{\boldsymbol{x}}}(t) &\triangleq \overline{\boldsymbol{x}}(t) - \boldsymbol{X}, \\ \hat{d}(t) &\triangleq d(t) - D, \\ \hat{\overline{\boldsymbol{v}}}(t) &\triangleq \overline{\boldsymbol{v}}(t) - \boldsymbol{V}. \end{aligned} \tag{1.33}$$

The state-space averaged, small-signal model of the converter is then

$$\boxed{\begin{aligned} \frac{d\hat{\overline{\boldsymbol{x}}}}{dt} &= \boldsymbol{A}\hat{\overline{\boldsymbol{x}}}(t) + \boldsymbol{F}\hat{d}(t) + \boldsymbol{B}\hat{\overline{\boldsymbol{v}}}(t), \\ \hat{\overline{\boldsymbol{y}}}(t) &= \boldsymbol{C}\hat{\overline{\boldsymbol{x}}}(t) + \boldsymbol{G}\hat{d}(t) + \boldsymbol{E}\hat{\overline{\boldsymbol{v}}}(t), \end{aligned}} \tag{1.34}$$

with

$$\boxed{\begin{aligned} \boldsymbol{F} &\triangleq (\boldsymbol{A}_1\boldsymbol{X} + \boldsymbol{B}_1\boldsymbol{V}) - (\boldsymbol{A}_0\boldsymbol{X} + \boldsymbol{B}_0\boldsymbol{V}), \\ \boldsymbol{G} &\triangleq (\boldsymbol{C}_1\boldsymbol{X} + \boldsymbol{E}_1\boldsymbol{V}) - (\boldsymbol{C}_0\boldsymbol{X} + \boldsymbol{E}_0\boldsymbol{V}). \end{aligned}} \tag{1.35}$$

Assume now an initial unperturbed condition $\hat{\bar{\boldsymbol{x}}}(0) = 0$ and derive the system's forced response via Laplace transformation of (1.34),

$$\begin{aligned} s\hat{\bar{\boldsymbol{x}}}(s) &= \boldsymbol{A}\hat{\bar{\boldsymbol{x}}}(s) + \boldsymbol{F}\hat{d}(s) + \boldsymbol{B}\hat{\bar{\boldsymbol{v}}}(s) \\ \hat{\bar{\boldsymbol{y}}}(s) &= \boldsymbol{C}\hat{\bar{\boldsymbol{x}}}(s) + \boldsymbol{G}\hat{d}(s) + \boldsymbol{E}\hat{\bar{\boldsymbol{v}}}(s) \\ \Rightarrow \hat{\bar{\boldsymbol{y}}}(s) &= \left(\boldsymbol{C}\left(s\boldsymbol{I} - \boldsymbol{A}\right)^{-1}\boldsymbol{F} + \boldsymbol{G}\right)\hat{d}(s) + \left(\boldsymbol{C}\left(s\boldsymbol{I} - \boldsymbol{A}\right)^{-1}\boldsymbol{B} + \boldsymbol{E}\right)\hat{\bar{\boldsymbol{v}}}(s). \end{aligned} \tag{1.36}$$

From this result, one can derive transfer functions needed for control design purposes. For instance, the *control transfer matrix*, which relates the effect of the control command on the converter outputs, is

$$\boxed{\boldsymbol{W}(s) \triangleq \left.\frac{\hat{\bar{\boldsymbol{y}}}(s)}{\hat{d}(s)}\right|_{\hat{\bar{\boldsymbol{v}}}=0} = \boldsymbol{C}\left(s\boldsymbol{I} - \boldsymbol{A}\right)^{-1}\boldsymbol{F} + \boldsymbol{G}}, \tag{1.37}$$

whereas the *disturbance transfer matrix* is

$$\boxed{\boldsymbol{W}_D(s) \triangleq \left.\frac{\hat{\bar{\boldsymbol{y}}}(s)}{\hat{\bar{\boldsymbol{v}}}(s)}\right|_{\hat{d}=0} = \boldsymbol{C}\left(s\boldsymbol{I} - \boldsymbol{A}\right)^{-1}\boldsymbol{B} + \boldsymbol{E}}. \tag{1.38}$$

1.4.3 Boost Converter Example

As an example, the state-space averaged small-signal model of the nonideal Boost converter illustrated in Fig. 1.3 is derived in this section.

With the switch in position 1, one has

$$\frac{di_L}{dt} = \frac{v_g(t) - r_L i_L(t)}{L} \tag{1.39}$$

for the inductor loop equation and

$$\frac{dv_C}{dt} = \frac{dv_o}{dt} = -\frac{v_C(t)}{R_o C} \tag{1.40}$$

for the capacitor node equation. Observe that, in this example, $v_o(t) = v_C(t)$ as zero ESR is assumed for the output capacitor.

Having defined the state vector as $\boldsymbol{x} \triangleq [i_L \quad v_C]^T = [i_L \quad v_o]^T$, the state equation of subtopology 1 is

$$\frac{d\boldsymbol{x}}{dt} = \underbrace{\begin{bmatrix} -\dfrac{r_L}{L} & 0 \\ 0 & -\dfrac{1}{R_o C} \end{bmatrix}}_{\boldsymbol{A}_1} \boldsymbol{x}(t) + \underbrace{\begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}}_{\boldsymbol{B}_1} v_g(t). \tag{1.41}$$

With the switch in position 0, on the other hand, one has

$$\frac{di_L}{dt} = \frac{v_g(t) - r_L i_L(t) - v_o(t)}{L} \tag{1.42}$$

and

$$\frac{dv_o}{dt} = \frac{i_L(t)}{C} - \frac{v_o(t)}{R_o C}. \tag{1.43}$$

The state equation relative to subtopology 0 is then

$$\frac{d\boldsymbol{x}}{dt} = \underbrace{\begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{R_o C} \end{bmatrix}}_{\boldsymbol{A}_0} \boldsymbol{x}(t) + \underbrace{\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}}_{\boldsymbol{B}_0} v_g(t). \tag{1.44}$$

Define now the system output to coincide with the state vector, that is, $\boldsymbol{y}(t) = \boldsymbol{x}(t)$, and therefore $\boldsymbol{C}_1 = \boldsymbol{C}_0 = \boldsymbol{I}$ and $\boldsymbol{E}_1 = \boldsymbol{E}_0 = 0$. Matrices $\boldsymbol{A}$, $\boldsymbol{B}$, and $\boldsymbol{C}$ of the averaged model can then be evaluated. The result is

$$\begin{aligned} \boldsymbol{A} &\triangleq D\boldsymbol{A}_1 + D'\boldsymbol{A}_0 = \begin{bmatrix} -\frac{r_L}{L} & -\frac{D'}{L} \\ \frac{D'}{C} & -\frac{1}{R_o C} \end{bmatrix}, \\ \boldsymbol{B} &\triangleq D\boldsymbol{B}_1 + D'\boldsymbol{B}_0 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}, \\ \boldsymbol{C} &\triangleq D\boldsymbol{C}_1 + D'\boldsymbol{C}_0 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}. \end{aligned} \tag{1.45}$$

Solving for the converter operating point according to (1.32) yields

$$\boldsymbol{X} = \begin{bmatrix} I_L \\ V_o \end{bmatrix} = \begin{bmatrix} \frac{1}{r_L + D'^2 R_o} \\ \frac{1}{D'} \frac{1}{1 + \frac{r_L}{D'^2 R_o}} \end{bmatrix} V_g. \tag{1.46}$$

As expected, this is the same result as (1.12).

As for the small-signal model, as $\boldsymbol{B}_1 = \boldsymbol{B}_0$, matrix $\boldsymbol{F}$ evaluates as

$$\boldsymbol{F} = (\boldsymbol{A}_1 - \boldsymbol{A}_0)\,\boldsymbol{X} = \begin{bmatrix} \dfrac{V_o}{L} \\ \\ -\dfrac{I_L}{C} \end{bmatrix}, \tag{1.47}$$

whereas $\boldsymbol{G} = 0$ as $\boldsymbol{C}_1 = \boldsymbol{C}_0$. The control transfer matrix is

$$\begin{aligned} \boldsymbol{W}(s) = \boldsymbol{C}\,(s\boldsymbol{I} - \boldsymbol{A})^{-1}\,\boldsymbol{F} + \boldsymbol{G} &= \begin{bmatrix} G_{id}(s) \triangleq \dfrac{\hat{\tilde{i}}_L(s)}{\hat{d}(s)} \\ \\ G_{vd}(s) \triangleq \dfrac{\hat{\tilde{v}}_o(s)}{\hat{d}(s)} \end{bmatrix} \\ &= \begin{bmatrix} \dfrac{2V_o}{r_L + D'^2 R_o}\,\dfrac{1 + s\frac{R_o C}{2}}{\Delta(s)} \\ \\ \dfrac{V_o}{D'}\,\dfrac{1 - \frac{r_L}{D'^2 R_o}}{1 + \frac{r_L}{D'^2 R_o}}\,\dfrac{1 - s\frac{L}{D'^2 R_o - r_L}}{\Delta(s)} \end{bmatrix}, \end{aligned} \tag{1.48}$$

with

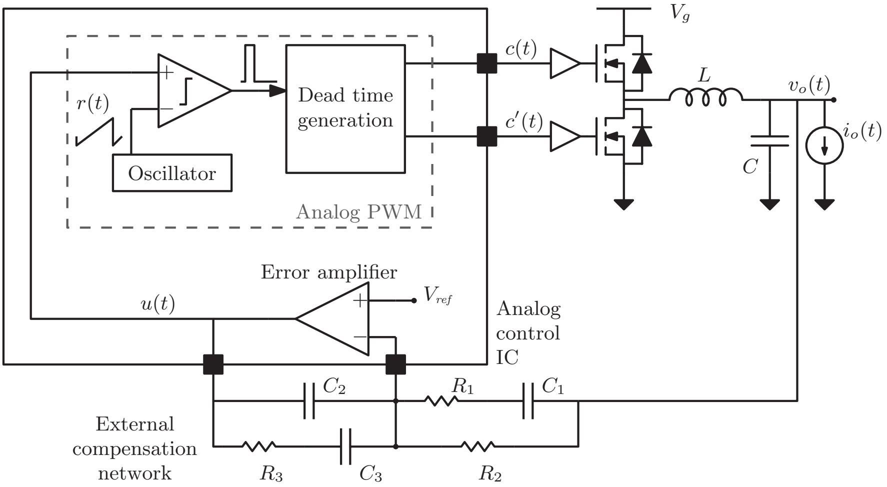
$$\Delta(s) \triangleq 1 + s\frac{r_L}{D'^2 R_o}\left(\frac{R_o C + \frac{L}{r_L}}{1 + \frac{r_L}{D'^2 R_o}}\right) + s^2 \frac{LC}{D'^2}\,\frac{1}{1 + \frac{r_L}{D'^2 R_o}}. \tag{1.49}$$

1.5 DESIGN EXAMPLES

This section presents some examples of analog control designs based on the converter small-signal models developed in Sections 1.3.1 and 1.4 and standard frequency-domain-based compensator design techniques.

1.5.1 Voltage-Mode Control of a Synchronous Buck Converter

Figure 1.12 illustrates an implementation example for an analog voltage-mode controller in the system of Fig. 1.6. The system makes use of an analog integrated circuit containing an error amplifier and an analog pulse width modulator. The control compensation is implemented via an external passive network, which shapes the response of the error amplifier.



V_g
$c(t)$
$c'(t)$
L
$v_o(t)$
$i_o(t)$
C
$r(t)$
Dead time generation
Oscillator
Analog PWM
Error amplifier
V_{ref}
$u(t)$
Analog control IC
C_2
R_1
C_1
External compensation network
R_3
C_3
R_2

Figure 1.12 Synchronous Buck example: analog voltage-mode control scheme.

TABLE 1.2 Synchronous Buck Example Parameters

Parameter	Value
Input voltage V_g	5 V
Output voltage V_o	1.8 V
Load current $I_{o,max}$	5 A
Switching frequency f_s	1 MHz
Filter inductance L	1 μH
Inductor series resistance r_L	30 mΩ
Filter capacitance C	200 μF
Capacitor equivalent series resistance r_C	0.8 mΩ
PWM carrier amplitude V_r	1 V
Voltage sensing gain H	1 V/V

Design specifications and power stage parameters are summarized in Table 1.2. As reported in the table, the power stage nonidealities include a nonzero inductor series resistance r_L and a nonzero capacitor ESR r_C.

The small-signal model of the system is presented in Section 1.3, and the uncompensated loop gain expression is given in (1.26). The magnitude and phase Bode plots of $T_u(s)$ are shown in Fig. 1.13. The dc value of the uncompensated loop gain is

$$T_{u0} \triangleq T_u(s=0) = \frac{G_{vd0}}{V_r} H = \frac{V_g}{V_r} = 5 \Rightarrow 14 \text{ dB}. \tag{1.50}$$

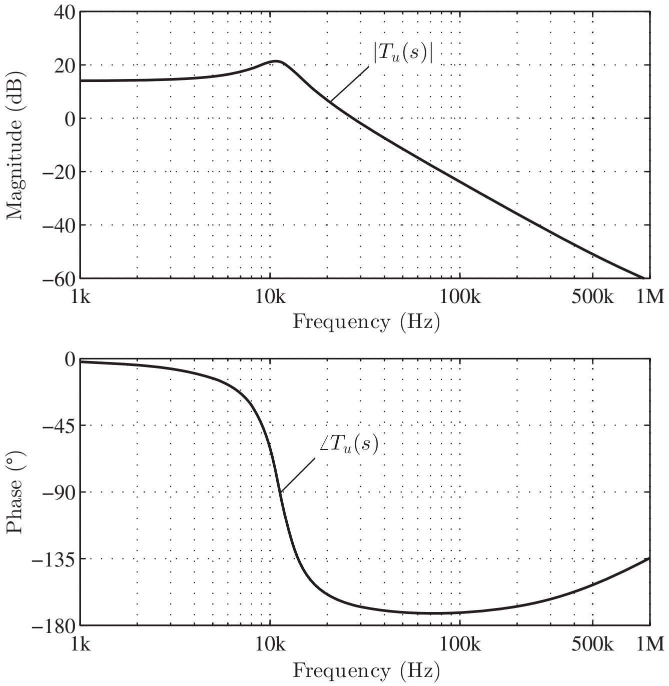


Figure 1.13 Synchronous Buck example: Bode plots of the uncompensated loop gain $T_u(s)$.

The system resonance occurs at

$$\omega_0 = \frac{1}{\sqrt{LC}} \approx 2\pi \cdot (11 \text{ kHz}), \tag{1.51}$$

while the r_C-related zero is located at

$$\omega_{ESR} = \frac{1}{r_C C} \approx 2\pi \cdot (1 \text{ MHz}). \tag{1.52}$$

As a design goal, the target crossover frequency is set at $f_c = 100$ kHz, that is, $1/10$ of the converter switching frequency, and a phase margin target is set at $\varphi_m = 55°$. At $f = f_c$, the uncompensated loop gain exhibits a phase of about $-171°$, implying that a *lead* type of compensation is required in the neighborhood of f_c to boost the phase margin by $\theta = 46°$. Such compensation is obtained by forming a pole-zero pair

$$G_{PD}(s) \triangleq G_{PD0} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}}. \tag{1.53}$$

Subscript *PD* stands for *proportional-derivative*, which is a term commonly used for the lead compensation.

The maximum phase boost generated by the *PD* pole-zero pair occurs at

$$\omega_{max} = \sqrt{\omega_z \omega_p} \tag{1.54}$$

and that it equals

$$\angle G_{PD}(j\omega_{max}) = \arctan\left(\sqrt{\frac{\omega_p}{\omega_z}}\right) - \arctan\left(\sqrt{\frac{\omega_z}{\omega_p}}\right) = \frac{\pi}{2} - 2\arctan\left(\sqrt{\frac{\omega_z}{\omega_p}}\right). \tag{1.55}$$

As the phase lead provided by the compensator should be equal to $\theta = 46°$, the required ω_z/ω_p ratio can be found from (1.55) which, using $\omega_c = \omega_{max} = \sqrt{\omega_z \omega_p}$, yields the values of both ω_z and ω_p,

$$\begin{aligned} \omega_z &= \omega_c\sqrt{\frac{1-\sin\theta}{1+\sin\theta}} = 2\pi\cdot(40\ \text{kHz}), \\ \omega_p &= \omega_c\sqrt{\frac{1+\sin\theta}{1-\sin\theta}} = 2\pi\cdot(250\ \text{kHz}). \end{aligned} \tag{1.56}$$

The dc gain G_{PD0} of the lead action is determined by imposing unity loop gain at the desired crossover frequency f_c,

$$|T(j\omega_c)| = |T_u(j\omega_c)|G_{PD0}\sqrt{\frac{1+\left(\frac{\omega_c}{\omega_z}\right)^2}{1+\left(\frac{\omega_c}{\omega_p}\right)^2}} = 1, \tag{1.57}$$

which yields

$$G_{PD0} = \frac{1}{|T_u(j\omega_c)|}\sqrt{\frac{1+\left(\frac{\omega_c}{\omega_p}\right)^2}{1+\left(\frac{\omega_c}{\omega_z}\right)^2}} \approx 6.2 \Rightarrow 15.8\ \text{dB}. \tag{1.58}$$

Figure 1.14 illustrates the magnitude and phase Bode plots of the lead compensation.

As a last design step, adding an integral action, that is, a compensation pole at dc nulls the steady-state regulation error and, more generally, improves the regulation by increasing the low-frequency loop gain magnitude. This is accomplished by including a *lag* term of the type

$$G_{PI}(s) \triangleq G_{PI\infty}\left(1 + \frac{\omega_l}{s}\right). \tag{1.59}$$

Such term is also known as *proportional–integral* (PI) compensation.

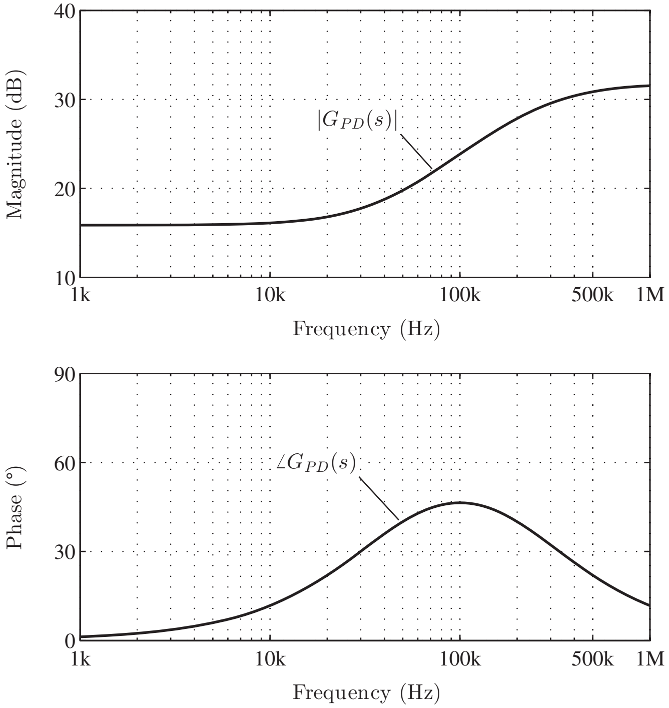


Figure 1.14 Synchronous Buck example: Bode plots of the lead (*PD*) compensation transfer function.

As a general rule, the *PI* term should not significantly affect either the system crossover frequency or its phase margin. Therefore, the high-frequency gain $G_{PI\infty}$ is set to one, and the zero corner frequency ω_l is selected such that $\omega_l \ll \omega_c$. A good choice is to let $\omega_l < \omega_c/10 = 2\pi \cdot (10\text{ kHz})$. In this design example, choose

$$\omega_l = 2\pi \cdot (8\text{ kHz})\,. \tag{1.60}$$

The complete *proportional-integral-derivative* (PID) compensator transfer function is therefore

$$G_{PID}(s) = \underbrace{\left(1 + \frac{\omega_l}{s}\right)}_{PI} \cdot \underbrace{G_{PD0}\frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}}}_{PD}\,, \tag{1.61}$$

where all the corner frequencies and gains are now determined. Figure 1.15 shows Bode plots of the designed PID compensator transfer function.

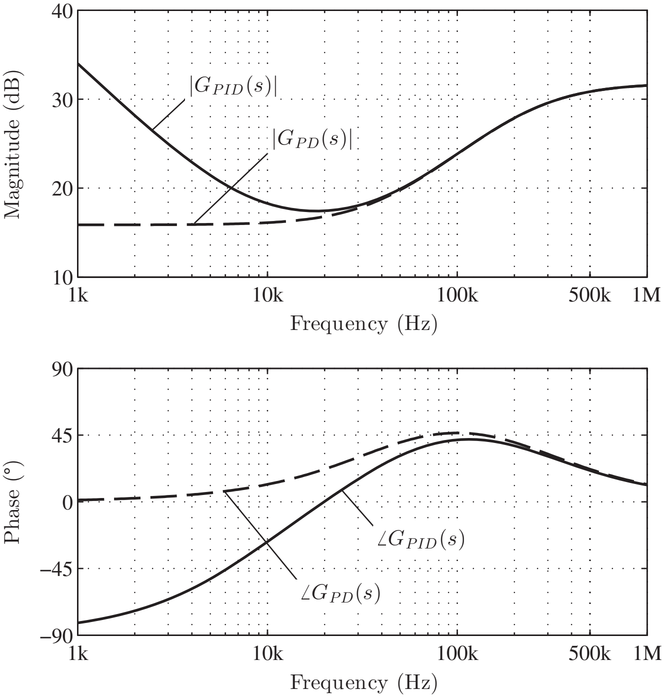


Figure 1.15 Synchronous Buck converter example: Bode plots of the lead (*PD*) and *PID* compensation transfer functions.

Going back to the external compensation network depicted in Figure 1.12, assuming $C_3 \gg C_2$ the corresponding transfer function is

$$G_c(s) \triangleq -\frac{\hat{u}(s)}{\hat{\bar{v}}_o(s)} = \underbrace{\left(1 + \frac{1}{sR_3C_3}\right)}_{PI} \cdot \underbrace{\frac{R_3}{R_2}\frac{1 + s\left(R_1 + R_2\right)C_1}{1 + sR_1C_1}}_{PD} \cdot \underbrace{\frac{1}{1 + sR_3C_2}}_{HF\ Pole}, \tag{1.62}$$

where the different portions of the control action have been highlighted. Circuit-level design of the compensation network can now be performed by equating (1.61) and (1.62). Note that (1.62) allows for an additional high-frequency pole to be placed at

$$\omega_{p_2} \triangleq \frac{1}{R_3C_2}. \tag{1.63}$$

Such pole is commonly used to attenuate the gain of the compensator at high frequencies and prevent the propagation of switching harmonics produced by the converter through the feedback loop—a circumstance that can otherwise result in undesired effects. A good choice for ω_{p_2} is

$$\omega_{p_2} = 10\omega_c = 2\pi \cdot (1\ \mathrm{MHz}), \tag{1.64}$$

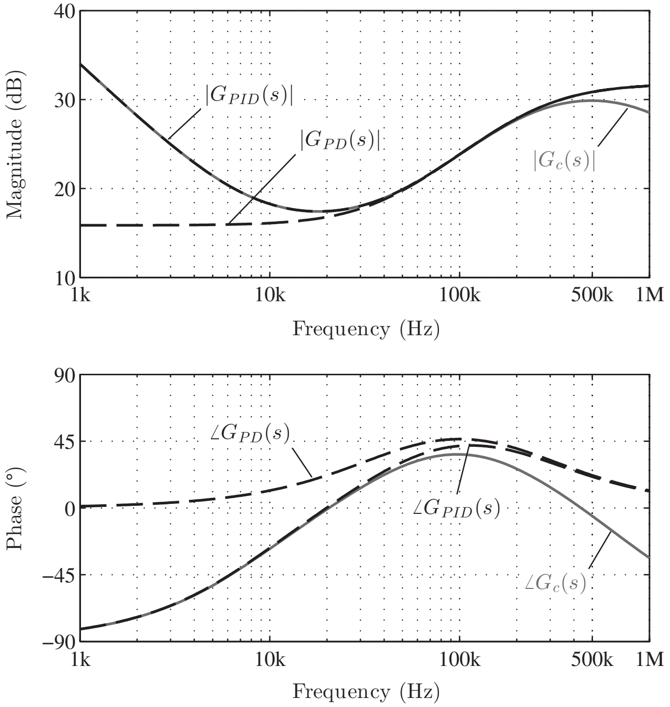


Figure 1.16 Synchronous Buck example: Bode plots of the lead (*PD*), *PID*, and overall compensation transfer functions.

which ensures that the added pole has limited impact on the designed phase margin. Figure 1.16 compares the Bode plots of $G_{PD}(s)$, $G_{PID}(s)$, and $G_c(s)$, while the magnitude and phase responses of the system loop gain are shown in Fig. 1.17. The combined effects of the low-frequency PI term and the high-frequency pole on the overall compensator transfer function lead to $\approx 10°$ phase margin loss with respect to the target $\varphi_m = 55°$. Such phase margin loss could be easily considered by imposing a correspondingly higher value on φ_m in the above-mentioned design procedure.

The above-mentioned compensator design can now be validated—and refined, if needed—via computer simulations. To this end, a Matlab® model of the voltage-controlled Buck converter pictured in Fig. 1.12 has been set up. The scheme depicted in Fig. 1.18 employs Middlebrook's approach [1, 78] to obtain $T(s)$ by simulation and to validate the averaged small-signal models employed in the design phase [1]. The closed-loop system is excited by a sinusoidal perturbation $u_{pert}(t)$ of small amplitude at frequency ω_{pert}. Signals $u_x(t)$ and $u_y(t)$ are acquired over a number of oscillation periods, and their Fourier components $u_x(\omega_{pert})$ and $u_y(\omega_{pert})$ at ω_{pert} are determined via an FFT-based postprocessing. The procedure is repeated for a number of perturbation frequencies, in order to extract the simulated loop gain

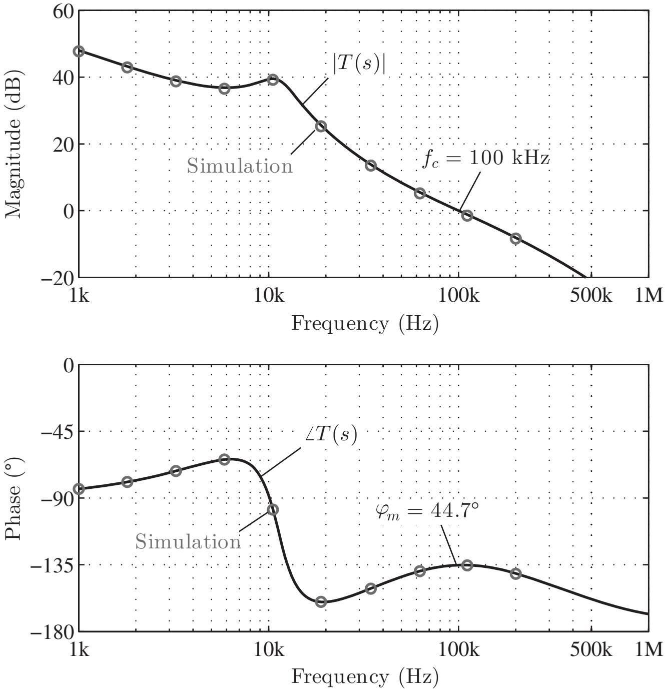


Figure 1.17 Synchronous Buck example: Bode plots of the theoretical and simulated system loop gain.

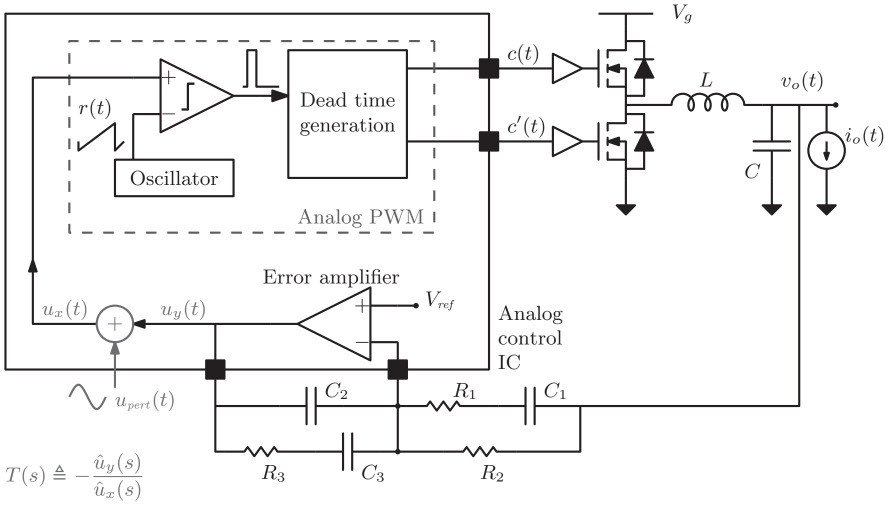

V_g
$c(t)$
$c'(t)$
L
$v_o(t)$
$i_o(t)$
C
$r(t)$
Dead time generation
Oscillator
Analog PWM
Error amplifier
V_{ref}
Analog control IC
$u_x(t)$
$u_y(t)$
$u_{pert}(t)$
C_2
R_1
C_1
R_3
C_3
R_2
$T(s) \triangleq -\frac{\hat{u}_y(s)}{\hat{u}_x(s)}$

Figure 1.18 Synchronous Buck example: simulation of the system loop gain $T(s)$.

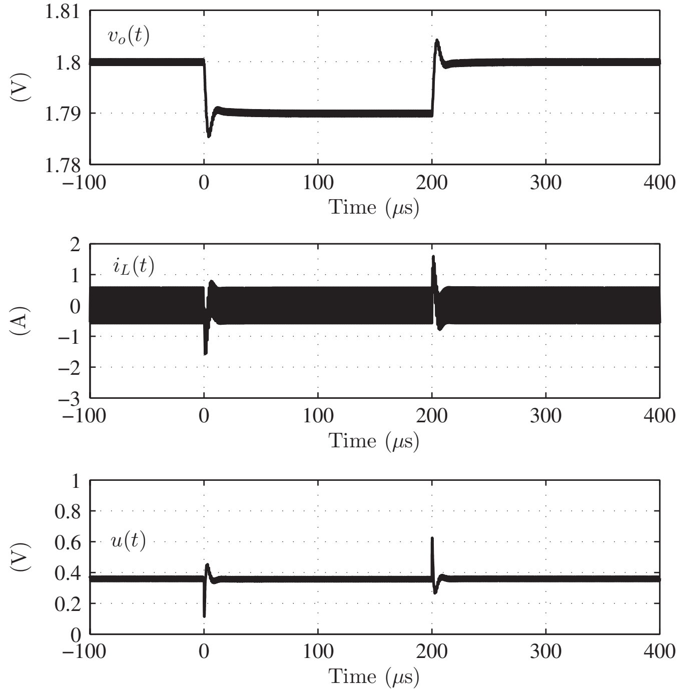


Figure 1.19 Synchronous Buck example: 1.79 V ↔ 1.8 V step reference responses.

$T_{sim}(j\omega_{pert})$ as

$$T_{sim}(j\omega_{pert}) = -\frac{u_y(\omega_{pert})}{u_x(\omega_{pert})}. \tag{1.65}$$

Simulation points thus determined are superimposed to the theoretical loop gain Bode plots in Fig. 1.17.

Figure 1.19 illustrates the simulated response of the closed-loop system to a 10 mV step of the reference voltage, from 1.79 to 1.8 V and then back to 1.79 V, while Fig. 1.20 reports the simulated response of the system to an abrupt step in the load current, from 2.5 to 5 A and then back to 2.5 A. The observed closed-loop transient responses correlate well with the expectations based on the values of the crossover frequency and phase margin in this design example.

Regarding the step load response, one important quantity to be evaluated at design stage is the *closed-loop output impedance* $Z_{o,cl}(s)$, defined as the converter small-signal output impedance evaluated with the control loop closed,

$$Z_{o,cl}(s) \triangleq -\left.\frac{\hat{\tilde{v}}_o(s)}{\hat{\tilde{i}}_o(s)}\right|_{\hat{\tilde{v}}_{ref}=0,\hat{\tilde{v}}_g=0}. \tag{1.66}$$

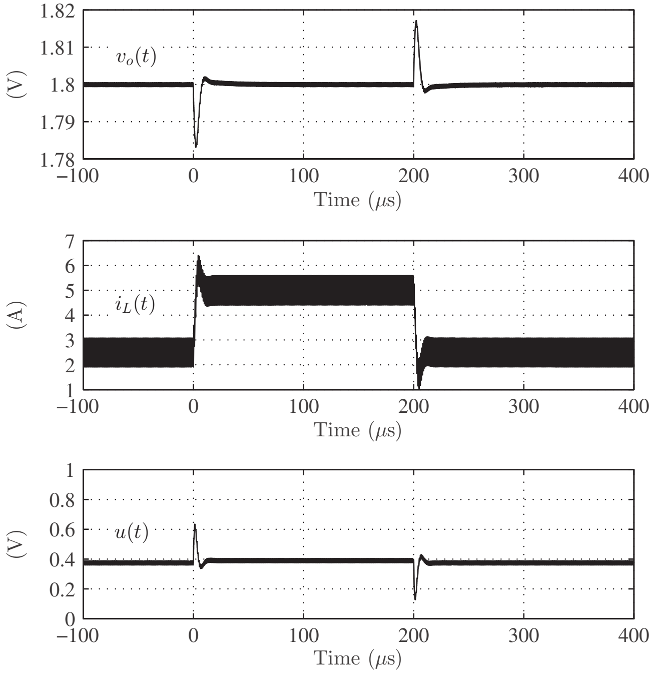


Figure 1.20 Synchronous Buck example: 2.5 A ↔ 5 A step load responses.

The closed-loop output impedance $Z_{o,cl}(s)$ can be expressed in terms of the converter *open-loop output impedance* $Z_o(s)$ and the system loop gain as [1]

$$Z_{o,cl}(s) = \frac{Z_o(s)}{1 + T(s)}, \tag{1.67}$$

with

$$Z_o(s) \triangleq - \left. \frac{\hat{v}_o(s)}{\hat{i}_o(s)} \right|_{\hat{u}=0, \hat{v}_g=0} . \tag{1.68}$$

The open-loop output impedance is readily evaluated from the averaged small-signal equivalent circuit of the Buck converter (Fig. 1.11),

$$Z_o(s) = r_L \frac{(1 + s r_C C)\left(1 + s \frac{L}{r_L}\right)}{1 + s(r_C + r_L)C + s^2 LC}. \tag{1.69}$$

Bode plots of both $Z_{o,cl}(s)$ and $Z_o(s)$ for the voltage-mode control loop under consideration are shown in Fig. 1.21. Below the control bandwidth, the output impedance

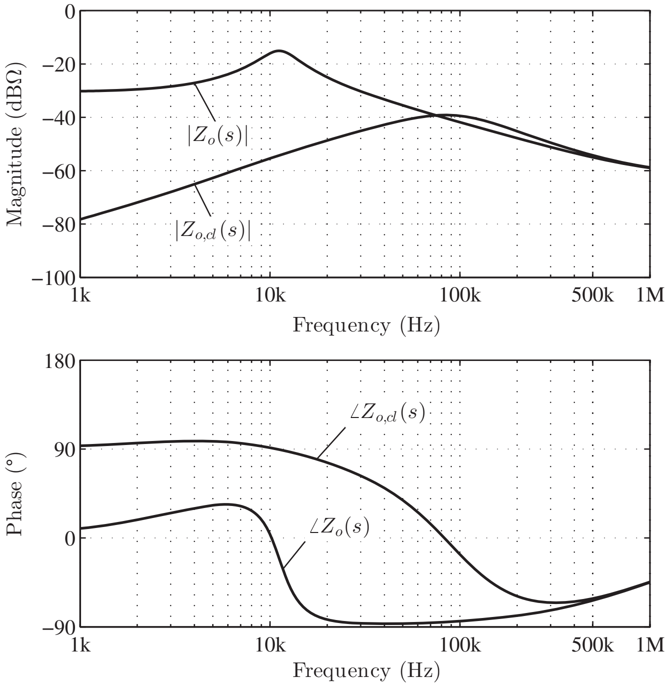


Figure 1.21 Synchronous Buck example: Bode plots of the open-loop and closed-loop output impedances.

is reduced by the feedback loop because of the large loop gain. At higher frequencies, on the other hand, $Z_{o,cl}(s)$ and $Z_o(s)$ practically coincide.

1.5.2 Average Current-Mode Control of a Boost Converter

As a second example, consider average current-mode control of a Boost converter depicted in Fig. 1.22. The converter parameters are listed in Table 1.3.

The Boost converter operates from a dc input voltage $V_g = 120$ V and delivers 500 W maximum power to a resistive load R_o. At the maximum power, the output voltage equals 380 V, so

$$P_o = \frac{V_o^2}{R_o} = \frac{(380 \text{ V})^2}{R_o} = 500 \text{ W} \Rightarrow R_o \approx 289 \; \Omega. \tag{1.70}$$

The Boost inductor current $i_L(t)$ is converted into a voltage $v_s(t)$ by a 0.1 Ω shunt resistor R_{sense} and compared with the control setpoint V_{ref}. The regulation error is processed by an analog compensator implemented by an op-amp-based circuit. A symmetrical (triangle-wave) analog pulse width modulator converts the output $u(t)$ of the error amplifier into the logic gate-drive control $c(t)$.

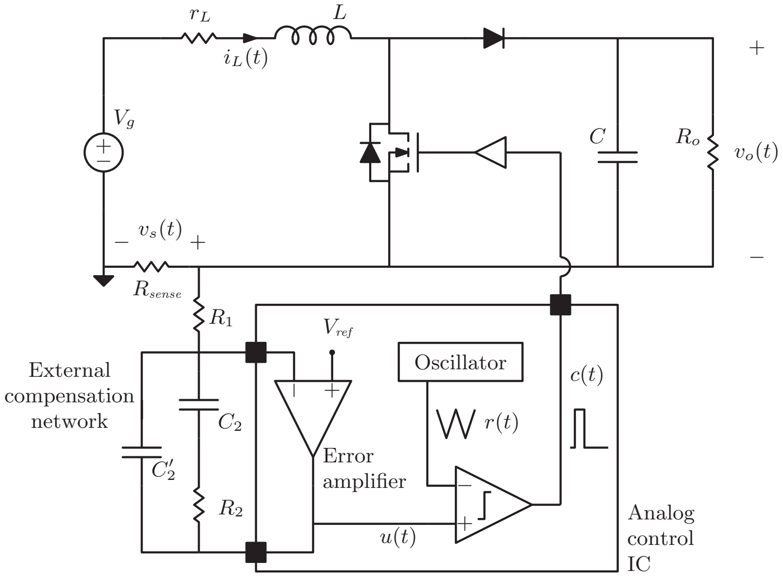

r_L
L
$i_L(t)$
V_g
$-$ $v_s(t)$ $+$
R_{sense}
R_1
C
R_o
$v_o(t)$
$+$
$-$
V_{ref}
Oscillator
$c(t)$
External compensation network
C_2
C_2'
R_2
$r(t)$
Error amplifier
$u(t)$
Analog control IC

Figure 1.22 Average current-mode control of a Boost converter.

TABLE 1.3 Boost Converter Example Parameters

Parameter	**Value**
Input voltage V_g	120 V
Output voltage V_o	380 V
Power rating P_o	500 W
Switching frequency f_s	100 kHz
Filter inductance L	500 μH
Inductor series resistance r_L	20 mΩ
Filter capacitance C	220 μF
PWM carrier amplitude V_r	1 V
Current sensing gain R_{sense}	0.1 Ω

At maximum output power and neglecting parasitics, the steady-state duty cycle is determined from

$$M(D) = \frac{V_o}{V_g} = \frac{380\text{ V}}{120\text{ V}} = \frac{1}{1-D}$$
$$\Rightarrow D \approx 0.68. \tag{1.71}$$

The averaged small-signal model of the Boost converter has been derived in Section 1.4.3. Accounting for the additional sensing resistance R_{sense} is simply accomplished by substituting r_L with $r_L + R_{sense}$,

$$r_L \rightarrow r_L + R_{sense}. \tag{1.72}$$

From (1.48), the control-to-inductor current dynamics, described by the transfer function $G_{id}(s)$, has the form

$$G_{id}(s) = G_{id0} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{{\omega_0}^2}}, \tag{1.73}$$

with

$$\begin{aligned} G_{id0} &= 26.3 \text{ A} \Rightarrow 28.4 \text{ dB}, \\ \omega_z &= 2\pi \cdot (5 \text{ Hz}), \\ \omega_0 &= 2\pi \cdot (152 \text{ Hz}), \\ Q &= 3.7. \end{aligned} \tag{1.74}$$

The uncompensated current loop gain is proportional to $G_{id}(s)$ and equals

$$T_u(s) = \frac{R_{sense}}{V_r} G_{id}(s). \tag{1.75}$$

Bode plots of $G_{id}(s)$ are illustrated in Fig. 1.23. Thanks to the LHP zero located at $s = -\omega_z$, the transfer function retains a -20 dB/decade slope above the system resonance, allowing for a high-bandwidth control to be designed using a simple PI compensation law,

$$G_{PI}(s) = G_{PI\infty} \left(1 + \frac{\omega_{PI}}{s}\right). \tag{1.76}$$

As discussed in the Buck voltage-mode control example, a high-frequency pole can be included in the compensator transfer function in order to provide some filtering action on the harmonic content of the sensed signal. For instance, set such high-frequency pole at half the switching rate, that is, at 50 kHz. With this choice, the compensator transfer function to be designed is

$$G_c(s) = \underbrace{G_{PI\infty} \left(1 + \frac{\omega_{PI}}{s}\right)}_{PI} \cdot \underbrace{\frac{1}{1 + \frac{s}{\omega_{HF}}}}_{HF\ Pole}, \tag{1.77}$$

$$\omega_{HF} = 2\pi \cdot (50 \text{ kHz}). \tag{1.78}$$

On the basis of the transfer function template, the objective is to design a $\omega_c = 2\pi \cdot (10 \text{ kHz})$ bandwidth compensation with a $\varphi_m = 50^\circ$ phase margin. The

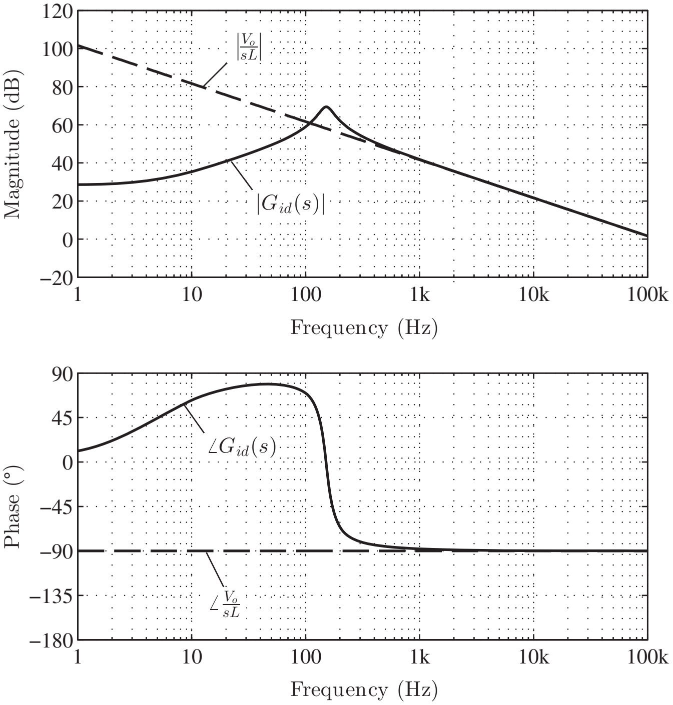


Figure 1.23 Boost converter example: Bode plots of the control-to-inductor current transfer function.

high-frequency pole located at 50 kHz introduces, at the desired control bandwidth, an additional phase *lag* equal to

$$\arctan\left(\frac{10\ \text{kHz}}{50\ \text{kHz}}\right) \approx 11^\circ, \tag{1.79}$$

and therefore the PI portion of the compensation must be designed for a target phase margin of $\varphi'_m = 50^\circ + 11^\circ$. Having clarified this point, calculation of the unknown PI coefficients $G_{PI\infty}$ and ω_{PI} is straightforward once the magnitude and the phase of the system uncompensated loop gain are evaluated at the target control bandwidth, that is, at the target crossover frequency,

$$\begin{aligned} |T_u(j\omega_c)| &\approx 1.2 \Rightarrow 1.6\ \text{dB}, \\ \angle T_u(j\omega_c) &\approx -90^\circ. \end{aligned} \tag{1.80}$$

An alternative, quicker approach to estimate $T_u(s)$ is to employ a high-frequency approximation of $G_{id}(s)$. From (1.48), it is easy to see that, as long as $\omega \gg \omega_0$, one has

$$G_{id}(s) \approx \frac{V_o}{sL} \qquad (\omega \gg \omega_0), \tag{1.81}$$

and therefore the inductor current dynamics behaves almost ideally around the target control bandwidth. This approximation is illustrated in Fig. 1.23 as well. One can verify that (1.81) very accurately predicts the values reported in (1.80).

Derivation of ω_{PI} is based on the required phase margin,

$$-\frac{\pi}{2} + \arctan\left(\frac{\omega_c}{\omega_{PI}}\right) + \angle T_u(j\omega_c) = -\pi + \varphi_m', \tag{1.82}$$

whereas the value of $G_{PI\infty}$ is imposed by the desired crossover frequency ω_c,

$$G_{PI\,\infty}\sqrt{1 + \left(\frac{\omega_c}{\omega_{PI}}\right)^2}\,|T_u(j\omega_c)| = 1. \tag{1.83}$$

Solving the above-mentioned equations yields

$$\begin{aligned} G_{PI\infty} &= 0.73 \Rightarrow -2.7\ \text{dB}, \\ \omega_{PI} &= 2\pi \cdot (5.5\ \text{kHz})\,. \end{aligned} \tag{1.84}$$

Bode plots of the compensator transfer function are shown in Fig. 1.24. Both the uncompensated and compensated current loop gains $T_u(s)$ and $T(s)$ are shown in

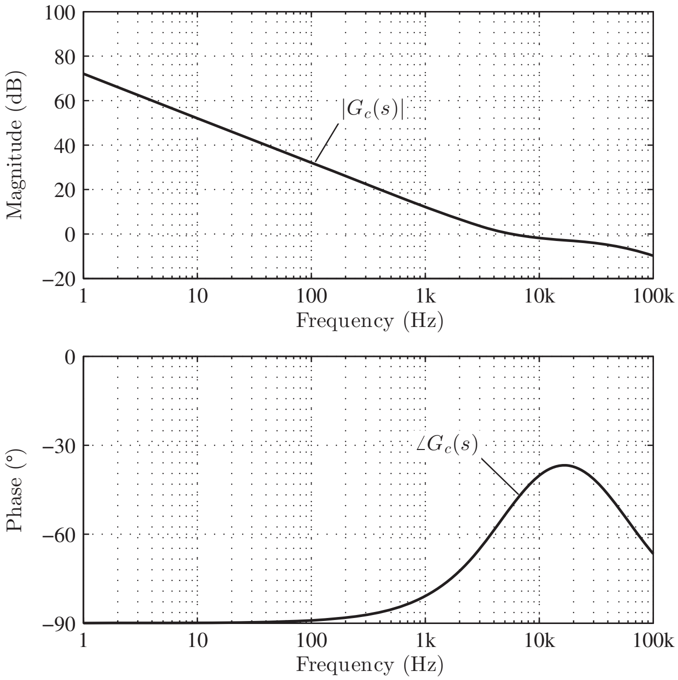


Figure 1.24 Boost converter example: Bode plots of the compensator transfer function.

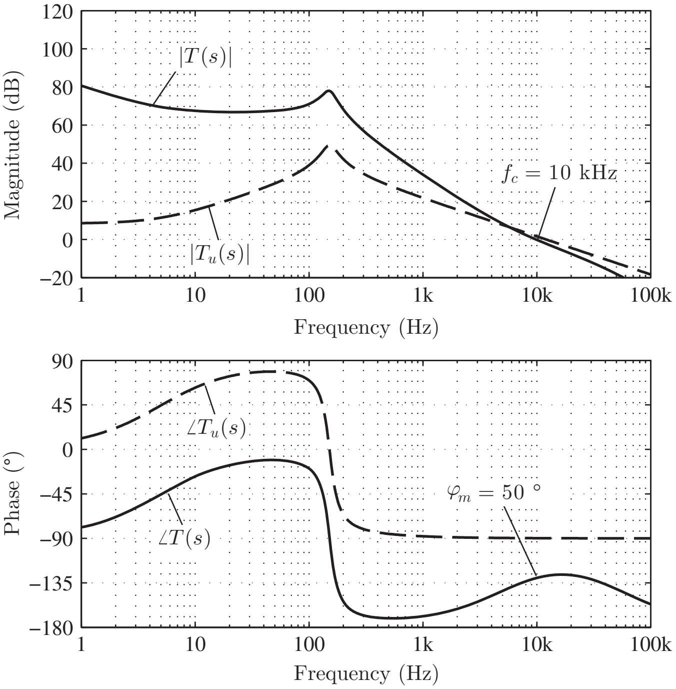


Figure 1.25 Boost converter example: Bode plots of the uncompensated and compensated current loop gains $T_u(s)$ and $T(s)$.

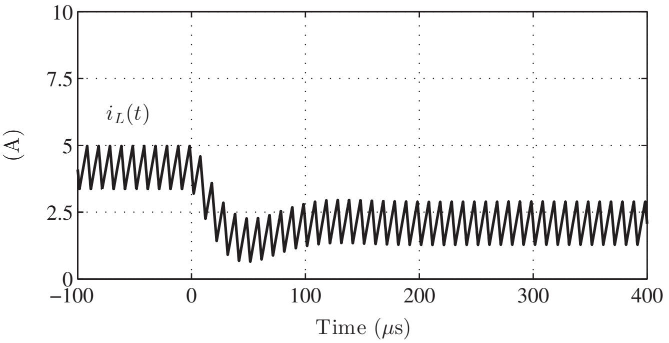


Figure 1.26 Boost converter example: 500 W→250 W step-reference response.

Fig. 1.25. Figure 1.26 illustrates the simulated closed-loop response to a step variation in the current setpoint corresponding to a 500 to 250 W reduction in the input power.

With the compensator transfer function so determined, one is in position to carry out the circuit-level design of the external compensation network (R_1, R_2, C_2, C_2') illustrated in Fig. 1.22. Within the finite gain-bandwidth product limitation of the error amplifier, the compensator transfer function is

$$G_c(s) \triangleq -\frac{\hat{u}(s)}{\hat{v}_o(s)} = \underbrace{\frac{R_2}{R_1}\left(1+\frac{1}{sR_2C_2}\right)}_{PI} \cdot \underbrace{\frac{1}{1+sR_2C_2'}}_{HF\ Pole} \qquad (C_2 \gg C_2'), \tag{1.85}$$

and determination of the compensation network parameters starts by equating (1.85) to (1.77).

1.6 DUTY RATIO *d*[*k*] VERSUS *d*(*t*)

In the foregoing discussions, the *cycle-by-cycle* duty ratio $d[k]$, intended as a discrete-time signal, and $d(t)$, that is, a continuous-time signal that acts as the control input for the converter in the context of averaged models, have intentionally been conflated. Before closing the review of analog (continuous-time) modeling and control in this chapter, it is useful to highlight a few aspects regarding the physical meaning of the duty cycle d as the control input, as well as relationships between $d[k]$ and $d(t)$.

Given the nature of the switched-mode power converter controlled by a PWM waveform, it is clear that a physical meaning can be attributed only to $d[k]$: the converter responds to $d[k]$, not to $d(t)$. Conceptually, the *duty cycle* is a property of a switching *interval* and not of a specific instant in time. Consequently:

The duty ratio is an inherently discrete-time signal, even in analog control.

Nonetheless, $d(t)$ as a continuous-time control signal has been employed in the context of averaged models and analog control of switched-mode converters. One interpretation of $d(t)$ is provided by [125]: $d(t)$ can be described as a baseband continuous-time signal interpolating $d[k]$ at the pulse width modulated switching events $T_k = DT_s + kT_s$,

$$d(t = T_k = kT_s + DT_s) = d[k]. \tag{1.86}$$

More formally, one could intend $d(t)$ as the baseband portion of the PWM output $c(t)$,

$$d(\omega) \triangleq \mathcal{R}(\omega)c(\omega), \tag{1.87}$$

where $\mathcal{R}(\omega)$ is the frequency response of the ideal brick-wall filter,

$$\mathcal{R}(\omega) = \begin{cases} 1, & -\dfrac{\omega_s}{2} < \omega < \dfrac{\omega_s}{2}, \\ 0 & \text{otherwise.} \end{cases} \tag{1.88}$$

This interpretation of $d(t)$ highlights an advantage as well as a limitation of the averaged modeling approach: the converter behavior is studied at frequencies well below the Nyquist rate $f_s/2$, where it behaves as if *continuously* responding to the low-frequency portion of the PWM spectrum. The difference between $d(t)$ and the true converter control input $d[k]$ only becomes important in the proximity and above the Nyquist rate $f_s/2$.

For analog pulse width modulators, it can be shown that $d(t)$ coincides with $u(t)$ itself apart from a scaling factor equal to $1/V_r$ [126]. The control signal then appears unaltered in the baseband of $c(t)$, and the fact that $d(t) = u(t)/V_r$ is in agreement with (1.23). This justifies the common practice in analog modeling to treat $d(t)$ as a scaled version of the analog control command $u(t)$.

The situation is depicted by the qualitative spectra reported in Fig. 1.27. The comparison between analog control signal $u(t)$ and the carrier operated by the comparator produces the sequence $d[k]$ driving the converter. A certain PWM spectrum $c(t)$ and a certain converter response $v_s(t)$ can be associated with $d[k]$.

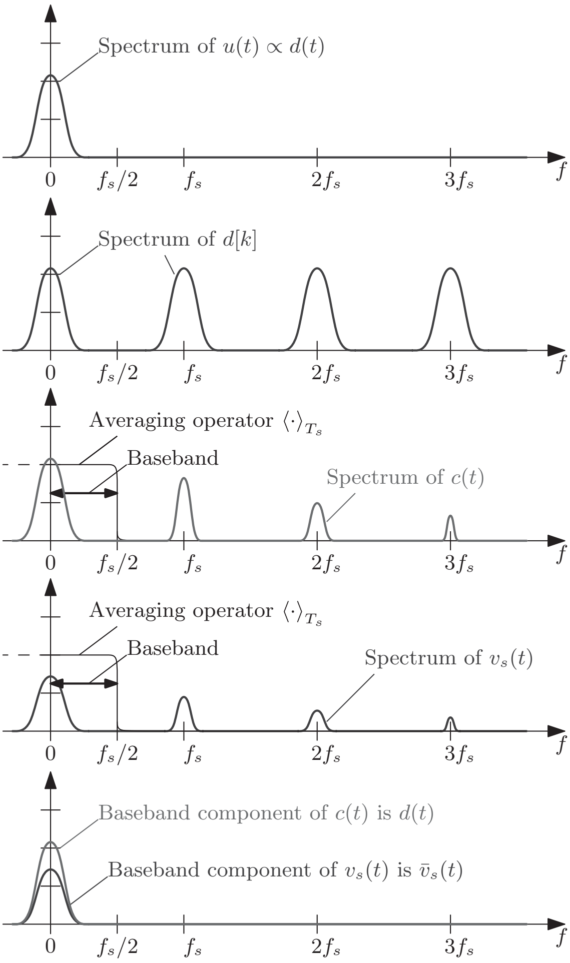


Figure 1.27 Qualitative signal spectra in analog control.

Averaged small-signal modeling, on the other hand, focuses on the baseband portion of $c(t)$ – that is, $d(t)$ – and puts it in relation with the baseband portion of $v_s(t)$, that is, with $\overline{v}_s(t)$.

The assumption that $u(t)$—and therefore $d(t)$—is a baseband signal is never strictly satisfied in practice, as $u(t)$ always includes some amount of switching content as a result of the switching harmonics not entirely filtered by the sensing path or the compensator. Differences between $u(t)$ and $d(t)$ arise when such switching frequency content is significant and make the PWM small-signal gain differ from $1/V_r$. One may note that the effect, usually undesired in PWM converters, is intentionally employed in analog peak current-mode controllers, where adding the compensation ramp to the modulating signal alters the small-signal gain of the modulator [1].

1.7 SUMMARY OF KEY POINTS

- PWM switched-mode power converters alternate between two or more subtopologies in a regular manner. In general, a switched-mode power converter is a time-varying nonlinear system.
- Steady-state analysis of switched-mode power converters is founded upon the volt-second and charge balance equations. Coupled with the small-ripple or linear-ripple approximations, averaged steady-state currents and voltages of the converter can be determined for any given operating point.
- Analysis of converter dynamics is founded upon applying an averaging operator to all converter waveforms. The resulting model is time-invariant but still nonlinear. Perturbation and linearization of the averaged model yields a linear small-signal model, which can be used to obtain all transfer functions relevant for the control design process. The averaged small-signal modeling framework formulates the above-mentioned concepts in terms of equivalent circuits that can be analyzed using conventional circuit analysis techniques. In general, the averaged models are intended to predict converter dynamics at frequencies well below the switching frequency.
- State-space averaging is a general formulation for the averaging/linearization process.
- The duty ratio $d(t)$ used in the continuous-time modeling is intended to represent the baseband component of the PWM signal $c(t)$. The difference between such control input and the true cycle-by-cycle duty ratio $d[k]$ can be neglected in the context of the *averaged* converter dynamics.