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Digital Control of Resonant Converters: Resolution Effects on Limit Cycles

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***Abstract*—The conditions for limit-cycle oscillations in digitally controlled resonant converters are explored theoretically and are tested by simulation and experiment. The analytical analysis reveals that in a manner similar to digital pulsewidth modulation (PWM) control, limit cycles occur in such systems when the LSB of the control changes the output by a value that is larger than the analog-to-digital converter (ADC) resolution. However, in resonant converters, unlike the case of PWM, limit-cycle oscillations depend on the steady-state control input, since both the power stage gain and the resolution of the digitally generated drive frequency are not constant over the operating frequency range. Consequently, at high gains (close to resonance), the required frequency resolution may not be supported by the digital core. A time-domain behavioral simulation model, developed, and experimentally verified, allows the steady-state behavior of digitally controlled resonant converters to be analyzed, including the phenomenon of limit cycles as well as the closed-loop response. A cycle-by-cycle Powersim (PSIM) simulation model of a digitally controlled resonant converter, developed in this study, includes a digital core realization using C code block. This simulation model enables the exploration of the system in fine details. The proposed method of static analysis and dynamic modeling is experimentally verified on a series-resonant parallel-loaded converter operated in closed-current loop. The digital control algorithm was implemented on a TMS320F2808 DSP core. Very good agreement is found between the analytical derivations, simulations, and experimental results.**

***Index Terms*—C code block, digital control, dynamic model, frequency control, frequency resolution, limit cycle oscillations, limit cycles criterion, PSIM, resolution effects, resonant converters, simulation.**

I. Introduction

ONE of the major culprits of digitally controlled switch-mode converters operating in closed-loop is the possible buildup of limit cycles, i.e., oscillations of the regulated output under steady-state operation [1]–[3], which result from the presence of quantizers (of the sampling and control units) in the control loop. The general control theory aspects of limit cycles were investigated in [4]–[8]. The issues of limit-cycle oscillations in digitally controlled pulsewidth modulation (PWM) converters were addressed in [2], [3], [9]–[12]. It has been shown in these studies that one of the main reasons for limit cycles onset is when the LSB of the digital PWM modules (DPWM) changes the output by a value that is larger than the analog-to-digital converter (ADC) resolution.

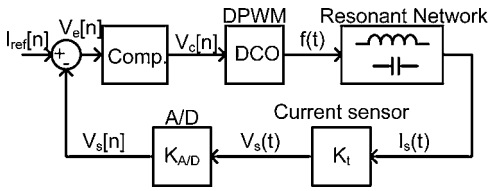

Fig. 1. Block diagram of a digitally controlled resonant converter.

The problem of limit cycles is traditionally overcome by either reducing the ADC resolution (resulting in lower regulation accuracy) or by increasing the DPWM resolution. The latter can be accomplished by reducing the switching frequency, by dithering [2], [3], [13]–[15], or by hardware acceleration [14], [16]–[19].

Analogous to the case of limit cycles in digital PWM control, a similar situation is expected when applying digital frequency control to resonant converters (see Fig. 1). The main differences between the PWM and resonant converter cases are: 1) unlike PWM control, where the duty ratio resolution is constant, the frequency resolution of resonant converters depends on the operating frequency of the converter; and more importantly: 2) the power stage gain is not constant, since it varies with frequency. These attributes of digital control make it difficult to predict the appearance of limit-cycle oscillations in such systems. Hitherto, there is no reported treatment in the literature of limit cycles in frequency-controlled systems.

The objective of this paper is to point out to the factors that might cause limit cycles in frequency-controlled systems (which could be different from PWM control). It derives the conditions for limit-cycle oscillations in digitally controlled resonant converters that stem from insufficient frequency resolution of the digital core and the operating conditions, and applies a time-domain model that takes into account quantization effects, to explore the static and dynamic behavior of such systems.

The results of this investigation will enable designers to predict the conditions that lead to limit-cycle oscillations in frequency-controlled converters as a function of the resolutions of the ADC and the frequency synthesizer. This could be beneficial in the selection of the required frequency resolution of the digital hardware.

II. Static Analysis of Limit Cycles

A key criterion for determining the existence of limit-cycle oscillations in digitally controlled switching converters relies on the comparison between the LSB value (i.e., resolution) of the

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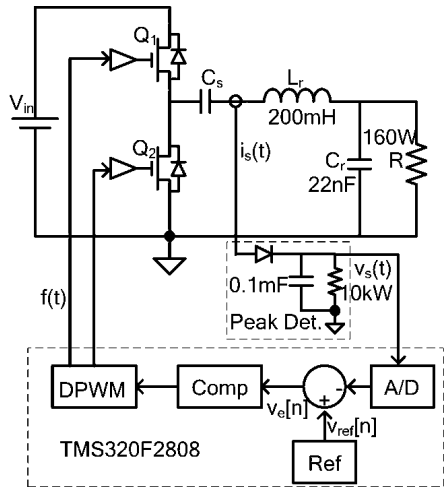

Fig. 2. Experimental digitally controlled series-resonant parallel-loaded converter.

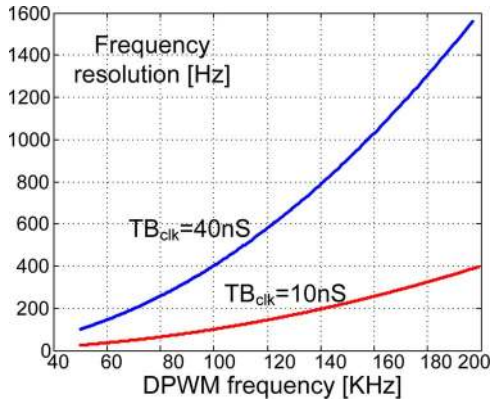

Fig. 3. Frequency resolution as a function of the running frequency of typical DCO unit for two cases of clock frequency.

ADC and the output signal variation due to a LSB change of the control [1], [9], i.e., a necessary condition for no limit cycles is that the variation of the output $\Delta_{S_{out}}$, due to a LSB change of control is smaller than the ADC resolution Δ_{ADC}

$$\left|\Delta_{S_{out}}\right| < \Delta_{ADC} = \frac{V_{ADC}}{2^{N_{ADC}}} \tag{1}$$

where V_{ADC} and N_{ADC} are the ADC reference voltage and number of bits in the ADC, respectively.

In the present static analysis of digitally controlled resonant converters (a typical block diagram is shown in Fig. 1), it is assumed that the system is dynamically stable in terms of describing function analysis [1]–[3], [9]. It is further assumed that the converter operates under steady-state conditions, that a zero control error is achieved [10], [11] and that the integral gain of the compensator is within satisfactory boundaries [2]. It is also assumed that the digital compensator (control law) adds no quantization error to the control loop (due to numerical truncation). Hence, under the aforementioned assumptions two quantizers can be identified in the system of Fig. 1: the ADC and the digital frequency generator.

The proposed method of analysis is demonstrated on a digitally controlled series-resonant parallel-loaded converter (see Fig. 2), where the aim of the control is to regulate the resonant current. To this end, the current is first sensed (converted to voltage), rectified, and then, fed to the digital controller for compensation.

Digital generation of frequency is normally carried out by timers that are programmed to reset at a desired value, while maintaining a fixed 50% duty ratio. In commercial digital controllers, it is convenient to use the DPWM unit as a digitally controlled oscillator (DCO) [14], [17], [19]. The generated frequency can be expressed as follows:

$$f_{DCO} = \frac{1}{N_{per}\mathrm{TB}} \tag{2}$$

where N_{per} is an integer and TB is the time base of the unit clock.

The frequency resolution can be calculated as the LSB change in N_{per}

$$\begin{aligned}\Delta f_{DCO} &= \frac{1}{N_{per}\mathrm{TB}} - \frac{1}{(N_{per}-1)\mathrm{TB}} \\ &\approx \frac{1}{N_{per}^2\mathrm{TB}} = \mathrm{TB}f_{DCO}^2.\end{aligned} \tag{3}$$

From (3), one finds that the frequency steps of a DCO are limited by the system clock frequency and increase as the square of the operating frequency (see Fig. 3), i.e., at lower running frequency, the frequency resolution would be finer than what can be achieved at a higher frequency. Considering this attribute by itself and neglecting all other effects (such as the system gain, etc.), it implies that a system could be free of limit-cycle oscillations at one drive frequency thanks to a fine frequency resolution that can be generated by the DCO, but may exhibit oscillations when operated at higher frequency due to poor resolution.

The next step is to determine the gain of the resonant network as a function of frequency. The s-domain representation of the resonant current circulating through the system (see Fig. 2) can be expressed by

$$i_s(s) = \frac{V_{in}}{(R/(sCR+1))(s^2LC + s(L/R)+1)} \tag{4}$$

where V_{in} is the input voltage, L, C are the resonant tank components, and R is the converter's load.

Replacing "s" by $j\omega$, and assuming that the system operates around the resonant frequency, (4) can be approximated by

$$i_s(j\omega) = \frac{V_{in}}{(1/(j\omega/\omega_0))(1-(s^2/\omega_0^2)+j(\omega/\omega_0 Q)+1)} \tag{5}$$

or in a normalized form [20]

$$|i_s(jP)| = \left|\frac{V_{in\_norm}}{Z(jP)}\right| = V_{in\_norm}\Big/\sqrt{Q^2+\left(P-\frac{1}{P}\right)^2} \tag{6}$$

where Q is the network's quality factor, $P = f/f_r$ is the ratio between the running frequency and the resonant frequency and V_{in_norm} is the normalized input voltage.

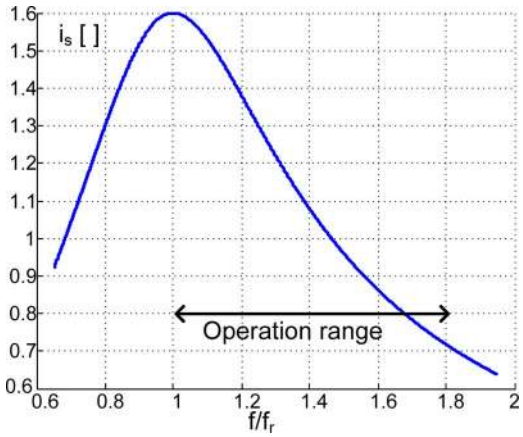

Fig. 4. Normalized frequency response of the power stage of Fig. 2 ($Q = 1.6$).

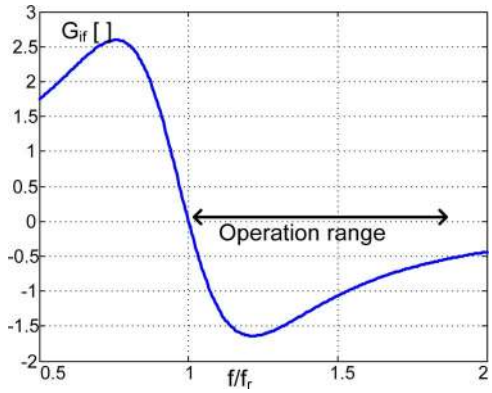

Fig. 5. Normalized frequency sensitivity of the resonant current for the system of Fig. 2 ($Q = 1.6$).

Fig. 4 shows the well-known frequency response of the resonant current of (6). The small-signal frequency to current gain of the power stage can be calculated by taking the derivative of (6)

$$G_{\rm if}(P) = \frac{{\rm d}i_s}{{\rm d}f} = -2V_{\rm in\_norm}\left(P - \frac{1}{P}\right)\left(1 + \frac{1}{P^2}\right) \Bigg/ \left[Q^2 + \left(P - \frac{1}{P}\right)^2\right]^{3/2}. \quad (7)$$

It should be noted that the derivative action carried out in (7) is valid under the assumption that the response of the resonant network to frequency changes is instantaneous as compared to the control bandwidth, i.e., itseffect on the system dynamic behavior is negligibly small.

The result of (7) is depicted in Fig. 5, which shows the local gradient of the resonant current gain as a function of the operating frequency of the converter. We observe that the system is less sensitive to frequency variations near the resonance peak and at frequencies that are far from $P = 1$. This implies that over these ranges of operation, the conditions for there to be no limit cycles of (1) can be satisfied with coarser frequency steps than required when operating at $1.2P$ where the slope of the function is highest.

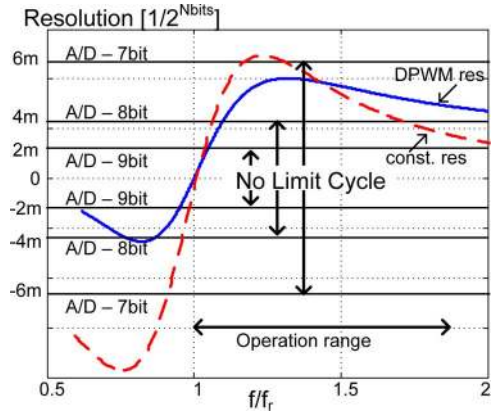

Fig. 6. System frequency sensitivity. Map of conditions for operation with no limit cycles for the system of Fig. 2 (10). Calculation parameters: $M = 26.5$, $Q = 1.6$, and TB = 10 ns.

Multiplying (7) by (3) and taking into account the value of the input voltage and the current sensing gain (k_t), the resonant current (output signal) gain can be expressed as a function of the DCO frequency variations

$$\Delta i_s = G_{\rm if}(P)\,\Delta f_{\rm DCO}(P)\,V_{\rm in}k_t. \quad (8)$$

The criterion for operation with no limit cycles for this system for the static conditions can now be established by rewriting (1)

$$\Delta i_s < \Delta_{\rm A/D} \Rightarrow |G_{\rm if}(P)\Delta f_{\rm DCO}(P)V_{\rm in}k_t| < \frac{V_{\rm ADC}}{2^{N_{\rm ADC}}}. \quad (9)$$

or

$$|G_{\rm if}(P) \times \Delta f_{\rm DCO}(P) \times M| < \frac{1}{2^{N_{\rm ADC}}} \quad (10)$$

where $M = V_{\rm in}k_t/V_{\rm ADC}$ is the measurement factor.

Fig. 6 depicts the value of output variation due to one LSB of the control as a function of the operation frequency compared to LSB value of the ADC. The figure maps the areas in which limit-cycle oscillations exist for the system of Fig. 2. The curves of Fig. 6 demonstrate two operation cases, one with constant frequency steps (dashed line) and the other (solid line) with a frequency resolution of an actual DCO realized by a DPWM unit. The curves of Fig. 6 were generated using MATLAB by calculating the left hand side of (10) starting from the operating point of $0.5P$ up to $2P$ in fine frequency increments. For the dashed line of Fig. 6, a constant frequency resolution $\Delta F_{\rm DCO}$, of 100 Hz was used. For the solid line, the frequency resolution value was calculated according to (3) assuming a time base of 10 ns. The horizontal lines of Fig. 6 represent various ADC levels that correspond to the right hand side of (10) for different values of $N_{\rm ADC}$.

The validity of (10) was tested with a dynamic model of a digitally controlled resonant converter and a cycle-by-cycle simulation model developed in the next sections.

III. Dynamic Model

The functional block diagram of the system (see Fig. 1) was the basis for the construction of the dynamic model. The concept behind the modeling methodology was to distinguish between

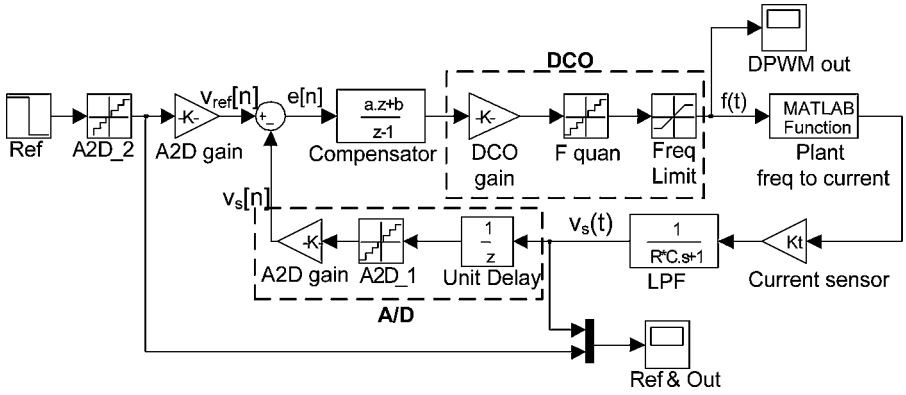

Fig. 7. Behavioral Simulink model, fixed quantizer DCO.

dynamic subunits that can be treated as linear transfer functions (TF) and algebraic frequency independent blocks [21]. In other words, since the control bandwidth is much smaller than the running frequency, the response of the resonant tank can be considered instantaneous as compared to the system's response.

In the following, we present details of the time-domain simulation model (see Fig. 7).

A. Resonant Power Stage

As was shown in the previous section, the value of the resonant current of the converter depends on the operating frequency (see Fig. 4). The resonant tank circuit is considered to respond instantaneously to changes in frequency as compared to the control loop bandwidth, and thus, its effect on the system's dynamic behavior can be neglected. Therefore, the functional relationship of this block can be described by the frequency-to-current algebraic function, which takes at the input the value of the drive frequency and generates at the output the peak resonant tank current, i.e., it generates the magnitude of i_s as a function of P, i.e.,

$$|i_s\,(jP)| = V_{\text{in\_norm}} \Bigg/ \sqrt{Q^2 + \left(P - \frac{1}{P}\right)^2} \qquad (11)$$

This algebraic equation is realized in the Simulink (Mathworks) model (see Fig. 7) as a frequency dependent gain using the "MATLAB fcn" block.

B. Digital Control Law

This block generates the control command $c[n]$ to the DCO as a function of the error $e[n]$, of a reference value and the measured output. In this study, a discrete-time PI control law [22] was applied, i.e.,

$$c[n] = c[n-1] + ae[n] + be[n-1] \qquad (12)$$

where "a" and "b" are the compensator's coefficients.

It should be noted that the response time of the control law lies within the range of system response; therefore, this block will be described as a discrete-time linear TF with inherent sampling rate from the ADC.

C. Current Sensor

To regulate the amplitude of the resonant current, a peak detector was applied (see Fig. 2). The behavioral Simulink model developed is transparent to the high-frequency resonant signals that actually pass through the converter and already produces the signals' envelop. Thus, there is no need for a peak detector in the model. A low-pass filter was still included to represent the phase lag contribution of the peak detector. This block is modeled as a dynamic continuous-time TF of the form

$$\frac{v_s}{i_s}(s) = \frac{k_t}{RCs + 1} \qquad (13)$$

where R and C are the low-pass filter components. The values of R and C were selected such that the phase delay of the low-pass filter will match the lagging effect of peak-detector action on the high-frequency envelope.

D. Digitally Controlled Oscillator (Quantizer)

The purpose of this block is to convert the digital value produced by the control into a frequency signal. The behavior of this block is modeled by a gain block that includes quantization action [9]. In this study, we realized the frequency gain and resolution by the static relationship obtained in (2) and (3). The frequency limiter (see Fig. 7) was added to ensure the proper operation range of the system as was carried out in the experimental unit (e.g., above the resonant frequency).

E. Analog-to-Digital Converter (Quantizer)

This block converts the continuous-time output to a digital value. It can be conventionally modeled by a gain plus quantization action. The sampling delay was taken into account by a discrete-time unit delay, which was also used to specify the sampling rate of the digital section.

Following the aforementioned approach, a time-domain Simulink model was constructed (see Fig. 7). Figs. 8 to 10 show some results that validate the proposed modeling approach and the static analysis. Simulations were run for different ADC resolutions and current reference settings, showing both the dynamic behavior of the system and steady-state operation. The simulation results were found to be in excellent agreement with the limit cycles condition derived in (10) and Fig. 6.

An interesting insight into the system's operation that supports the static analysis can be gained from the simulation

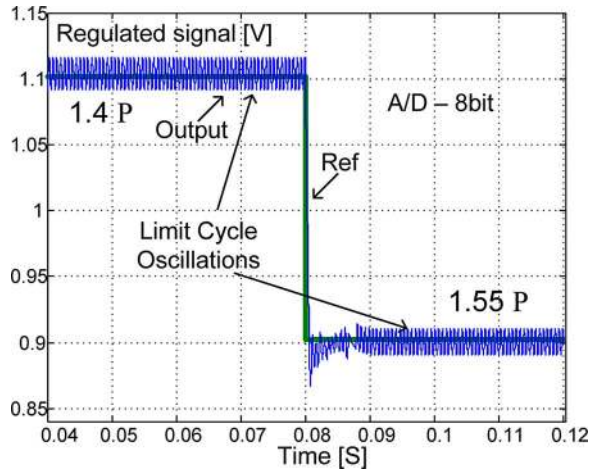

Fig. 8. Simulation results of the model of Fig. 7 for a step change of current amplitude from 1.1 to 0.9 (arbitrary units), ADC level of 8 bits. Limit-cycle oscillations.

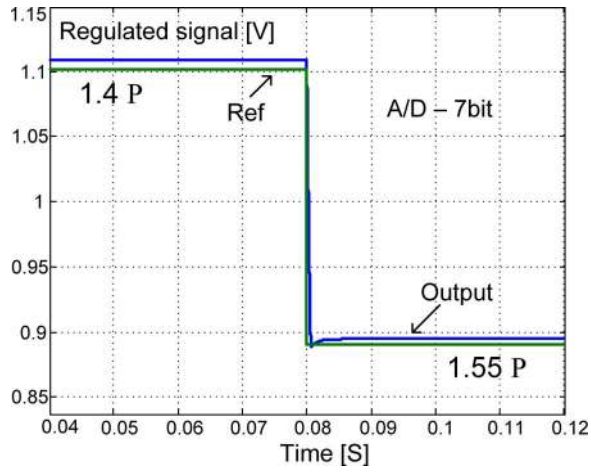

Fig. 9. Simulation results of the model of Fig. 7 for a step change of current amplitude from 1.1 to 0.9 (arbitrary units), ADC level of 7 bits. Free of limit-cycle oscillations.

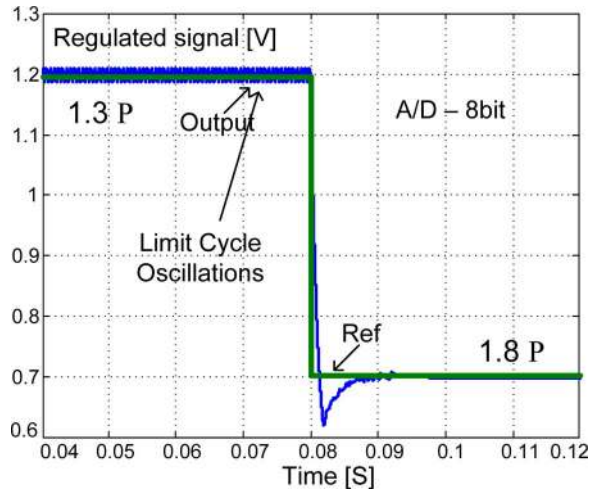

Fig. 10. Simulation results of the model of Fig. 7 for a step change of current amplitude from 1.2 and 0.7, ADC level of 8 bits. Limit-cycle oscillation at 1.2 amplitude, but no oscillations at 0.7.

results. Taking Fig. 10 as a reference, it can be observed that limit cycles exist when the ADC is set to a resolution of 8 bits and the system attempts to regulate a current value of 1.2 (arbitrary units). This is due to the high gain at $1.3P$ operating frequency (see Fig. 4) that is required to achieve this output level. Indeed from the results of the static analysis (see Fig. 6), the condition of (10) for no limit cycles is indeed not satisfied. However, when a lower current value is called for (which will require a higher operating frequency of about $1.7P$), the criterion set in (10) is satisfied and the oscillations cease.

1) Model Expansion: The simplified Simulink model of Fig. 7 considers the DCO as a quantizer with a fixed gain. However, as discussed earlier, the DCO local gain and resolution are dependent on the running frequency. This can be taken into account by replacing the fixed DCO quantizer of Fig. 7 by a variable gain quantizer. This was done by first calculating ΔF_{DCO} for the given running frequency by modifying (2)

$$\Delta F_{\mathrm{DCO}} = \mathrm{TB}F_{\mathrm{DCO}}^2 = \mathrm{TB}P^2 f_r^2 \tag{14}$$

and in the normalized form (to f_r)

$$\Delta F_{\mathrm{DCO\_n}} = \frac{\Delta F_{\mathrm{DCO}}}{f_r} = \mathrm{TB}F_{\mathrm{DCO}}^2 = \mathrm{TB}P^2 f_r \tag{15}$$

then the quantizer model was written in the normalized form (to f_r) as follows:

$$P_{\mathrm{quant}} = \frac{f}{f_r} = \Delta F_{\mathrm{DCO\_n}} \mathrm{round}\left(\frac{P}{\Delta F_{\mathrm{DCO\_n}}}\right) \tag{16}$$

where P_{quant} is the quantized value of P.

The algebraic functions of (15) and (16) were realized in Simulink by MATLAB function blocks.

Fig. 11 shows the expanded Simulink model that takes into account the effect of variable frequency resolution of the DCO. A simulation result of the model is given in Fig. 12. It shows that for the same conditions of Fig. 10 (fixed gain quantizer) and an ADC resolution of 8 bits, limit cycles exist for reference current values of 1.2 and 0.7 (arbitrary units), since the conditions do not satisfy (10) as can be observed in Fig. 6 (solid line).

The MATLAB code that includes all of the Simulink model parameters is given in Appendix A.

IV. Cycle-by-Cycle Simulation Model

To verify the proposed limit-cycles criterion, a cycle-by-cycle simulation was configured in PSIM simulator version 8.0.7 (Powersim) based on the experimental system of Fig. 2. The simulation model is depicted in Fig. 13. It includes the circuits of the power stage and the current sensor that were used in the experimental setup. The digital controller was realized in the PSIM environment as a C code block, which includes the digital compensator, the ADC, and realization of variable frequency resolution. The DCO itself and the gates driver were realized by a programmable one-shot and D-flip-flop assembly (see Fig. 13), which is controlled and triggered by the software.

The complete C code that was used in PSIM to realize the digital controller is given in Appendix B.

Figs. 14 and 15 show some cycle-by-cycle simulation results obtained by the proposed PSIM model, which takes into account

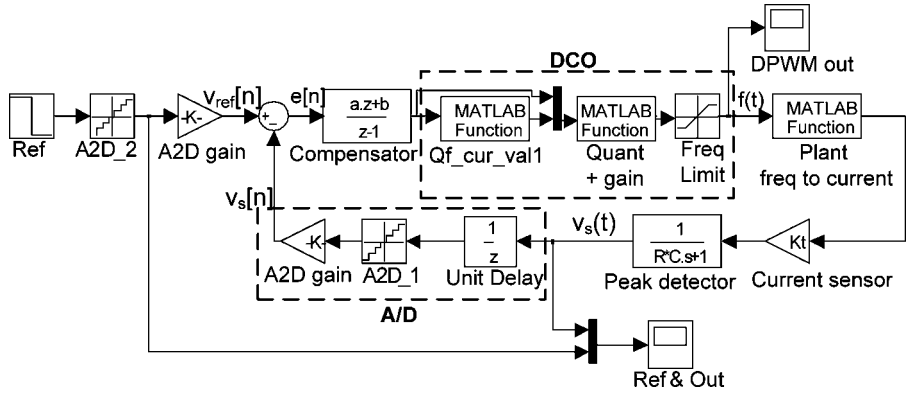

Fig. 11. Expanded version of the behavioral Simulink model that includes a DCO with variable quantization.

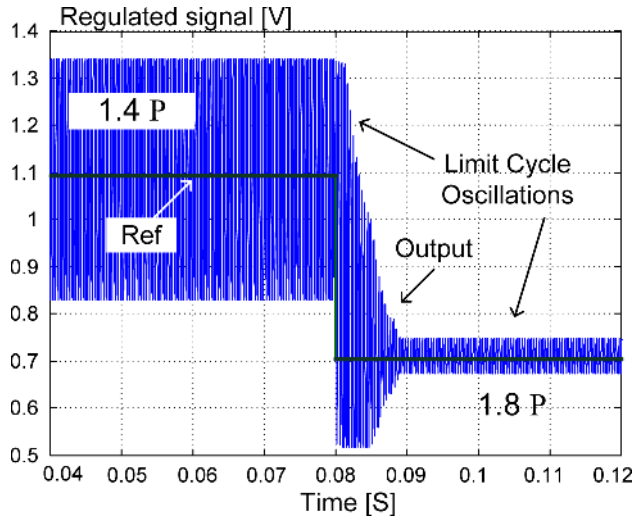

Fig. 12. Simulation results that show limit-cycle oscillations obtained by the model of Fig. 11 for a step change of current amplitude from 1.1 to 0.7 (arbitrary units), ADC level of 8 bits.

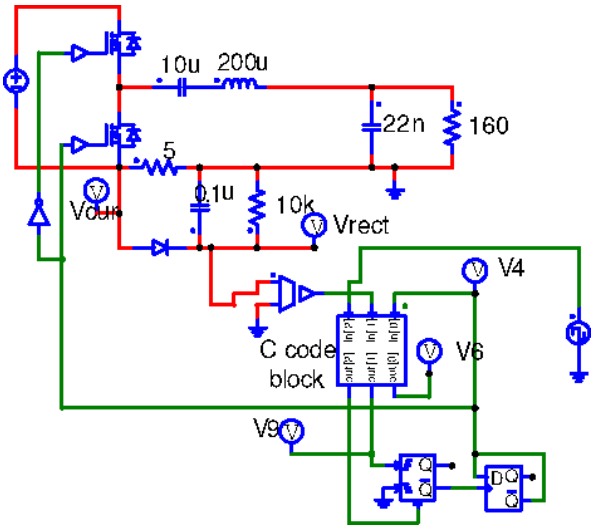

Fig. 13. Cycle-by-cycle PSIM model of a digitally controlled resonant converter. The C code is given in Appendix B.

quantization and other effects of the digital controller, such as calculation roundings, etc. The results were found to be in very good agreement with the solid line of Fig. 6 for various resolutions settings in different operating points.

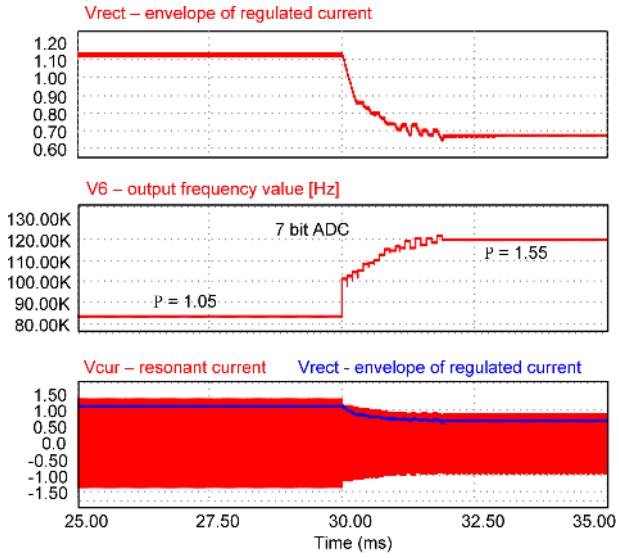

Fig. 14. PSIM cycle-by-cycle simulation results that show no limit-cycle oscillations obtained by the model of Fig. 13 for a step change of current reference amplitude from 0.22 to 0.14 A (current sensing over 5 Ω resistor), and ADC level of 7 bits. Upper trace: Envelope of sensed resonant current. Middle trace: Value of the drive frequency. Lower trace: Sensed resonant current and signal's envelope.

This model has the advantage of accurately representing the actual time-domain response of the system in better details than the behavioral Simulink model, such as producing nonsinusoidal limit-cycle oscillations. However, the major drawback of such detailed simulation is the very fine time-step that is required in order to obtain accurate results, and hence, the relatively long simulation times required for observing limit-cycle oscillations.

V. Experimental Verification

To verify the analytical derivation and the simulation model, the resonant converter of Fig. 2 was built and tested experimentally. The digital control algorithm was implemented on a TMS320F2808 (TI) DSP core.

Throughout the experiments, the compensation control and sampling rate were maintained without change, while changing the ADC levels and attempting to regulate for different current values. The operating frequency range was limited to operation above the resonant frequency (80 kHz $\equiv 1P$ to 145 kHz $\equiv 1.8P$)

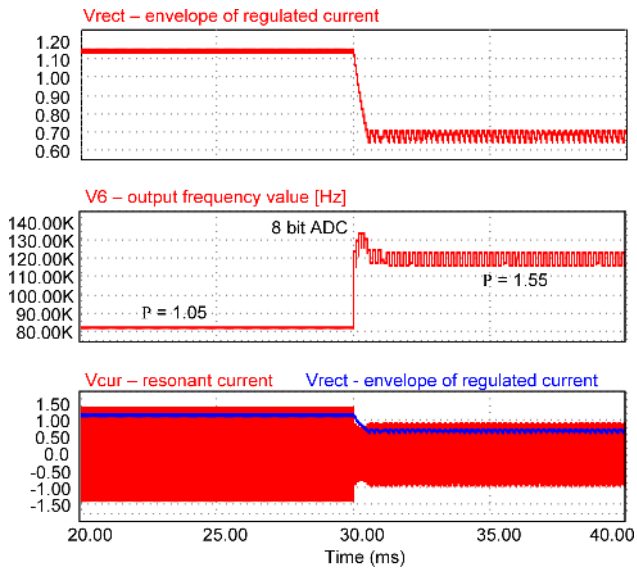

Fig. 15. PSIM cycle-by-cycle simulation results of the model of Fig. 13 for a step change of current reference amplitude from 0.22 (free of limit-cycle oscillations) to 0.14 A (showing limit cycles). ADC level of 8 bits. Upper trace: Envelope of sensed resonant current. Middle trace: Value of the drive frequency. Lower trace: Sensed resonant current and signal's envelope (current sensing resistor: 5 Ω).

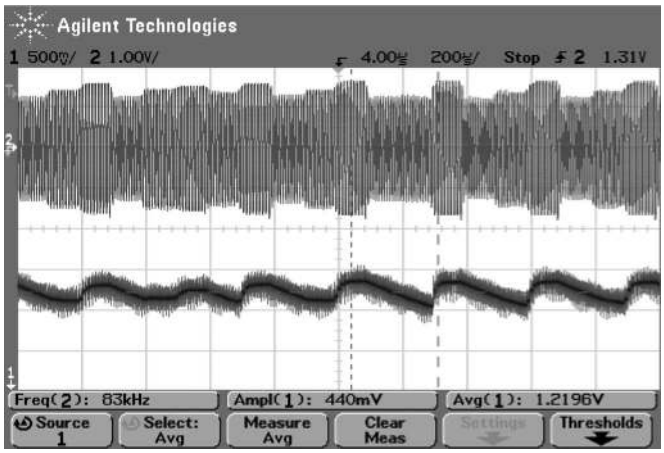

Fig. 16. Experimental results of the converter of Fig. 2 showing limit cycles. Current amplitude: 0.15 A (drive frequency of $1.3P$) with 9 bit ADC. Upper trace: Resonant current 0.2 A/div. Lower trace: Peak detector output 0.5 V/div. Horizontal scale 200 μs/div.

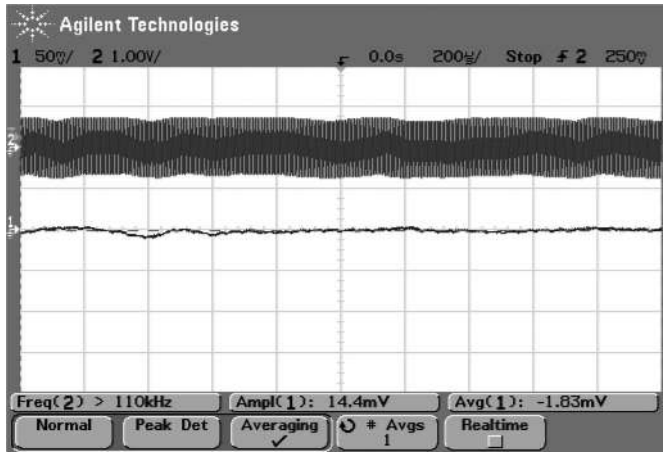

Fig. 17. Experimental results for the converter of Fig. 2 with a current amplitude of 0.15 A (drive frequency of $1.3P$) with a 7 bit ADC. Stable steady-state operation. Upper trace: Resonant current 0.2 A/div. Lower trace: Peak detector output 50 mV/div. Horizontal scale 200 μs/div.

TABLE I
EXPERIMENTAL LIMIT-CYCLES MAP OF THE SYSTEM OF FIG. 2

I [A]	f [KHz] (P)	10bit	9bit	8bit	7bit	6bit
0.175	90k (1.15)	LC	LC	LC	LC	No LC
0.15	100k (1.3)	LC	LC	LC	No LC	No LC
0.138	110k (1.4)	LC	LC	LC	No LC	No LC
0.11	120k (1.55)	LC	LC	LC	No LC	No LC
0.0875	135k (1.8)	LC	LC	No LC	No LC	No LC

The results correspond to the solid line of Fig. 6.

to assure zero voltage switching operation of the power switches. The frequency resolution of the frequency generator (DPWM unit) was set to a maximum by the digital hardware, between 11 bits at lower frequencies (around the resonant frequency) and 9 bits at higher frequencies.

Figs. 16 and 17 verify the proposed criterion and analytical results of limit-cycle conditions in such systems. The figures show the rectified output signal (ADC input) when attempting to regulate the resonant current amplitude to 0.15 A (drive frequency of $1.3P$) by the system with 9 bit ADC (see Fig. 16), where limit-cycle oscillations can be observed and with 7 bit ADC (see Fig. 17), where there is a limit cycle free operation. The minor perturbation that is observed in Fig. 17 (note the scale difference from Fig. 16), is considered to be measurement noise and not limit-cycle oscillations, since the disturbance is irregular and of relatively small amplitude.

A further verification of the proposed criterion [(10), Fig. 6] was obtained by mapping the occurrences of limit cycles in the experimental circuit. This was done by setting a constant current reference and changing the resolution of the ADC from 10 to 6 bits, and observing the regulated output, this process was repeated for various operating points, i.e., current references. The results, which are summarized in Table I, were found to be in very good agreement with the analytical prediction (Fig. 6 solid line).

VI. Discussion and Conclusion

In this study, the effect of digital resolution on the onset of limit cycles in digitally controlled resonant converters was explored. It was found that the criterion for no limit cycles in resonant converters needs to take into account both the frequency resolution and the power stage frequency-to-current gain, which are strongly dependent on the system's operating frequency at any given instance. This stems from the fact that the frequency resolution decreases as the square of the frequency and the small-signal power stage gain changes as a function of the operating frequency. Based on the static analysis under steady-state conditions, a criterion for the relative resolutions of the ADC and the DCO, for no limit cycles, was derived and verified. The analytical model developed in this study is capable of predicting the existence of limit cycles over the entire operating range of the system. Simulations and experimental measurements validated the accuracy of the model. The dynamic behavioral simulation model that was developed allows the transient operation of the system to be investigated, as well as operation under steady-state conditions (including the limit cycling phenomenon).

It should be noted that the no limit-cycles criterion derived in this study is a necessary condition that assumes zero steady-state error and do not take into account the integrator's effect and/or the changes in the loop gain due to the describing functions of the quantizers. The present static derivations address the issue of quantizers' resolution and the local gain of the system in a static operating point. In cases, where the error is nonzero, there is a drift in the operating conditions that needs to be taken into account. A full dynamic analysis in terms of the influence of the integral gain and dynamic stability by means of describing functions are beyond the scope of this study. However, these effects of can be examined by the proposed Simulink model and cycle-by-cycle PSIM simulation. It was found, for example, that by increasing the gain of the integrator, while maintaining infinite resolution of the DCO, one may observe limit cycles, similar to the PWM case [2], [3], [9]–[11].

This study reveals that the conditions for limit cycles in these systems are largely dependent on the power stage characteristics, and in particular, on the quality factor of the resonant network. This is observed in Fig. 5, where the frequency locations of the sensitivity peaks appear near the resonant frequency and by examination of (7), which implies that the peaks depend on Q and get closer to the network's resonant frequency.

The implication for the closed-loop operation of such systems is that regulation of the high Q resonant tank circuit in frequency regions that are relatively far from the resonant frequency requires modest frequency resolution to avoid limit cycles. However, when attempting to regulate the same system around resonance, the resolution requirements are much more demanding.

One of the major obstacles in the design of digitally controlled resonant converters is the limited frequency resolution capability that can be attained by simple microcontrollers. This limitation may affect control accuracy and make the system more prone to limit-cycle oscillations. One solution to this problem is to increase the resolution by frequency dithering as proposed in [15].

The criterion for no limit cycles that was derived not only highlights the importance of high-resolution frequency generation, but also emphasizes the significance of the operating point, which determines the local gain.

Appendix A

MATLAB Code and Parameters of Proposed Simulink Model

```
Vin=25.*4./3.14./2;           % input voltage - 1st harmonic sine
Zr=95;                        % Characteristic impedance
fr=77e3;                      % Resonant frequency
Q = 1.6;                      % Resonant Q-factor
V_A2D = 3;                    % A2D max voltage
Kt = 5;                       % Current sensing gain   (I to V translator)
N_A2D =8;                     % A2D resolution bits
Ts = 100e-6;                  % Sampling period
TB_M = 1;                     % Timebase multiplier (frequency resolution)
TB=10e-9.*TB_M;               % Counter timebase

s=tf('s');
comp=c2d((2.05+1000/s),100e-6,'matched')
[c_n,c_d,T]=tfdata(comp,'v');
a= c_n(1); b= c_n(2) ;        % Controller constants

Q_A2D = V_A2D./2.^N_A2D       % ADC
st_i =1.1; st_f=0.7;   st=80e-3;     %step values
fmin = 1; fmax=2;

Nclk = round(1./(1.2.*fr)./TB)

%sensing network
R=.21e3;
C=100e-9;

sim('res_lc_7')
```

APPENDIX B

PSIM C BLOCK CODE FOR A DIGITALLY CONTROLLED RESONANT CONVERTER

```
#include <Stdlib.h>
#include <String.h>
 int g_nInputNodes=0;
 int g_nOutputNodes=0;
 int g_nStepCount=0;

//Variable declaration
float x, y, Vs, temp;
float NP_t, tt,v;
unsigned int a=1, b=0, c=0, res, Vref, samp;
int Verr;
int Verr_old;
unsigned int NP_old;

//  assignments
x=2.1;                  //compensator  coefficients
y= -2;
res=256;                // ADC resolution
temp=0.0000125;         // initial switching period (temp/2 = T)
v=1.15;                 //reference voltage (analog)
Vref=round(v*res/5);    //reference value (integer)
Verr_old=0;
NP_old=1;

//  RunSimUserFunction - main routine

// I/O assigenment
out[2]=temp;
out[1]=0;
b = in[0];
samp=in[2];
out[0]=1/(2*temp);

if ( b !=a )  {
      out[1]=1;
      a = b;
 }

if(samp) {                          // sampling trigger
      c++;
      if(c>3000){
            c=0;
            Vref=(0.7*res/5);
      }
      Vs=in[1];
// clamping the sensor voltage
      if (Vs>5) Vs=5;
      if (Vs<0) Vs=0;
// normalization and conversion
      Vs=(Vs*res/5);                //ADC measurment
      Vs=round(Vs);
      Verr=(Vref-Vs);
      NP_t=(NP_old+x*Verr+y*Verr_old);        // PI control law
      NP_t=round(NP_t);
      tt=(10e-9*NP_t);
// frequency limiter
      if (1/tt<77e3) tt=1/77e3;
      if (1/tt>160e3) tt=1/160e3;
      temp=tt/2;
      NP_old=round(tt/10e-9);
      Verr_old=Verr;
}
```

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