Digital Controller for Multi-Phase DC-DC Converters with Logarithmic Current Sharing

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***Abstract* - This paper describes a novel current-program mode digital controller and a multiphase dc-dc converter with non-uniform current sharing that optimize converter efficiency over the full range of operation. The converter phases are operated as binary-weighted constant current sources, i.e. scaled in a binary-logarithmic fashion. To minimize the system size and provide fast dynamic response, the phases switch at different frequencies and their components are selected so that the most efficient operating points correspond to the set currents. The digital controller operates on a modification of the "phase dropping" principle. Depending on the output load, the number of active phases is dynamically changed. The new architecture of the controller does not require an analog-to-digital converter for current measurement and is suitable for high-frequency low-power converters. An experimental 4-phase buck converter utilizing the digital control architecture with logarithmic current sharing was built. A comparison of the efficiency with an equivalent uniform current shared converter shows that, at medium and light loads, the presented system results in the efficiency improvements of up to 6% and 25 %, respectively.**

I. INTRODUCTION

The efficiency of a typical multi-phase dc-dc switch-mode power supply (SMPS) used in telecommunication devices, consumer electronics, and personal computers depends on its load. Even though the supplied devices usually do not operate at full power all of the time, the converters are often designed to be most efficient when the load is heavy. As a result the efficiency at light and medium loads is degraded [1]. In the multi-phase system the load current is usually equally shared among several converter's stages [2,3], to reduce inductor current ripple, stress on components, and improve dynamic response. However, due to a relatively large size of semiconductor components of individual phases, at light and medium loads, the converter losses are still significant.

To optimize converter efficency over the full range of operation several approches have been proposed. The phase droping technique presented in [4] improves efficency of a converter with uniform current sharing by switching off phases at lighter loads. This technique provides a significant efficiency improvement over the full-range of operation but requires a relatively large number of phases to achieve almost flat efficency curve. The method based on the non-uniform current sharing [5] utilizes multiple power stages with different current ratings. To improve the efficency, in this implementation, the phases are switched on and off in a predermined fashion, where based on the load current one, two or three phases are active. This method results in a smaller number of phases but also has an efficency curve that has a large deviation from the ideal flat characteristic. Compared to [4] the overall efficency of this system is lower. In additon, in both of the presented methods only power stages are presented but the controller implementation issues have not been addressed at all. In particular, stability problems during mode transients, which as will be shown soon, cannot be solved in a simple manner. Hence, the authors demonstrate steady-state operation of the presented architectures only and suggest possible controller implementations.

The main goals of this paper are to address problems of practical controller implementation and show a new system that results in small number of phases having both flat and optimized efficency curve. To achieve these characteristics the system of Fig.1 utilizes two novel elements. A digital current program-mode based controller, which does not require an analog-to-digital converter for the inductor current measurement, and a power stage with logarithmic current sharing. The system utilizes *N* parallel converters operating as binary-weighted constant current sources. Each of *N* phases of

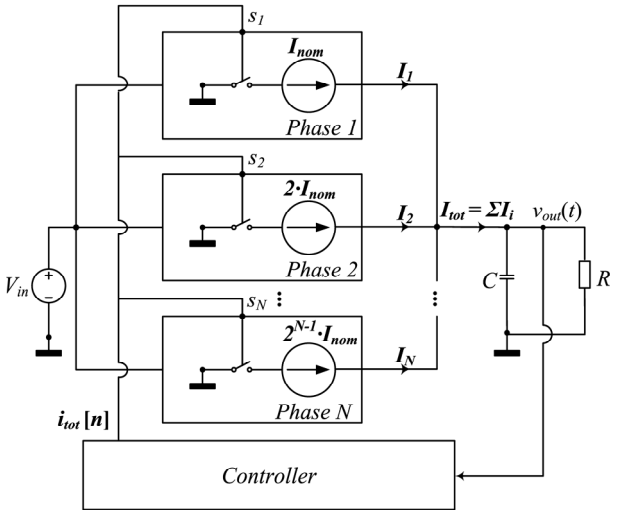

Fig.1. Block diagram of a digitally controlled multiphase converter with logarithmic current sharing.

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Fig.1 is optimized (size of semiconductor switches, inductor value, and switching frequency) to have the maximum efficiency at current $I_i = 2^n I_{nom}$, where $i = 1,2,\ldots,N$. The instantaneous number of phases operating at any point of time is regulated by the digital current program mode controller (DCPM). Depending on the load current I_{load} requirements, the controller generates a digital control variable $i_{tot}[n]$ that enables or disables the phases, such that $I_{load} = \Sigma I_i$.

The state of each phase is controlled through phase enable signals s_1, s_2,…, s_N. In this implementation, s_1 corresponds to the least significant bit (LSB) of $i_{tot}[n]$ and s_N, controlling the current of $(2^N\text{-}1)\cdot I_{nom}$, is equal to the most significant bit (MSB). Since each of the converters operates at the most efficient point, in this way, the optimal efficiency over the full range of operation is achieved. Also, as will be discussed in the following section, the hardware requirements for a relatively complex current loop are minimized.

II. System Architecture

Fig.2 shows a 4-phase implementation of the new system. Its controller has a digital voltage loop containing an analog-to-digital converter (ADC) for output voltage error $e[n]$ measurement and a PI compensator producing the control signal $i_{tot}[n]$. The sampling of the output voltage and the update of $i_{tot}[n]$ is performed at the frequency equal to the rate of the fastest-switching converter.

Compared to the traditional implementation of DCPM [6]-[8], which would require multiple ADCs for the phase current measurements, the system of Fig.2 is much simpler. It eliminates the need for a large number of fast ADCs and instead, as shown in Fig.2, uses a set of comparators, which thresholds v_{nom}, $2v_{\text{nom}}$, and $4v_{nom}$ are proportional to the binary weighted currents. As a result, the peak current control in all phases is achieved. It should be noted that the elimination of the current-measurement ADCs hugely simplifies the controller implementation and complexity. To capture fast changing current waveforms a costly ADCs, whose sampling rate needs to be at least equal to the switching frequency is needed. In modern multi-phase converters often operating at frequencies significantly higher than 1 MHz [9,10] the complexity of the ADCs can exceed that of the all other parts of the controller. On the other hand, the comparators of Fig.2 can be fairly simple. They only need to be fast and not necessarily very accurate. Any offset in the comparator threshold is automatically compensated by the voltage loop and in most of the cases only has a negligible effect on the phase efficiency.

To provide accurate current regulation and eliminate a stability problem related to the phase toggling, which will be addressed in the following section, a simple digital-to-analog converter (DAC), an additional low-current phase, and hysteretic logic block are added.

Similar to conventional implementations [11], the controller also has current amplifiers and an SR latch, whose operation is enabled/ disabled with the phase enable signal s_i.

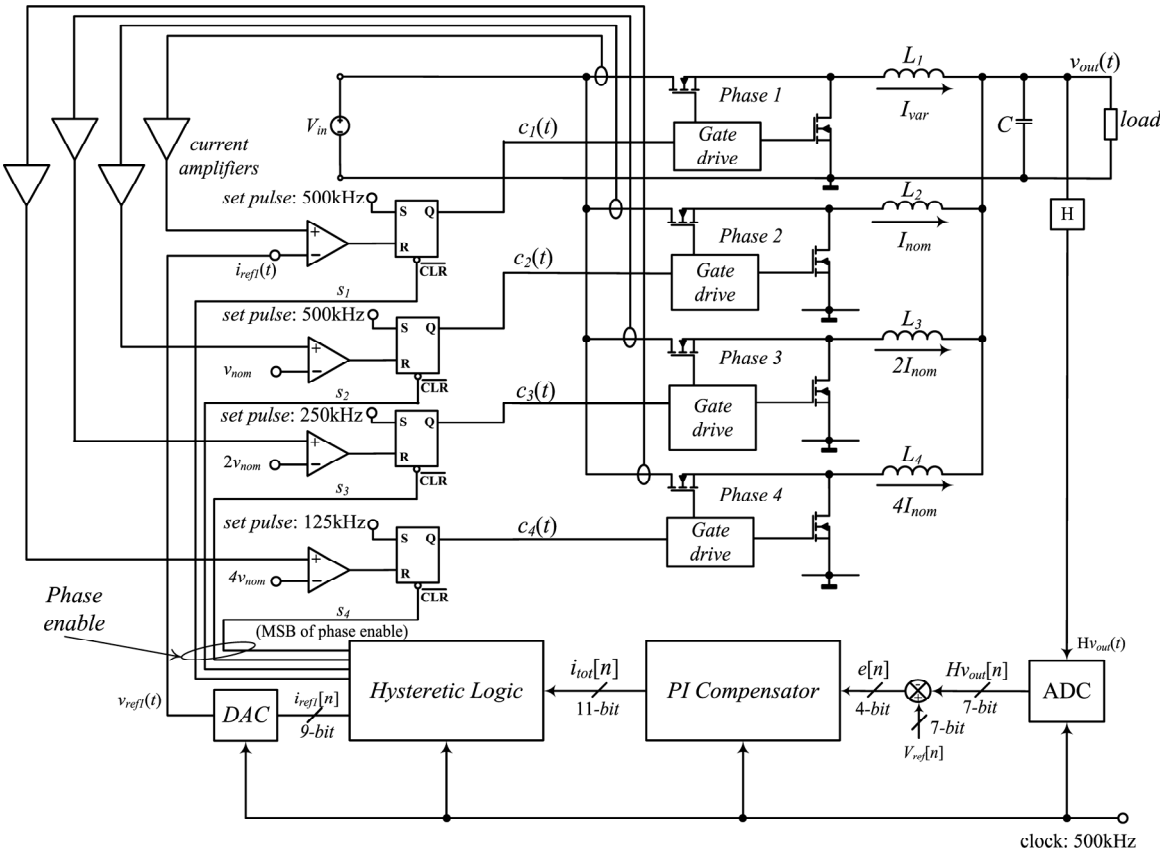

Fig.2. Detailed system architecture of the proposed controller with a logarithmic current sharing

III. System Stability and Phase Toggling Elimination

In this system the stability problem of conventional current program mode controllers for duty ratio values larger than 0.5 [11] can be minimized. Often, the constant-current phases can be designed such that the duty ratio never exceeds the critical value and the artificial ramp can only be added to the smallest phase having variable current.

An additional advantage of this implementation over the previously proposed voltage-mode controllers [4], [5] is in the simplicity of the controller implementation. Since in this case the control-to-output transfer function is not affected by the inductor value [12] a simple PI or PID compensator can be used and no additional compensation due to the change of the inductance because of the phase switching is needed.

However, the system of Fig.2 suffers from two other quantization problems that are addressed and solved here.

A. Accurate current regulation

The main problem of the architecture shown in Fig.1 is that the accuracy of current regulation depends on the number of phases. To eliminate nonlinear effects caused by coarse current adjustments, i.e. limited resolution of the current regulation, without a significant increase in the number of phases, the originally proposed structure is modified. The currents of three phases are constant and scaled as I_{nom}, $2I_{nom}$, and $4I_{nom}$ and the 4th phase has a variable current that can be changed from 0 to $1.5I_{nom}$. Such selection of the variable current range is made to avoid phase toggling that will be addressed shortly.

To achieve the current regulation with an 11-bit resolution, 3 MSBs of the control signal are used as phase enable/disable variables and the 9 LSBs are fed into a simple 1-bit Σ-Δ DAC, which sets the reference for the phase with variable current. Depending on the operation of the hysteretic logic the 9th bit of $i_{tot}[n]$ is either fed to the phase I_{nom} or to the input of the DAC. It should be noted that, as explained in [13], the implementation of the DAC is significantly simpler than that of an ADC and its introduction has a relatively small effect on the system complexity. Also, since the power rating of the variable-current phase is small its wide-range operation does not significantly affect system efficiency.

B. Elimination of the control signal toggling

An additional difficulty is that the jittering (chattering) of the control signal $i_{tot}[n]$ and undesirable limit-cycling can occur in steady-state when the PI controller changes its output constantly between two values such that a frequent phase reconfiguration occurs. For example, assume that the output load requires the current reference to change between $3.9I_{nom}$ and $4.1I_{nom}$. That action can be performed by switching between two modes of operation. In the first mode, to provide current $3.9I_{nom}$, 3 smaller phases are on (I_{nom}, $2I_{nom}$ and the variable-current phase). In the second mode the most of the current $4.1I_{nom}$ can be provided by phase $4I_{nom}$ and the remaining part of $0.1I_{nom}$ from the phase with the variable current. However, such an operation is undesirable. The frequent change in the number of active phases causes inductor current of each phase to move from zero to the nominal value and as a result undesirable oscillations affecting output voltage regulation occur. For that reason, a hysteretic logic block of Fig.2 is introduced, and the maximum current of the variable-current phase is set to $1.5I_{nom}$. The operation of the hysteretic logic that creates actual phase enabling signal is described with the diagram of Fig.3.

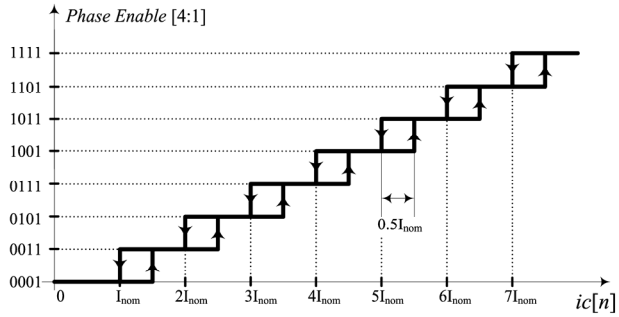

Fig.3. Operation of the hysteretic logic – output phase enable signal versus input control value $i_c[n]$.

IV. Experimental verification and Simulation Results

Based on the block diagram of Fig. 2 an experimental 4-phase 12 V to 1.8 V system was built. Digital blocks (PI compensator, hysteretic logic) are implemented with an Altera FPGA DE2 board as well as the DAC that also uses an external reference and an RC filter. The main characteristics of the prototype buck converter are listed in Table. I. The nominal current I_{nom} is set to be 0.75 A, and the switching frequencies of all stages but the two largest ones are the same. In addition, detailed models of this binary-weighted power stage and an equivalent one with the uniform current sharing are developed and their efficiencies are compared.

A. Steady-state operation of the experimental system

The steady-state converter operation for two output loads is shown in Figs 4.*a*) and 4.*b*). Fig. 4.a) shows the case when the output current is 6.2 A, and all the phases are turned on

TABLE I

Important parameters of the 4-phase logarithmic buck converter

Converter Phase	Load Current [A]	Switching Frequency [kHz]
I_{var}	0-1.125 A	500
I_{nom}	0.75A	500
$2I_{nom}$	1.5A	250
$4I_{nom}$	3A	125

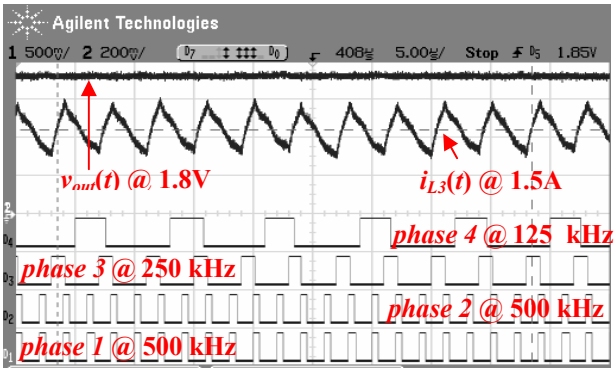

Fig.4.a). Steady-state converter operation for the load current of 6.2 A; Ch.1: Output voltage (500mV/div); Ch.2: The inductor current of phase 3 – the current sensor gain is 0.3A/V (200mV/div); D1-D4: Gate drive signals of all four phases. The time scale is 5µs/div.

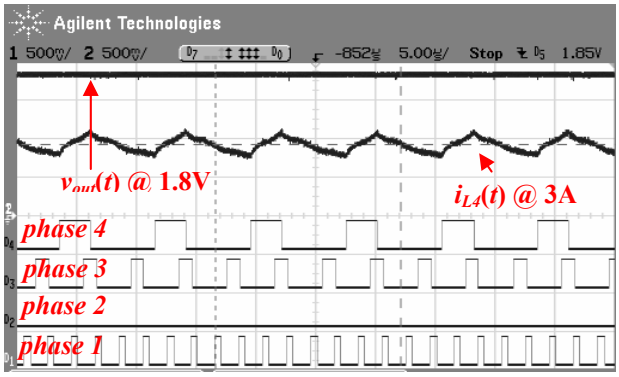

Fig.4.b). Steady-state converter operation for the load current of 4.8 A; Ch.1: Output voltage (500mV/div); Ch.2: The inductor current of phase 4 – the current sensor gain is 0.3A/V (500mV/div); D1-D4: Gate drive signals of all four phases. The time scale is 5µs/div.

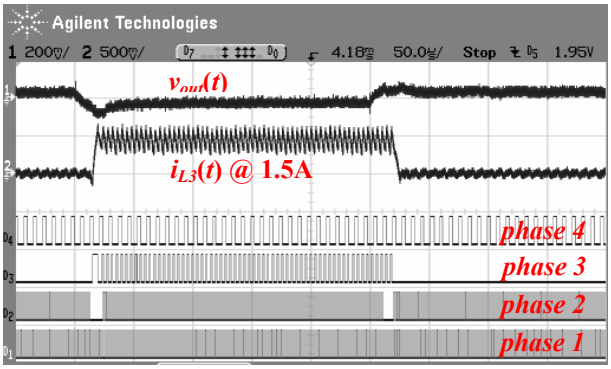

Fig.5.a). Load transient response between 4.3A and 5.8A; Ch.1: Output voltage (200mV/div); Ch.2: The inductor current of phase 3 – the current sensor gain is 0.3A/V (500mV/div); D1-D4: gate drive control signals of all four phases. The time scale is 50µs/div.

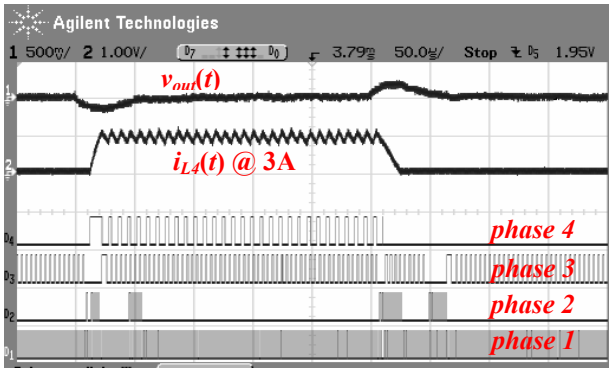

Fig.5.b). Load transient response between 2.2 A and 4.9 A; Ch.1: Output voltage (500mV/div); Ch.2: The inductor current of phase 4 – the current sensor gain is 0.3A/V (1V/div); D1-D4: gate drive control signals of all four phases. The time scale is 50µs/div.

($4I_{nom}$ = 3A, $2I_{nom}$ = 1.5 A, I_{nom} = 0.75 A, and the current of the variable phase is I_{var} = 0.95 A). The other case shows the situation when the load current is 4.8 A and the phase I_{nom} is turned off. A tight output voltage regulation in both cases can be observed.

B. Load Transient Response

The converter operation is also verified for two load steps 4.3 A - 5.8 A – 4.3 A and 2.2 A - 4.9A -2.2 A, shown in Figs. 5.a) and 5.b), respectively. In both cases, during the load transient, since the total current command $i_c[n]$ is dynamically changing to accommodate new load conditions, the phases are turned on and turned off until the output voltage settles down and $i_c[n]$ becomes constant. The response time ranges between 30µs and 50µs. Fast response of phases 1 and 2 due to the higher switching frequency and smaller phase inductance helps to reduce the peak of the voltage drop at the output capacitor during the load transient. This is illustrated in Fig. 6, where the peak of the voltage deviation is suppressed by a short-lasting current coming from phase 2.

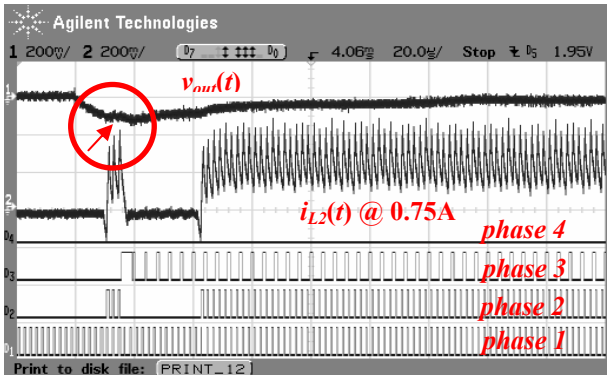

Fig.6. Load transient response between 1.1A and 3.1A; Ch.1: Output voltage (200mV/div); Ch.2: The inductor current of phase 2 – the current sensor gain is 0.3A/V (200mV/div); D1-D4: control signals. The time scale is 20µs/div.

C. Efficiency

Fig.7 shows simulated efficiency of the converter with logarithmic current sharing and that of an equivalent 4-phase power stage with equal current distribution. The simulations

are performed using Matlab Simulink tool, in which detailed switching and conductions losses of the power stages, as well as those of gate drive circuits are included. The models are

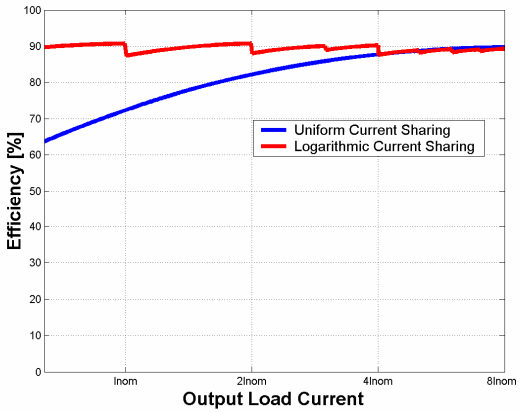

Fig.11. Simulated efficiencies of the converters with logarithmic and equal current sharing.

developed based on the guidelines given in [13].

It can be seen that the converter with logarithmic current sharing has virtually flat characteristic over the analyzed range of operation and results in the efficiency improvement of up to 25 % at light loads, and about 6% at medium loads.

V. Conclusion

A novel current-program-mode based digital controller and power stage with logarithmic current sharing are introduced. It is shown that by using a relatively simple controller and a small number of phases virtually flat efficiency characteristic can be achieved. The digital controller requires no analog-to-digital converters for inductor current measurement and, as such, is suitable for systems operating at high switching frequencies. In addition, due to the use of the current-program mode, stability problems characteristic for similar voltage mode configurations are eliminated. Quantization effects and phase toggling problems existing due to coarse current adjustments are addressed and solutions for the same are proposed. The new system is implemented on an 4-phase prototype and efficiency improvements and good dynamic characteristics are verified.

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