Digital Current Controller with Error-Free Feedback Acquisition and Active Resistance

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***Abstract*— Digital current controllers have the key impact on the performance of grid-side converters and ac drives. The voltage disturbances are commonly suppressed by enhancing the controller with an inner active resistance feedback. In cases where the switching noise and parasitic oscillations introduce sampling errors, conventional sampling is replaced by the oversampling-based error-free feedback acquisition which derives the average of the measured currents over the past switching period. The time delay introduced into the feedback path creates difficulties in designing the current controller with the active resistance. In this paper, we introduce a novel structure of the current controller which includes the error-free sampling and the active resistance feedback. Devised structure improves the disturbance rejection by extending the range of permissible values of the active resistance. Controller structure is based on the internal model principles and it maintains the input step response unaffected. The paper comprises analytical design, the gain setting procedure, computer simulation and experimental results obtained from an experimental setup with a three-phase inverter, digital controller, and a permanent magnet synchronous motor.**

***Index Terms*— Ac motor drives, Active resistance feedback, Current control, High-performance control.**

I. Introduction

Digital current controllers represent an important part of the inner control loop of both vector-controlled high-performance ac drives [1] and grid-connected inverters and their influence on the overall control system characteristics is profound [2], [3]. The structure of the current controllers typically includes proportional-integral (PI) action and decoupling terms [4], [5].

Important contributions to the theory and practice of current controller design have been provided in [3], [4], [5], where the analysis was conducted in the *s*-domain, using Pade's approximation of the transport delays and Tustin's approximation of the integrator. Design process of current controllers typically ignores the fact that the output voltage of a three-phase PWM inverter is limited and governed by the dc-bus voltage. Voltage limit may lead to the integrator wind-up and voltage distortion. Negative effects of the voltage limit may be avoided by current reference modification [6].

Direct digital synthesis and application of the internal-model-control concept in *z*-domain enable controller design without approximations [7], leading to an improved response with decoupled control even at very high operating frequencies. Input step response of a synchronous frame controller is characterized with a closed loop bandwidth f_{BW} of up to 10% of the sampling frequency f_S without an overshoot.

However, disturbance rejection properties (i.e. suppression of the impact of a voltage change, as an external disturbance, on controlled current) of such current controllers are unsatisfactory [4], [8]. Disturbance rejection can be significantly improved by using an active resistance feedback [8], at the expense of worsening the input step response. This can be circumvented to some extent by increasing the controller integral gain [8].

Due to the existence of switching noise and parasitic oscillations [9], [10] sampling errors take place [11]. Sampling errors can be eliminated entirely by means of period-averaging feedback acquisition [11], which however introduces delay and makes application of active resistance feedback difficult.

This paper considers a digital current controller with error-free feedback acquisition [11]. A controller that enables use of active resistance feedback, despite of the delay introduced by the feedback acquisition, is designed. The final result is a digital current controller which (1) is free of sampling error, (2) contains active resistance feedback, thus improving the disturbance rejection, and (3) is characterized with a bandwidth commensurate with the current state-of-the-art controllers, without overshoot, and without negative impact of the active resistance feedback on the input step response.

The paper is organized as follows. Sampling schemes and active resistance feedback concept are revisited in Section II. Section III addresses the plant behavior with the active resistance feedback under different sampling scenarios. The complete digital current controller with error-free signal acquisition, active resistance feedback, and full decoupling is developed in Section IV, with a subsequent full experimental verification provided in Section V. Section VI summarizes the conclusions of the study.

II. Active Resistance and Sampling Schemes

An important capability of digital current controllers is the disturbance rejection, namely, the ability to minimize the impact ΔI of the voltage disturbances ΔU on the controlled currents. It is desirable to have the admittance $Y = \Delta I/\Delta U$ as low as possible. The admittance Y can be reduced by subtracting the product of the feedback currents and the gain R_a from the voltage command. Insertion of the active resistance R_a results in considerably improved disturbance

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rejection [8], [12], [13], [14]. In order to keep the input step response unaffected by the insertion of R_a inner feedback, it is necessary to introduce a delayed integral action into the structure of the controller [4].

A. Active Resistance Control with Synchronous Sampling

In an ideal case, the sampling at the center of the voltage pulses [10] provides the feedback samples at instants where the PWM ripple crosses zero. Synchronous sampling implies capturing two samples within each PWM period T_{PWM}. The samples are spaced by $T_S = T_{PWM}/2 = 1/f_S$. Synchronous sampling can be advantageously used with integral motors and all other applications where the feedback samples do not get compromised by switching noise and the parasitic capacitance of the cabling and the windings.

The current controller with synchronous sampling and the active resistance is discussed in [4]. Both analytical and experimental findings prove that the introduction of the active resistance feedback improve the disturbance rejection by the factor of $(1+R_a/R)$ [4], where R_a is the active resistance gain while R is the resistance of the load. In order to maintain the input step response unaffected by the inner R_a feedback, the controller structure (Fig. 1) has an additional control action. The direct path comprises a new, delayed integrator with the gain R_a and time delay of $T_d = d \cdot T_S$. With synchronous sampling, computation and modulation delay T_d is equal to one and a half sampling periods T_S (d = 3/2). The new, enhanced controller ("modified controller" in Fig. 1) is obtained by applying the internal model concept on the plant which comprises the load with added inner active resistance feedback ("modified plant" in Fig. 1).

Analytical considerations and experimental results in [4] prove that the optimum value of R_a is equal to the optimum proportional gain of the current controller. The structure in Fig. 1 maintains the input step response unaffected by the inner active resistance feedback.

B. Active Resistance Control with Feedback Averaging

With only one feedback sample per each period T_S, synchronous sampling schemes are sensitive to the switching noise. In cases with perceptible cable capacitance, winding capacitance or load capacitance, the consequential switching-related parasitic oscillations introduce considerable sampling errors [11]. The sampling errors are also introduced by the analog anti-alias pre-filters which move the current-ripple zero-crossing away from the voltage pulse center [10].

The introduction of the active resistance (Fig. 1) increases the noise within the system, since the sampling errors get multiplied by R_a. In support of this claim, the experimentally obtained waveforms of the i_q current in the steady state have been checked. The lower trace in Fig. 2 is obtained with the conventional current controller that employs synchronous sampling, enhanced by the local R_a feedback. The experimental setup, used throughout the paper, is described in Appendix I. Apart from an increased PWM frequency (from 8 kHz to 10 kHz), the key features of the setup correspond to [11]. The conventional controller is enhanced by the active resistance feedback with the gain set to R_a^{opt} of [4]. Although obtained with a moderate gain, the bottom trace in Fig. 2 demonstrates a considerable increase in i_q disturbances.

In order to suppress the sampling errors and to enable disturbance-free increase of R_a, conventional synchronous sampling has to be replaced by the error-free feedback acquisition which calculates the feedback i^{FB} from the set of samples acquired over the past switching period (Fig. 3, [11]). The upper trace in Fig. 2 is obtained by replacing the synchronous sampling by the error-free feedback acquisition scheme of [11]. The consequential disturbances of i_q current are reduced significantly.

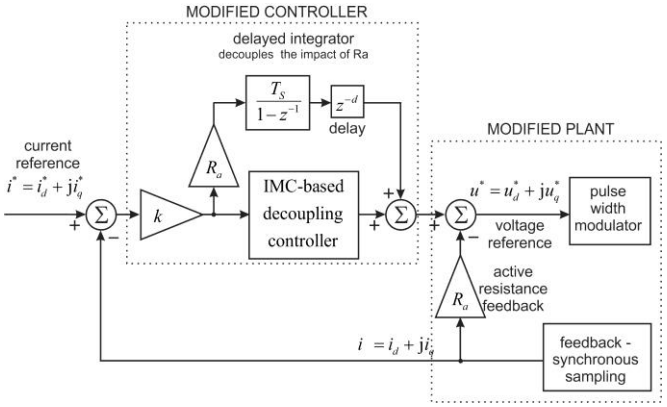


Fig. 1. The current controller with synchronous sampling and inner active resistance feedback. Additional direct branch of the controller comprises an integrator delayed by T_d [4]. In [4], delay T_d is $d \cdot T_S = 3T_S/2$.

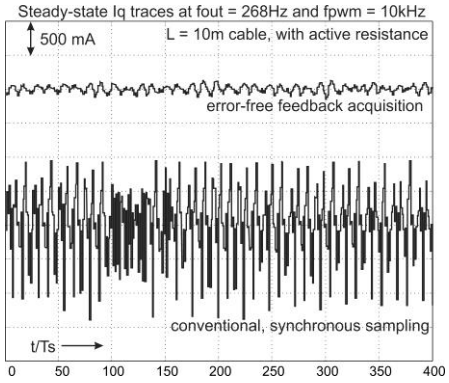


Fig. 2. Steady state waveforms of the q-axis current obtained with conventional synchronous sampling (lower trace) and with the error-free feedback acquisition of [11]. The traces are obtained by adding the active resistance feedback with $R_a = R_a^{opt}$ [4], and by using a 10m long cable that connects the load and the PWM inverter (experimental results).

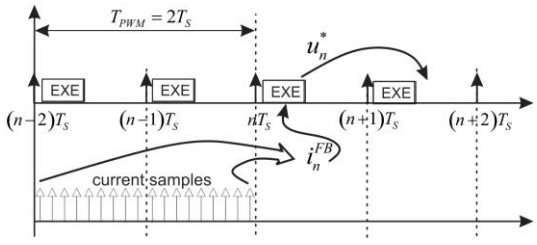


Fig. 3. Oversampling-based, error-free feedback acquisition calculates the feedback signal i_n^{FB} as the average value of the current samples acquired in the interval $[(n-2)T_S \,..\, nT_S]$. The feedback i_n^{FB} is derived in interrupt (EXE) triggered at nT_S, and it is used to calculate the voltage reference u_n^*, which gets applied within the interval $[(n+1)T_S \,..\, (n+2)T_S]$.

Based on one-period-averaging, the error-free sampling scheme increases the equivalent computation and modulation delay from $3T_S/2$ to $5T_S/2$. The time delay deteriorates the input step response, and it poses a problem in designing the current controllers with the active resistance feedback.

Despite the time delay, the overshoot-free step response can be achieved by adopting the corresponding controller structure [11]. With appropriate parameter setting, the relevant closed loop bandwidth $f_{BW} > f_S/10$ compares to the state-of-the-art solutions which operate with synchronous sampling [4], [7].

The current controller proposed in [11] does not include the active resistance (R_a) feedback. To investigate the possibility of using the R_a feedback in conjunction with the error-free feedback acquisition, the current controller of [11] has been modified by adding the R_a feedback and inserting the delayed integrator of Fig. 1, in accordance with rules laid out in [4]. The experimental traces in Fig. 4 show the input step response of i_q current in cases with no active resistance feedback, with $R_a>0$, and with the delayed integrator.

The first trace in Fig. 4 is obtained with $R_a = 0$, and it corresponds to the control structure proposed in [11]. The second trace is obtained by adding the active resistance feedback with $R_a = R_a^{opt}$ [4]. In absence of the delayed integrator (Fig. 1), the trace 2 exhibits a sluggish response with considerable settling time. The trace 3 in Fig. 4 is obtained by adding the delayed integrator (Fig. 1), following the procedure in [4]. The trace is obtained with $R_a = 0.3 \cdot R_a^{opt}$, since any further increase in R_a results in oscillations that are not acceptable. The traces in Fig. 4 confirm that the active resistance controller designed for the use with synchronous sampling [4] cannot be used in conjunction with the error-free feedback acquisition of [11].

C. Active Resistance Control with Improved Task Scheduling

Reduction of time-delays introduced by the oversampling-based error-free feedback acquisition (Fig. 3, [11]) can be achieved by rescheduling the current control tasks [15]. Improved task scheduling is illustrated in Fig. 5, where $\Delta t_{EXE} << T_S$ represents the time required to calculate the average of the feedback samples and to execute the relation of the digital current controller. The equivalent computation and modulation delay is reduced from $5T_S/2$ (in [11]) down to $3T_S/2$. With appropriate parameter setting [15], the input step response with no overshoot is maintained even with the closed loop bandwidth $f_{BW} > 0.17 \cdot f_S$. The current controller of [15] does not include the active resistance feedback, and the voltage disturbances produce non-negligible current errors [15]. To evaluate the possibility of introducing the R_a feedback into the current controller with error-free feedback acquisition and improved scheduling, the current controller of [15] is modified by adding the active resistance feedback and the delayed integrator [4]. The experimental traces are given in Fig. 6.

Trace 1 in Fig. 6 is obtained with $R_a = 0$, and it corresponds to the control structure proposed in [15]. Trace 2 is obtained by adding the active resistance feedback with $R_a = R_a^{opt}$ while keeping the delayed integrator off. The trace 3 in Fig. 6 is obtained by adding again the delayed integrator [4]. The gain R_a is set to $0.55 \cdot R_a^{opt}$. Larger values of R_a gave rise to unacceptable oscillations. The experimental traces in Figs. 4 and 6 demonstrate the problems of implementing the active resistance in conjunction with error-free feedback acquisition [11], underlying the need to resolve such problems by devising a new controller structure.

III. Load Transfer Function with Active Resistance

The load and the active resistance feedback can be regarded as the modified plant (Fig. 1). It is necessary to derive the

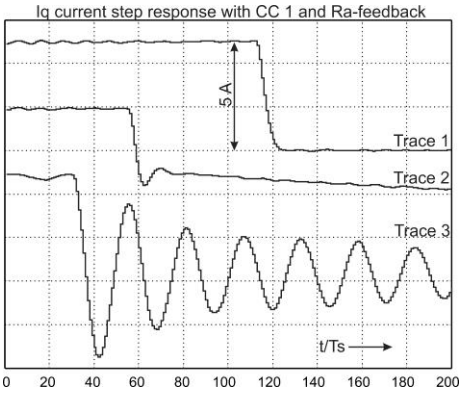


Fig. 4. The input step response obtained with error-free feedback acquisition and with the task scheduling of Fig. 3 [11]. Trace 1 is obtained without the R_a feedback. Trace 2 is obtained with R_a feedback but without delayed integrator (Fig. 1). Trace 3 is obtained with R_a feedback and with delayed integrator [4] (experimental results).

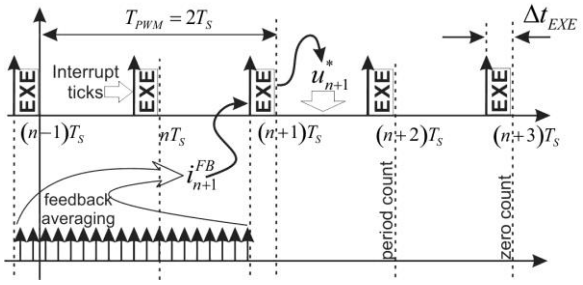


Fig. 5. Improved schedule of the control tasks. Control interrupts (EXE) are triggered $\Delta t_{EXE} << T_S$ before the reload instants of PWM register. The interrupt $(n+1)T_S$ uses the feedback sample $i_{n+1}{}^{FB}$ which represents the average value of the samples acquired in the interval $[(n-1)T_S .. (n+1)T_S]$. The feedback $i_{n+1}{}^{FB}$ is used to calculate the voltage reference $u_{n+1}{}^*$, which gets applied in the interval $[(n+1)T_S .. (n+2)T_S]$.

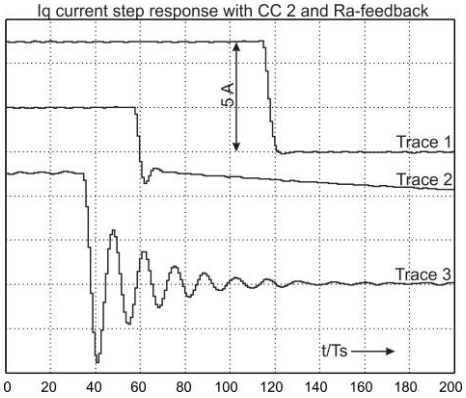


Fig. 6. The input step response obtained with error-free feedback acquisition and the improved task scheduling of Fig. 5 [15]. Trace 1 is obtained without the R_a feedback. Trace 2 is obtained with R_a feedback but without delayed integrator (Fig. 1). Trace 3 is obtained with R_a feedback and with delayed integrator [4] (experimental results).

pulse transfer function of the modified plant with the standard, synchronous sampling scheme, and also with the error-free feedback acquisition scheme that operates with improved task scheduling of Fig. 5.

A. Modified Plant with Synchronous Sampling

With complex vector notation of [16], the current vector in the $\alpha\beta$ frame can be defined as $i^s = i_\alpha + ji_\beta$. The complex vectors of currents and voltages in dq frame are $i^e = i_d + ji_q$ and $u^e = u_d + ju_q$. The $\alpha\beta$ vectors are obtained by multiplying the d-q vectors by $\exp(j\theta)$, where θ is the position of the dq frame ($i^s_n = i^e_n \exp(j\theta_n)$).

Considering the synchronous sampling scheme illustrated in Fig. 3, the load current is described by the difference equation

$$i^s_{n+2} = \beta \cdot i^s_{n+1} + \frac{1-\beta}{R}\left(u^s_n - e^s_{n+1}\right), \quad (1)$$

where $\beta = \exp(-R \cdot T_S/L)$, R and L are the load parameters, i^s_{n+2} and i^s_{n+1} are the samples of the load current in the $\alpha\beta$ frame, while e^s_{n+1} is the average value of the voltage disturbance in the interval $[(n+1)\cdot T_S \,..\, (n+2)\cdot T_S]$. Due to $L/R >> T_S$, $(1-\beta)$ is close to $R \cdot T_S/L$ and $(1-\beta)/R$ close to T_S/L. The transformation of $\alpha\beta$ currents into the dq frame is obtained by $i^e_n = i^s_n \exp(-j\theta_n)$. The d-q frame revolves with the speed ω_{dq} and the change of ω_{dq} over one sampling period T_S can be neglected. For this reason, the position θ_n can be approximated by $\omega_{dq}T_S + \theta_{n-1}$. By transforming (1) into d-q frame, dividing the outcome by $\exp(j\theta_{n+1})$, and transforming the difference equation into z domain, one obtains

$$i^e(z)\cdot z^2 \cdot e^{j\omega_{dq}T_S} = i^e(z)\cdot z \cdot \beta + \quad (2)$$
$$+\frac{T_S}{L}\left(u^e(z)\cdot e^{-j\omega_{dq}T_S} - e^e(z)\cdot z \cdot e^{\frac{j\omega_{dq}T_S}{2}}\right),$$

where $i^e(z)$, $u^e(z)$ and $e^e(z)$ are the dq frame currents, voltages and the voltage disturbance in z domain. The factor $\exp(j\omega_{dq}T_S/2)$ is explained in [15]. The pulse transfer function of the load $W_{O1}(z)$ corresponds to $i^e(z)/u^e(z)$ in the case where $e^e(z) = 0$.

$$W_{O1}(z) = \frac{T_S/L}{z\cdot e^{j\omega_{dq}T_S}\left[z\cdot e^{j\omega_{dq}T_S} - \beta\right]}. \quad (3)$$

The block diagram in Fig. 7a is obtained from (2) and (3). It contains the load transfer function W_O, the transfer function of the feedback path and the active resistance feedback R_a. With synchronous sampling, $W_{FB}(z) = 1$. The compact form of the diagram is given in Fig. 7b, where the pulse transfer function $W_{ORA} = W_O/(1+R_a \cdot W_O \cdot W_{FB})$ represents the load with the inner active resistance feedback, with $W_{FB}(z) = 1$,

$$W_{ORA1}(z) = \frac{T_S/L}{z^2 e^{2j\omega_{dq}T_S} - ze^{j\omega_{dq}T_S}\beta + \frac{R_aT_S}{L}}. \quad (4)$$

B. Modified Plant with Error-free Feedback Acquisition and Improved Task Scheduling

The feedback sample $i_{n+1}{}^{FB}$ in Fig. 5 can be calculated from the samples i_{n-1}, i_n and i_{n+1} of the load current. The samples are spaced by T_S. With $T_S << L/R$, the load current exhibits a linear change within each voltage pulse. Therefore, according to [11], [15], the sample $i_{n+1}{}^{FB}$ can be expressed as $(i_{n-1}+2i_n+i_{n+1})/4$. The pulse transfer function W_{FB} of the feedback chain is

$$W_{FB}(z) = i^{FB}(z)/i^e(z) = \left(z^2 + 2\cdot z + 1\right)/\left(4z^2\right). \quad (5)$$

The sample $i_{n+1}{}^{FB}$ of Fig. 5 is used to calculate the voltage reference $u_{n+1}{}^*$, which commands the average voltage from $(n+1)T_S$ until $(n+2)T_S$. Thus, the change of the load current is determined by the difference equation

$$i^s_{n+2} = \beta \cdot i^s_{n+1} + \frac{1-\beta}{R}\left(u^s_{n+1} - e^s_{n+1}\right). \quad (6)$$

Applying the z transformation to (6), one obtains

$$i^e(z)\cdot z \cdot e^{j\omega_{dq}T_S} = i^e(z)\cdot\beta + \frac{T_S}{L}\left(u^e(z) - e^e(z)\cdot e^{\frac{j\omega_{dq}T_S}{2}}\right). \quad (7)$$

The pulse transfer of the load $W_{O2}(z)$ corresponds to $i^e(z)/u^e(z)$ in the case where $e^e(z) = 0$,

$$W_{O2}(z) = \left.\frac{i^e(z)}{u^e(z)}\right|_{e^e=0} = \frac{T_S/L}{z\cdot e^{j\omega_{dq}T_S} - \beta}. \quad (8)$$

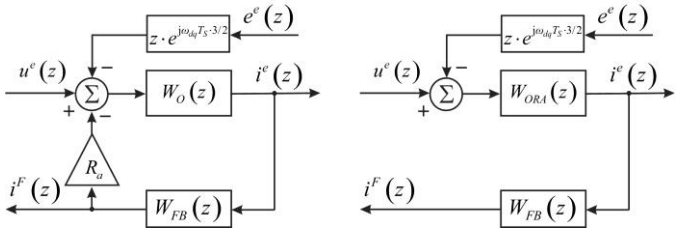
By introducing $W_{FB}(z)$ of (5) and $W_{O2}(z)$ into the block diagram in Fig. 7a, the pulse transfer function $W_{ORA} = W_O/(1+R_a \cdot W_O \cdot W_{FB})$ of the load with the inner active resistance feedback is obtained as

$$W_{ORA2}(z) = \frac{z^2\frac{T_S}{L}}{z^3 e^{j\omega_{dq}T_S} + z^2\left(\frac{R_aT_S}{4L} - \beta\right) + z\frac{R_aT_S}{2L} + \frac{R_aT_S}{4L}}. \quad (9)$$

C. The Range of Applicable R_a Gains

Parameter tuning for the current controllers with synchronous sampling [4] sets the proportional gain to $k_p = k \cdot L$, with $k_{opt} = \alpha_{opt}/T_S = 0.246/T_S$ for the input step response with negligible overshoot and $k_{max} = \alpha_{max}/T_S = 0.582/T_S$ for the step response with an overshoot of 40%. The same setting is proposed for the active resistance, $R_{a(opt)} = \alpha_{opt}\cdot(L/T_S)$ and $R_{a(max)} = \alpha_{max}\cdot(L/T_S)$.

It is of interest to check the range of gains R_a that can be used in the pulse transfer functions (4) and (9). With $R_a \cdot T_S/L = \alpha_a$ and $\omega_{dq} = 0$, denominator in (4) becomes $f_1(z) = z^2 - \beta\cdot z + \alpha_a$, and the one in (9) becomes $f_2(z) = z^3 + (\alpha_a/4-\beta)\cdot z^2 + \alpha_a/2\cdot z + \alpha_a/4$. With standard, synchronous sampling (W_{ORA1}), the roots of f_1 are stable for $\alpha_a < 1$. The roots are real for $\alpha_a < 0.246$. With error-free feedback acquisition (W_{ORA2}), the roots of f_2 are stable for $\alpha_a < 1.33$. The roots are real for $\alpha_a < 0.223$.



a) b)

Fig. 7. a) Block diagram of the load with the voltage disturbance, the feedback transfer function W_{FB} and the inner active resistance feedback R_a; b) Simplified block diagram with $W_{ORA} = W_O/(1+R_a \cdot W_O \cdot W_{FB})$, where W_{ORA} and W_O acquire additional indices 1 and 2, as per subsections III-A and III-B.

The above analysis of the pulse transfer function W_{ORA} implies that the introduction of error-free feedback acquisition with improved task scheduling does not reduce the range of applicable active resistance gains. The current controller suitable for the use with W_{ORA2} is introduced next.

IV. Decoupling Current Controller

With the load and the active resistance feedback represented by W_{ORA}, the closed loop system is shown in Fig. 8. The goal of further developments is to arrive at the current controller W_{REG} capable of decoupling the impact of the R_a feedback on the step input response.

A. Controller Design

The internal model control (IMC) defines the controller which includes the inverse of the plant transfer function W_{PL} and an integrator [4], [7], [8], [16]. In (10), α represents the adjustable gain.

$$W_{REG}(z) = \frac{1}{W_{PL}(z)} \cdot \frac{\alpha}{\left(1 - z^{-1}\right)} \cdot \tag{10}$$

In an ideal case with $W_{FB} = 1$, design (10) reduces the open loop transfer function to a plain integrator, thus resulting in the closed loop transfer function with a single real pole, defined by the gain α.

The plant transfer function W_{PL} may comprise the time delays and zeros out of the unit circle. Attempted inversion of such elements results in unfeasible prediction and unstable poles. With z^2 in numerator and z^3 in denominator, the inverse of the modified transfer function W_{ORA2} of (9) would imply prediction of one sampling period T_S. For this reason, decoupling controller has to be designed as

$$W_{REG}(z) = \frac{1}{W_{ORA2}(z)} \cdot \frac{\alpha}{\left(1 - z^{-1}\right)} \cdot \frac{1}{z} \cdot \tag{11}$$

Rather than considering $i^e(z)$ as the output in Fig. 8, it is also possible to adopt $i^{FB}(z)$, changing the plant transfer function into $W_{PL} = W_{ORA2} \cdot W_{FB}$. Yet, the inversion of $W_{FB}(z)$ of (5) results in two unacceptable poles at $z = -1$. Therefore, the subsequent design steps are based on (11).

B. The Closed Loop Transfer Function

By introduction of W_{ORA2} of (9) into expression (11), the transfer function of the decoupling controller becomes

$$W_{REG}(z) = \alpha \cdot \frac{L}{T_S} \cdot \frac{z}{z-1} \cdot \cdot \left[e^{j\omega_{dq}T_S} + z^{-1}\left(\frac{R_a T_S}{4L} - \beta\right) + z^{-2}\frac{R_a T_S}{2L} + z^{-3}\frac{R_a T_S}{4L} \right] \tag{12}$$

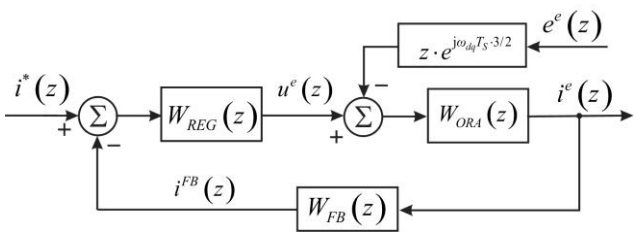


Fig. 8. The block diagram of the digital current controller in the *d-q* frame.

The block diagram of the decoupling controller is given in Fig. 9. The output $u^e = u_d + ju_q$ is the voltage reference that gets limited by commonly used vector limiter which checks the amplitude and maintains the angle. With $W_{REG}(z)$ of (12), the product $W_{REG} \cdot W_{ORA2}$ is equal to $\alpha/(z\text{-}1)$. The closed loop transfer function is

$$W_{SS}(z) = \left.\frac{i^e(z)}{i^*(z)}\right|_{e^e(z)=0} = \frac{W_{REG}W_{ORA2}}{1 + W_{REG}W_{ORA2}W_{FB}} = \frac{\alpha \cdot z^2}{z^3 + z^2\left(-1 + \frac{\alpha}{4}\right) + z\frac{\alpha}{2} + \frac{\alpha}{4}} = \frac{\alpha \cdot z^2}{f_A(z)} \tag{13}$$

In (13), $f_A(z)$ represents the characteristic polynomial in the denominator. The active resistance R_a does not affect the closed loop transfer function $W_{SS}(z)$. Therefore, one expects the experimental traces of the input step response that do not depend on the presence or value of the active resistance R_a. The absence of R_a in (13) makes the frequency characteristics of $W_{SS}(z)$ insensitive to changes of the active resistance.

C. Disturbance Transfer Function

The capability of suppressing the voltage disturbances can be examined from the disturbance transfer function $Y^e(z)$,

$$Y^e(z) = \left.\frac{i^e(z)}{-e^e(z)}\right|_{i^s=0} = \frac{T_S \cdot \left(z^5 - z^4\right)/L}{f_A(z) \cdot f_B(z)} \cdot e^{\frac{j\omega_{dq}T_S}{2}}, \tag{14}$$

where the polynomial

$$f_B(z) = z^3 e^{j\omega_{dq}T_S} + z^2\left(\frac{R_a T_S}{4L} - \beta\right) + z\frac{R_a T_S}{2L} + \frac{R_a T_S}{4L} \tag{15}$$

resides in the denominator of the pulse transfer function $W_{ORA2}(z)$ of the modified plant (9), while $f_A(z)$ is the denominator in (13).

Disturbance transfer function (14) defines the response of the load current i^e in the *dq* frame to the voltage disturbance $-e^e$ in *dq* frame. It is of interest to obtain the transfer function $Y^s = i^s/(-e^s)$ that defines the load current response i^s in the stationary frame to voltage disturbances in the same coordinate frame. Considering the stationary frame voltage disturbance at the frequency ω_x, and assuming that the synchronous *dq* frame revolves at the speed ω_{dq}, Y^s can be obtained from Y^e,

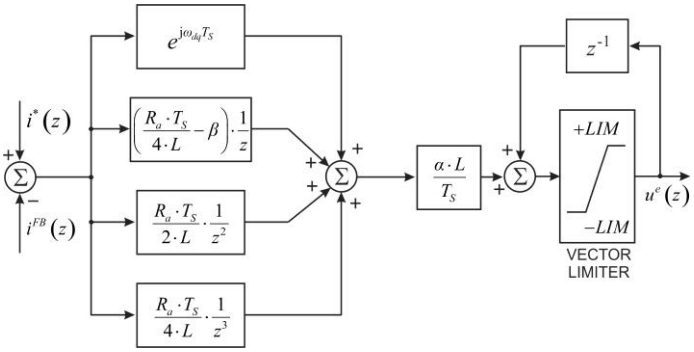


Fig. 9. Block diagram of the proposed decoupling controller.

$$Y^s\left(z\right)=Y^s\left(\mathrm{e}^{\mathrm{j}\omega_x T_S}\right)=Y^e\left(\mathrm{e}^{\mathrm{j}\omega_x T_S}\mathrm{e}^{-\mathrm{j}\omega_{dq}T_S}\right)=Y^e\left(\mathrm{e}^{\mathrm{j}\left(\omega_x-\omega_{dq}\right)T_S}\right). \quad (16)$$

Thus, when considering the stationary frame voltage disturbance at the frequency ω_x and with the amplitude U_x, the amplitude I_x of the load current response is obtained as $Y^s U_x$, where Y^e is obtained by replacing the frequency ω_x and the speed ω_{dq} of the dq frame into (16).

D. The Useful Range of R_a Gains

Disturbance rejection is increased with larger values of the active resistance gain R_a which resides in the denominator of $Y^e(z)$ (14). It is of interest to establish the range of acceptable R_a gains. With the proposed current controller (12), the resulting closed loop transfer function (13) does not get affected by R_a, and it does not impose any R_a limit.

While the decoupling controller of (12) compensates dynamics of the modified plant $W_{ORA2}(z)$ (9) and keeps the input step response $W_{SS}(z)$ (13) unaffected, disturbance transfer function $Y^e(z)$ (14) does get affected by $W_{ORA2}(z)$, since both transfer functions include the polynomial $f_B(z)$ (15) in the denominator. In order to insure a well damped disturbance-step response, it is necessary to control the roots of $f_B(z)$ by limiting the values of R_a. For this purpose, the R_a limits for the pulse transfer function W_{ORA1} (4) (obtained with the conventional synchronous sampling) and for the pulse transfer function W_{ORA2} (9) (obtained with the error-free sampling (Fig. 5) have been checked. In addition to checking W_{ORA2}, it is also of interest to verify the stability of the closed loop pulse transfer function W_{SS} (13).

E. Stability and Robustness

With IMC controller, dynamic modes of the subsystem W_{ORA2} are decoupled from the closed loop pulse transfer function W_{SS} of (13). The closed loop system is stable if the polynomial $f_A(z)$ in denominator of (13) has the roots which reside within the unit circle of the z-plane. Applying the Jury stability criterion to $f_A(z)$, stability limit of the gain α is 1.33, far beyond the values that provide well-damped, low-overshoot response, as shown in Table I of [15].

It is also of interest to check the stability of the subsystems W_{ORA1} and W_{ORA2}. To that purpose, the Jury stability criterion has to be applied to polynomials in denominator of (4) and (9). The limit values for the relative gains $R_a \cdot T_S/L$ are given in Table I. Stability limit obtained with $\omega_{dq}T_S = 0.1 \cdot 2\pi$ is lower than the limit obtained with $\omega_{dq}T_S = 0$. The maximum values of $R_a \cdot T_S/L$ that maintain the poles of $W_{ORA1}(z)$ real are some 9% larger than the corresponding values obtained with $W_{ORA2}(z)$.

In addition to stability and aperiodicity, it of interest to test the effect of the parameter changes on transfer functions $W_{ORA1}(z)$ and $W_{ORA2}(z)$. The robustness of the controller can be quantified by the vector margin VM [7]. The values of VM lower than 0.5 are usually associated with elevated sensitivity to parameter changes and with consequential oscillatory response. In Table I, the last two columns contain the gains $R_a \cdot T_S/L$ that bring the vector margin to VM = 0.5 and VM = 0.6. Adopting the vector margin of VM = 0.5, the gain $R_a \cdot T_S/L$ that corresponds to $W_{ORA1}(z)$ is some 20% lower than the corresponding value obtained with $W_{ORA2}(z)$.

In Table I, the gain limit that maintains aperiodic response is relatively close to R_a^{opt} in [4]. The gain limit that maintains VM > 0.5 for W_{ORA2} is relatively close to R_a^{max} in [4]. Further developments will consider W_{ORA2} and $R_{am} < R_a \cdot T_S/L < R_{aM}$, where $R_{am} = 0.22$, $R_{aM} = 0.54$.

F. Disturbance Rejection

In absence of the active resistance feedback, the synchronous frame current controllers exhibit considerable output errors in response to the voltage disturbances [4], [15]. By introducing L = 3.38 mH, T_S = 50 μs and $\omega_{dq} = 2\pi \cdot 50$ in (14), and considering the voltage disturbance $-e^e = (1 + \mathrm{j} \cdot 0)$ V, the inverse z transformation provides the corresponding output errors $i_d(t)$ and $i_q(t)$ given in Fig. 10. The traces are obtained for $R_a = 0$ and for $R_aT_S/L = R_{am}/5$. The peak error in excess of 50 mA, obtained with $R_a = 0$, suggests that the error reaches the rated current for the disturbance of 150 V within the setup described in Appendix I. The initial $i_q(t)$ pulse lasts roughly $200 \cdot T_S$ = 10 ms. According to the second pair of traces in Fig. 10, it takes just 20% of R_{am} to achieve considerable reduction of the settling time.

The case studied in Fig. 10 is repeated in Fig. 11 for larger values of the active resistance. The three sets of traces are obtained with $R_aT_S/L = R_{am}$, R_{aM}, and $1.5 \cdot R_{aM}$. With R_{am}, disturbance response is aperiodic and it settles below 1% in roughly $14 \cdot T_S$ = 700 μs. With R_{aM}, the response is well damped, and it has noticeably reduced integral of the error. With $1.5 \cdot R_{aM}$, the response is even quicker, but the damping is considerably reduced. Thus, the traces of Fig. 11 justify the choice $R_{am} < R_a \cdot T_S/L < R_{aM}$.

In addition to the analysis of the time response, it is of interest to study the impact of the gain R_a on the function $|Y^S(\mathrm{j}\omega)|$. In Fig. 12, it is assumed that the dq frame revolves at $\omega_{dq} = 2\pi \cdot 50$. The function $|Y^S(\mathrm{j}\omega)|$ is obtained for R_a = 0, R_{am}, and R_{aM}. All the curves drop to zero for $\omega = \omega_{dq}$. In the region of the inverse component ($-2\pi \cdot 50$), the active resistance reduces Y^s by more than 30 times. At the same time, the gain increase from R_{am} up to R_{aM} has significant impact on reduction of Y^s.

TABLE I
THE LIMIT VALUES FOR THE RELATIVE GAIN R_aT_S/L

Limit values of the gain $R_a \cdot T_s/L$	Stability limit $\omega_{dq}T_s = 0$	Stability limit $\omega_{dq}T_s = 0.1 \cdot 2\pi$	Real poles limit	Vector margin VM > 0.5	Vector margin VM > 0.6
W_{ORA1} (4)	1.00	0.62	0.24	0.45	0.35
W_{ORA2} (9)	1.33	0.96	0.22	0.54	0.41

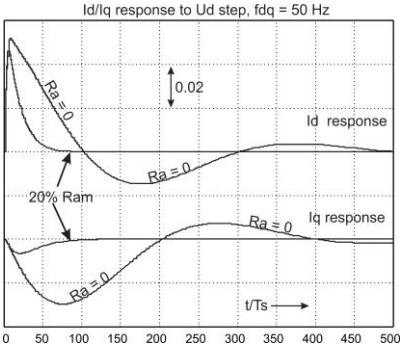


Fig. 10. Disturbance step responses i_d and i_q obtained from the transfer function Y^e (14) for f_{dq} = 50 Hz, and with disturbance step of U_d = 1V. The traces are obtained by computer simulation for $R_a = 0$ and for $R_aT_S/L = R_{am}/5$.

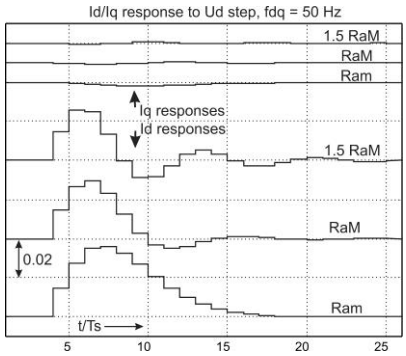


Fig. 11. Disturbance step responses i_d and i_q obtained from the transfer function Y^S (14)-(16) for f_{dq} = 50 Hz, and with disturbance step of U_d = 1V. Simulation traces are obtained for $R_aT_S/L = R_{am}$, R_{aM}, and 1.5 R_{aM}.

The integral error *IE* [4] is a widely accepted indicator of the disturbance rejection capability. It is calculated as the integral of $|\Delta i_d(t) + j\Delta i_q(t)|$ obtained for the unit step of the voltage disturbance [4]. In Table II, the values of IE/T_S are given for $0 < R_aT_S/L < R_{aM}$. The active resistance gain R_{am} reduces the integral error more than 34 times. An increase from R_{am} to R_{aM} results in an ultimate reduction of IE/T_S from 0.23 to 0.12, which comes at the cost of losing the aperiodic nature of the disturbance step response (Fig. 11).

V. Experimental Results

Analytical considerations and simulation results have been corroborated by the corresponding experimental results. The setup includes a pair of mechanically coupled three-phase synchronous permanent magnet motors, wherein the second motor is used as a brake that maintains the desired steady state speed. An industrial PWM-controlled IGBT inverter [17] with DSP controller is used and the switching frequency is 10 kHz. The experimental rig is shown in Fig. 13 (as noted, the relevant parameters are given in Appendix I). A more detailed description of the error-free oversampling-based acquisition of the feedback signals is available in [11].

The experimental verification has the following goals:

- To compare simulated and experimental responses to input step changes of the reference current;
- To explore the range of active resistance gains which do not impair the input step response;
- To compare simulated and experimental responses to step changes of the voltage disturbances;
- To check disturbance responses obtained with active resistance gains in excess of R_{aM}.

The step responses obtained from the previous analytical considerations and simulation traces correspond to the output current i^e in Fig. 8. However, the subsequent experimental traces correspond to the feedback current i^{FB} in Fig. 8. The relation between i^e and i^{FB} is given in (5).

The impact of the active resistance on the input step response is studied in Fig. 14. The traces $i_d(t)$ and $i_q(t)$ are obtained for the step change of the current reference i_q^*. The three pairs of traces are obtained without the active resistance gain (R_a=0), with R_{am}, and with R_{aM}. The *q*-axis current step response remains unaffected by the introduction of R_{am} and R_{aM}. In all cases (including R_a=0) the *d*-axis current remains at $i_d(t) = 0$ with a minuscule ripple.

Along with the step response of the *q*-axis current, it is of interest to verify the step response of the *d*-axis current at high speeds. Experimental traces in Fig. 15a represent the step response of $i_d^{FB}(t)$ obtained with R_{aM} at f_{dq} = 270 Hz. At the same time, it is of interest to verify the step response of the controller at very low speeds. Experimental traces in Fig. 15b represent the step response of $i_q^{FB}(t)$ obtained with R_{aM} at f_{dq} = 0 Hz. The results prove that the step response of both i_q and i_d currents is maintained over the range of operating conditions.

In order to explore the range of practical R_a gains, the i_q current step response is shown again in Fig. 16 with $R_a{\cdot}T_S/L$ reaching $2.25{\cdot}R_{aM}$ = 1.215, the value just slightly below the stability limit of the modified plant W_{ORA2} (1.33 in Table I). While the traces obtained with $0 < R_a{\cdot}T_S/L < 1.5{\cdot}R_{aM}$ remain seemingly unaffected by R_a, the case with excessive gain $2.25{\cdot}R_{aM}$ brings the subsystem W_{ORA2} to the brink of instability and gives rise to noticeable oscillations of the i_q waveform. Thus, the value of $1.5{\cdot}R_{aM}$ should not be exceeded, while the recommended range remains $R_{am} < R_a{\cdot}T_S/L < R_{aM}$.

Simulation traces in Figs. 10 and 11 comprise the traces of i_d and i_q obtained with the step change of the voltage disturbance. With the present experimental rig, it is not possible to assert the step change of the back electromotive force. Therefore, the experimental traces with the disturbance step responses (Fig. 17) are obtained by introducing the step change into the reference voltage u_q^*. The voltage step is set to 67V, so as to keep the resulting peak current within reasonable range. In Fig. 17a, disturbance step response is obtained without the active resistance feedback. The relevant traces are in accordance with the simulated traces of Fig. 10. In Figs. 17b, 17c, and 17d the active resistance gain is set to R_{am}, R_{aM} and $1.5{\cdot}R_{aM}$. Experimental traces are in reasonable agreement with the simulation traces of Fig. 11. The peak currents in Fig. 11 are obtained with the unit step change of the voltage disturbances. When multiplied by 67 V, the values correspond to the peak currents in Fig. 17. Slight difference between simulated and experimental traces comes from the fact that the former represent the output current i^e, before the W_{FB}, while the latter represent the feedback current i^{FB}, the outcome of the feedback processing within W_{FB} of (5).

Disturbance response of Fig. 17a is obtained with R_a = 0, and it agrees with the simulation given in Fig. 10. The peak current reaches 3.5 A, and it barely settles in $500{\cdot}T_S$ = 25 ms. With R_{am} in Fig. 17b, the peak current reduces to 2.3 A, and the settling time reduces to $15{\cdot}T_S$ = 0.75 ms. Reduction of the peak current and the settling time are compatible with predicted reduction of the integral error (*IE*) given in Table II. Further increase of the gain to R_{aM} makes the current pulse shorter at the cost of minor oscillations (Fig. 17c). Any further increase of the gain (to $1.5{\cdot}R_{aM}$ in Fig. 17d) introduces more oscillations and protracts the settling time. Thus, the recommended range remains $R_{am} < R_a{\cdot}T_S/L < R_{aM}$.

Frequency response of the feedback line with the error-free sampling is obtained according to Fig. 5 and expression (2) of [11]. Corresponding amplitude characteristic is calculated for the sampling period of T_S = 100 μs and given in Fig. 18. It features complete removal of any noise at the frequency $1/(2T_S)$ and its multiples. Attenuation appears to be limited to approximately 200 dB for purely numerical reasons.

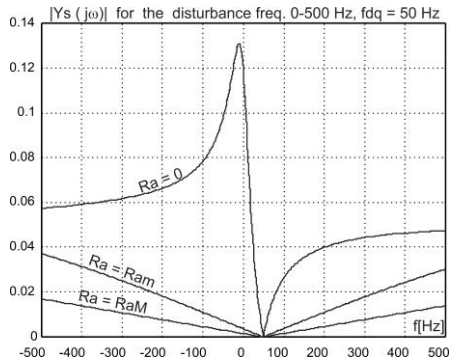


Fig. 12. The amplitude characteristic of the disturbance transfer function Y^s for f_{dq} = 50 Hz, obtained for $R_aT_S/L = 0$, R_{am}, and R_{aM}.

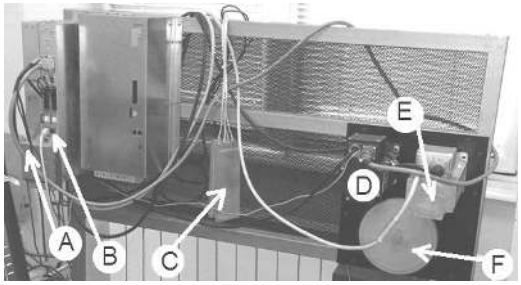


Fig. 13. Experimental setup with 6-pole synchronous permanent magnet motor: (A) Main power supply unit providing dc-bus voltage of 520V; (B) Two-axis module comprising two 3-phase inverters and control circuits; (C) Dynamic breaking resistor; (D) Speed controlled motor; (E) Torque controlled motor; (F) Inertia coupled by a toothed belt with the two motors.

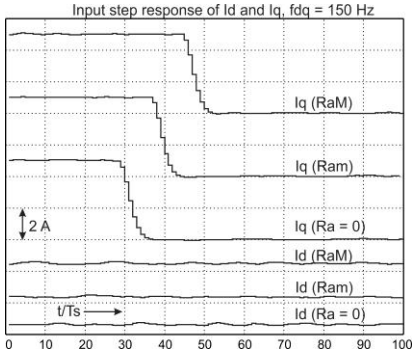
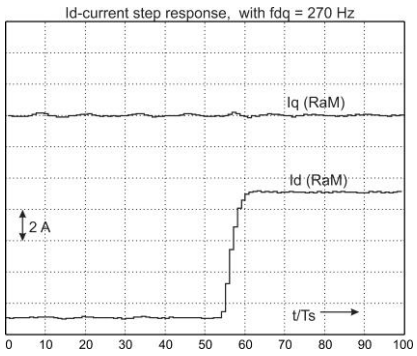


Fig. 14. Response traces of $i_d^{FB}(t)$ and $i_q^{FB}(t)$ for the step change of the current reference i_q^*. The traces are obtained with no active resistance feedback (R_a=0) and with active resistance gains of R_{am} and R_{aM}. The electrical frequency was f_{dq} = 150 Hz (n = 3000 rpm).

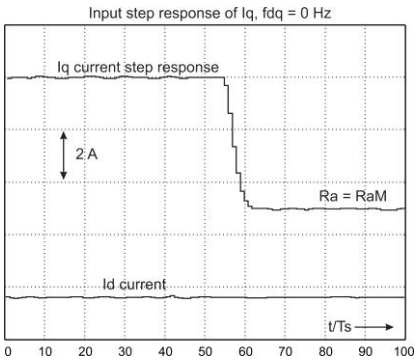
TABLE II
THE INTEGRAL ERROR IE [4] FOR f_{dq} = 50 HZ AND U_d STEP OF 1V

$R_a \cdot T_s/L$	0	0.02	0.04	0.08	0.1	**0.22**	0.3	0.4	0.5	**0.54**
IE/T_S	7.68	1.98	1.15	0.60	0.49	0.23	0.18	0.15	0.13	0.12

The frequency response of the closed loop transfer function is considered in Fig. 19. It compares the conventional, synchronous sampling current controller of [7] to the one obtained with the controller proposed in this paper. The amplitude and phase characteristics are obtained from the closed loop transfer function given in equation (12) of [7], and also from the closed loop transfer function of (13). The results prove that the new current controller with the error-free sampling performs the same or better than the traditional controller with error-sensitive synchronous sampling.



a)



b)

Fig. 15. a) Input step response of the d-axis current $i_d^{FB}(t)$ obtained with R_{aM} at f_{dq} = 270 Hz. b) Input step response of the q-axis current $i_q^{FB}(t)$ obtained with R_{aM} at f_{dq} = 0 Hz. The q-axis current steps from +5A down to 0A.

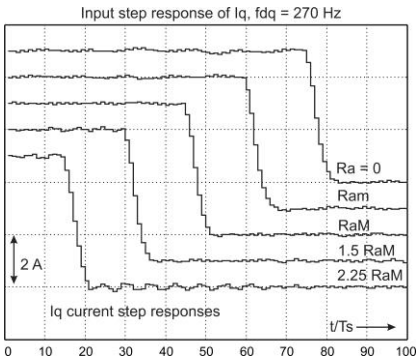


Fig. 16. Input step response of $i_q^{FB}(t)$ obtained with no active resistance feedback (R_a=0) and with active resistance gains of R_{am}, R_{aM}, $1.5 \cdot R_{aM}$ and $2.25 \cdot R_{aM}$. The electrical frequency was f_{dq} = 270 Hz.

VI. CONCLUSION

The paper shows that application of active resistance feedback in conjunction with the conventional sampling leads to excessive noise and current ripple in current controlled inverter applications. The noise can be removed by means of a different, error-free sampling, which however introduces a delay. It is shown that the existing method of active resistance feedback cannot be used in systems with error-free sampling, because the deterioration in the step input response.

Next, a novel digital current controller structure is designed, such that the active resistance feedback can be applied in conjunction with error-free sampling while keeping the quality of the input step response the same as before the introduction of the active resistance feedback. Design of such a controller,

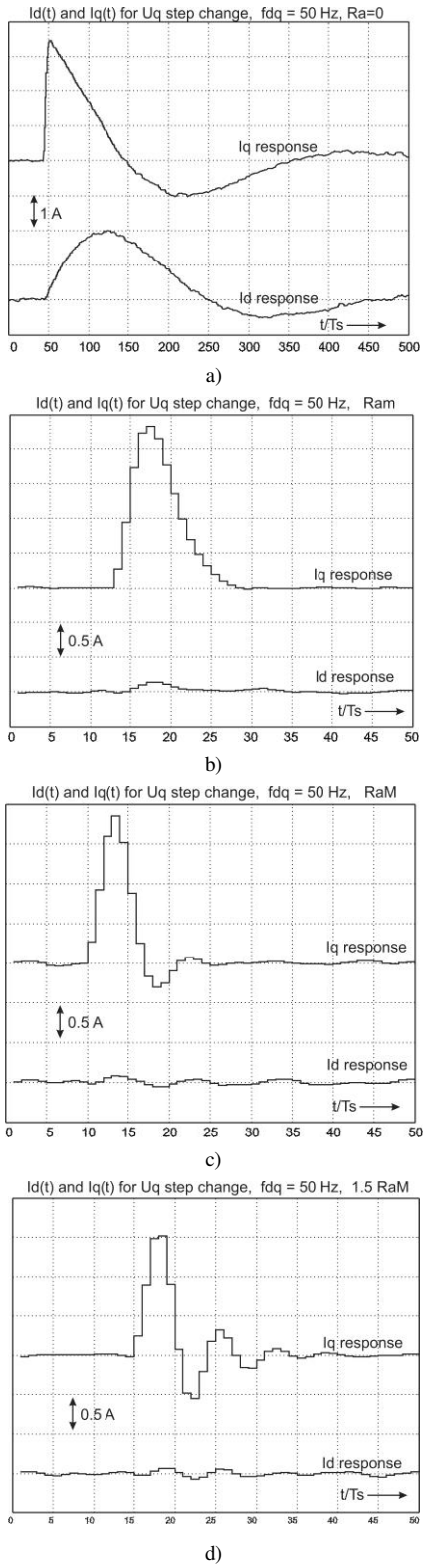


Fig. 17. Response traces of $i_d^{FB}(t)$ and $i_q^{FB}(t)$ for the step change of the voltage command u_q^* by 67 V. Disturbance step response is obtained at the electrical frequency of 50 Hz (1000 rpm), with the active resistance gain set to: a) 0, b) R_{am}, c) R_{aM}, and d) $1.5 \cdot R_{aM}$.

which is characterized with an original structure, is described in detail. The applicable range of the active resistance feedback values is derived analytically and the results are confirmed by simulations and experiments.

It is verified analytically, by simulation, and experimentally that the input step response of the novel controller is decoupled from the active resistance feedback for all active resistance values up to the one that would bring the system (i.e. modified plant) at the stability limit. The experiments confirm that (1) the active resistance feedback can be used in conjunction with error-free sampling while keeping the input step response decoupled, and (2) the integral error as a measure of the disturbance rejection quality is reduced by more than 30 times.

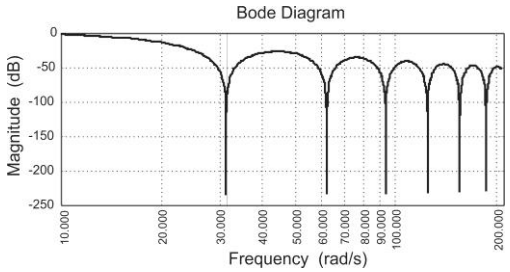


Fig. 18. Frequency response (amplitude characteristic) of the feedback line with the error-free sampling.

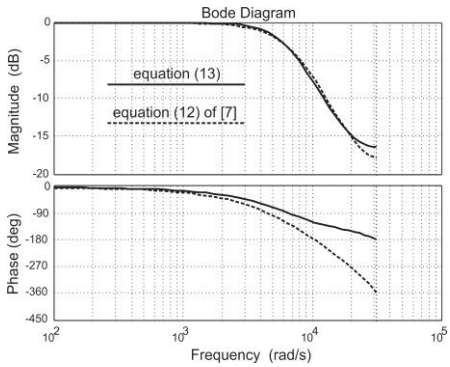


Fig. 19. The frequency response of the current controller: The amplitude and phase characteristic of the closed loop transfer function. The plot compares the frequency response obtained with synchronous-sampling digital current controller of [7] to the one proposed in this paper.

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APPENDIX I: EXPERIMENTAL SET-UP DATA

Number of poles:	$2p = 6$
Motor rated current:	$I_{nom} = 7.3$ Arms
Motor torque constant:	$k_t =$ 0.821 Nm/Arms
Back EMF constant:	$k_e = 0.687$ Vpeak/(rad/s)
Stator resistance:	$R_S = 0.47\ \Omega$
Stator inductance:	$L_S = (L_d + L_q)/2 = 3.38$ mH
DC bus voltage:	$E_{DC} = 520$ V dc
Peak current (current limit):	$I_{max} = 45$ A
PWM frequency:	$f_{PWM} = 1/T_{PWM} = 10$ kHz
Rated lockout time:	$t_{DT} = 3\ \mu s$
DSP controller:	TMS320F28335
ADC resolution:	$N_{ADC} = 12$-bit
Oversampling period:	$T_{ADC} = T_{PWM}/32$
PWM method:	Symmetrical PWM

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