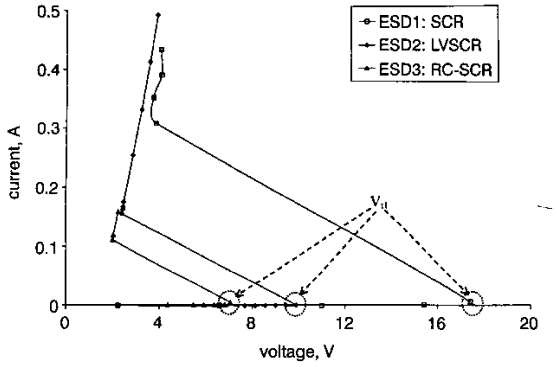

Fig. 4 *I–V characteristics for plain SCR, LVSCR and RC-SCR by TLP tests*

Conclusions: A simple, novel RC-coupling-based ESD protection circuit is designed and implemented in 0.35 μm plain CMOS to realise ultra low triggering. The new concept is proved by both simulation and tests. The low V_{t1} of 7 V, a 60% and 28% reduction over a plain SCR and LVSCR, respectively, makes RC-SCR a viable ESD protection solution for CMOS mixed-signal and RF ICs.

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Digital-domain self-calibration technique for video-rate pipeline A/D converters using Gaussian white noise

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A digital-domain self-calibration technique for video-rate pipeline A/D converters based on a Gaussian white noise input signal is presented. The proposed algorithm is simple and efficient. A design example is shown to illustrate that the overall linearity of a pipeline ADC can be highly improved using this technique.

Introduction: A broad area of applications with enhanced performance requires high-resolution analogue-to-digital (A/D) conversion with sampling rates (F_S) in the order of tens of MHz range. The most attractive solutions for implementing this type of A/D converters (ADCs) employ pipelining as a means of relaxing the speed requirements of the analogue components. Such architectures use a cascade of stages comprising a low-resolution flash quantiser and a multiplying digital-to-analogue converter (MDAC), which computes and amplifies the residue for the next stages. As a consequence, the precision requirements are more critical in the front-end stage of the pipeline, which must exhibit the accuracy of the overall ADC, and are progressively relaxed towards the last stage. Without using either trimming or self-calibration techniques, the overall resolution of these ADCs is limited by the linearity and gain errors of the front-end MDACs. These errors are bounded around the 8 to 10 bit level by the component matching accuracy of most CMOS processes available today. As trimming is expensive, self-calibration either in the analogue or in the digital domain must be considered for extending the resolution of such ADCs above 10 bits. The analogue techniques proposed in the literature require separate calibration DACs and precision analogue components [1, 2]. Although, digital calibration techniques do not require sophisticated analogue circuitry they put an extra burden on the digital part [3, 4]. Furthermore, the MDAC of a calibrated stage has to be modified (introduction of many additional switches) to perform the required code-error measurements [4]. Moreover, the technique proposed in [3] can only be employed in 1.5 bit MDACs and, therefore, it is not suitable for power-optimised high-resolution architectures where multibit rather than single-bit front-end stages are preferred [5].

Proposed technique: The technique proposed in this Letter consists of applying a Gaussian white noise (GWN) stimulus to the ADC and calculating the calibrating codes from the histogram of the output codes. There are several advantages of this digital-domain self-calibration technique when compared with those reported in [3, 4]: (i) the entire ADC does not need to be modified; (ii) it is suitable for ADCs with multibit front-end stages; (iii) wideband ($2F_s$) GWN is relatively easy to generate on-chip using a lateral PNP transistor followed by a gain-stage and by a switched-capacitor programmable-gain amplifier (PGA) for standard-deviation adjustment; on-chip self-testing can be performed; (iv) GWN having a uniform power spectral density allows a full-speed characterisation of the ADC [6]; and (v) the use of a cumulative technique (histogram) will eliminate uncertainties from the calibrating codes due to noise.

In an N-bit pipeline ADC comprising an M_1-bit front-end stage and N_S stages, the overall linearity is mainly limited by the mismatches in the first stage. A typical conversion characteristic consists basically on 2^{M_1} segments dislocated from an 'almost' ideal straight line. The digital amounts of dislocation can be measured during a calibration cycle and stored in a memory. These 2^{M_1} calibrating codes can be addressed later and recalled during normal conversion mode, using the coarse digital outputs from the first stage M_1-bit quantiser, and the conversion characteristic moved back to the ideal line by digitally subtracting these codes. Applying centred GWN to the input of the ADC, a $2^{(M_1+2)}$ bins histogram can be computed by counting the number of occurrences of the output codes inside the corresponding bins defined by the (M_1+2) bits of the output code. This histogram, $H[i]$, will have a Gaussian shape, more or less 'distorted' by the existing deviations of the segments. Assume now that there is a specific table, $T[i]$, with $2^{(M_1+2)}$ values, truncated and stored in a memory, and defined by

$$T[i] = (A[i])^{-1},$$
$$A[i] = \int_{(i-1)2^{(N-(M_1-2))}}^{i\cdot 2^{(N-(M_1+2))}} (\sigma \cdot \sqrt{2\pi})^{-1} e^{-(x-\mu)^2/2\sigma^2} dx$$

where $A[i]$ represents the ideal $2^{(M_1+2)}$ histogram produced mathematically using a Gaussian distribution function with $\mu = 2^{(N-1)}$ and $\sigma = 2^{(N-1)}/2$. $T[i]$ is used to normalise $H[i]$, resulting, in the ideal case, in a histogram with $2^{(n-(M_1+2))}$ occurrences in each bin. The differences from this expected value can be used to calculate the calibrating codes. Thus, assuming a large number of samples, n, these differences are given by

$$D[i] = \frac{H[i] \cdot T[i]/2^{(M_1+2)} - 2^{(n-(M_1+2))}}{2^{(n-N)}} + \left|\frac{n - 2 \cdot N_N}{n}\right|$$

where the second term comprises the offset of the GWN generator and the offset error of the ADC, which can easily be computed by counting

the number of samples, below the mid-scale code, N_N. Since differential MDAC implementations usually exhibit code-error symmetry around the most-significant bit transition, only $2^{(M_1-1)}$ calibrating codes have to be found. Using $D[i]$, $2^{(M_1-1)}$ segment deviations, $Dev[k]$, can be determined according to:

$$Dev[k] = \sum_{j=0}^{i}[D[k \cdot 2^{(M_1-1)} + j] + D[2^{(M_1+2)} - k \cdot 2^{(M_1-1)} + j]]$$

The gain error of the ADC, ε_{GAIN}, as well as the $2^{(M_1)}$ calibrating codes, $C_{CODE}(k)$, can be found according to

$$C_{CODE}(1) = -\varepsilon_{GAIN} = -0.5 \sum_{k=1}^{2^{(M_1-1)}} Dev[k]$$

$$C_{CODE}(k) = C_{CODE}(k-1) + 0.5 \cdot Dev[k], \quad 1 < k \leq 2^{(M_1-1)}$$

$$C_{CODE}(k) = -C_{CODE}(2^{M_1} - k + 1), \quad k > 2^{(M_1-1)}$$

The number of samples in each bin is described by the binomial distribution, $B(\mu = n \cdot p[i], \sigma = \sqrt{(n \cdot p[i] \cdot (n - p[i]))}$, where $p[i]$ represents the probability of a given sample falling into the ith bin (that depends on the bin width). For an accuracy of 0.25 LSB at N-bit, if the standard deviation of the noise generator is adjusted to $\pm 2\sigma$ compared to the full-scale of the converter and for a 3σ yield, n must verify

$$n > \frac{3 \cdot (n-p) \cdot 2^{(N+M_1)}}{p}$$

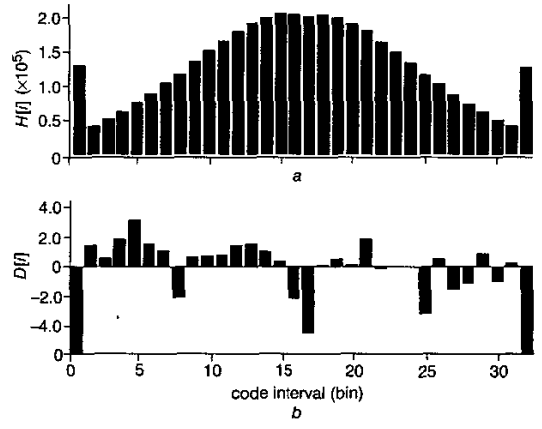

Fig. 1 *Histograms*
a H[i]
b D[i]

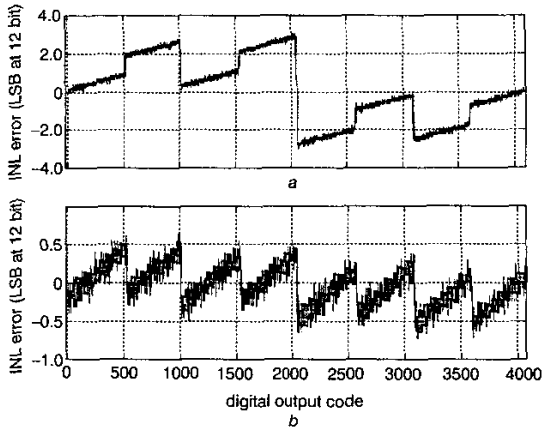

Fig. 2 *INL errors*
a Before calibration
b After calibration

Results: To validate the theoretical findings and assess the performance of the proposed technique an $N = 12$ bit pipelined ADC with digital correction and overflow/underflow detection was modelled using MATLAB code. A three-bit *per*-stage architecture ($M_1 = 3$ bit) was adopted. The main static non-ideal effects were included, namely the offset voltages in the comparators of the quantisers and the matching accuracy (9 bit) in the capacitor arrays in all MDAC blocks. The input-referred thermal noise of the ADC was also included and defined at 0.5 LSB below the quantisation noise. During the initial step of the calibration, the standard deviation of the GWN generator was adjusted to $\pm 2\sigma$ as required by measuring the counts in bins $H[1]$ and $H[32]$ and digitally adjusting the gain of the GWN generator (through the PGA). An amount of $n = 2^{22}$ samples was then used to compute the histogram $H[i]$ with 32 bins. Figs. 1*a* and *b* show the histograms of $H[i]$ and $D[i]$, respectively. Figs. 2*a* and *b* show, respectively, an INL before and after calibration, measured using a static method by sweeping the input of the ADC with a full-scale ramp with steps of 1/8 LSB at 12 bit. The initial INL errors are at the 9 bit level and after calibration the observed linearity is approximately $+0.6/-0.8$ LSB at the 12 bit level. Several simulations were carried out and the maximum INL errors after calibration were always within ± 1 LSB, since 1 bit is lost due to the accumulation of the digital truncation errors.

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Dual-mode pipeline A/D converter for direct conversion receivers

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An embedded dual-mode 8 bit 1/15.36 MS/s CMOS pipeline A/D converter for 2G and 3G multimode direct conversion receivers in presented. Power dissipation is minimised by optimising the architecture and by utilising voltage reference circuitry and operational amplifier, which are reconfigured between the narrow- and wide-band modes.

Introduction: Third generation (3G) systems are currently being utilised. However, the high costs of the required new infrastructure mean that second generation (2G) cellular systems are still used alongside them, at least in rural areas—a need for multi-mode transceivers is evident. To keep the size, cost, and power dissipation of such devices attractively low, as many building blocks as possible must be shared between different systems, including the analogue front-end. The direct-conversion receiver architecture offers high integration density and adaptation capability. Reconfigurable