Digital electrostatic electron-beam array lithography

L. R. Baylor,[a] D. H. Lowndes, M. L. Simpson, C. E. Thomas,[b] M. A. Guillorn, V. I. Merkulov, J. H. Whealton, E. D. Ellis, D. K. Hensley, and A. V. Melechko
Oak Ridge National Laboratory, Oak Ridge, Tennessee 37831

(Received 25 May 2002; accepted 16 September 2002)

A concept for maskless digital electrostatically focused e-beam array direct-write lithography (DEAL) has been developed at Oak Ridge National Laboratory. This concept incorporates a digitally addressable field-emission array (DAFEA) integrated into a logic and control circuit implemented as an integrated circuit. The design goal is for 3 000 000 individually addressable field-emission cathodes with a 4 μm by 8 μm pitch on a single $\sim$1 cm^2 integrated circuit. The DAFEA design includes built-in electrostatic focusing for each emitter with feedback dose-control circuits to drive each emitter for tightly controlled electron delivery. With the electrostatic focusing, an array of $\sim$460 of these integrated circuits (up to 30 across by $\sim$23 rows deep) are suspended on a back plane $\sim$100 μm above a 300 mm semiconductor wafer. This arrangement could lithographically expose an entire 300 mm wafer, with 30 nm pixels, in less than 45 s, with every wafer pixel redundantly illuminated eight times allowing gray-scale edge placement. Only $\sim$1.5 cm of wafer motion is required for complete wafer exposure. High-speed data paths are proposed to program the patterns into the DAFEA to be written to the wafer. The DEAL concept thus requires no mask and can be extended to the 10 nm linewidth regime. © *2002 American Vacuum Society.*
[DOI: 10.1116/1.1520559]

I. INTRODUCTION

It is well known that optical lithography for semiconductor wafer production is limited by the wavelength of light. Diffraction limits the focus ability of a point to a circle approximately equal to the wavelength. Electrons also have a wavelength and have a theoretical diffraction limit, but as a practical matter the electron wavelength is so short that optical aberrations (electrostatic or magnetic lenses) limit the resolution—typical distortions are on the order of nanometers. This makes electron beam technology a strong candidate for the next several generations of lithographically produced semiconductor devices, with linewidths the order of 50 nm and smaller. Writing with a single electron beam is slow, however, and therefore expensive given the required capital resources. The concept described here writes simultaneously with millions of electron beamlets in an easily programmable field-emitter array (FEA), potentially patterning an entire 1 cm circuit device layer, with 50 nm linewidths, in a period the order of 5 s. The concept is also scalable to linewidths nearly 1 order of magnitude smaller (10 nm).

There has been intense research in recent years into the possibility of increasing the throughput of electron beam direct-write technology to be competitive for wafer production for linewidths of 100 nm and below. The most straightforward method for achieving higher throughput from direct-write technology is to dramatically increase the current in the electron-beam column. Several systems have been proposed that rely on the generation of an extended, high current (several μA) exposing beam for electron or ion image projection.[1,2] Other proposed systems have included the use of a large array of secondary sources or blanking apertures following a wide-area, collimated beam.[3] It has also been suggested that multiple primary sources may achieve useful throughput with total currents to the wafer between 0.5 and 5 μA.[4] Here we propose a system configuration in which multiplexed primary sources illuminate the wafer through the use of a simple, electrostatic focusing system. Because the system employs a large array of independently modulated beamlets, a raster scan system can be used that has the advantage of being maskless. The key element of this configuration is a field emitter electron source nanotechnology currently under development at Oak Ridge National Laboratory (ORNL).

This article outlines a method based on millions of miniature electron beams operating in parallel for lithography in the 50 nm and below linewidth regime. Throughput on the order of 60 or more 300 mm wafers per hour is possible depending on the number of emitter arrays employed. It offers the potential capability of a low-cost high-throughput lithographic manufacturing process for the next generation of ultradense devices.

In Sec. II we describe the overall lithography system concept, then in Sec. III we present a detailed description of the electron sources. In Sec. IV the electron optics design for the system is presented and then in Sec. V the logic, memory, and control circuit is described. Finally in Sec. VI we discuss the present development of the concept and future planned work.

II. LITHOGRAPHY SYSTEM DESIGN CONCEPT

FEAs are two-dimensional arrays of miniature cathodes used for electron beam sources. Custom made FEAs with addressable emitters are proposed for direct writing of litho-

[a]Author to whom correspondence should be addressed; electronic mail: baylorlr@ornl.gov
[b]Currently with nLine Corporation, 4150 Freidrich Lane, Suite A, Austin, TX 78744.

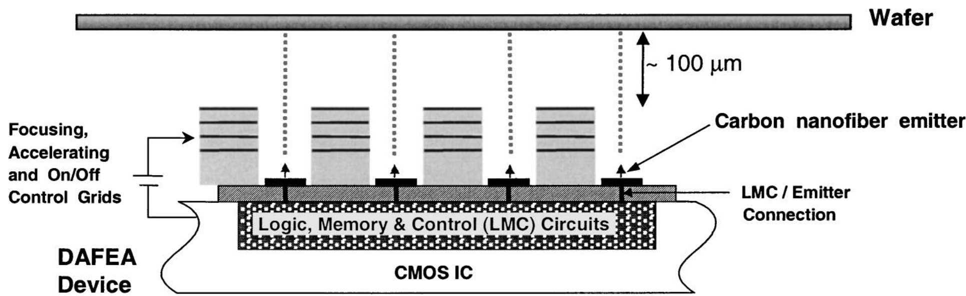

FIG. 1. Schematic diagram of the proposed DAFEA structure fabricated on a silicon wafer containing completed electronic circuitry for logic, memory, and current control.

graphic patterns on semiconductor wafers coated with suitable resist material. A schematic diagram of the proposed approach for a digitally addressable FEA (DAFEA) microfabricated on a silicon integrated circuit containing the logic and memory needed to individually control each emitter is shown in Fig. 1. The individual beamlets from each emitter cathode are addressable, thus enabling patterns to be programmed into the DAFEA before being written onto the target wafer. Turn-on and turn-off of the entire array is achieved by switching the extraction grid (first grid in the stack) to a more negative value. When the extraction grid is "on" emitters biased sufficiently negative relative to the grid will emit. This extraction grid layer on the DAFEA should have relatively small capacitance, and thus can be biased a few 10s of volts positive or negative with switching times the order of 1 μs or less to turn the writing current on and off. In addition to rapidly writing large areas, this concept has the advantage of being effectively a digitally programmable mask, which can be reprogrammed for new layers within 10 ms. The electrostatic focusing is integrated on the DAFEA and consists of additional grids produced lithographically above the emitters and extraction grid, separated by dielectric (nominally low-temperature SiO_2) layers. The separation distances and voltages between the additional grids can be designed to focus each cathode to a 25 nm or smaller spot size with about a 100 μm working distance between the DAFEA device array and wafer to be exposed. This allows lithography to $\sim$50 nm feature sizes.

The resolution of electron-beam lithography is limited by the proximity effect,[5] which is due to the forward scattering of incident electrons on their path through the resist and to backward scattering from the substrate. This scattering leads to exposure of neighboring areas and, therefore, to pattern degradations. The electron beamlets in the digital electrostatic e-beam array lithography (DEAL) concept are designed to have low energies in the 200–1000 eV range. Thus the scattering cross section for these electrons is much lower than conventional electron-beam lithography systems. The proximity effect for DEAL is therefore not expected to have an appreciable effect on the achievable resolution.

Since the density of emitter cathodes is so high ($\sim 3 \times 10^6/\mathrm{cm}^2$), the DAFEAs can be angled slightly with respect to the wafer motion (an angle of about 0.4°). With this arrangement, shown conceptually in Fig. 2, multiple emitters on the DAFEA array can individually illuminate every 30 nm pixel on a 300 mm wafer. This allows for redundancy of emitters addressing any pixel on the wafer, in case of failure of a particular emitter, and also opens up the possibility of gray-scale illumination of the photoresist. The present design proposes that ten emitters pass over and eight emitters illuminate every pixel on the wafer. The number of illuminations and amount of gray scale is a design choice, which can be changed in real time for each lithographic level. Redundancy allows for the possibility of multiple bad emitters on the DAFEA chips (e.g., 1% bad emitters would be easily tolerated). Two extra emitters in all the columns on each DAFEA chip allow for up to two bad cathodes per ten-emitter column, while still allowing eight full emitter illuminations per wafer pixel.

Each DAFEA integrated circuit will produce a time-average current of $\sim$30 μA, from $\sim 3 \times 10^6$ cathodes ($\sim$1 nA from each cathode for 1 μs per illumination, at a frequency of $\sim$10 kHz). Every DAFEA added to the system adds another 30 μA of average current, up to the point where the wafer being patterned is fully overlaid with DAFEAs. An array of 460 DAFEA integrated circuits would have a time-average current of $\sim$9 mA, which is more than 100 times the

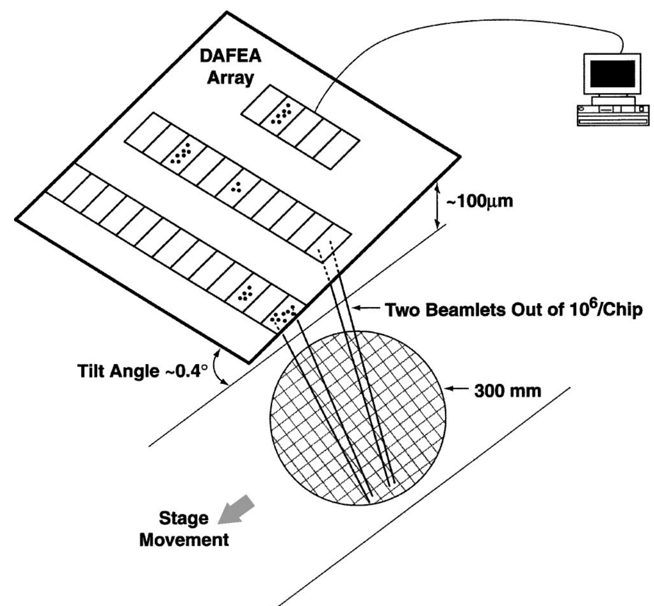

FIG. 2. Conceptual diagram of an addressable field emitter array lithography system. Slight rotation of the DAFEA arrays with respect to the wafer movement allow for redundant coverage of each wafer pixel by multiple writing beamlets.

time-average current of electron-beam projection lithography systems, implying a similar increase in throughput.

III. ELECTRON SOURCES

The selection of the emitter material and geometry for DEAL are related key issues and we therefore examine some of the possible emitter materials. The earliest FEAs employed sharply pointed Spindt tips[6] to provide a greatly enhanced field at the emitter tip, which is important for materials such as tungsten or molybdenum, which require field strengths greater than 1000 V/μm to initiate electron emission at room temperature. This type of structure has the disadvantage of a small effective tip area (i.e., all the emission occurs from the very end of the tip), and a difficult fabrication procedure. Silicon based microtip arrays[7] have also been fabricated for field emission applications, but also require relatively high field strengths. Recent research in flat-panel displays using FEAs has centered on the use of carbon nanotube based emitter material[8,9] because of its high geometric enhancement of the electric field and its mechanical stability.

A cold-cathode material related to the carbon nanotube that has been deterministically grown in vertically aligned arrays is the carbon nanofiber.[10,11] The vertically aligned carbon nanofibers (VACNFs) possess the high geometric field enhancement of the carbon nanotube and small size suitable for massively parallel arrays. This coupled with the ability to deterministically grow the VACNF with a plasma enhanced chemical vapor deposition process on a silicon wafer make it an attractive material to use as the cold-cathode emitters for the DEAL concept.

IV. ELECTRON OPTICS

Electrostatic lenses[12] have been used to focus beams of charged particles for many applications. The purely electrostatic lens is chosen for DEAL instead of a combination of magnetic and electrostatic lens as used in other electron-beam array lithography concepts[13] because of the simplicity and ability to incorporate the entire lens system into the FEA structure as shown in Fig. 1.

A number of different designs are possible for the DAFEA electrostatic focusing grids. A code developed at ORNL for charged-particle beam optics designs[14] is used to compute the electron trajectories in the DAFEA geometry. One such particular computational case is shown in Fig. 3 where the grid stack is 4 μm deep with a 10 nm diam emitter in a 0.9 μm diam opening. This stack would be produced by lithographic methods with the emitter laid down on a pad on top of the logic, memory, and control circuits (LMCs) and the electrostatic focusing stacks overlaid. For this design example the emitted beam is focused to a spot less than 10 nm in diameter (full-width at half maximum) at a working distance of 100 μm from the DAFEA final grid. The depth of focus is on the order of $+/-10$ μm for this design. Critical for the focusing of the beam are the localization of the electron emission from the very tip of the VACNF and well-centered VACNFs in the grid stack.

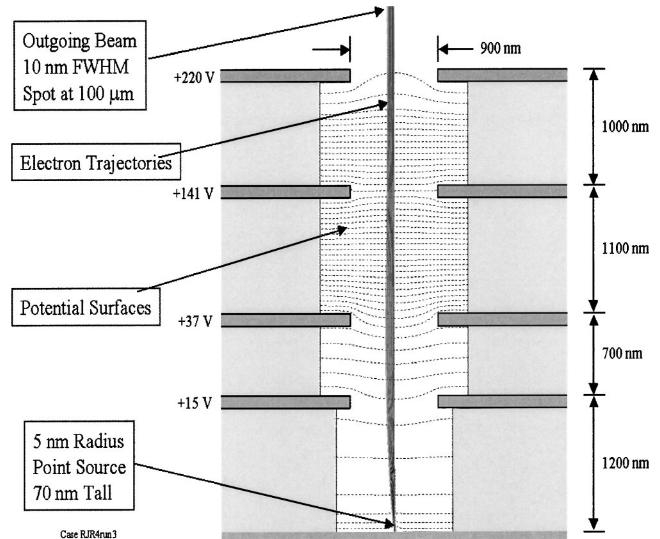

FIG. 3. Computer-generated DAFEA extraction, acceleration, and focusing optics design for a 10 nm diameter VACNF electron source.

Unlike electron-projection lithography systems and other electron-beam systems where there is a crossover of the beam, there is no space-charge limitation[15] since the current density from the DAFEA is so small. Therefore, the nominal 1 nA emitter beams do not undergo space-charge blowup over their 100 μm length. In fact, on average there is only one electron in the beam path at any time for the proposed $\sim$100 μm working distance.

V. LOGIC, MEMORY, AND CONTROL CIRCUIT

The DEAL concept hinges on the DAFEA of Fig. 1, which illustrates a gated emitter array and the LMC circuits. Because of the number of interconnects required and the difficulty in aligning and bonding substrates with micron-scale resolution, a two-part construction technique (i.e., FEA and LMC circuits on separate substrates) is not feasible. Therefore it is necessary to fabricate the FEA on the wafer where the LMC has been implemented using complimentary metal–oxide–semiconductor technology.

The LMC circuit, shown schematically in Fig. 4, consists of logical shift registers that allow a pattern of "on" and "off" pixels to be stored on the DAFEA device. This function in effect replaces the mask of conventional lithography, and such a storage system is a requirement of every maskless technology. Programming the array is accomplished by writing values into the first latch in the array and clocking the values through in a bucket-brigade fashion. If only one data input line is used (complete serial programming), the time t_p to program the array is $t_p = N t_c$, where N is the number of elements in the DAFEA and t_c is the period of the serial write clock. For a 1 cm^2 device with $\sim$32 μm^2 per emitter, there will be $\sim$3 000 000 elements in a DAFEA. A complete serial programming of this device would require about 30 ms if a 100 MHz write clock were used. This programming time can be reduced to less than 1 ms by using multiple data lines (serial/parallel programming).

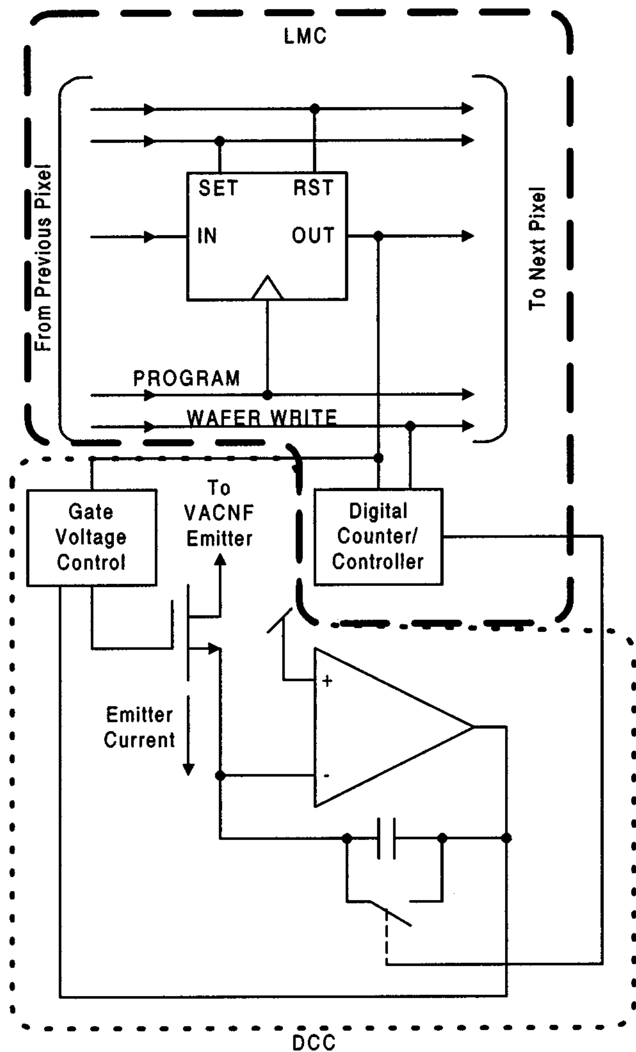

FIG. 4. Schematic of the proposed logic, memory, and control circuit. The dose control circuit is directly connected to each VACNF emitter.

The control part of the LMC circuit consists of a dose-control circuit (DCC) that keeps the dose delivered during each write cycle matched despite emitter-to-emitter mismatching and temperature and aging effects. For a fixed writing time, the dose delivered during each write cycle D_{WC} is given by

$$D_{\mathrm{WC}}=\int_0^{T_{\mathrm{fixed}}} i(t)dt,$$

where $i(t)$ is the emitter current and T_{fixed} is a fixed amount of time during which emission takes place. Close matching of the emission current of all emitters would be required for the dose delivered during each write cycle to be uniform across the array. However, both because threshold voltages of emitters will differ by as much as 15% or more and because field emitters are known to exhibit noise far in excess of shot noise predictions, dose uniformity cannot be provided by emitter matching alone. Therefore, a control circuit that terminates the emission at a fixed dose as opposed to a fixed time is required. The DCC is an integral component of the emitter and is directly connected to it as shown in Fig. 4. The ultimate functionality of VACNF emitters and the DEAL concept cannot be fully exploited without the DCC.

The design of the data-path architecture for the DEAL concept is critical to the development of a high-throughput lithography system. A data transfer rate on the order of 10 Tb/s will be needed to write an entire wafer at the rates envisioned.[16] Thus compression ratios for the data streams will need to be on the order of a factor of 10 for the data transfer rate to be realizable. The specific design will have to examine tradeoffs in compression efficiency and on-chip decoding complexity and circuit complexity, which are limited by space and power dissipation on the DAFEA. The data flow management for the DEAL concept is a key area for future research.

VI. DEVELOPMENT OF DEAL COMPONENTS

Presently, the field emitter array, dose control circuit, electrostatic lens model, and fabrication of emitter-grid structures are under development heading toward a proof-of-lithography demonstration. The proposed VACNF emitters have been shown at ORNL to be robust field emitters well suited to the DEAL application. An isolated emitter has demonstrated continuous operation at 10 nA of current for 175 h (equivalent to over 10 000 h at the proposed 1% duty cycle).[17,18] The fabrication and operation of VACNF emitters in gated devices has been demonstrated for a single gate (diode)[19] and with two gates to form a triode.[20] The fabrication technique for these devices requires the VACNF to be buried in SiO_2 and then uncovered using a reactive ion etch. The etch process does not harm the VACNF and in fact improves the field-emission properties.[18] The recent development of a wafer scale self-aligned process[21] for massively parallel FEA fabrication promises to make the technology attractive for manufacturing.

VII. CONCLUSIONS

The DEAL concept has been shown to lead to a highly parallel lithography system that can pattern semiconductor wafers at high-throughput rates without the use of a mask. The programmability of the DEAL concept makes it an attractive system for patterning complex features at small scales. The challenge is to produce uniform arrays of reliable VACNF emitters that are necessary to make the DEAL concept a reality. Much progress has been made in developing the processes to fabricate the DAFEA and realize a working prototype. A proof-of-lithography demonstration is the next step on the path to the development of DEAL.

ACKNOWLEDGMENTS

This research was partially sponsored by the Defense Advanced Research Projects Agency (DARPA) under Contract No. DARPA-MIPR-97-1357 with Oak Ridge National Laboratory (ORNL), by the Laboratory Directed Research and Development Program of ORNL, and by the Office of Basic Energy Sciences, Division of Materials Sciences, U.S. De-

partment of Energy. The research was carried out at ORNL, managed by UT-Battelle, LLC, for the U.S. Department of Energy under contract No. DE-AC05-00OR22725.

[1]S. D. Berger and J. M. Gibson, Appl. Phys. Lett. **57**, 153 (1990).
[2]G. Stengl *et al.*, J. Vac. Sci. Technol. B **9**, 2824 (1992).
[3]T. H. Newman, R. F. W. Pease, and W. Devore, J. Vac. Sci. Technol. B **1**, 999 (1983).
[4]T. H. P. Chang *et al.*, J. Vac. Sci. Technol. B **10**, 2743 (1992).
[5]T. H. P. Chang, J. Vac. Sci. Technol. **12**, 1271 (1975).
[6]C. A. Spindt, C. E. Holland, and R. D. Stowell, Appl. Surf. Sci. **16**, 268 (1982).
[7]D. Temple *et al.*, J. Vac. Sci. Technol. B **13**, 150 (1995).
[8]A. Hellemans, Science **273**, 1173 (1996).
[9]A. P. Burden, Int. Mater. Rev. **46**, 213 (2001).
[10]Z. F. Ren *et al.*, Science **282**, 1105 (1998).
[11]V. I. Merkulov, D. H. Lowndes, Y. Y. Wei, G. Eres, and E. Voekl, Appl. Phys. Lett. **76**, 3555 (2000).
[12]D. W. O. Heddle, *Electrostatic Lens Systems,* 2nd ed. (Institute of Physics, University of Berkshire, Reading, 2000).
[13]G. X. Guo *et al.*, J. Vac. Sci. Technol. B **19**, 862 (2001).
[14]J. H. Whealton, R. W. McGaffey, and P. S. Meszaros, J. Comput. Phys. **63**, 20 (1986).
[15]L. R. Harriott *et al.*, J. Vac. Sci. Technol. B **13**, 2404 (1995).
[16]V. Dai and A. Zakhor, Proc. SPIE **3997**, 467 (2000).
[17]V. I. Merkulov, D. H. Lowndes, and L. R. Baylor, J. Appl. Phys. **89**, 1933 (2001).
[18]L. R. Baylor *et al.*, J. Appl. Phys. **91**, 4602 (2002).
[19]M. A. Guillorn *et al.*, Appl. Phys. Lett. **79**, 3506 (2001).
[20]M. A. Guillorn *et al.*, J. Vac. Sci. Technol. B (to be published).
[21]M. A. Guillorn, A. V. Melechko, V. I. Merkulov, D. K. Hensley, D. H. Lowndes, and M. L. Simpson, Appl. Phys. Lett. **81**, 3660 (2002).