Digital Implementation of a Line Current Shaping Algorithm for Three Phase High Power Factor Boost Rectifier Without Input Voltage Sensing

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***Abstract*—In this paper the implementation of a simple yet high performance digital current mode controller that achieves high power factor operation for three phase boost rectifier is described. The indicated objective is achieved without input voltage sensing and without transformation of the control variables into rotating reference frame. The controller uses the concept of resistance emulation for shaping of input current like input voltage in digital implementation. Two decoupled fixed frequency current mode controllers calculate the switching instants for equivalent single phase boost rectifiers. A combined switching strategy is developed in the form of space vectors to simultaneously satisfy the timing requirements of both the current mode controllers in a switching period. Conventional phase locked loop (PLL) is not required as converter switching is self-synchronized with the input voltage. Analytical formula is derived to obtain the steady state stability condition of the converter. A linear, low frequency, small signal model of the three phase boost rectifier is developed and verified by measurement of the voltage control transfer function. In implementation Texas Instruments's DSP TMS320F240F is used as the digital controller. The algorithm is tested on a 10-kW, 700-V dc, three phase boost rectifier.**

***Index Terms*—Digital current mode controller, DSP(TMS320F240) based implementation, high power factor operation, input voltage sensorless control, three phase boost rectifier.**

I. Introduction

BOOST CIRCUIT has emerged as the most widely used topology for three phase high power factor rectification. The high power low switching frequency application such as this is more suitable for digital implementation. The control methods proposed for these converters in recent publications [1]–[3] are all implemented in digital hardware. In digital implementation, the controller for various power hardware configurations and parameter values can be standardized and the protection and control functions can be programmed and tuned. The digital controllers can implement very complex and precise control schemes. It is also insensitive to component variations due to temperature changes or aging. Moreover, two basic building blocks of digital hardware, the digital signal processors (DSP) and the analog to digital converters (ADCs), are nowadays available in the same package at affordable cost.

It is shown in [4] that for single-phase full-bridge converter system DSP based controller can implement a pulse-by-pulse current programmed control strategy. In three phase, the control strategy most often employed for Boost rectification controls the active and reactive components of the line current. For this purpose, the sensed currents, after three phase to two phase conversion, need to be transformed from stationary reference frame to the synchronously rotating reference frame [5] of line frequency, so that they appear as dc quantities to the closed loop controller. As a result a phase locked loop (PLL) becomes a necessity, which is not so easy to design, if various nonidealities like frequency variation and distortions in the line voltage waveform as would be present in a real life system, are to be taken into account.

A few power factor correction strategies have been proposed in literature that do not require input voltage sensors. The virtual flux direct power control (VF-DPC) [2] is structurally similar to the well known direct torque control (DTC). The switching frequency of the VF-DPC is not constant and the sampling frequency needs to be much higher than the switching frequency. As a result fast ADCs and microprocessors are required for digital implementation of the scheme. In comparison, the power factor correction method proposed in this paper is based on constant switching frequency and low sampling frequency. It has been implemented using low speed digital hardware such as DSP TMS320F240 (20 MHz-6.6 μs ADC). The other input voltage sensorless method proposed in [3] has the structure of a voltage oriented control (VOC). In comparison, the control structure of the method proposed in this paper is simpler because there are no current error amplifiers and input voltage observers in the control loop. This scheme has eliminated the need for transforming any quantity from stationary reference frame to synchronously rotating reference frame. As a consequence the PLL is not required.

The control objective is defined by this controller as: shape the line current like line voltage. This would ensure high power factor operation of the rectifier. To achieve that first, two decoupled fixed frequency current mode controllers are used to determine the switching states of the converter. Subsequently this information is processed to obtain the switching duty ratios of a three phase full bridge converter.

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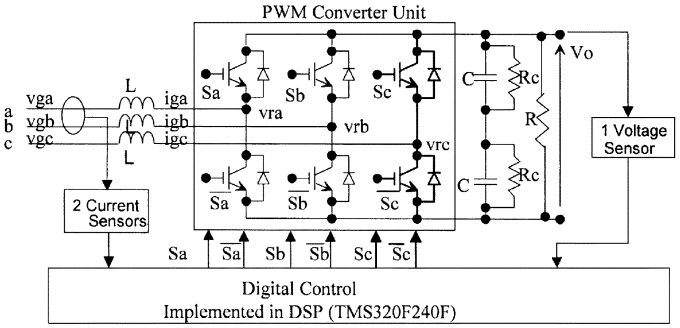

Fig. 1. Power and control schematic of the three phase high power factor boost rectifier with the digital controller implemented in DSP TMS320F240.

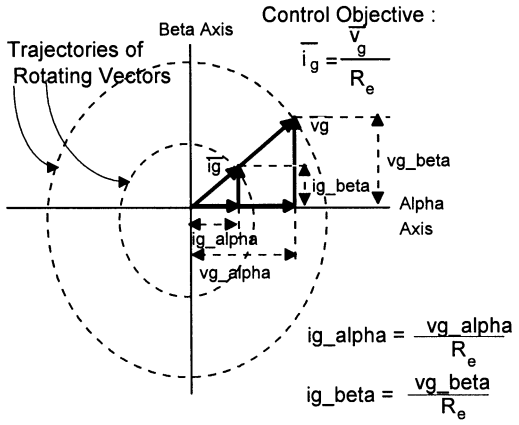

Fig. 2. Control objectives in alpha and beta axes.

II. Controller

We can define the control objective of a three phase high power factor Boost rectifier, shown in Fig. 1, as

$$\overline{i_g} = \frac{\overline{v_g}}{R_e} \tag{1}$$

where R_e is the emulated resistance of the rectifier. The $(\bar{})$ above a variable indicates a space phasor. The mathematical description of the input voltage vector is

$$\overline{v_g} = v_{ga} + v_{gb}e^{j\frac{2\pi}{3}} + v_{gc}e^{\frac{j4\pi}{3}} = v_{g\alpha} + jv_{g\beta}. \tag{2}$$

The current vector needs to be scaled by 2/3 inorder to maintain power balance between input and output

$$\overline{i_g} = \frac{2}{3}\left(i_{ga} + i_{gb}e^{j\frac{2\pi}{3}} + i_{gc}e^{j\frac{4\pi}{3}}\right) = i_{g\alpha} + ji_{g\beta}. \tag{3}$$

If we take components along α and β axes, which are stationary and orthogonal to each other, the control objective can be expressed in terms of two scalar equations

$$i_{g\alpha} = \frac{v_{g\alpha}}{Re} \tag{4}$$

$$i_{g\beta} = \frac{v_{g\beta}}{Re} \tag{5}$$

as shown in Fig. 2.

Equations (4) and (5) can be employed as the control objectives of two single phase Boost converters, one in α axis and the other in β axis. We may consider that the input supply consists of two independent single phase ac sources, $v_{g\alpha}$ and $v_{g\beta}$ and

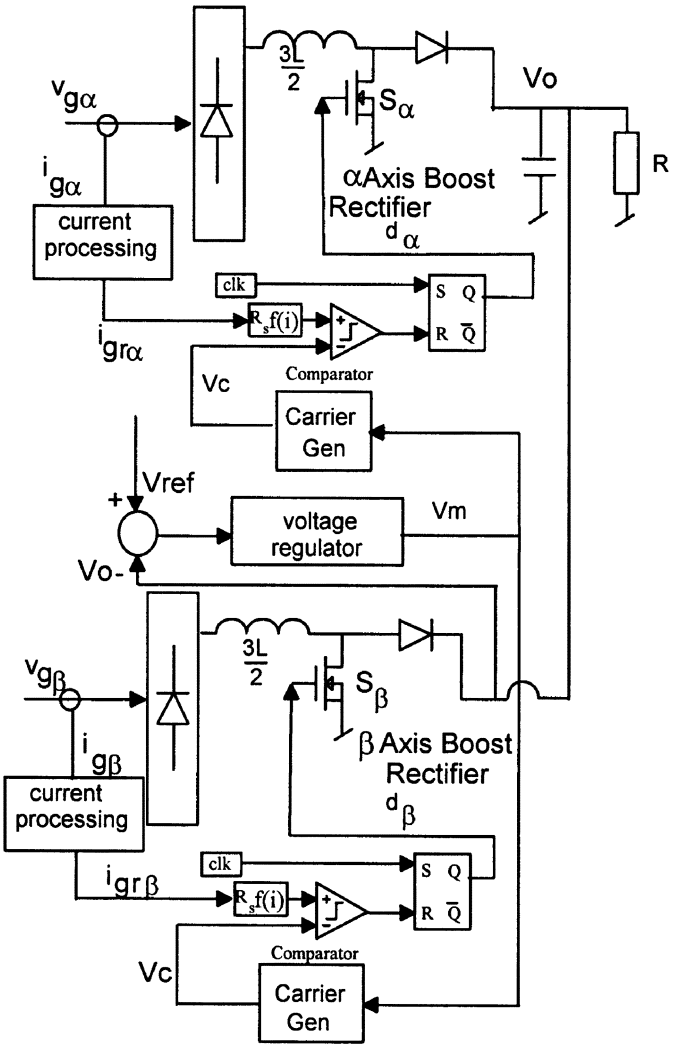

Fig. 3. Functional representation of three phase high power factor boost rectifier with two independent single phase rectifiers in current mode control structure.

the output of the rectifier is V_o, same as the output of the three phase rectifier. The input currents $i_{g\alpha}$ and $i_{g\beta}$ should be made proportional to the respective input voltages $v_{g\alpha}$ and $v_{g\beta}$. From the point of view of the control objective in (α, β) reference frame, the circuit schematics of Fig. 1 and Fig. 3 are equivalent.

Let us assume that the duty ratios d_α and d_β of these two switches Q_α and Q_β can be independently controlled. Therefore we can write the continuous conduction mode input-output conversion equations for the two independent boost rectifiers as

$$v_{gr\alpha} = (1 - d_\alpha)V_o \tag{6}$$

$$v_{gr\beta} = (1 - d_\beta)V_o \tag{7}$$

V_o is the regulated output voltage of the three phase rectifier.

Since d_α and d_β are both positive quantities we need to use dc variables $v_{gr\alpha}$ and $v_{gr\beta}$ in (6) and (7). Similarly $i_{gr\alpha}$ and $i_{gr\beta}$ are dc variables obtained after rectification of $i_{g\alpha}$ and $i_{g\beta}$. By using (6) and (7) the control objective can be reformulated as

$$i_{gr\alpha} = \frac{V_o(1 - d_\alpha)}{Re} \tag{8}$$

$$i_{gr\beta} = \frac{V_o(1 - d_\beta)}{Re}. \tag{9}$$

Conceptually this is equivalent to two current sources charging the same capacitor for voltage output.

The duty ratio of the α and β axis rectifiers may be obtained as

$$d_\alpha = \left(1 - \frac{i_{gr\alpha} Re}{V_o}\right) \tag{10}$$

$$d_\beta = \left(1 - \frac{i_{gr\beta} Re}{V_o}\right). \tag{11}$$

Scaling down the output voltage and the emulator resistance to the control level ($V_o/R_e = V_m/R_s$) we get

$$d_\alpha = \left(1 - \frac{i_{gr\alpha} R_s}{V_m}\right) \tag{12}$$

$$d_\beta = \left(1 - \frac{i_{gr\beta} R_s}{V_m}\right) \tag{13}$$

V_m is the output voltage of the modulator and R_s is the current sense resistance. Under closed loop V_m becomes the output of the outer loop voltage error amplifier. Depending of the samples of the i_{gr} employed, we may identify peak current, average current and end of the period current controls. These functions of current are generalized in Fig. 3 as $f(i)$.

In continuous time domain, $i_{gr\alpha}$ and $i_{gr\beta}$ can be made to represent peak current [6], average current [7], or end of the period current [8] of the inductor in every switching period T_s. The effect of these switching strategies on inductor current is shown in Fig. 4(a)–(c), respectively. However, for simple digital implementation, we would like to select a control strategy that does not require the current to be sampled at a rate higher than the switching frequency. Therefore, unless the sampling instant in a period is varied, as in [9], the control objectives shown in Fig. 4(a) or (b) can not be implemented. In contrast, the switching law shown in Fig. 4(c) is very convenient for digital implementation, because the sampling instant can be kept fixed at the beginning of every switching period. From (12) and (13) we can calculate the duty ratios $d_\alpha[n]$ and $d_\beta[n]$ for the "n" th switching period as

$$d_\alpha[n] = \left(1 - \frac{i_{gr\alpha e}[n-1] R_s}{V_m}\right) \tag{14}$$

$$d_\beta[n] = \left(1 - \frac{i_{gr\beta e}[n-1] R_s}{V_m}\right). \tag{15}$$

The suffix "e" in (14) and (15) indicates that the current is sampled at the end of the switching period. It should be noted that the current at the end of period $[n-1]$ is same as the current at the beginning of period $[n]$. So $i_{gr\alpha}[n] = i_{gr\alpha e}[n-1]$ and $i_{gr\beta}[n] = i_{gr\beta e}[n-1]$. This is shown in Fig. 4(d). The control law can therefore be expressed as

$$d_\alpha[n] = \left(1 - \frac{i_{gr\alpha}[n] R_s}{V_m}\right) \tag{16}$$

$$d_\beta[n] = \left(1 - \frac{i_{gr\beta}[n] R_s}{V_m}\right). \tag{17}$$

Evaluation of $d_\alpha[n]$ and $d_\beta[n]$ for the period "n" is shown in Fig. 5.

In the three phase bridge converter eventually the switch combination (S_a, S_b, S_c) has to be evaluated from the duty ratio variables $d_\alpha[n]$ and $d_\beta[n]$. The conversion of $d_\alpha[n]$ and $d_\beta[n]$ to active vector durations $T_1[n]$ and $T_2[n]$ using space vector approach is taken up next. The space vectors produced by (S_a, S_b, S_c) are shown in Fig. 6. Effectively they produce six active vectors ($\overline{V_1}, \overline{V_2}, \ldots, \overline{V_6}$) of magnitude V_o and a null vector ($\overline{V_o}$, $\overline{V_7}$). The sectors, $(1, 2, \ldots, 6)$, that is the space between two

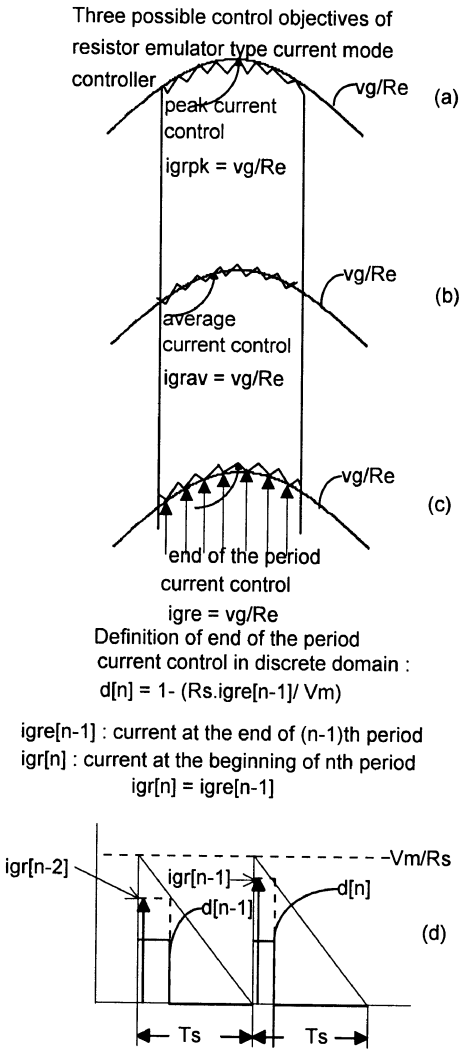

Fig. 4. Resistor emulator digital current mode controller.

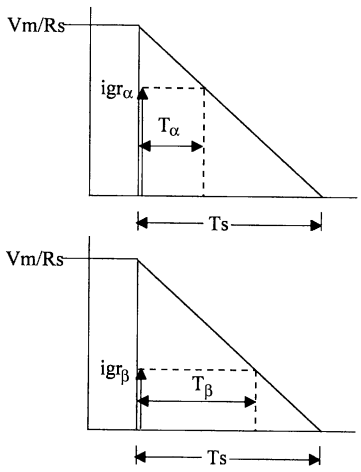

Fig. 5. Evaluation of $d_\alpha[n]$ and $d_\beta[n]$ for the period "n."

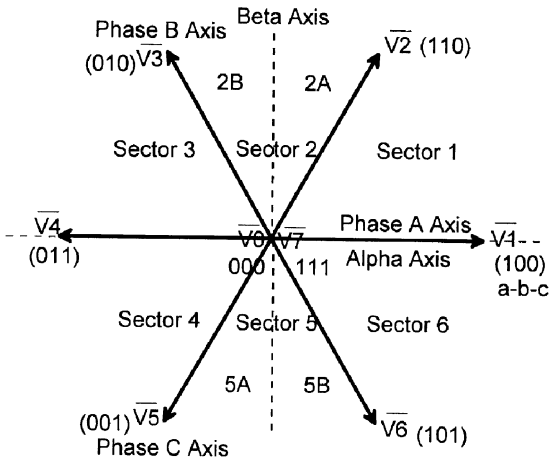

Fig. 6. Voltage vectors produced by PWM converter. The sector definitions are also given.

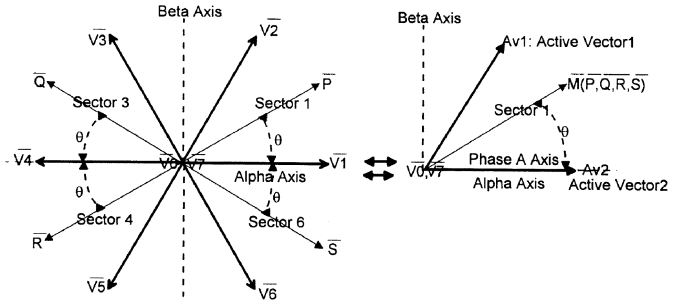

Fig. 7. Mapping of $\overline{P}$, $\overline{Q}$, $\overline{R}$, $\overline{S}$ vectors into $\overline{M}$ in sector 1 of positive alpha-beta axis for solution of T1 and T2; for example: $\overline{A_{v1}} = \overline{V_3}$ *and* $\overline{A_{v2}} = \overline{V_4}$ for vector $\overline{Q}$.

active vectors, are also defined in the same figure. The strategy of relating $(S_a,\ S_b,\ S_c)$ to S_α and S_β uses the fact that the volt–second excitation to the inductors are same at the (α, β) reference frame. In sector 1, the active vectors used for switching are $\overline{V_2}$ for duration T_1 and $\overline{V_1}$ for duration T_2. The volt-second excitation for the (α, β) axis inductors with the active vectors $A_{v1}(= \overline{V_2})$ and $A_{v2}(= \overline{V_1})$ may be equated as

$$\frac{T_1[n]}{2} + T_2[n] = (1 - d_\alpha[n])\, T_s \tag{18}$$

$$\frac{\sqrt{3}}{2} T_1[n] = (1 - d_\beta[n])\, T_s. \tag{19}$$

The switching time transformations valid for sector 1 has to be extended for the sectors 1, 3, 4, and 6 of the (α, β) plane. This is done as follows. Consider the input voltages at $(\overline{P}, \overline{Q}, \overline{R}, \overline{S})$ with an angle θ with respect to the α axis of the segment, as shown in Fig. 7. The same may be located at $\overline{M}$ and $T_1[n]$ and $T_2[n]$ may be obtained. However the active vectors will be different for different sectors. The active vectors A_{v1} and A_{v2} for sectors 1, 3, 4, and 6 are identified as in Table I.

The active vectors employed for input voltage vector in sector 2A are $A_{v1} = \overline{V_2}$, switched for duration T_1 and $A_{v2} = \overline{V_3}$, switched for duration T_2. The volt–second excitation for the

TABLE I
SELECTION OF A_{v1} AND A_{v2} IN SECTOR 1, 3, 4, AND 6

Sector	A_{v1}	A_{v2}
1	$\overline{V_2}$	$\overline{V_1}$
3	$\overline{V_3}$	$\overline{V_4}$
4	$\overline{V_5}$	$\overline{V_4}$
6	$\overline{V_6}$	$\overline{V_1}$

TABLE II
SELECTION OF A_{v1} AND A_{v2} IN SECTOR 2A, 2B, 5A, AND 5B

Sector	A_{v1}	A_{v2}
$2A$	$\overline{V_2}$	$\overline{V_3}$
$2B$	$\overline{V_3}$	$\overline{V_2}$
$5A$	$\overline{V_5}$	$\overline{V_6}$
$5B$	$\overline{V_6}$	$\overline{V_5}$

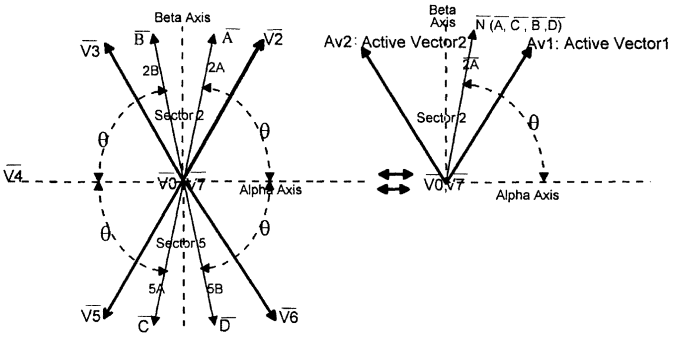

Fig. 8. Mapping of $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$ vectors into $\overline{N}$ in Sector 2A of positive alpha-beta axis for solution of T1 and T2; For example: $\overline{A_{v1}} = \overline{V_2}$ *and* $\overline{A_{v2}} = \overline{V_3}$ for vector $\overline{A}$ whereas $\overline{A_{v1}} = \overline{V_3}$ *and* $\overline{A_{v2}} = \overline{V_2}$ for vector $\overline{B}$ mode controller.

(α, β) axis inductors with the active vectors $A_{v1}(= \overline{V_2})$ and $A_{v2}(= \overline{V_3})$ may be equated as

$$\frac{1}{2} T_1[n] - \frac{1}{2} T_2[n] = (1 - d_\alpha[n])\, T_s \tag{20}$$

$$\frac{\sqrt{3}}{2} T_1[n] + \frac{\sqrt{3}}{2} T_2[n] = (1 - d_\beta[n])\, T_s. \tag{21}$$

Similarly for sectors $2A$, $2B$, $5A$, and $5B$, Table II gives the selection of vectors. Any vector $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$ in those sectors can be mapped as $\overline{N}$ in the positive-positive quadrant, as shown in Fig. 8, for the solution of $T_1[n]$ and $T_2[n]$. The remaining time of the period $(T_0[n] = T_s - T_1[n] - T_2[n])$ should be utilized by the null vector.

The current processing function of the modulator is as follows. First, the two phase currents $i_{ga}[n]$ and $i_{gb}[n]$ are sensed and converted to $i_{g\alpha}[n]$ and $i_{g\beta}[n]$ by standard three phase to two phase transformation

$$i_{g\alpha}[n] = i_{ga}[n] \tag{22}$$

$$i_{g\beta}[n] = \frac{1}{\sqrt{3}} \left(2 i_{gb}[n] + i_{ga}[n]\right). \tag{23}$$

TABLE III
GENERATION OF RECTIFIED CURRENT VARIABLES $i_{gr\alpha}[n]$ AND $i_{gr\beta}[n]$

Sector	$i_{gr\alpha}[n]$	$i_{gr\beta}[n]$
1	$i_{ga}[n]$	$i_{g\beta}[n]$
2*A*	$i_{ga}[n]$	$i_{g\beta}[n]$
2*B*	$-i_{ga}[n]$	$i_{g\beta}[n]$
3	$-i_{ga}[n]$	$i_{g\beta}[n]$
4	$-i_{ga}[n]$	$-i_{g\beta}[n]$
5*A*	$-i_{ga}[n]$	$-i_{g\beta}[n]$
5*B*	$i_{ga}[n]$	$-i_{g\beta}[n]$
6	$i_{ga}[n]$	$-i_{g\beta}[n]$

However the modulators work on dc quantities, so based on the sector information, we generate the rectified current variables $i_{gr\alpha}[n]$ and $i_{gr\beta}[n]$ from Table III, and use them in (16) and (17) for calculation of duty ratios.

It can be seen that input voltage need not be sensed for computation of $T_1[n]$ and $T_2[n]$. However the sector information should be known for appropriate selection of active vectors (Table I and Table II), and also for rectification of input current (Table III). This controller implements self-synchronization of the converter switching with respect to line voltage based on the following logic: as long as the sector selection is correct, the α and β axis modulators will produce duty ratios less than 1, i.e., $d_\alpha[n] < 1$ *or* $d_\beta[n] < 1$. Further $T_2[n] > 0$ also has to be true for the modulator to operate in the correct sector. When any one of these conditions are violated, the next sector in sequence is chosen, as shown in Fig. 9. This sector change can take place in the same switching cycle in which invalid duty ratio solutions were obtained because of initial incorrect selection of sectors. The change will continue in sequence until valid solutions are obtained. The modulator will produce appropriate switching signals only after latching to the correct sector.

III. SIMULATION

The proposed controller is simulated on MATLAB-SIMULINK (version 5.3) software platform. The nominal rating of the three phase Boost rectifier is chosen to be 10 Kw, 415 Vac, 700 Vdc. The inductance/phase in simulation is 6 mH/phase and the switching frequency of the converter is 10 KHz. The block diagram of the overall system as well as the subsystems are shown in Fig. 10. The power circuit of the three phase Boost rectifier has been modeled in its ideal form as a system with six inputs and four outputs. The inputs are three line voltages and three basic ON/OFF switching signals. The outputs are three line currents and the rectified dc voltage. The relationship between input-output variables can be expressed by a set of differential and algebraic equations. These equations are given in Appendix I with reference to the circuit schematic of Fig. 1 and are used in simulating the power circuit. The digital controller has three inputs: two phase currents and the rectified dc voltage. The inputs are sampled at the rate of 10 KHz. Three ON/OFF signal for the switches are obtained

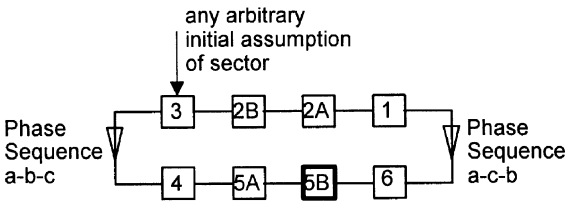

Fig. 9. Sequence of sector change to be followed to eventually synchronize with the location of voltage vector: for example if the voltage vector is in sector 5B and the initial assumption of sector is 3 then 3, 4 and 5A will not produce acceptable solution but the modulator will lock at sector 5B (A-B-C).

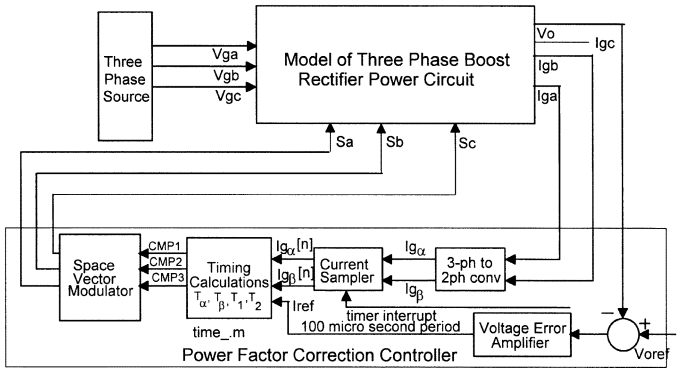

Fig. 10. Block diagram of the power factor correction controller in simulation (SIMULINK).

as outputs from the controller. The digital current mode controllers for α and β axes and the subsequent space vector implementation of a combined switching strategy have been simulated using the equations derived in the previous section. The time calculations based on (18)to (21) are performed by a MATLAB program named "time_.m." The simulation results of Fig. 11 show waveforms of v_{ga}, i_{ga}, and v_0 at quarter, half, and full loads.

IV. STEADY STATE STABILITY

The current mode control may exhibit steady state stability problem under certain operating conditions because of the presence of a local feedback in its control structure [10]. In this section we derive the steady state stability limit of the digitally controlled three phase boost rectifier described in Section II by analysis of an equivalent single phase boost rectifier. The analysis is graphical in nature and is basically the same as has been used for a current programmed dc-dc converter in [10]. It has been assumed in the derivation that, under quasi steady state condition, the inductor current at the end of a switching period is same as the current at the beginning of that period. This assumption is valid because the switching frequency of the converter is much higher than the line frequency.

Let i_g be the current in the inductor at the beginning of the switching period T_s, as shown in Fig. 12. If there is a perturbation Δi_{g1} in i_g due to some reason, then it would change duty ratio of that period. Therefore at the end of the same switching period the current will not come back to its steady state value i_g. In general we can say that at the end of the switching period T_s the perturbation would propagate by an amount Δi_{g2}. For

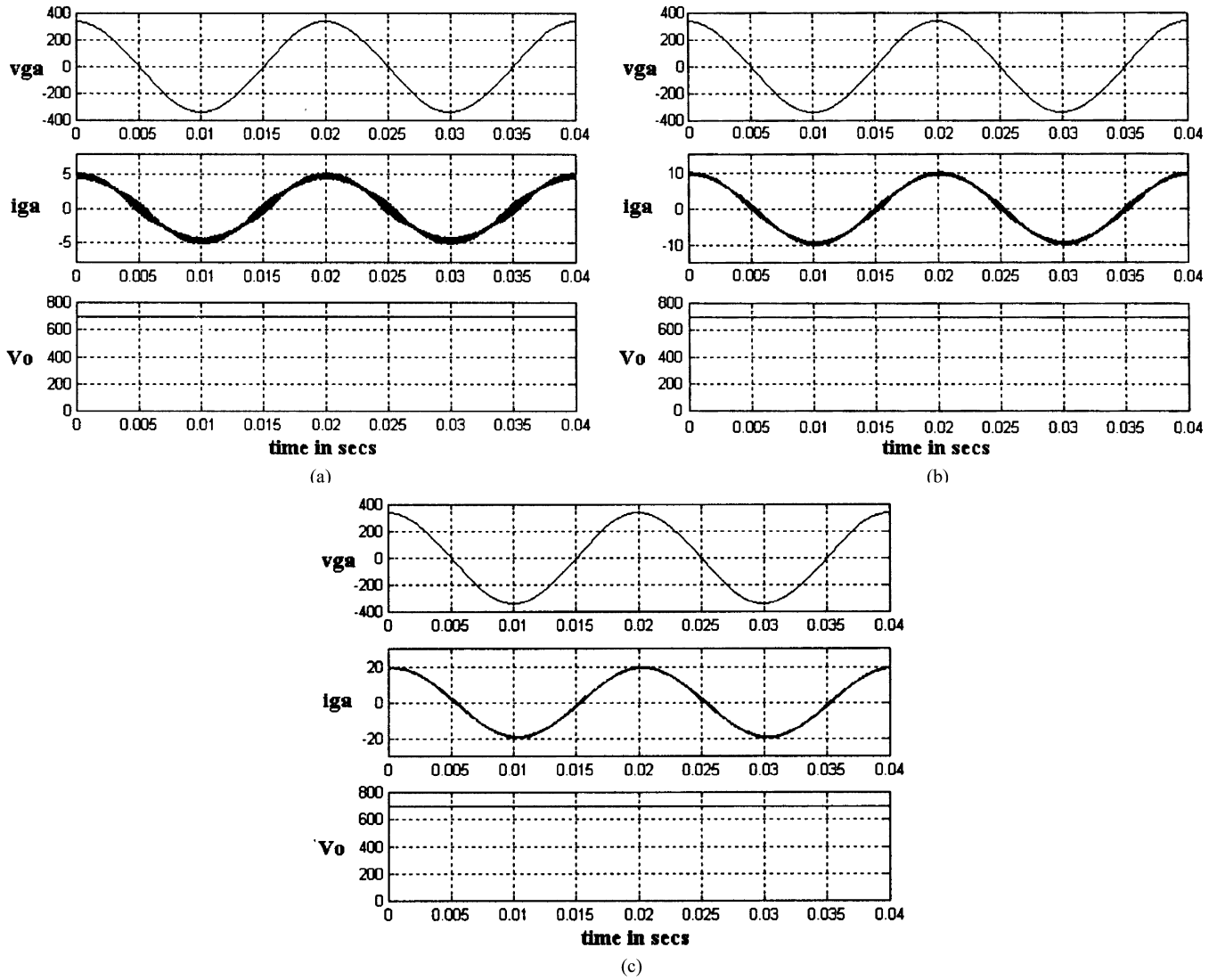

Fig. 11. Simulation results of the three phase boost rectifier at different loads: (a) input phase voltage (v_{ga}), input phase current (i_{ga}) and output voltage (V_o) at $R = 200\ \Omega$, (b) input phase voltage (v_{ga}), input phase current (i_{ga}) and output voltage (V_o) at $R = 100\ \Omega$, and (c) input phase voltage (v_{ga}), input phase current (i_{ga}) and output voltage (V_o) at $R = 50\ \Omega$.

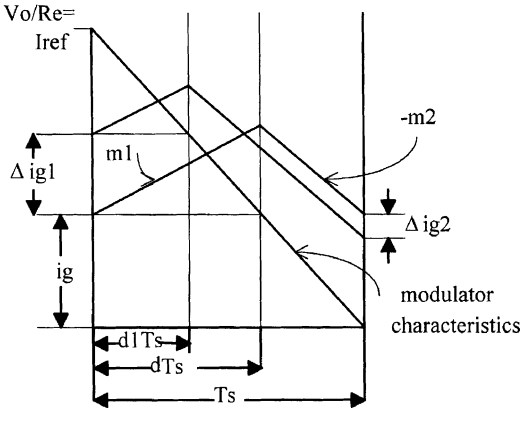

Fig. 12. Derivation of the steady state stability condition for the discrete implementation of resistor emulator type current mode controller.

steady state stability condition to be fulfilled the magnitude of Δi_{g2} should be less than the magnitude of Δi_{g1}.

The steady state condition for the inductor current is given by

$$m_1 d = m_2(1-d) \tag{24}$$

where m_1 is the ON state slope, m_2 is the OFF state slope, in a switching period T_s and d is the steady state duty ratio as shown in Fig. 12. The duty ratio of the period under perturbed condition is d_1

$$m_1 = \frac{2v_g}{3L} \tag{25}$$

$$m_2 = \frac{2(V_o - v_g)}{3L} \tag{26}$$

$$d_1 = d - \frac{\Delta i_{g1}}{I_{ref}} = d - \frac{\Delta i_{g1} Re}{V_o}. \tag{27}$$

If Δi_{g2} is the deviation in current at the end of the period, then it can be expressed as

$$\begin{aligned}\Delta i_{g2} &= \Delta i_{g1} + m_1 d_1 T_s - m_2(1-d_1)T_s \\ &= \Delta i_{g1} - (m_1 + m_2)\frac{\Delta i_{g1}}{I_{ref}} Ts.\end{aligned} \tag{28}$$

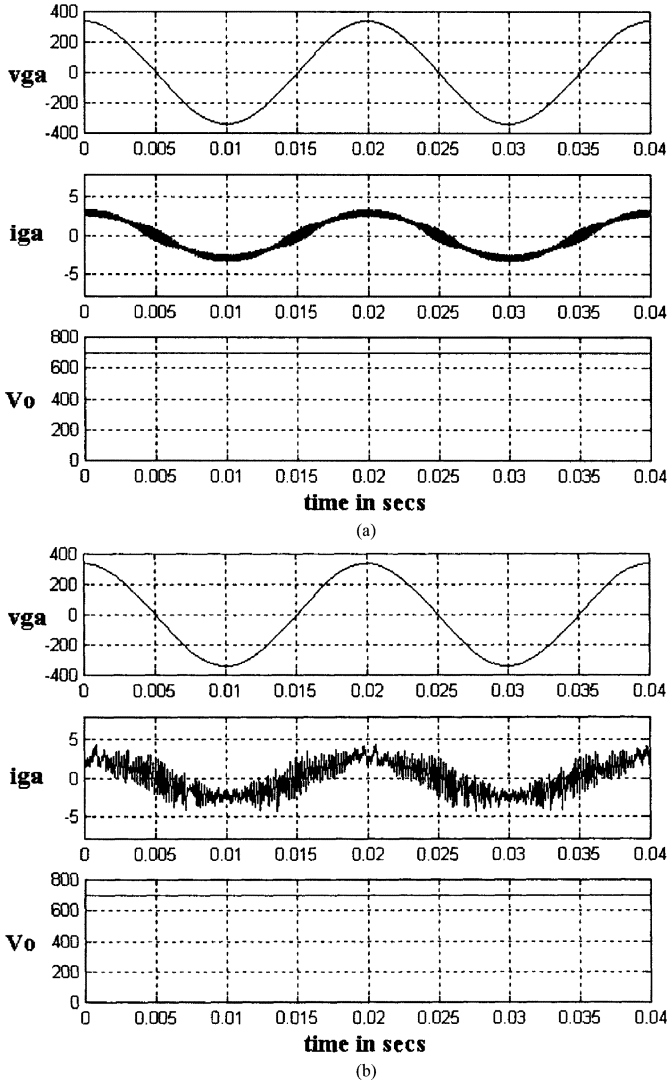

Fig. 13. Simulation results of the converter verifying the steady state stability analysis (a) input phase voltage (v_{ga}), input phase current (i_{ga}) and output voltage (V_o) at $R = 325\ \Omega$ (b) input phase voltage (v_{ga}), input phase current (i_{ga}) and output voltage (V_o) at $R = 375\ \Omega$. The analysis predicts steady state stability limit at $R = 340\ \Omega$ for $L = 6$ mH, $T_s = 100\ \mu$S, $M_g = .726$.

Let us define M_g as the ratio of the peak input voltage to the output voltage

$$M_g = \frac{V_{gm}}{V_o}; \quad where\, V_{gm} = v_{g\alpha}(\max) = v_{g\beta}(\max) \quad (29)$$

and the relationship between R_e and R is obtained from the power balance condition

$$2\left(\frac{V_{gm}^2}{2Re}\right) = \frac{V_o^2}{R}; \quad or, \quad Re = M_g^2 R. \quad (30)$$

R is the load resistance of the boost rectifier. The load resistance of the equivalent single phase rectifier is $2R$ since both the α axis and β axis rectifiers charge the output capacitor in parallel. Similarly from voltage ($v_{ga} = 1.5v_{ga}$) and power balance ($i_{ga} = i_{ga}$) conditions we get $(3/2)L$ as the inductance of the equivalent single phase rectifier, where L is the per phase inductance of the three phase system.

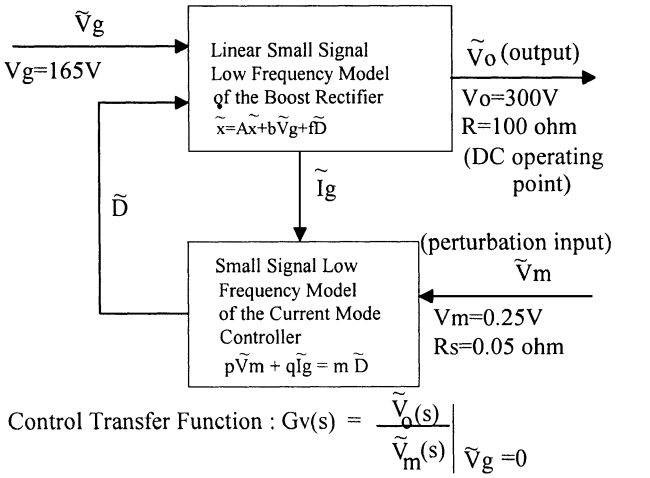

Fig. 14. Voltage control transfer function $G_v(s)$ for linear, low frequency, small signal model of the three phase boost rectifier.

Using (25), (26), and (30), the ratio between Δi_{g2} and Δi_{g1} can be obtained from (28) as

$$\frac{\Delta i_{g2}}{\Delta i_{g1}} = 1 - \frac{2M_g^2 RT_s}{3L}. \quad (31)$$

If $(2M_g^2 RT_s/3L) > 2$ then $|\Delta i_{g2}/\Delta i_{g1}| > 1$ and in subsequent cycles the deviation in current from steady state value i_g will not diminish. Therefore steady state stability is ensured if (32) is satisfied

$$R < \frac{3L}{M_g^2 T_s}. \quad (32)$$

The analysis predicts steady state stability limit $R = 340\ \Omega$ for $L = 6$ mH, $T_s = 100\ \mu$S, $M_g = 0.726$. The simulation results of Fig. 13(a) and (b) are presented for $R = 325\ \Omega$ and $R = 375\ \Omega$, respectively. It can be seen that the input current is steady state stable for $R = 325\ \Omega$ but not so for $R = 375\ \Omega$.

V. Small Signal Low Frequency Model

The objective of this section is to develop a low frequency, small signal, linear model of the three phase high power factor boost rectifier switched by the digital controller described in Section II. In [11], linearized, small signal model of a three phase boost rectifier has been derived in d-q reference frame by transforming all the states into rotating reference frame of line frequency, so that the states appear as dc quantities under steady state. In contrast the small signal model developed here is based on the current mode control structure in the stationary reference frame of (α, β) coordinates. With the assumption of low modulating frequency and selection of an appropriate nominal operating point, the number of state variables of the converter has been reduced in this model compared to d-q axis model.

The final objective is to find out the voltage control transfer function $G_v(s) = \widetilde{V_o}(s)/\widetilde{V_m}(s)$ of the boost rectifier. $G_v(s)$ is necessary for the design of the voltage error amplifier. The variables used in this analysis are denoted by capital letters (nominal as well as dc) and small signal deviation by $\sim$ on the top of the symbol. It can be seen from Fig. 14 that the external small signal

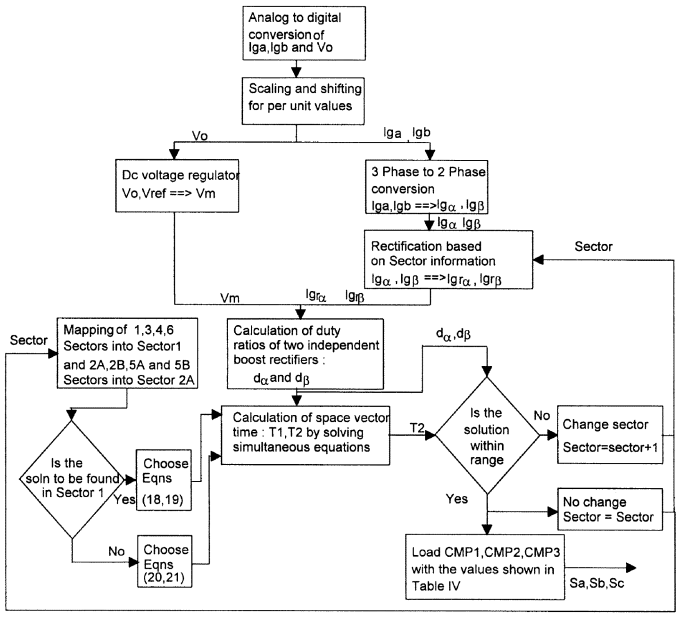

Fig. 15. Flow chart of the control algorithm implemented in TMS320F240 DSP for resistor emulator type line current shaping controller.

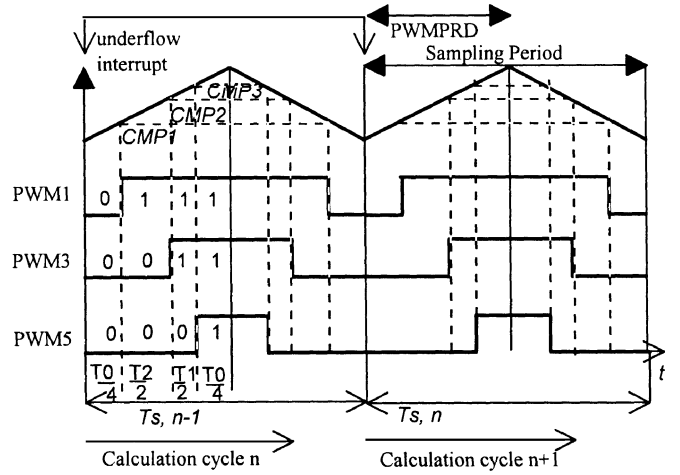

Fig. 16. Generation of symmetrical PWM signals using Full Compare Unit of the TMS320F240 DSP Controller.

TABLE IV
COMPARE REGISTER VALUES FOR SYMMETRIC PWM GENERATION

Sector	*CMP*1	*CMP*2	*CMP*3
1	$T_x = (T_s - T_1 - T_2)/2$	$T_x + T_2$	$T_x + T + T$
2*A*	$T_x + T_2$	$T_x = (T_s - T_1 - T_2)/2$	$T_x + T_2 + T_1$
2*B*	$T_x + T_1$	$T_x = (T_s - T_1 - T_2)/2$	$T_x + T_2 + T_1$
3	$T_x + T_2 + T_1$	$T_x = (T_s - T_1 - T_2)/2$	$T_x + T_1$
4	$T_x + T_2 + T_1$	$T_x + T_1$	$T_x = (T_s - T_1 - T_2)/2$
5*A*	$T_x + T_1$	$T_x + T_2 + T_1$	$T_x = (T_s - T_1 - T_2)/2$
5*B*	$T_x + T_2$	$T_x + T_2 + T_1$	$T_x = (T_s - T_1 - T_2)/2$
6	$T_x = (T_s - T_1 - T_2)/2$	$T_x + T_2 + T_1$	$T_x + T_2$

input to the modulator is $\widetilde{V_m}$ and the output is the duty ratio variation $\widetilde{D}$. $\widetilde{I_g}$ also acts as small signal input to the modulator since the current mode control has inner closed loop in its structure. The small signal model of the three phase boost rectifier is

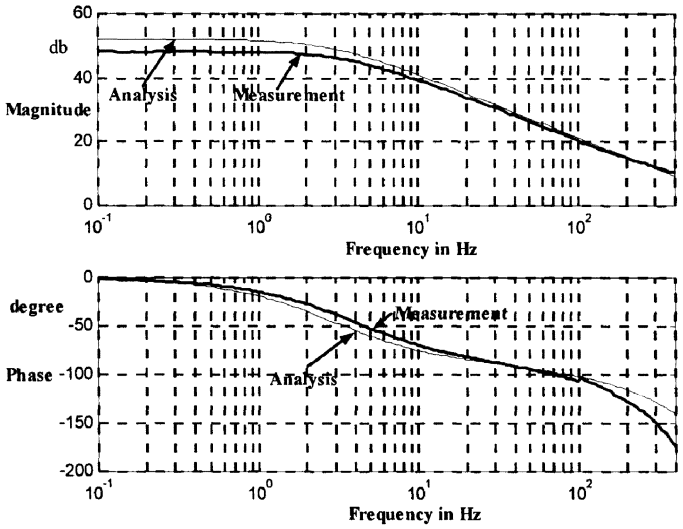

Fig. 17. Frequency response plot of voltage control transfer function $G_v(s) = \widetilde{V_o}(s)/\widetilde{V_m}(s)$; $V_{ga}(phase) = 110\ \mathrm{V(rms)}$, $V_o = 300\ \mathrm{V}$, $V_m = 0.25\ \mathrm{V}$ $L = 7.5\ \mathrm{mH/phase}$, $R = 100\ \Omega$, $C = 1650\ \mu\mathrm{F}$, $R_s = 0.05\ \Omega$.

derived from the equivalent functional representation of Fig. 3. The inductor currents of the α and β axis converters charge the same capacitor. So we can write

$$\frac{3}{2}L\frac{dI_{gr\alpha}}{dt} = V_{gr\alpha} - (1 - D_\alpha)V_o \tag{33}$$

$$\frac{3}{2}L\frac{dI_{gr\beta}}{dt} = V_{gr\beta} - (1 - D_\beta)V_o \tag{34}$$

$$C\frac{dV_o}{dt} = (1 - D_\alpha)I_{gra} + (1 - D_\beta)I_{gr\beta} - \frac{V_o}{R}. \tag{35}$$

We assume that the input voltages are sinusoidal and balanced. Then the power input to the three phase boost rectifier is same at any instant of the line cycle and equal to the output power. We therefore can choose any instant as the nominal operating point before perturbing the variables by small amount compared to the nominal value for the development of the small signal model of the converter. However, it is convenient to choose $V_{gr\alpha} = V_{gr\beta} = 1.5V_{ga\,\max}\sin(45°) = V_g$ as the nominal operating point representing one fourth of the entire line cycle. Then, the input currents being proportional to input voltages, are given by $I_{gr\alpha} = I_{gr\beta} = I_{ga\,\max}\sin(45°) = I_g$. From (8) and (9) we get $D_\alpha = D_\beta = D$. The small signal linear model of the converter is therefore given by

$$\frac{3}{2}L\frac{d\widetilde{I_g}}{dt} = \widetilde{V_g} - (1 - D)\widetilde{V_o} + V_o\widetilde{D} \tag{36}$$

$$C\frac{d\widetilde{V_o}}{dt} = 2(1 - D)\widetilde{I_g} - 2I_g\widetilde{D} - \frac{\widetilde{V_o}}{R}. \tag{37}$$

The steady state values are

$$V_o = \frac{V_g}{(1 - D)} \tag{38}$$

$$I_g = \frac{V_g}{(1 - D)^2 2R}. \tag{39}$$

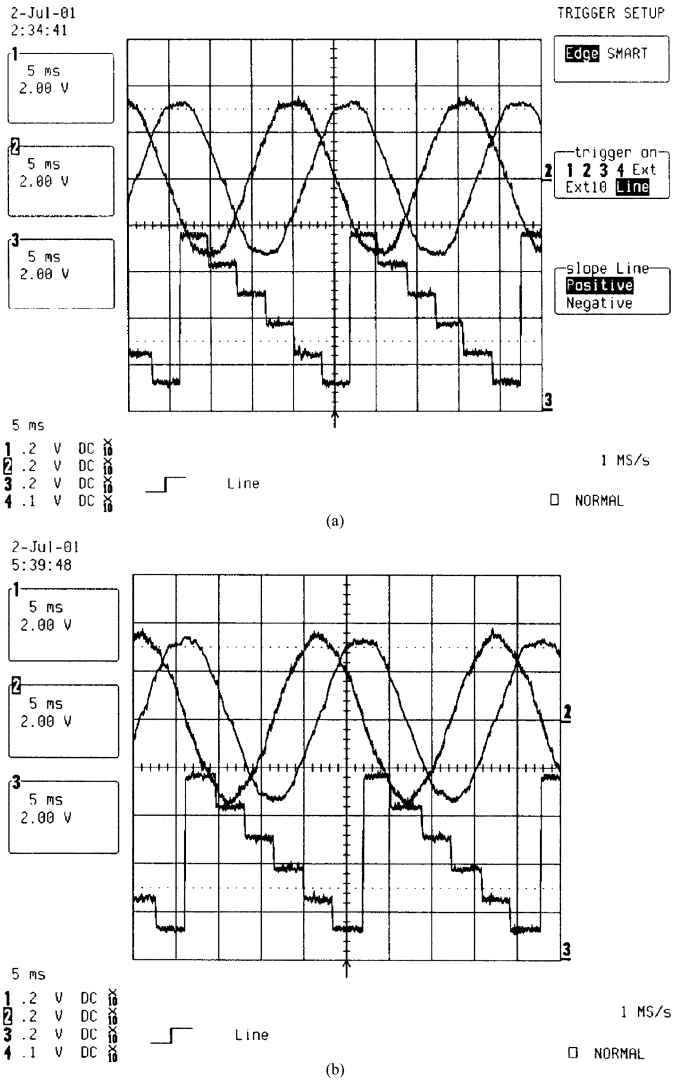

Fig. 18. Experimental results at $V_{ab} = 415$ V *and* $V_o = 700$ V (a) i_{ga} (ch1), i_{gb} (ch2) and sector—1 to 6 (ch3) and (b) $i_{g\alpha}$ (ch1), $i_{g\beta}$ (ch2) and sector (ch3). Current scale: 12.5 A/div. Sector scale: each sector is equivalent to 0.625 division.

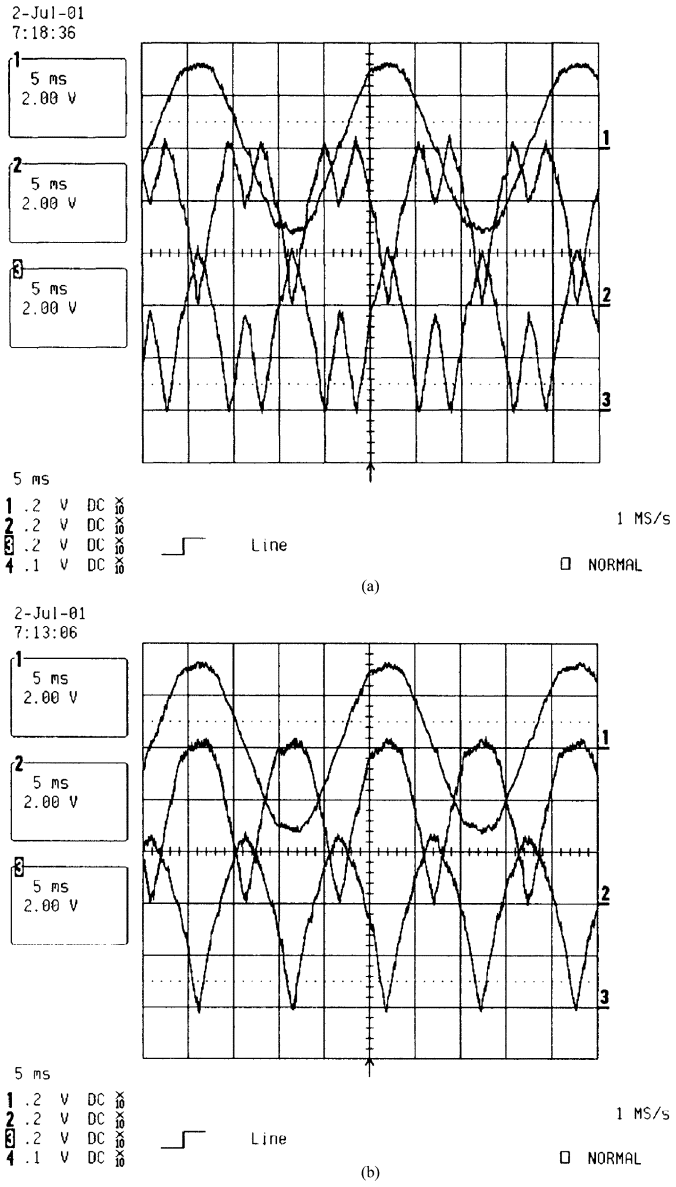

Fig. 19. Experimental results at $V_{ab} = 415$ V *and* $V_o = 700$ V (a) i_{ga} (ch1), T_1 (ch2) and T_2 (ch3) and (b) i_{ga} (ch1), T_{α_off} (ch2) and T_{β_off} (ch3). Current scale: 12.5 A/div. Time scale: 24 μs/div.

The dc and small signal linear model of the modulator are given by

$$D = 1 - \frac{I_g R_s}{V_m} = 1 - \frac{V_g R_s}{(1-D)^2 2RV_m} \tag{40}$$

$$\widetilde{D} = \frac{(1-D)}{V_m}\widetilde{V_m} - \frac{R_s \widetilde{I_g}}{V_m}. \tag{41}$$

The steady state outputs D and V_0 as function of steady state inputs V_g and V_m are given by

$$D = 1 - \left(\frac{V_g R_s}{V_m 2R}\right)^{\frac{1}{3}} \tag{42}$$

$$V_o = V_g^{\frac{2}{3}} \left(\frac{V_m 2R}{R_s}\right)^{\frac{1}{3}}. \tag{43}$$

In digital implementation of the modulator the current is sensed at the beginning of the switching cycle. So in a very strict sense the sensed current I_{ge} is not exactly equal to the average current I_g of that period. However in order to keep the derivation simple we have ignored the effect of ripple on the inductor current and used the approximation $I_g \approx I_{ge}$. Now we can follow the same procedure as described in [12] to replace $\widetilde{D}$ by the RHS of (41) and subsequently by eliminating $\widetilde{I_g}$ by $\widetilde{V_m}$ and $\widetilde{V_o}$ we can determine the voltage control transfer function as

$$\frac{\widetilde{V_o}(s)}{\widetilde{V_m}(s)} = \frac{\frac{1}{3}\left[\left(\frac{V_g}{V_m}\right)^2 \left(\frac{2R}{R_s}\right)\right]^{\frac{1}{3}} \left[1 - \left(\frac{V_m 2R}{V_g R_s}\right)^{\frac{2}{3}} \left(\frac{3L}{4R}\right) s\right]}{\left[1 + s\left(\frac{L}{4R}\left(\frac{V_m 2R}{V_g R_s}\right)^{\frac{2}{3}} + \frac{RC}{3}\right) + s^2 \frac{LC}{4}\left(\frac{V_m 2R}{V_g R_s}\right)^{\frac{2}{3}}\right]}. \tag{44}$$

VI. Digital Implementation in TMS320F240

The control algorithm is implemented in Texas Instruments DSP TMS320F240. The current mode control calculations for the two axes are performed in software each time the control

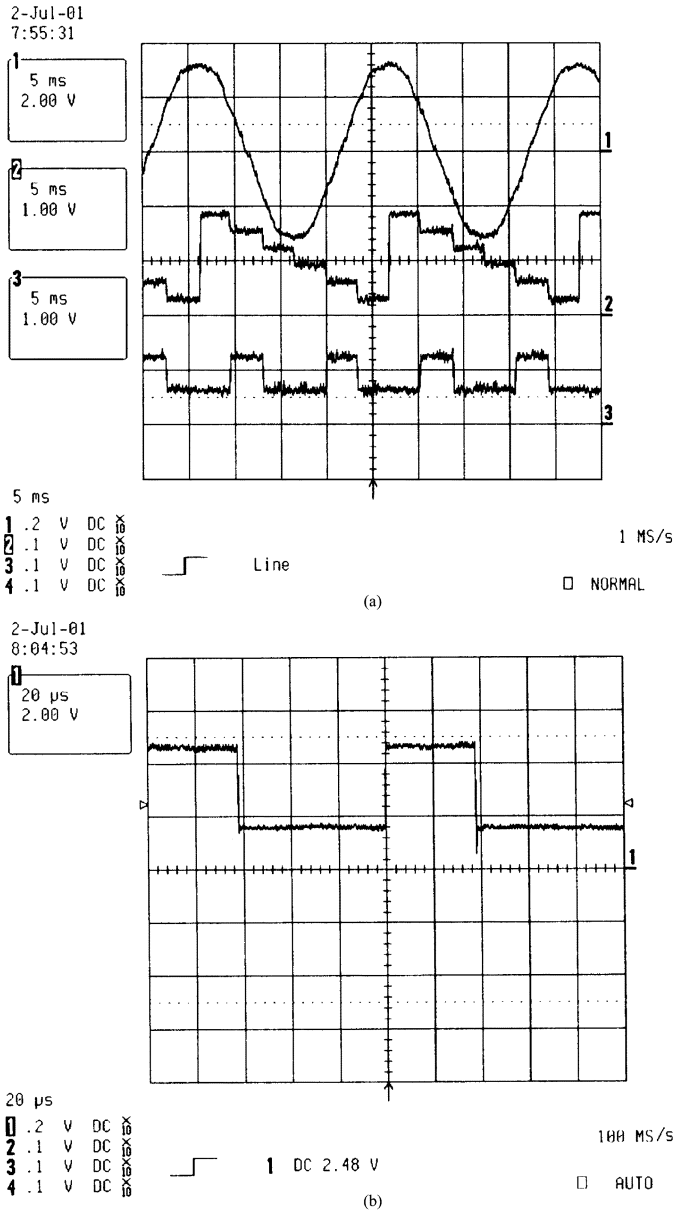

Fig. 20. Experimental results at $V_{ab} = 415\,\mathrm{V}$ *and* $V_o = 700\,\mathrm{V}$ (a) i_{ga} (ch1), sector (ch2) and a signal (ch3) showing the mapping all sectors into sector 1 (low) and sector 2A (high) Current Scale: 12.5 A/div and (b) Control loop time shown as signal high duration (ch1).

loop is executed. The flowchart of the controller is shown in Fig. 15.

The Event Manager module in the peripheral library of TMS320F240 provides necessary hardware support for the generation of PWM pulses for the switching devices of the three phase Boost rectifier. The general purpose (GP) timer 1 [13] of the Event Manager Module is configured in the initialization part of the program to work in continuous up-down counting mode for the generation of symmetric waveform as shown in Fig. 16. The timer 1 is clocked by CPU clock CPUCLK at 20 MHz. The timer 1 period register T1PR is loaded with a constant $\mathrm{PWMPRD} = 1000$, corresponding to 50 μs. In the up-down counting mode it generates a triangle waveform of frequency 10 KHz. The execution of the control loop is initiated by the GP timer1 underflow interrupt, i.e., when the timer counter reaches 0000H, that has a period of 100 μs. In each underflow interrupt the dual 10-b analog to digital converter module (ADC) of the TMS320F240 measures two phase currents and the dc output voltage. The current conversions are simultaneous in the two ADCs followed by dc output voltage conversion thus requiring a total conversion time of 13.2 $\mu(= 6.6\ \mu * 2)$ s. The current mode controllers receive as input the output of the dc voltage regulator. The duration for which each switch of the three phase converter is to be turned ON is computed from the timing results of the two current mode controllers. These values are loaded to the Full Compare Units of the Event Manager Module. The Full Compare Unit [13] has three 16-b compare registers CMPR1, CMPR2 and CMPR3 to control the individual duty cycle of the switches as shown in Fig. 16. The values that need to be loaded to these registers to generate symmetrical PWM pulses are given in Table IV. Necessary adjustments to the basic ON and OFF times of each switch are performed in the Dead Band units. The switch dead time is controlled by dead time control register DBTCON. The output PWM pulses are obtained by comparison of values in timer 1 counter register T1CNT and compare registers CMPR1-2-3. The Output Logic Units of the Event Manager Module determine the logic level, i.e., active high or active low, of each PWM output. The six output signals are available on dedicated PWM output pins PWM1 to PWM6. If odd numbered pin is used for driving top device then the corresponding even numbered pin should be used for the bottom device. The execution time of the control algorithm is less than 40 μs.

VII. Experimental Results

The control algorithm is tested for experimental verification on a 10 KW three phase boost rectifier unit. The ac-line input is 415 V (line-to-line) $\pm 15\%$, and the regulated dc output is 700 V. The measured value of the line inductance is 7.5 mH/phase. Switching frequency of the IGBT based (IPM Module) converter is chosen to be 10 KHz. The value of the boost inductance could be less if we could use higher switching frequency. However, the high power converters are generally switched at frequencies around 10 KHz, as in [2], so as to utilize the converter for maximum possible power output. Moreover, in order to operate the converter at a substantially higher frequency than 10 KHz a DSP with higher CPU speed and lower ADC conversion time than TMS320F240 should be used. Otherwise the ADC conversion time, that is 6.6 μS for each conversion in TMS320F240, becomes substantial compared to the loop time of the control algorithm. It may also be noted that an input voltage sensorless algorithm is less demanding on digital hardware as fewer numbers of analog to digital conversions are required. The computational burden on the controller is less as well because the design of phase lock loop (PLL) circuit is not required in this method.

The line currents i_{ga} and i_{gb} are sensed by "*LEM*" made Hall effect current sensors of model *LA*50. It has a turns ratio of 1:1000. For each current sensor the primary has two turns and the output of the current sensor has been terminated by a 100 Ω resistance. The output voltage V_o is isolated by high

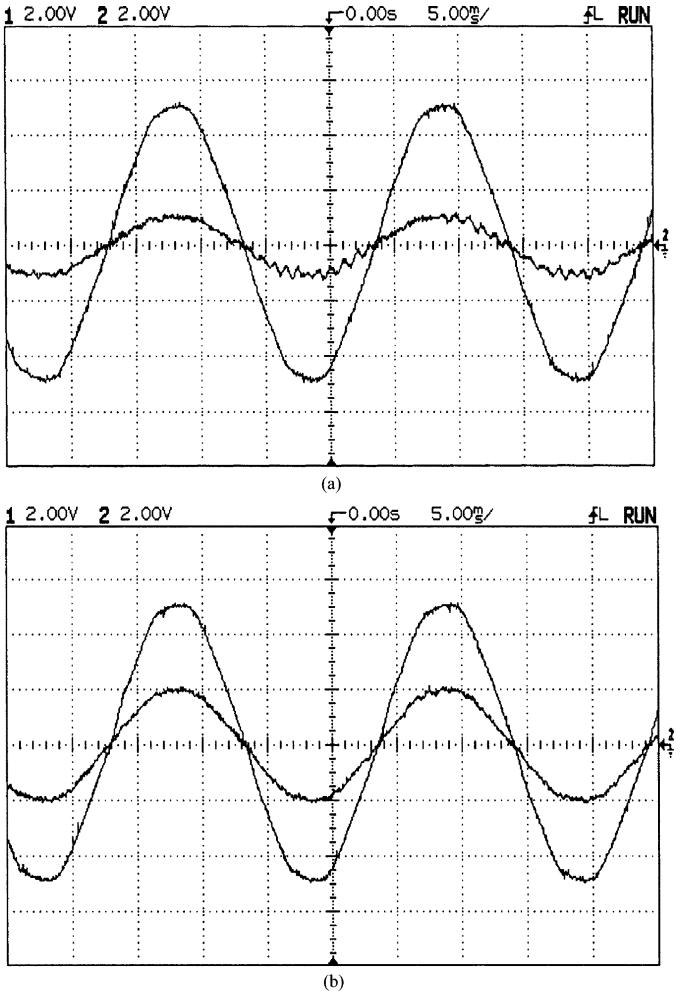

Fig. 21. Experimental results: v_{ga} and i_{ga} at $V_{ab} = 415$ V *and* $V_o = 700$ V (a) 2.8 kW (b) 5 kW Total harmonic Distortion (a) 5.6% (b) 2.9% Voltage Scale: 133.5 V/div Current Scale: 10.4 A/div Inductance/Phase: 7.5 mH Power Factor: (a) 0.999 and (b) 0.999.

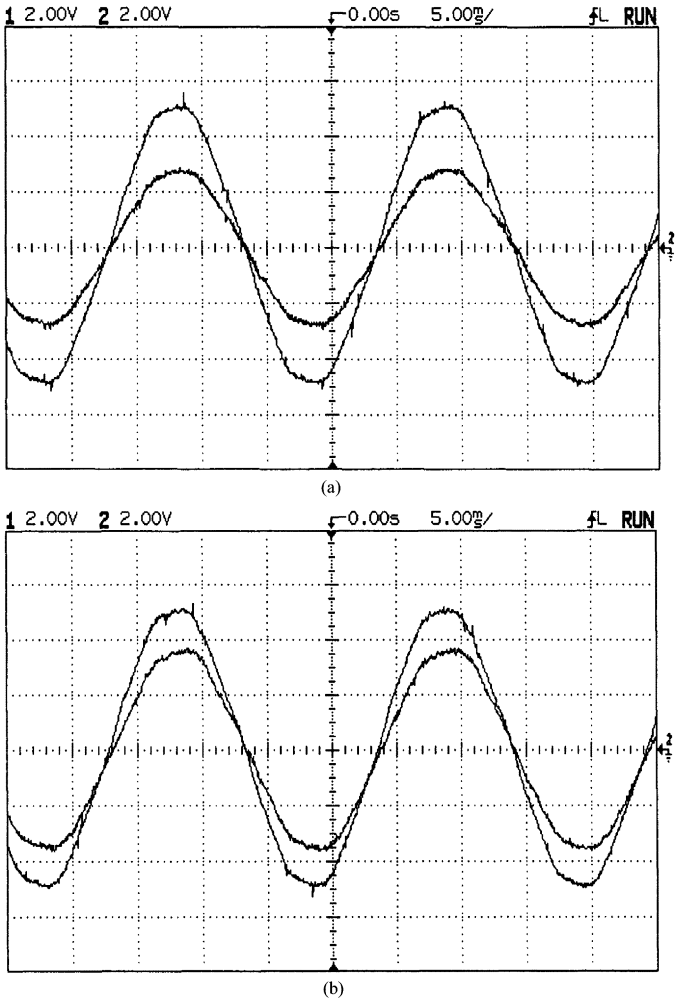

Fig. 22. Experimental results: v_{ga} and i_{ga} at $V_{ab} = 415$ V *and* $V_o = 700$ V (a) 7.5 kW (b) 9 kW. Total harmonic Distortion = (a) 2.5\% (b) 2.4% Voltage Scale: 133.5 V/div Current Scale = 10.4 A/div Inductance/Phase = 7.5 mH Power Factor = (a) 0.998 (b) 0.995.

CMR isolation amplifier *HCPL* 7800. The analog signals are scaled by 0.25 and dc shifted by 2.5 V in the analog signal conditioner board, before passing them on to analog input channels of *TMS*320*F*240. This has been done so as to make sure that the analog input channels of the DSP receive unipolar signals between 0–5 V range. Therefore the effective value of the current sense resistance is $R_s = 0.05$.

Fig. 17 shows the frequency response plot of the voltage control transfer function $G_v(s) = \widetilde{V_o}(s)/\widetilde{V_m}(s)$ measured using Schlumberger 1250 frequency response analyzer (FRA) instrument. The nominal operating point of the converter is defined in Fig. 14.

It is also given as

$$V_{ga}(phase) = 110\ \text{V(rms)},\ V_o = 300\ \text{V},$$
$$V_m = 0.25\ \text{V},\ L = 7.5\ \text{mH/phase},$$
$$R = 100\ \Omega,\ C = 1650\ \mu\text{F},\ R_s = 0.05\ \Omega.$$

The analog modulating signal $\widetilde{V_m}$ of the FRA is converted to its digital equivalent using one of the spare ADC channels of TMS320F240 and then added to the nominal operating reference V_m inside the digital controller. For measurement, the analog signal $\widetilde{V_m}$ and the scaled output signal $\widetilde{V_o}$ are connected to the input and output channels of the FRA respectively. The frequency response plot of the same transfer function obtained through linear, small signal, low frequency analysis of the three phase boost rectifier is placed in the same figure (Fig. 17) for easy comparison. It can be seen that qualitatively the analysis and the measurement results match over the entire frequency range of the plot. However there exists a phase difference between analysis and measurement results in the frequency range above 100 Hz. This difference is due to the phase contribution from the pole introduced by the zero order hold circuit of the ADC of TMS320F240. The pole is located approximately at 1590 Hz, if we model zero order hold as a low pass filter at low frequency. This correction, when taken into account, makes the analytical and measurement results of the frequency response of $G_v(s)$ follow each other very closely.

Therefore we can conclude that an accurate low frequency model of the three phase boost rectifier can be developed by following the standard small signal analysis methods of a current mode controlled dc–dc converter if the nominal dc operating point is chosen as $V_g = 1.5 V_{ga} \sin(45°)$.

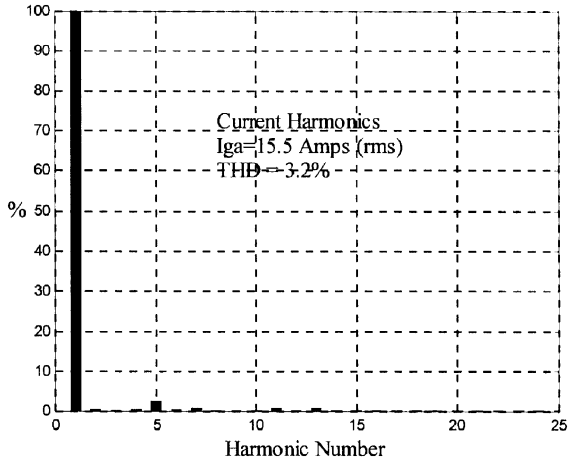

Fig. 23. Measurement result from LEM HEME ANALYST 2060: Harmonic spectrum of the input current (RMS 15.5 Amp, THD 3.2%) at maximum load (10 Kw, 700 V DC).

Figs. 18–20 show different control variables through 12-b bipolar digital to analog converter (DAC) outputs of the DSP control board.

In Fig. 18(a) we can see the sequence of sector change that occurs under closed loop condition with respect to currents i_{ga} and i_{gb}. Fig. 18(b) shows the sequence of sector change with respect to $i_{g\alpha}$ and $i_{g\beta}$. They prove the validity of the self-synchronization logic described in Section II.

In Section II we have indicated that the control algorithm based on the sector information uses a set of simultaneous equations to calculate the switching time durations. Fig. 19(a) and Fig. 19(b) show the profile of the switching times T_α, T_β and T_1, T_2 that are obtained after solving those equations in real time over a line frequency period of $i_{g\alpha}$.

Fig. 20(a) shows the signal that indicates in real time the selection of the set of simultaneous equations for calculation of T_1, T_2. It may be noted that the sectors 1-3-4-6 have been mapped as low level and sectors 2A-2B-5A-5B have been mapped as high level. The execution time of the control algorithm in DSP TMS320F240 is less than 40 μs, as can be seen from Fig. 20(b).

Fig. 21(a) and (b) show the phase voltage and phase current waveforms under regulated dc voltage of 700 V dc, at two different load conditions of 2.5 kW and 5 kW, respectively.

Under same input and output voltage conditions Fig. 22(a) and (b) show high power factor operation at loads of 7.5 kW and 9 Kw.

The input current and voltage waveforms are analyzed for power factor and total harmonic distortion (*THD*) results by "*LEM*" made *HEME ANALYST* 2060 m. Power factor greater than 0.995 and *THD* less than 6% are achieved on input current over a load range of 20% to 110% The harmonic spectrum of the input current at maximum load under rated operating condition is shown in Fig. 23.

The dynamic response of the output dc voltage at step change of the load resistance from 116 Ω to 58 Ω is shown in Fig. 24(a). For the same step change in load resistance the dynamic response of the input current is shown in Fig. 24(b).

One of the disadvantages of this method is that it requires certain minimum load to be applied on the converter output so as

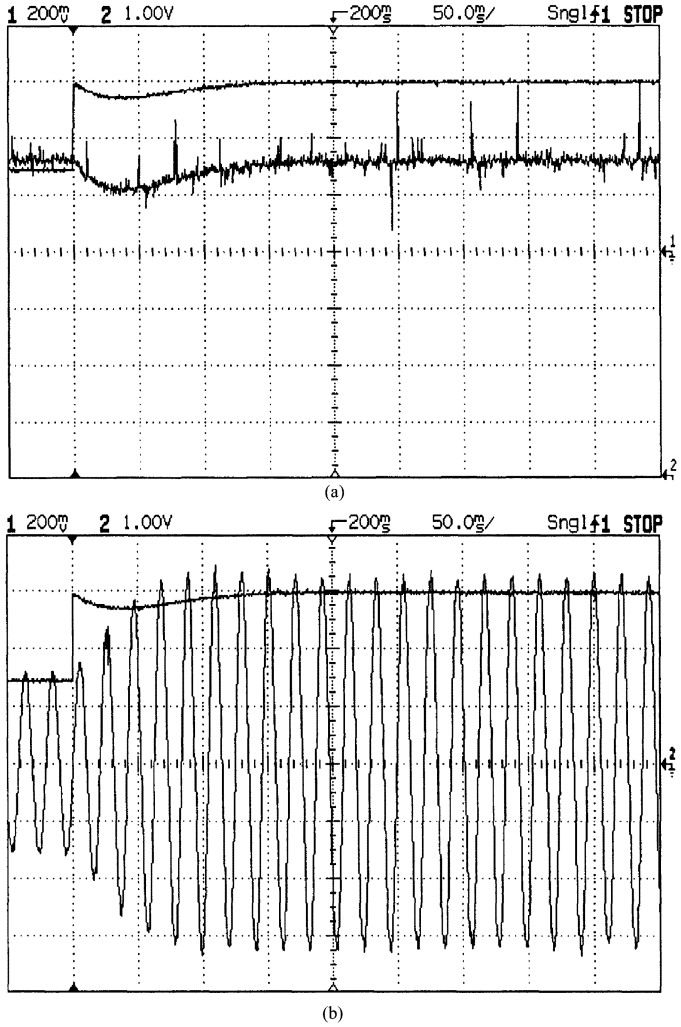

Fig. 24. Experimental Results: dynamic Response of the (a) output dc voltage at a step change in the load resistance Channel 1: load current, $\mathrm{Scale\ (ch1)} = 4\ \mathrm{A/div}$ Channel 2: output dc voltage V_o, Scale (ch2): 125 V/div (b) input phase current at a step change in the load resistance Channel 1: Load current, $\mathrm{Scale\ (ch1)} = 4\ \mathrm{A/div}$ Channel 2: Input phase current i_{ga}, Scale (ch2): 5.2 A/div load resistance initial: 116 ohm, Load Resistance Final: 58 ohm, $\mathrm{Inductance/Phase} = 7.5\ \mathrm{mH}$.

to operate stably as has been shown analytically in Section IV of this paper. It is also important that the inductive drop is substantially low compared to the input voltage so that (6) and (7) can be valid for every switching period of the converter. If such a condition is not satisfied there will be steady state error in phase angle of input current. Therefore, it will be better to operate the converter at as high switching frequency as possible, under the constraint of the power circuit design, so that the boost inductance can be of low value. The other limitation of this method is that if the input voltage itself contains harmonics then the input current being proportional to the input voltage will contain the those harmonics that are within its bandwidth.

VIII. Conclusion

This paper describes the DSP based implementation of a discrete current mode control algorithm that performs high power factor rectification for a three phase boost converter. In this controller input voltage sensing is not required, because switching

pulses get self-synchronized with the frequency and phase of the input voltage. There is no need to use conventional PLL, as the controller works in stationary reference frame. Two decoupled fixed frequency current mode controllers generate the switching instants for the equivalent single phase boost rectifiers. A combined switching strategy is developed in the form of space vectors to simultaneously satisfy the timing requirements of both the current mode controllers in a switching period. The steady state stability condition of the digitally controlled boost rectifier has been derived. It is shown that if the nominal dc operating point is chosen as $V_g = 1.5V_{ga}\sin(45°)$ then a low frequency model of the three phase boost rectifier can be developed by following the standard small signal modeling technique of a current mode controlled dc-dc converter.

The control algorithm is computationally simple. In TMS320F240 which has a clock frequency of 20 MHz and ADC conversion time of 13.2 μs$(= 6.6\ \mu\text{s} * 2)$, the control algorithm gets executed in less than 40 μs. In conclusion, it can be said that, this method of control of three phase high power factor Boost rectifier provides comparable or better performance over existing methods with a much simpler control structure.

APPENDIX I

The simulation model of the three phase-three wire PWM converter of Fig. 1 is based on the following equations:

$$\begin{aligned} L\frac{di_{ga}}{dt} &= v_{ga} - v_{ra} \\ L\frac{di_{gb}}{dt} &= v_{gb} - v_{rb} \\ L\frac{di_{gc}}{dt} &= v_{gc} - v_{rc} \\ C\frac{dV_o}{dt} &= (i_{ga}U_a + i_{gb}U_b + i_{gc}U_c) - \frac{V_o}{R} \end{aligned}$$

where

$$\begin{aligned} v_{ra} &= 0.5V_0M_a + v_{no} \\ v_{rb} &= 0.5V_0M_b + v_{no} \\ v_{rc} &= 0.5V_0M_c + v_{no} \\ v_{no} &= \frac{1}{3}\left[v_{ga} + v_{gb} + v_{gc} - 0.5V_o(M_a + M_b + M_c)\right] \\ U_i &= 1\ if\ S_i\ is\ ON \quad and \\ U_i &= 0\ if\ S_i\ is\ OFF,\ i = a,b,c \\ M_i &= 1\ if\ S_i\ is\ ON \quad and \\ M_i &= -1\ if\ S_i\ is\ OFF,\ i = a,b,c. \end{aligned}$$

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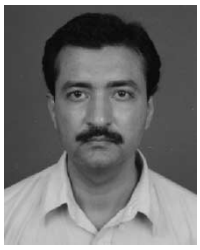

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