# Digital Implementation of a Unity-Power-Factor Constant-Frequency DCM Boost Converter

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**Abstract- A DSP implementation of digital control for constant-frequency, unity-power-factor, and discontinuous-conduction-mode boost rectifier is described. By employing variable-duty-cycle control, the power factor of over 0.99 is achieved in the entire universal line-voltage range (90-264 V). In addition, the transient response of the rectifier is optimized by utilizing a non-linear PI-controller with anti windup that is independently optimized for U.S. line-voltage range (90-132 V) and for European line-voltage range (180-264 V) and by temporarily increasing the bandwidth of the control loop during transients. The performance of the proposed DSP control was verified on a 100-kHz, 400-W unity-power-factor rectifier prototype.**

**Index Term: Boost, PFC, DCM, DSP, Digital Control**

## I. INTRODUCTION

The discontinuous-conduction-mode (DCM) boost converter is extensively used in power-factor-correction (PFC) applications due to the simplicity of its control and good performance [1]. The application of the DCM boost converter is usually limited to relatively low-power levels because of the increased current stresses of the semiconductor components. However, by employing the interleaving technique, the DCM boost converter application range can be extended to high power levels without performance degradation [2].

The control of the DCM boost PFC converter can be performed either by variable- or constant-frequency control. In both control approaches the on-time of the boost switch is kept constant during a half line cycle by reducing the bandwidth of the output-voltage feedback loop well below the rectified frequency of the line voltage, i.e., well below 100 Hz. The variable-frequency control offers slightly lower current stress and input-current distortion compared to the constant-frequency control, but its implementation requires input-current sensing. The constant-frequency control does not require input-current sensing and it is also more conducive to interleaving applications.

A universal-line (90 – 264 V) DCM boost PFC converter with either variable- or constant-frequency constant on-time control can easily meet the EN-61000-3-2 and corresponding Japanese line-current harmonic current limits. However, the power factor (PF) of the line voltage and line current is strongly dependent on the line voltage and is not as high as in the PFC control approaches that also employ line-current control loop. Degradation of PF is especially noticeable at high line (European rms line range 180 – 264 V) where a PF of approximately 0.95 can be achieved at best.

Theoretically, unity PF (UPF) of the constant-frequency DCM boost PFC converter can be achieved in the entire line range by resorting to variable on-time (duty-cycle) control implemented with input-voltage feed forward [3]-[5]. In this approach, the implementation of the feed forward path control law governing the duty cycle changes over the half-line cycle requires a division, a multiplication, and a square root operation. Since an exact analog implementation of all of these operations is too complex, a number of approximate implementations that have a reduced number of algebraic operations were proposed [3]-[5]. For example, the implementation of the feed forward control law in [5] with two analog integrators with reset switches eliminates the need for division and square root operations, whereas the implementations proposed in [3] and [4] eliminate the division operation. By employing a DSP-based digital control, the implementation of the control law algorithm is greatly simplified [6]. Generally, the implementations described in [3]-[6] exhibit good performance if the output voltage ripple is kept low. However, their performance deteriorates as the output ripple increases [5].

Because the minimization of line-current distortion in a PFC converter requires that the output voltage control loop have a very low bandwidth, there is a strong trade-off in achieving a good input PF and fast transient response of the output voltage. A number of analog and digital approaches have been proposed to improve the transient response of the output voltage without a degradation of PF [4], [7]-[11]. Generally, these approaches are either based on the techniques that prevent the feedback of the inevitable low-frequency output-voltage ripple into the control loop so that the control loop bandwidth can be maximized [7]-[10], or on the techniques that implement a low-bandwidth adaptive control where the bandwidth is temporarily increased during transients [4], [7], [11].

In this paper, a digital implementation of the variable duty-cycle control of UPF, constant-frequency, DCM boost rectifier that offers a very low line-current distortion and fast transient response of the output voltage is described. The

current distortion is minimized by employing low-bandwidth output-voltage control and by exactly implementing the required feed-forward path control law that governs duty-cycle variations. The fast-output-voltage transient response that features reduced overshoot/undershoot and settling time is achieved by implementing a regulation-band control. The performance of the proposed digital control implementation is verified on a 400-W, 100-kHz, UPF DCM boost rectifier designed to operate in the universal line range (90 – 264 V).

## II. DIGITAL CONTROL IMPLEMENTATION

As derived in [3]-[5], in the constant-frequency DCM boost PFC converter, the rectified line current averaged over a switching cycle, $i_{IN(rec)}^{av}$, is

$$i_{IN(rec)}^{av} = \frac{1}{2L_B f_{SW}} \cdot \frac{d^2}{(1-\frac{v_{IN(rec)}}{v_O})} \cdot v_{IN(rec)}, \qquad (1)$$

where, $v_{IN(rec)}$ is the rectified line voltage, $v_O$ is the output voltage, $L_B$ is the inductance of the boost inductor, $f_{SW}$ is the switching frequency, and d is the duty cycle.

As can be seen from Eq. (1), UPF can be achieved at any line voltage if the second term in the product on the right-hand side of Eq. (1) is kept constant, i.e., if duty cycle d is controlled so that

$$d = \lambda \cdot \sqrt{1-\frac{v_{IN(rec)}}{v_O}}, \qquad (2)$$

where coefficient $\lambda$ is constant over a half line cycle.

Figure 1 shows a DSP implementation of the constant-frequency, variable-duty-cycle DCM UPF boost converter. The variation of the duty cycle is implemented by the feed forward path, whereas the output voltage regulation is achieved by output-voltage feedback control. Because of DSP's adequate calculation capabilities, relationship in Eq. (2) that governs duty-cycle changes is implemented exactly. In the circuit in Fig.1, both the input and output voltages are sensed, scaled down by respective resistor-dividers, sampled and digitized by an on-chip analog-to-digital converter, and then processed by the DSP to generate duty cycle d. From Fig. 1, if input-voltage divider gain $K_{DIN}$ is selected equal to output-voltage divider gain $K_{DOUT}$, i.e., $K_{DIN} = K_{DOUT}$, duty cycle d is given by

$$d = K_F \cdot F_M \cdot v_C^* \sqrt{1-\frac{K_{DIN} \cdot K_{ADC} \cdot v_{IN(rec)}}{K_{DOUT} \cdot K_{ADC} \cdot v_O}}, \qquad (3)$$

or,

$$d = \lambda \cdot \sqrt{1-\frac{v_{IN(rec)}}{v_O}},$$

where, $K_{ADC}$ is the gain of the A/D converter, $K_F$ is the feed forward gain, $F_M$ is the gain of digital pulse width modulator (DPWM), and $v_C^*$ is the output of digital controller $G_C(z)$. It should be noted that, the star (*) notation is used to denote the digitized quantities.

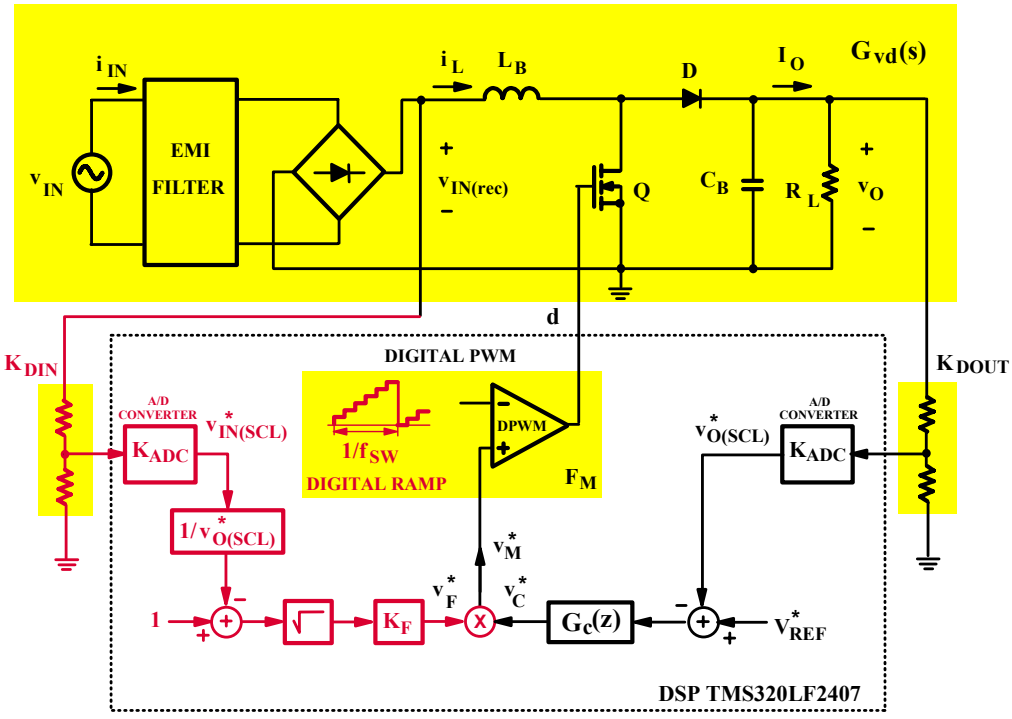



Fig.1 DSP implementation of constant-frequency, variable-duty-cycle DCM UPF boost rectifier.

To keep coefficient $\lambda$ that is given by

$$\lambda = K_F \cdot F_M \cdot v_C^* \tag{4}$$

constant over a half line cycle, controller output $v_C^*$ must be constant over a half line cycle. Control voltage $v_C^*$ can be made approximately constant by limiting the bandwidth of the output-voltage control loop well below the rectified line frequency of 100/120 Hz.

## III. CONTROL LOOP DESIGN

If the sampling frequency in a digital control is selected to be much higher than the control-loop bandwidth, the design of the digital controller can be performed in the analog domain (s-domain) and than translated into the digital domain. This approach, known as the digital redesign approach, is taken in the design of the digital control of the circuit in Fig. 1 since the selected sampling frequency $f_S = 100\,\text{kHz}$ is much greater than the output-voltage control-loop bandwidth that is well below 100 Hz.

A simplified block diagram of the digitally controlled UPF DCM boost converter in Fig. 1 is shown in Fig. 2. In the block diagram in Fig. 2, the ADC conversion time and DSP computation time are neglected since combined these two delays are shorter than one sampling period of 10 µs so that they virtually do not produce any phase delay in the control loop with a crossover frequency below 100 Hz.

From Fig. 2, loop gain $T_V$ in s-domain is given by

$$T_V(s) = K_{DOUT} \cdot K_{ADC} \cdot G_C(s) \cdot G_{VC}(s)\,, \tag{5}$$

since for the sampling frequency much higher than the loop bandwidth z-domain digital controller $G_C(z)$ can be approximated by its s-domain counterpart $G_C(s)$.

The low-frequency output-to-control transfer function $G_{vc}(s)$ of the UPF DCM boost PFC converter supplying a resistive load is a single-pole transfer function given by

$$G_{vc}(s) = \left.\frac{\hat{v}_O}{\hat{v}_C^*}\right|_{\hat{v}_{IN}=0} = \frac{K_{VC}}{1+\dfrac{s}{\omega_P}}\,, \tag{6}$$

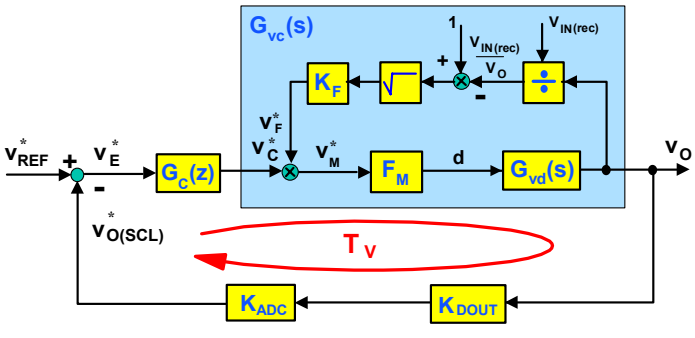



Fig. 2 Voltage loop of digitally controlled UPF DCM boost rectifier.

where,

$$K_{VC} = \frac{\sqrt{2}V_{IN}K_F F_M}{2}\sqrt{\frac{R_L}{L_B f_{SW}}}\,, \tag{7}$$

$$\omega_P = \frac{2}{R_L C_B}\,. \tag{8}$$

As can be seen from Eqs. (6) through (8), dc gain $K_{VC}$ is dependent on load resistance $R_L$ and proportional to the rms of line voltage $v_{IN}$, whereas pole frequency $\omega_P$ is only load dependent. Since the position of pole $\omega_P$ does not change with the line voltage, the control design does not suffer from design trade-offs found in some other DCM boost PFC circuits that have a line-voltage-dependent pole frequency.

Because control-to-output transfer function $G_{vc}(s)$ is a single-pole transfer function, a proportional and integral (PI) control

$$G_C(s) = K_P + \frac{K_I}{s} = K_P\frac{s+\omega_{ZV}}{s} \tag{9}$$

is employed for voltage loop compensation. In Eq. (9), $K_P$ is the proportional gain of the controller, $K_I$ is the integral gain, and

$$\omega_{ZV} = \frac{K_I}{K_P} \tag{10}$$

is the PI controller zero.

Because dc gain $K_{VC}$ and pole-frequency $\omega_P$ of transfer function $G_{vc}(s)$ depend on the line voltage and output load current (power), the loop compensation must be performed for worst case so that the loop stability and a proper loop bandwidth are ensured over the entire operating range. The worst-case design requires that the compensation be calculated based on the maximum rms line voltage $V_{IN(MAX)} = 264\,\text{V}$ and minimum load current $I_{O(MIN)}$. However, for such compensation, the loop bandwidth at minimum rms line voltage $V_{IN(MIN)} = 90\,\text{V}$ would be very much reduced since gain $K_{VC}$ at the minimum line is much lower than at the maximum line. This would significantly deteriorate the transient response of the converter operating off the 115-V power line (U.S. power line).

For a universal line-voltage PFC front, a DSP-based control offers the opportunity to virtually eliminate the variations of the bandwidth with the line voltage. Namely, in a DSP-based control it is easy to implement the controller with two sets of parameters, one that is optimized for the European line-voltage range (nominal rms voltage $V_{IN(NOM)} = 220\,\text{V} \pm 20\%$) and the other that is optimized for U.S. rms line-voltage range ($V_{IN(NOM)} = 115\,\text{V} \pm 20\%$). Since in the control shown in Fig. 1 the rectified line voltage is sensed, the controller has the information about the line voltage so it can execute the appropriate control algorithm.

Furthermore, once the controller design is separated into two narrow-line-range designs, the 20% variation of the line voltage around the nominal line voltage can be neglected since it translates to a variation of less than 3 dB. Therefore, for each line-voltage range the compensator optimization can be performed based on nominal line voltage $V_{IN(NOM)}$ and minimum load current $I_{O(MIN)}$.

To ensure stable operation with acceptable phase over the entire load range within each of the two line-voltage ranges, the controller zero $\omega_{ZV}$ should be placed at approximately one-to-two octaves above the frequency of minimum-load pole $\omega_{P(MIN)}$ [4], [6]. By following the design procedure in [6], i.e., by placing the frequency of the compensator zero at three times the frequency of the minimum load pole, i.e.,

$$\omega_{ZV} = 3\omega_{P(MIN)}, \tag{11}$$

proportional gain $K_P$ and integral gain $K_I$ are given by

$$K_P = \frac{\sqrt{1+\omega_{CV}^2/\omega_{P(MAX)}^2}}{K_{VC(MAX)} \cdot K_{DOUT} \cdot K_{ADC} \cdot \sqrt{1+\omega_{ZV}^2/\omega_{CV}^2}}, \tag{12}$$

$$K_I = \omega_{ZV} \cdot K_P, \tag{13}$$

where, $K_{VC(MAX)}$ and $\omega_{P(MAX)}$ are dc gain and pole frequency of $G_{vc}$ at full load $I_{O(MAX)}$ and nominal rms line voltage $V_{IN(NOM)}$, respectively, and $\omega_{CV}$ is the desired crossover frequency of the voltage loop.

Having controller gains $K_P$ and $K_I$ calculated for each line-voltage range, the mapping of the s-domain PI-controller $G_C(s)$ into z-domain ($z = e^{sT_S}$) digital PI controller $G_C(z)$ can be performed. In this development, a digital PI controller with anti windup is employed to further improve transient response of the control loop by preventing the controller output saturation during transients. Generally, the PI controller with anti windup is implemented by limiting the output of the integral part of the controller. Using bilinear transformation, a recursive algorithm of the digital PI controller with anti windup can be expressed as [6]

$$v_C^*(n) = v_{INT}^*(n) + K_P \cdot v_E^*(n), \tag{14}$$

$$v_{INT}^*(n) = v_{INT}^*(n-1) + \frac{K_I T_S}{2} \cdot \left[v_E^*(n) + v_E^*(n-1)\right], \tag{15}$$

where $v_{INT}^*$ is the integral part of digital controller output, $T_S$ is the sampling period, and n and (n-1) are $n^{th}$ and ($n^{th}$ -1) sampling instants, respectively.

A block diagram implementation of the digital controller algorithm given in Eqs. (14) and (15) is shown in Fig. 3. The limiter block at the output of the integrator part of the controller models the anti windup function of the controller. As can be seen from Fig. 3, the integral part of the controller $v_{INT}^*$ is limited to the values between $-K_P \cdot v_E^*$ and $v_{C(MAX)}^* - K_P \cdot v_E^*$ since the value of the output of the controller $v_C^*$ is limited between zero and $V_{C(MAX)}^*$ due to the duty cycle of the converter that is limited to the values between zero and $D_{MAX}$. A flow chart of the described algorithm of the PI-digital controller with anti windup is given in [6].

Although the implementation with a non-linear PI controller with anti windup that is optimized for each line-voltage range improves the transient response over a single, universal-line range controller, the transient response of the UPF DCM boost converter is still relatively slow because of a low control-loop bandwidth that is required to minimize the line-current harmonic distortion. Slow output voltage transient response imposes additional design trade-offs on the UPF front-end boost converter as well as the downstream converters due to transient overpower conditions and large overshoots and undershoots of the output voltage during load transients. The transient response of the converter can be significantly improved by employing a regulation-band control i.e., by temporarily increasing the control loop bandwidth during transients, [4], [7], [12]. As illustrated in Fig. 4, when during load transients, output voltage goes outside a preset output voltage range around the steady-state value $v_O$, the controller bandwidth is increased to speed-up the transient. Specifically, for step-up load transients, the controller bandwidth is increased when instantaneous output voltage $v_O$ falls below low-level threshold $v_{OL} = v_O - \Delta v_{ORB}$, or when it exceeds high-level threshold $v_{OH} = v_O + \Delta v_{ORB}$ during step-down transients. When the instantaneous output voltage $v_O$ returns to the preset voltage range, the controller reverts to its steady-state low-bandwidth control. To function properly, the preset

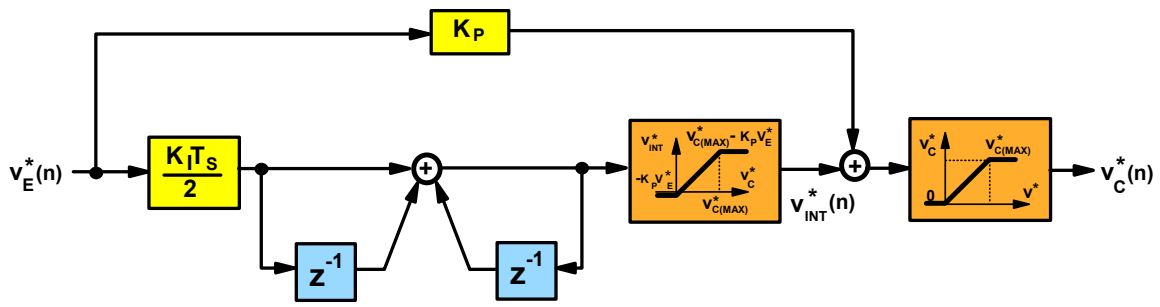



Fig.3 Implementation of digital PI controller with anti windup.

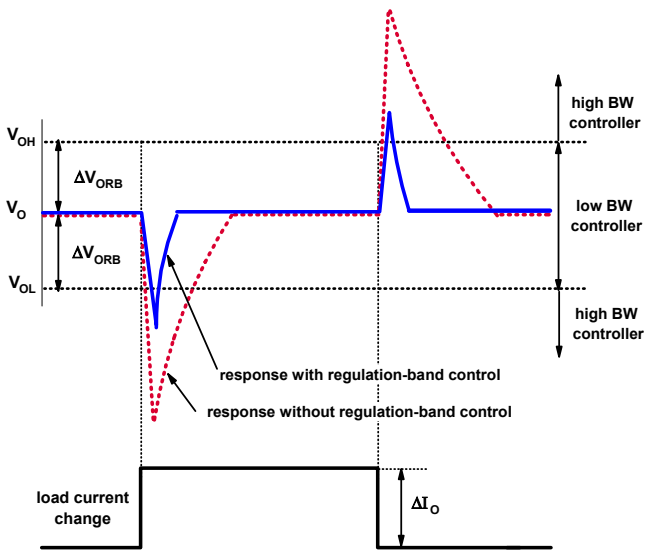



Fig. 4 Illustration of voltage regulation-band control.

voltage range must be larger than the worst-case full-load output voltage peak-to-peak ripple $v_{O(ripple)}^{pk-pk}$, i.e., $v_{OH} - v_{OL} = 2\Delta v_{ORB} > v_{O(ripple)}^{pk-pk}$. The bandwidth change is implemented in each line-voltage range by changing corresponding coefficients $K_P$ and $K_I$ of the controller.

## IV. EXPERIMENTAL EVALUATION

The performance evaluation of the described DSP-based control was verified on a 400-W, DCM boost PFC converter designed to operate at constant-switching frequency $f_{SW} = 100\,\text{kHz}$ in the universal line-voltage range $V_{IN} = 90 - 264\,\text{V}$. The output voltage of the experimental circuit was regulated at $V_O = 385\,\text{V}$ in the entire load range, i.e., from $I_{O(MAX)} = 1.04\,\text{A}$ (or $R_{L(MIN)} = 370\,\Omega$) down to $I_{O(MIN)} = 0.10\,\text{A}$ ($R_{L(MAX)} = 3.7\,\text{K}\Omega$). As indicated in Fig. 1, the experimental power stage was built with $L_B = 47\,\mu\text{H}$, and $C_B = 470\,\mu\text{F}$. With this selection of $L_B$ and $C_B$, the boost power stage operating at a switching frequency of 100 kHz always operates in DCM with the maximum (full-load) output voltage peak-to-peak ripple of approximately 8 V.

The control was implemented with the fixed-point TMS320LF2407A DSP with a clock frequency of $f_{CLK} = 40\,\text{MHz}$ and sampling rate $f_S = 100\,\text{KHz}$. Gain of feed-forward path $K_F = 400$ was selected in this implementation. The square root operation required to calculate the feed-forward signal was implemented by the Taylor series approximation with first seven terms. Since the reference voltage of the embedded ADCs in the TMS320LF2407A is $V_R = 3.3\,\text{V}$, the output-voltage divider gain is set so that for nominal output voltage $V_O = 385\,\text{V}$ the voltage at the input of ADC is 2.64 V. This selection of the divider gain makes it possible to design an over-voltage protection circuit that ensures that the input of ADC never exceeds its maximum rating. In this design, $K_{DOUT} = K_{DIN} = 2.64/385 = 6.9 \cdot 10^{-3}$. As explained in [6], the gain of ADC is $K_{ADC} = 1/V_R = 0.3$, whereas the gain of DPWM is given by $F_M = f_{SW}/f_{CLK} = 2.5 \cdot 10^{-3}$. For the selected values of gains $K_{DOUT}$ and $K_{ADC}$, the digital output reference is $V_{REF}^* = 0.80$ [6].

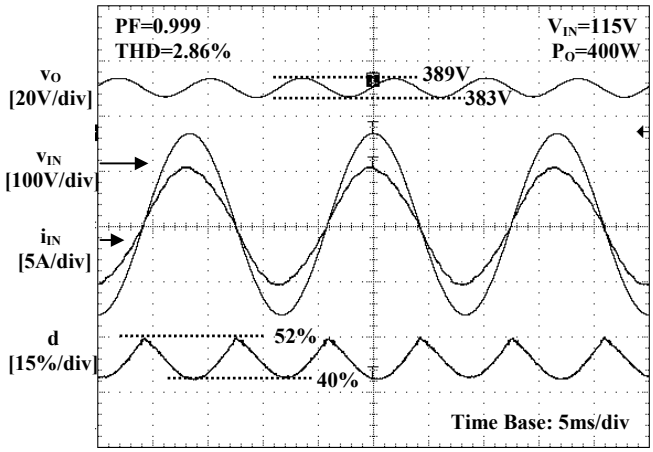
The steady-state control-loop bandwidth of the experimental circuit was set to $f_{CV} = 8\,\text{Hz}$, i.e. $\omega_{CV} = 2\pi f_{CV} = 50\,\text{rad/s}$ for both low voltage range ($V_{IN(NOM)} = 115\,\text{V}$) and high voltage range ($V_{IN(NOM)} = 220\,\text{V}$). During transients, the bandwidth is increased to $f_{CV} = 40\,\text{Hz}$ by changing the parameters of the controller whenever the output voltage goes out of the preset regulation band. Since the maximum output voltage ripple is $v_{O(ripple)}^{pk-pk} \approx 8\,\text{V}$, the regulation band of $2\Delta v_{ORB} = 24\,\text{V}$ was selected. Table I summarizes the PI controller parameters for steady-state and transient operation for each voltage range.

Figures 5(a) and (b) show the measured line-voltage, line-current, duty ratio, and output-voltage waveforms of the experimental DCM boost PFC converter with the described variable-duty-cycle digital control at full load and for the nominal input voltage at $V_{IN(NOM)} = 115\,\text{V}$ and $V_{IN(NOM)} = 220\,\text{V}$, respectively. As can be seen from the oscillograms in Figs. 5 (a) and (b), the line current does not exhibit any noticeable distortion at both line voltages. In fact, the measured power factor (PF) and total harmonic distortion (THD) at $V_{IN(NOM)} = 115\,\text{V}$ are 0.999 and 2.86%, respectively, whereas PF and THD at $V_{IN(NOM)} = 220\,\text{V}$ are 0.993 and 3.88%, respectively. The measured PF and THD at the nominal input voltages for different loads (output power) are summarized in Table II.

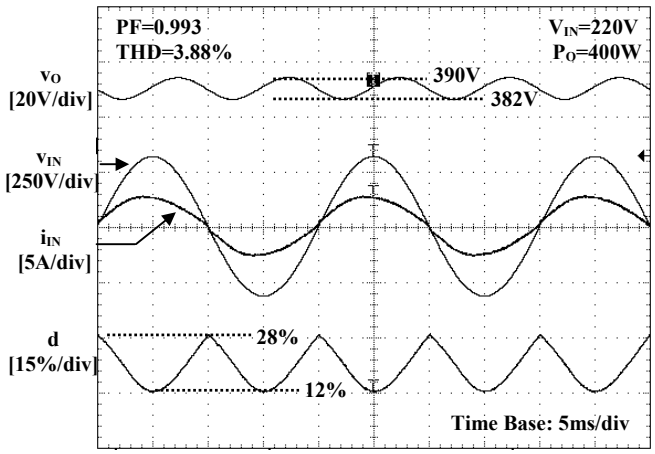
To illustrate the improvement in the transient response brought about by the implementation of the regulation-band

Table I
Parameters of the non-linear PI controller.

| Operating conditions | $K_P$ | $K_I$ |
|---|---|---|
| Low-range line voltage (90-132 V) steady state | 2000 | 4133 |
| Low-range line voltage (90-132 V) transients | 5867 | 20213 |
| High-range line voltage (180-264 V) steady state | 627 | 2160 |
| High-range line voltage (180-264 V) transients | 3067 | 10566 |

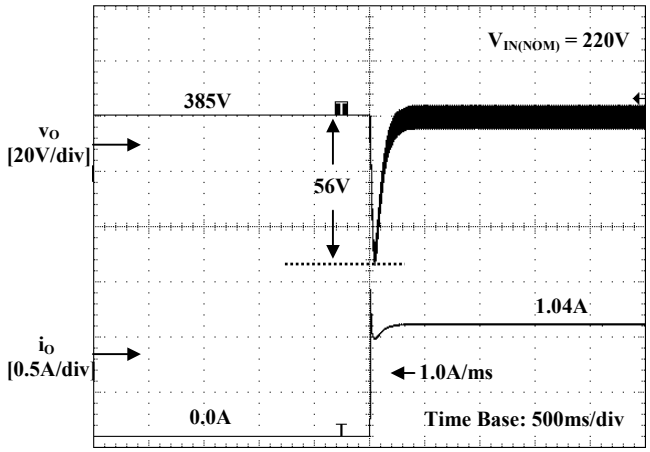



(a)

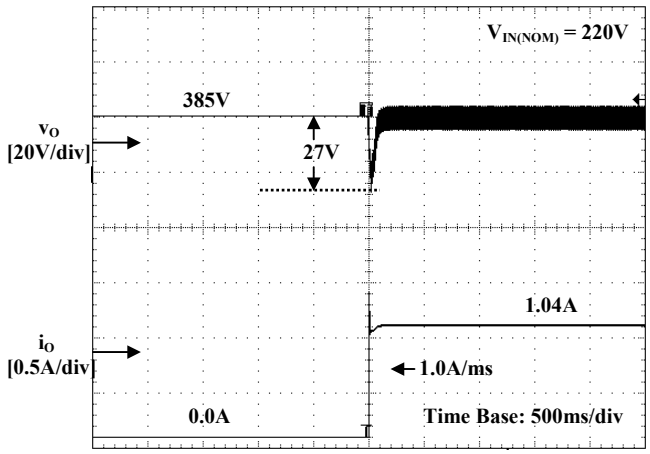



(b)

Fig. 5 Waveforms of output voltage $v_O$, line voltage $v_{IN}$, line current $i_{IN}$, and duty cycle d at: (a) $V_{IN(NOM)}$ = 115V; (b) $V_{IN(NOM)}$ = 220 V.




(a)




(b)

Fig. 6 Voltage undershoot for no-load-to-full-load transient at $V_{IN(NOM)}$ =220V (a) without voltage regulation-band control; (b) with voltage regulation-band control.

Table II
Measured PF and THD at different loads

| $V_{IN}$ (V) | $P_{OUT}$ (W) | THD (%) | PF | $f_L$ (Hz) |
|---|---|---|---|---|
| 115 | 50 | 6.25 | 0.982 | 60 |
| 115 | 100 | 3.52 | 0.994 | 60 |
| 115 | 200 | 2.98 | 0.998 | 60 |
| 115 | 300 | 2.67 | 0.998 | 60 |
| 115 | 400 | 2.86 | 0.999 | 60 |
| 220 | 50 | 7.65 | 0.886 | 50 |
| 220 | 100 | 4.51 | 0.962 | 50 |
| 220 | 200 | 3.58 | 0.987 | 50 |
| 220 | 300 | 3.95 | 0.992 | 50 |
| 220 | 400 | 3.88 | 0.993 | 50 |

control, Figs. 6(a) and (b) show no-load-to-full-load output voltage transients at $V_{IN(NOM)} = 220\,V$ without and with the regulation-band control, respectively, whereas Figs. 7(a) and (b) show the corresponding waveforms for full-load-to-no-load transients.

As can be seen by comparing Fig. 6(a) with Fig. 6(b), regulation-band control reduces the undershoot of the output voltage for the no-load-to-full-load transient from 56 V down to approximately 27 V. Similarly, by comparing Fig. 7(a) with Fig. 7(b), regulation-band control reduces the overshoot of the output voltage for the full-load-to-no-load transient from 46 V down to approximately 23 V. In addition, the settling times of the transients are very much reduced by the employment of the regulation-band control. It should be noted that, if necessary, the further reduction of the output voltage overshoot/undershoot can be achieved by reducing the regulation-band width $\Delta V_{ORB}$.

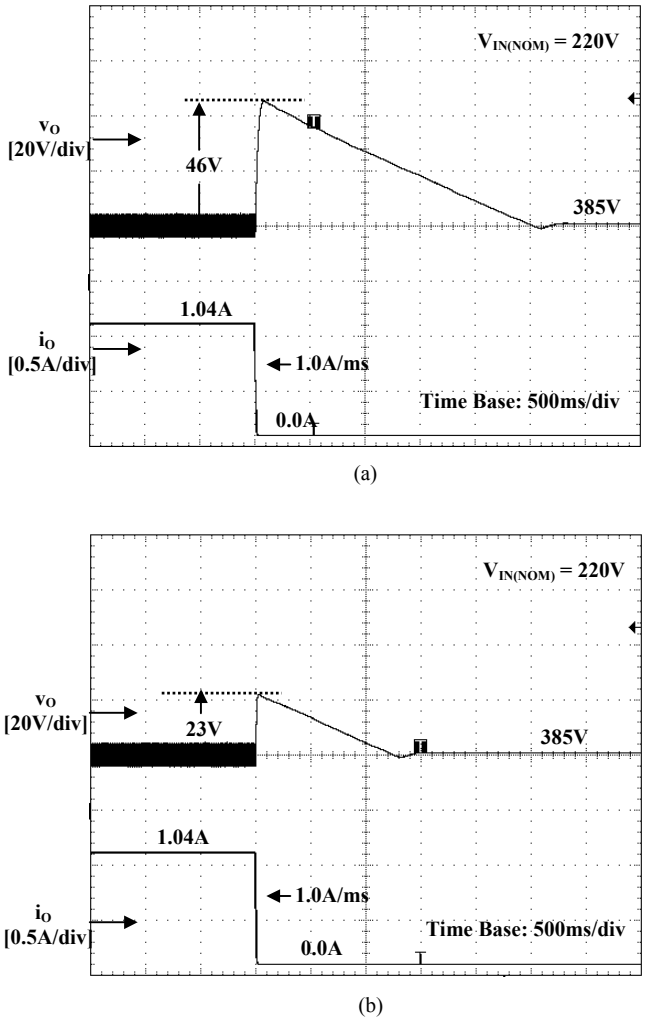



Fig. 7 Voltage overshoot for full-load-to-no-load transient at $V_{IN(NOM)}$ =220V (a) without voltage regulation-band control; (b) with voltage regulation-band control.

Finally, because the parameters of the non-linear controller are optimized to maintain the same bandwidth at $V_{IN(NOM)} = 115\,V$ and $V_{IN(NOM)} = 220\,V$, the corresponding transient responses with and without regulation-band control at $V_{IN(NOM)} = 115\,V$ are practically identical to those at $V_{IN(NOM)} = 220\,V$.

## V. SUMMARY

It has been shown that DSP-based digital control of the universal-line-range, constant-frequency, variable-duty-cycle, unity-power-factor DCM boost rectifier offers excellent performance. In addition to complying with the required harmonic-current limits for both European and Japanese power lines, the implemented control features a power factor greater than 0.99 in the entire universal line-voltage range. Moreover, due to the implementation of the regulation-band control, the no-load-to-full-load undershoot and full-load-to-no-load overshoot of the output voltage of a 400-W unity-power-factor rectifier prototype are limited to below 27 V and 23 V, respectively.

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