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Digital Implementation of Fractional Order PID-Type Controller for Boost DC–DC Converter

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ABSTRACT In this paper, the problem of designing a fractional order PID-type controller is considered for a boost converter. By using the output capacitance and input inductance values this paper characterizes integer order PID-type control gains which will make the closed-loop system transfer function approximately equal to a first order system with a unit DC gain and prescribed time constant τ. Next, a procedure to compute the design parameters of a fractional order PID-type controller is given together with a descritized control algorithm for DSP implementation. By using a floating-point DSP, the proposed control algorithm is implemented in real time. Finally, experimental results are given to show the practical feasibility and effectiveness of the proposed fractional order PID-type control system under several operating conditions. The results illuminate that the proposed controller can be better than a conventional integer order PID-type controller.

INDEX TERMS Boost converter, PID control, fractional order system, DSP, DC-DC converter.

I. INTRODUCTION

DC-DC converters have been popular in many industrial applications, including power supplies and power drives. DC-DC converters have several different operation modes. And they are represented by nonlinear continuous-time dynamical equations which can exhibit nonlinear phenomena such as chaos, bifurcation, periodic behavior, and multiple equilibrium points or so [2], [4], [5], [7]. The input value is confined in the set {0, 1} or it is assumed that the input is within the interval [0, 1] and the state representing the inductor current should be equal to or larger than zero. Due to these nonlinearity and constraints on the input or state variables, it is difficult to design a high performance DC-DC converter control system. DC-DC converters are usually subject to parameter or load uncertainties that can significantly degrade control system performances. In order to solve these problems, various advanced DC-DC converter control design methods have been proposed in the literature. In [1], [10], [12], [19]–[21], [25], [28], [42], [45], [46], [48], the model predictive control approach has been applied for converters. In a model predictive control method, an optimal control input is constructed through optimizing a user-defined cost function which is usually selected as a weighted sum of the input and state variables. A model predictive control method can make a trade-off among several control performance criteria by setting the cost function as a weighted sum of the control performance criteria with appropriately chosen weighting factors. And, the model predictive control methods can easily consider the constraints on the input or state variables in the design procedure. The nonlinear control methods [14], [17], [30], [31], [34], [36] have also been developed under nonlinearity and constraints on the input or state variables. The sliding mode approach has been applied for robust DC-DC converter controller design problems in [29], [35], [37], [39], [47]. It should be noted that the sliding mode approach has been very effective to attack the robust feedback control design and analysis problem for uncertain nonlinear systems where the uncertainties can be lumped into unknown but bounded functions. The sliding mode control methods

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can improve the robustness against nonlinear uncertainties. The sliding mode control methods yield good performances such as fast transient response, insensitiveness to external disturbances, and invariance to internal parameter variations. On the other hand, several authors [3], [11], [16], [27], [32] have proposed intelligent control methods based on the fuzzy control theory which has been successfully applied for nonlinear system modeling and control. In [3], a Takagi-Sugeno fuzzy model for a boost converter has been derived and a global stabilizing fuzzy controller for the fuzzy model has been designed. The authors of [16] have proposed a fuzzy controller for a buck converter and they have shown that the fuzzy controller can be better than a proportional-integral-derivative (PID) controller via some experimental comparison. In [27] a PI-like fuzzy controller design method has been proposed. The authors of [32] have improved the PI-like fuzzy controller design procedure based on a conventional PI controller tuning method. The previous advanced DC-DC converter control design methods yield not only good transient responses but satisfactory steady-state performances. However, the PID-type control methods are widely adopted to control the DC-DC converters because they are simple, practical, effective, and easily tuned [14], [16], [23], [24], [32], [49].

On the other hand, the fractional order control system approach has been widely used to improve control system performances. And various fractional order PID-type control system analysis and design methods have been developed in the literature [6], [8], [9], [18], [22], [26], [33], [40], [41], [43], [44]. Motivated by the fact that a fractional order PID controller can outperform conventional integer order PID controllers, this paper considers the problem of designing a fractional order PID-type controller for a boost converter. Firstly, this paper characterizes integer order PID-type control gains which will make the closed-loop system transfer function approximately equal to a first order system with a unit DC gain and prescribed time constant τ. These gains are used for the PID gains of the fractional order PID-type controller. A systematic procedure to tune the fractional orders of the fractional order PID-type controller is given together with a descritized control algorithm for DSP implementation. The descritized control algorithm is implemented on a Texas Instruments TMS320F28335 DSP in order to verify the feasibility and practicality of the proposed method. Finally, experimental results are presented to verify that the proposed algorithm can be effectively applied to real-time control of a boost converter in response to load or input voltage variations. The fractional order control system design problem for converters has also been considered in [6], [8], [18]. However, only [6] has considered a boost converter and none of the previous results of [6], [8], [18] has given an explicit formula of PID gains.

In Section 2, a continuous-time boost converter dynamic equation is given and the design problem is formulated. Section 3 gives a parameterization of a class of integer order PID-type controllers enabling the closed-loop system transfer function approximately equal to a first order system with a unit DC gain and prescribed time constant τ. Section 3 also presents a procedure to determine the design parameters of fractional order PID-type controllers, together with a descritized algorithm for DSP implementation. Section 4 compares the experimental results performed under different operating conditions. Finally, Section 5 gives some concluding remarks.

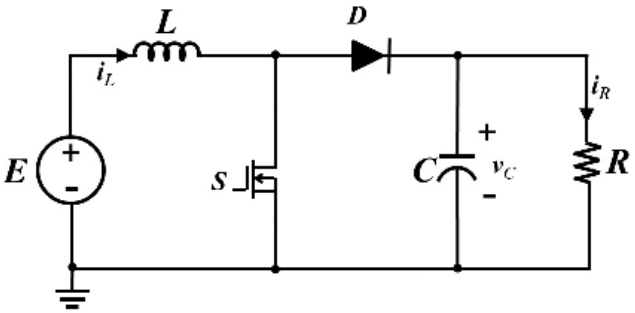

FIGURE 1. Topology of boost DC-DC converter.

II. MODEL DESCRIPTION AND PROBLEM FORMULATION

A boost DC-DC converter of Figure 1 can be represented by the following nonlinear continuous-time dynamic equation [3], [14], [35], [36]:

$$\begin{aligned}\dot{i}_L &= -\frac{1}{L}v_C\zeta + \frac{1}{L}v_C u + \frac{E}{L}\zeta \\ \dot{v}_C &= \frac{1}{C}i_L\zeta - \frac{1}{RC}v_C - \frac{1}{C}i_L u\end{aligned} \tag{1}$$

where i_L, i_R, v_C, u are the input inductor current, the output capacitor voltage, the output load resistor current, the discrete-valued control input confined in the set $\{0, 1\}$, and E, R, L, C represent the external source voltage value, the output load resistance, the inductance of the input circuit, the capacitance of the output filter, respectively. S and D of Figure 1 are an active controllable switch and a diode. The symbol ζ means the auxiliary binary variable defined by

$$\zeta = \begin{cases} 1, & \text{If } u = 1, \text{ or } u = 0 \text{ and } i_L > 0 \\ 0, & \text{If } u = 0 \text{ and } i_L = 0 \end{cases} \tag{2}$$

It should be noted that the converter operates in continuous conduction mode in case of $\zeta = 1$ whereas the converter is in discontinuous conduction mode when $\zeta = 0$. This paper will use the following assumptions:

A1: i_L and v_C are available.

A2: The inductor current can never be zero, i.e. the converter is in continuous conduction mode.

As [14], [34]–[36], we assume that the control input u is generated via a PWM device controlled by the duty ratio input function $d(\cdot)$ ranging on the interval [0, 1]. Then under A2 we can obtain the following approximate averaged model

$$\begin{aligned}\dot{i}_L &= \frac{1}{L}v_C(d-1) + \frac{E}{L} \\ \dot{v}_C &= -\frac{1}{C}i_L(d-1) - \frac{1}{RC}v_C\end{aligned}$$

The previous results of [14], [36] imply that for given desired reference output voltage V_r satisfying $V_r \geq E > 0$ the equilibrium points for the current i_L and the input d are uniquely determined as V_r^2/RE and $1 - E/V_r$, respectively. Along the similar line of [14], we introduce the following error terms

$$x_1 = \frac{V_r^2}{RE} - i_L, \quad x_2 = V_r - v_C,$$
$$x_3 = \int_0^t (V_r - v_C)ds, \quad v = d + \frac{E}{V_r} - 1 \tag{3}$$

then

$$\dot{x}_1 = -\dot{i}_L = -\frac{1}{L}(V_r - x_2)\left(v - \frac{E}{V_r}\right) - \frac{E}{L}$$
$$\dot{x}_2 = -\dot{v}_C = \frac{1}{C}\left(\frac{V_r^2}{RE} - x_1\right)\left(v - \frac{E}{V_r}\right) + \frac{1}{RC}(V_r - x_2)$$
$$\dot{x}_3 = x_2$$

After all, the following approximate averaged state space error model can be obtained

$$\dot{x} = Ax + Bv + \Delta Bv \tag{4}$$

where $x = [x_1, x_2, x_3]^T$ and

$$A = \begin{bmatrix} 0 & -\frac{E}{LV_r} & 0 \\ \frac{E}{CV_r} & -\frac{1}{RC} & 0 \\ 0 & 1 & 0 \end{bmatrix},$$
$$B = \begin{bmatrix} -\frac{V_r}{L} \\ \frac{V_r^2}{RCE} \\ 0 \end{bmatrix}, \quad \Delta B = \begin{bmatrix} \frac{x_2}{L} \\ -\frac{x_1}{C} \\ 0 \end{bmatrix} \tag{5}$$

The nonlinear model (4) can be linearized at the operating point $x = 0$ as follows:

$$\dot{x} = Ax + Bv \tag{6}$$

Since the Lyapunov's linearization method implies that the original nonlinear system is stable if the linearized system is stable [38], the previous converter control methods such as [14], [16], [23], [24], [32], [49] have used PID-type controllers similar to the following integer order control law which stabilizes the linearized boost DC-DC converter model (6)

$$v = -K_1x_1 - K_Pe - K_I\int_0^t ed\theta - K_D\dot{e} \tag{7}$$

where K_1, K_P, K_I, and K_D are the gains, and e is the output error, i.e. $e = v_C - V_r = y = x_2$. It should be noted that if x_2 is noisy then the control performance can be significantly degraded due to the derivative term $K_D\dot{x}_2$. Figure 2 shows a block diagram of a PID-type controller for a boost converter. The control law (7) can be rewritten as

$$v = -K_1x_1 - K_Px_2 - K_Ix_3 - K_D\dot{x}_2 \tag{8}$$

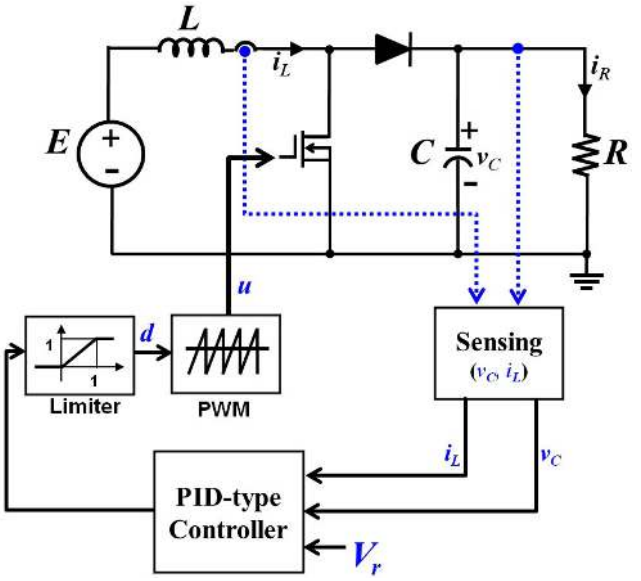

FIGURE 2. Block diagram of PID-type controller for boost DC-DC converter.

On the other hand, motivated by the fact that a fractional order PID controller can outperform conventional integer order PID controllers, this paper will consider the following fractional order PID-type control law

$$v = -K_1x_1 - K_Px_2 - K_ID^\mu x_3 - K_DD^\lambda x_2 \tag{9}$$

where $0 \leq \mu \leq 1$ and $0 \leq \lambda \leq 1$. The term D represents the continuous differential operator and thus D^μ means d^μ/dt^μ. It should be noted that the integer order PID-type controller (7) corresponds to the special case of the proposed fractional order PID-type control law with $\mu = 0$ and $\lambda = 1$. The proposed fractional order controller gives more flexibility to adjust the dynamic performances of the closed-loop control system.

After all, our design problem can be formulated as determining the design parameters λ, μ, K_1, K_P, K_I, and K_D.

III. MAIN RESULTS

A. CHARACTERIZATION OF INTEGER ORDER PID-TYPE CONTROL LAW

Consider the PID-type control law (7) with the following gains:

$$K_1 = k_1, \quad K_P = \frac{LE + k_1RCEV_r}{\tau RE^2 + LV_r^2},$$
$$K_I = \frac{RE^3 + 2k_1EV_r^3}{\tau RE^2V_r^2 + LV_r^4}, K_D = \frac{RLCE}{\tau RE^2 + LV_r^2} \tag{10}$$

where $k_1 > 0$ and $\tau > 0$. In order to derive the closed-loop transfer function, $G_{cl}(s)$, where s is the Laplace variable, let's decompose the PID-type control law (7) as

$$v = v_1 + v_2,$$
$$v_1 = -K_1x_1, \; v_2 = -K_Py - K_I\int_0^t yd\theta - K_D\dot{y} \tag{11}$$

then we can obtain the following equations

$$\begin{aligned} v_1 &= -k_1\, x_1 = -k_1[1,0,0]x, \\ \dot{x} &= (A - k_1\, B[1,0,0])x + Bv_2, \\ y &= x_2 = [0,1,0]x \end{aligned}$$

and thus we can obtain

$$\begin{aligned} sX(s) - x(0) &= (A - k_1\, B[1,0,0])X(s) + BV_2(s), \\ Y(s) &= [0,1,0]X(s) \end{aligned}$$

where A and B are defined in (5), and $X(s)$, $V_2(s)$, and $Y(s)$ are the Laplace transforms of x, v_2, and y, respectively. After all, we can obtain the transfer function from v_2 to y, $G_1(s)$, as follows:

$$\begin{aligned} G_1(s) &= [0,1,0](sI - A + k_1 B[1,0,0])^{-1}B \\ &= \frac{N_G(s)}{D_G(s)} \end{aligned} \tag{12}$$

The terms $N_G(s)$ and $D_G(s)$ are given by

$$\begin{aligned} N_G(s) &= RE^2V_r^2 - LV_r^4 s, \\ D_G(s) &= RLCEV_r^2 s^2 + (LEV_r^2 + k_1 RCEV_r^3)s \\ &\quad + RE^2 + 2k_1 EV_r^3 \end{aligned} \tag{13}$$

The equation (11) implies that $V_2(s) = H(s)(Y_r(s) - Y(s))$ where $Y_r(s)$ is the Laplace transforms of the reference input of $G_{cl}(s)$, and

$$H(s) = K_P + \frac{K_I}{s} + K_D s = \frac{N_H(s)}{D_H(s)} \tag{14}$$

where $N_H(s)$ and $D_H(s)$ are defined by

$$\begin{aligned} N_H(s) &= RLCEV_r^2 s^2 + (LEV_r^2 + k_1 RCEV_r^3)s \\ &\quad + RE^2 + 2k_1 EV_r^3, \\ D_H(s) &= (\tau RE^2 V_r^2 + LV_r^4)s \end{aligned} \tag{15}$$

It should be noted that $N_H(s) = D_G(s)$ leading to $G_1(s)H(s) = N_G(s)/D_H(s)$. By using (12), (14), and the following equation

$$\begin{aligned} Y(s) &= G_1(s)V_2(s) = G_1(s)H(s)[Y_r(s) - Y(s)] \\ &= \frac{N_G(s)}{D_H(s)}[Y_r(s) - Y(s)] \end{aligned} \tag{16}$$

we can show that $D_H(s)Y(s) = N_G(s)Y_r(s) - N_G(s)Y(s)$ leading to $\big[N_G(s) + D_H(s)\big]Y(s) = N_G(s)Y_r(s)$. After all, we can obtain $G_{cl}(s)$ as

$$\begin{aligned} G_{cl}(s) &= \frac{Y(s)}{Y_r(s)} = \frac{N_G(s)}{N_G(s) + D_H(s)} \\ &= \frac{RE^2V_r^2 - LV_r^4 s}{RE^2V_r^2 + \tau RE^2 V_r^2 s} = \frac{1 - {\omega_c}^{-1}s}{1 + \tau s} \end{aligned} \tag{17}$$

where $\omega_c = LV_r^2/RE^2$. It should be noted that usually $0 < L \ll 1 \ll R$ leading to

$$1 \ll \omega_c = \frac{RE^2}{LV_r^2} \tag{18}$$

Therefore, if we set the desired time constant τ as

$$\tau > \frac{1}{\omega_c} = \frac{LV_r^2}{RE^2} \tag{19}$$

then by the rules to draw a Bode plot straight-line approximation [15] the closed-loop transfer function $G_{cl}(s)$ of (17) can be approximated within the frequency range $\omega \in [0\ \omega_c)$ as the following first order system with a unit DC gain and prescribed time constant τ:

$$G_{cl}(s) \approx \frac{1}{\tau s + 1} \tag{20}$$

After all, the following theorem can be obtained:

Theorem 1: Consider the linearized boost DC-DC converter model (6) and the PID controller (8) with the gains (10). Then the closed-loop system dynamics is given by the stable first order system (17). Additionally, if the desired time constant τ satisfies (19) then the closed-loop system dynamics can be approximated by the first order system with a unit DC gain and prescribed time constant τ, (20), within the frequency range $\omega \in [0\ \omega_c)$.

B. FRACTIONAL ORDER PID-TYPE CONTROL LAW

Now, consider the fractional PID-type control law (9) with the gains of (10). It should be noted that fractional order control systems have been widely introduced to improve control system performances. Various fractional order PID-type control system analysis and synthesis methods have been developed in the literature and it has been shown that a fractional order PID controller can outperform conventional integer order PID controllers [6], [8], [9], [18], [22], [26], [33], [40], [41], [43], [44]. In the proposed control law (9), the term $K_D D^{\lambda} x_2 = K_D D^{\lambda} e$ can be rewritten as $K_D D^{\lambda-1}\dot{e}$ where $-1 \le \lambda - 1 \le 0$. The derivative term $K_D\dot{e}$ of the conventional integer order control law (7) is replaced with the $(\lambda - 1)$th integration term $K_D D^{\lambda-1}\dot{e}$ in the proposed control law. This implies that the proposed control law can reduce performance degradation due to the high frequency noise magnified by the derivative term $K_D\dot{e}$.

In order to practically implement a fractional order controller, we should obtain a finite dimensional approximation of the fractional order integral and differential operators. Several methods have been proposed to obtain finite dimensional approximations in frequency domain and in the time domain. In obtaining a practical approximation, we must consider the computation time and the amount of the required memory. Thus the approximation should have a minimal set of parameters [9], [40], [41], [43], [44]. In the recent papers [41], [43], [44], various approximation methods have been extensively compared via mathematical analysis and simulations. The previous works implies that if $\mu > 1$ the approximation methods can yield unsatisfactory characteristics but if $-1 \le \mu \le 1$ the following first order approximation gives desirable characteristics

$$D^{\mu} = \left(\frac{2}{T_s}\right)^{\mu} \frac{1 - \mu z^{-1}}{1 + \mu z^{-1}} \tag{21}$$

where z^{-1} is the unit delay operator and T_s is the sampling period. By using a higher order approximation instead of the above first order approximation, we may obtain better performances. However, we will consider the above first order approximation for efficient and simple implementation of the proposed fractional order PID-type control law. Denote $D^{\mu}x_3(k)$, $D^{\lambda}x_2(k)$, and $x_3(k) = D^{-1}x_2(k)$ as $D^{\mu}x_3(k) = a(k)$, $D^{\lambda}x_2(k) = b(k)$, and $x_3(k) = D^{-1}x_2(k)$ at the sampling instant kT_s, respectively. Then the above approximation (21) implies that

$$a(k) + \mu a(k-1) = \left(\frac{2}{T_s}\right)^{\mu} [x_3(k) - \mu x_3(k-1)]$$
$$b(k) + \lambda b(k-1) = \left(\frac{2}{T_s}\right)^{\lambda} [x_2(k) - \lambda x_2(k-1)]$$
$$x_3(k) - x_3(k-1) = \frac{T_s}{2}[x_2(k) + x_2(k-1)]$$

After all, the fractional order differential value $D^{\mu}x_3$ at the sampling instant kT_s is computed by using the following update equation:

$$a(k) = \left(\frac{2}{T_s}\right)^{\mu} [x_3(k) - \mu x_3(k-1)] - \mu a(k-1) \quad (22)$$

the value $D^{\lambda}x_2(k)$ is constructed by

$$b(k) = \left(\frac{2}{T_s}\right)^{\lambda} [x_2(k) - \lambda x_2(k-1)] - \lambda b(k-1) \quad (23)$$

and the state variable $x_3(k)$ is updated by

$$x_3(k) = \frac{T_s}{2}[x_2(k) + x_2(k-1)] + x_3(k-1) \quad (24)$$

Using the above update equations the fractional order PID-type control law can be computed by

$$v(k) = -K_1 x_1(k) - K_P x_2(k) - K_I a(k) - K_D b(k) \quad (25)$$

The control performances of the proposed fractional order PID-type controller (9) with the gains (10) depend heavily on the values of μ and λ. Because the integral performance index $J(\mu, \lambda) = \int_0^{t_f} e^2\, dt$ is the most popular one to compare the control performances of PID controllers where t_f is the final time, this paper considers the integral performance index J to find the optimal orders μ and λ. The problem of finding the optimal orders μ and λ minimizing J is difficult to solve analytically, however we can easily find a minimum solution by the following simple direct search algorithm:

Tuning Algorithm of (μ, λ)

TA1: Set $\mu_0^* = 0$, $\lambda_0^* = 1$, and $k = 0$.

TA2: Evaluate the integral performance index $J_k^* = J(\mu_k^*, \lambda_k^*) = \int_0^{t_f} e^2\, dt$ with μ_k^*, λ_k^*, and the gains of (10).

TA3: Find an optimal $\mu^* \in [0, 1]$ guaranteeing $J(\mu^*, \lambda_k^*) \le J_k^* = J(\mu_k^*, \lambda_k^*)$ by iterating μ for the given fixed μ_k^*, λ_k^*, and the gains of (10). Set $\mu_{k+1}^* = \mu^*$.

TA4: Find an optimal $\lambda^* \in [0, 1]$ guaranteeing $J(\mu_{k+1}^*, \lambda^*) \le J(\mu_{k+1}^*, \lambda_k^*)$ by iterating λ for the given fixed μ_{k+1}^*, λ_k^*, and the gains of (10). Set $\lambda_{k+1}^* = \lambda^*$.

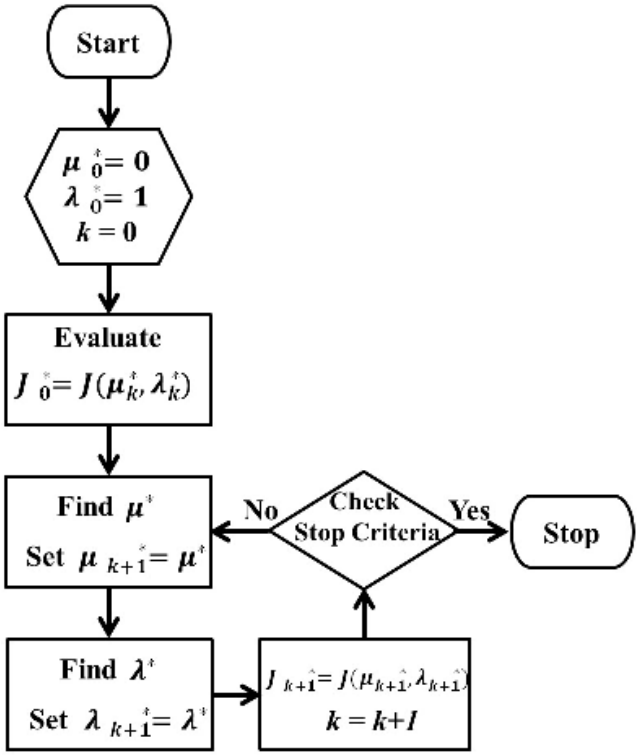

FIGURE 3. Flow chart of tuning algorithm of (μ, λ).

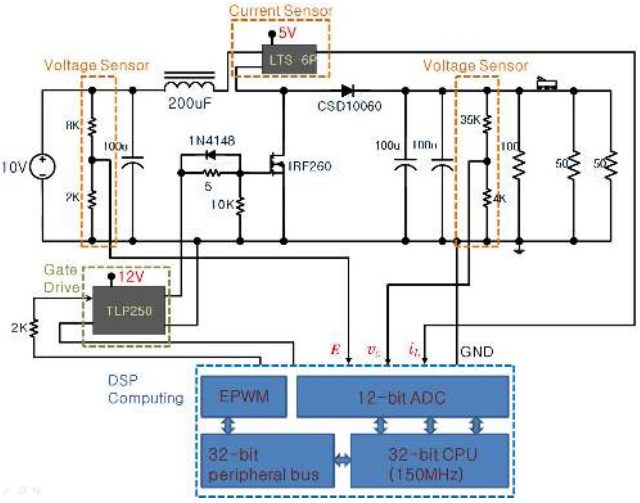

FIGURE 4. Schematic diagram of experimental testbed.

TA5: Set $J_{k+1}^* = J(\mu_{k+1}^*, \lambda_{k+1}^*)$ and $k = k + 1$.

TA6: If stop criteria hold then stop, otherwise go to TA3.

Remark 1: Figure 3 shows a flow chart of the *Tuning Algorithm of* (μ, λ). The following stop criteria can be used for the *Tuning Algorithm of* (μ, λ): The maximum iteration number k_{max} is reached; J_k^* converges or becomes smaller than a prescribed value.

Remark 2: Our results can be summarized as the following design procedure:

Step1: Set the initial gain $k_1 > 0$ and time constant $\tau > 1/\omega_c$.

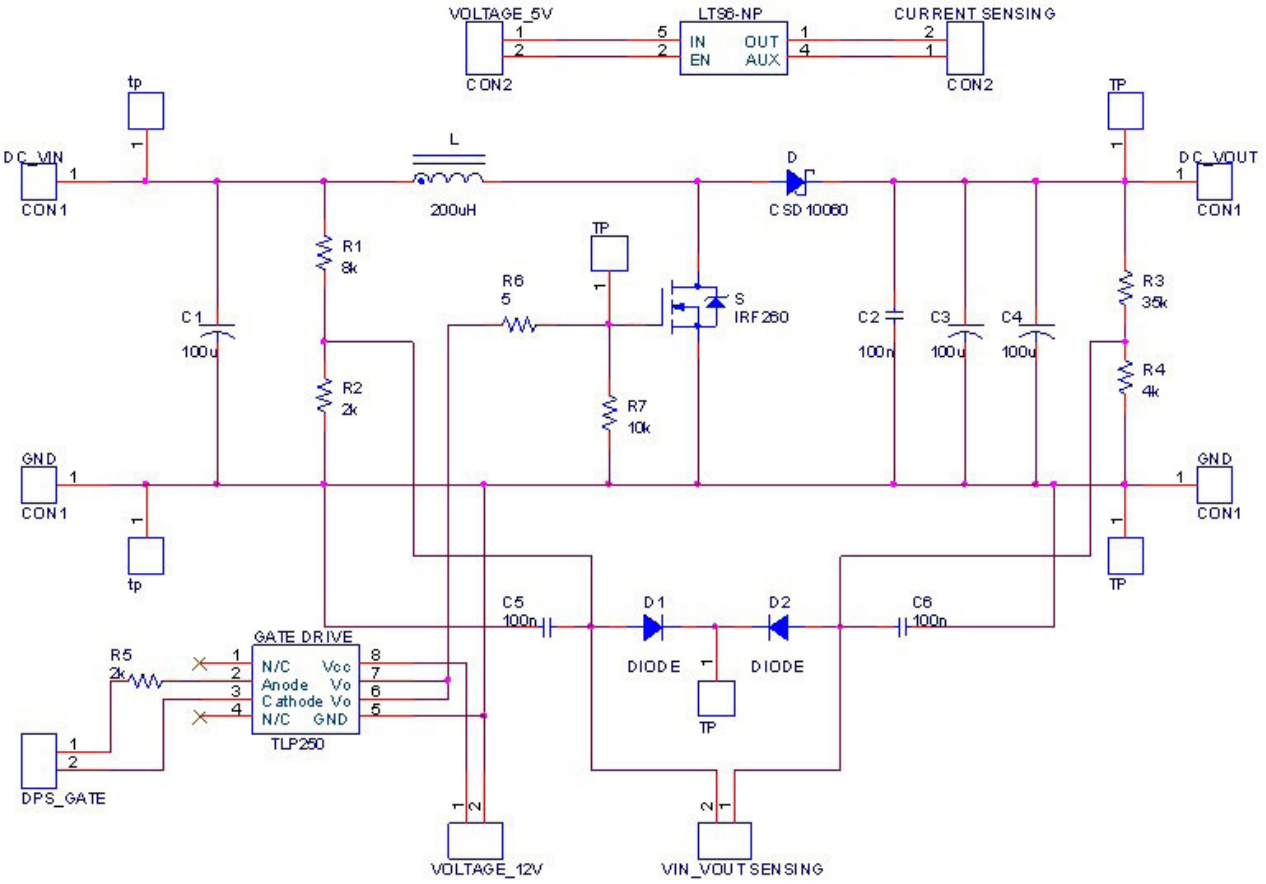

FIGURE 5. Power stage circuit schematic diagram of boost DC-DC converter.

Step2: Compute the PID gains K_P, K_I, and K_D by using (10).
Step3: Find optimal orders μ and λ by using the *Tuning Algorithm of* (μ, λ).
Step4: If the control performances are unsatisfactory then select alternative k_1 and τ and go to Step2. Otherwise stop.

Remark 3: From the fact that the integer order PID-type controller corresponds to the special case of the proposed fractional order PID-type control law (25) with $\mu = 0$ and $\lambda = 1$, we can easily see that the integer order PID-type controller requires 6 multiplications and 7 additions whereas the proposed fractional order PID-type control law (25) requires 9 multiplications and 9 additions, thus the total execution time increase is 3 multiplications and 2 additions. This increase is not serious considering traditional powerful and fast DSPs. The experimental study given below also verifies that the total execution time increase is small compared to the sampling period.

Remark 4: In order to design the integer order PID-type controller (7), the four design parameters K_1, K_P, K_I, and K_P should be selected within the conventional frameworks such as [14] while only the two design parameters K_1 and τ have to be specified within our framework. The design parameters of the proposed fractional order controller (25) are K_1, τ, μ, and λ. Thus, the number of the design parameters of the proposed fractional order controller is 4. In the conventional integer order PID controllers, the derivative term $\dot{e}(k) = \dot{x}_2(k) = b(k)$ at the sampling instant kT_s is usually computed by using the following update equation

$$b(k) = \frac{2}{T_s + 2\epsilon}[x_2(k) - x_2(k-1)] - \frac{T_s - 2\epsilon}{T_s + 2\epsilon}b(k-1)$$

or

$$b(k) = \frac{1}{T_s + \epsilon}[x_2(k) - x_2(k-1)] + \frac{\epsilon}{T_s + \epsilon}b(k-1)$$

where $\epsilon \geq 0$ is a filter time constant which is tuned to reduce performance degradation due to the high frequency noise magnified by the derivative term. This implies that the discretized conventional integer order PID-type control design methods may require to select the parameter value ϵ besides K_1, K_P, K_I, and K_P.

Remark 5: Denote $H_F(s)$ and $\Delta(s)$ as

$$H_F(s) = K_P + K_I s^{\mu-1} + K_D s^{\lambda} \tag{26}$$

$$\begin{aligned}\Delta(s) &= [H_F(s) - H(s)]/H(s) \\ &= [K_I(s^{\mu-1} - s^{-1}) + K_D(s^{\lambda} - s)]/H(s)\end{aligned} \tag{27}$$

FIGURE 6. Experimental testbed.

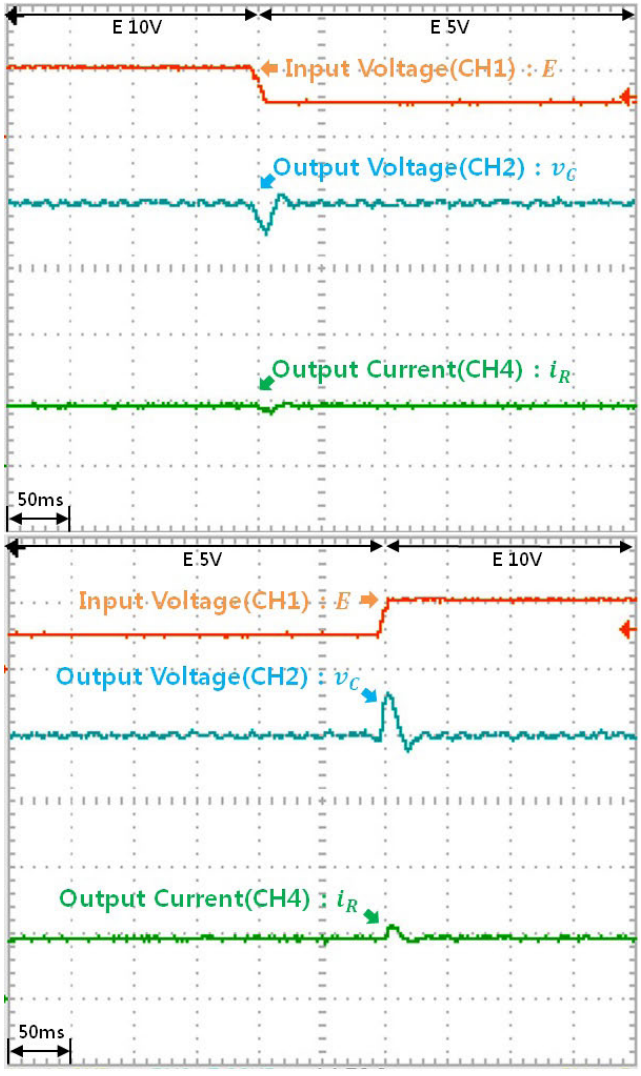

FIGURE 7. Experimental results by proposed method under C1. (Top)10[V] → 5[V]. (Bottom)5[V] → 10[V].

where $H(s)$ is defined in (14). Then by using (17) and the small gain theorem [13], we can show that the linearized boost DC-DC converter model (6) with the proposed fractional order PID-type controller (9) is stable if the following

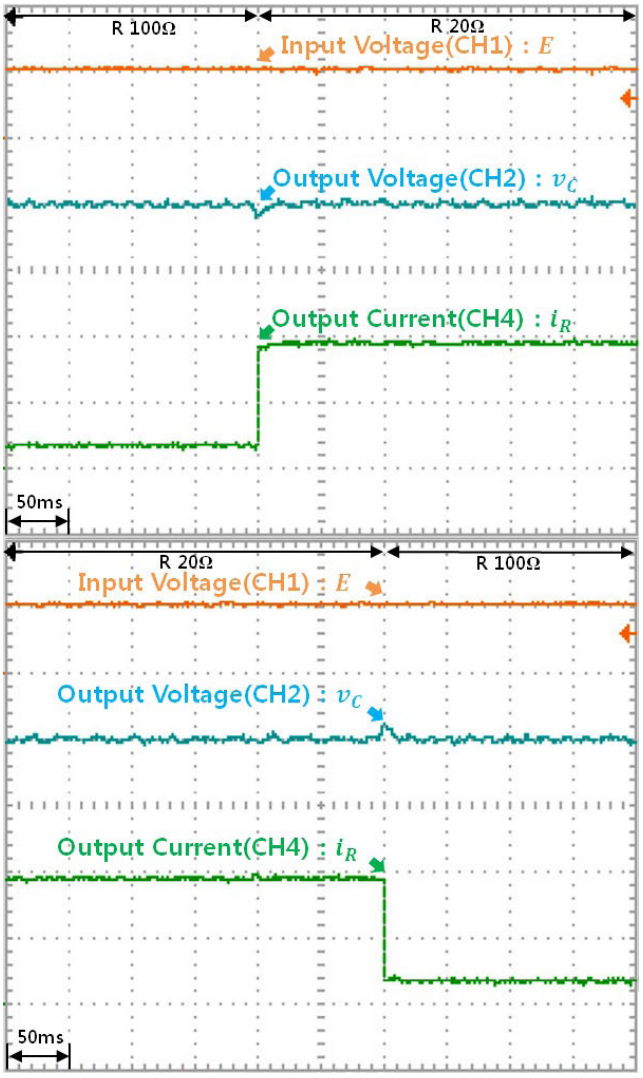

FIGURE 8. Experimental results by proposed method under C2. (Top)100[Ω] → 20[Ω]. (Bottom)20[Ω] → 100[Ω].

condition is satisfied

$$\|\Delta(j\omega)\| < \frac{1}{\max \|G_{cl}(j\omega)\|} \tag{28}$$

for all frequency range. We can see that

$$\|G_{cl}(j\omega)\| = \sqrt{\frac{1+\omega_c^{-2}\omega^2}{1+\tau^2\omega^2}} \leq \max(1, \frac{1}{\tau\omega_c}) \tag{29}$$

which implies that the stability condition (28) can be rewritten as

$$\|\Delta(j\omega)\| < \min(1, \tau\omega_c) \tag{30}$$

For the case of $\tau > 1/\omega_c$, the stability condition (30) can be reduced to $\|\Delta(j\omega)\| < 1$. The stability condition (30) is only a sufficient one, thus the closed-loop control system can be stable even (30) does not hold. The stability condition (30) is trivially satisfied in the case of the integer order PID-type controller (7) because $\Delta(s) = 0$. We can see that if the nonnegative design parameters μ and λ are chosen as $\mu \ll 1$

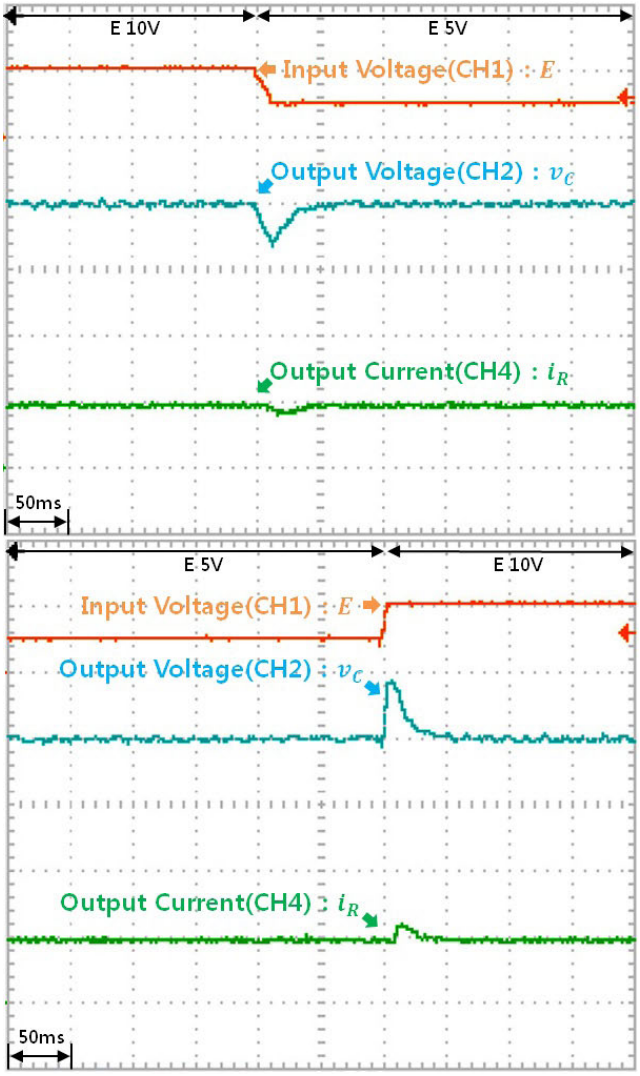

FIGURE 9. Experimental results by conventional method under C1. (Top)10[V] → 5[V]. (Bottom)5[V] → 10[V].

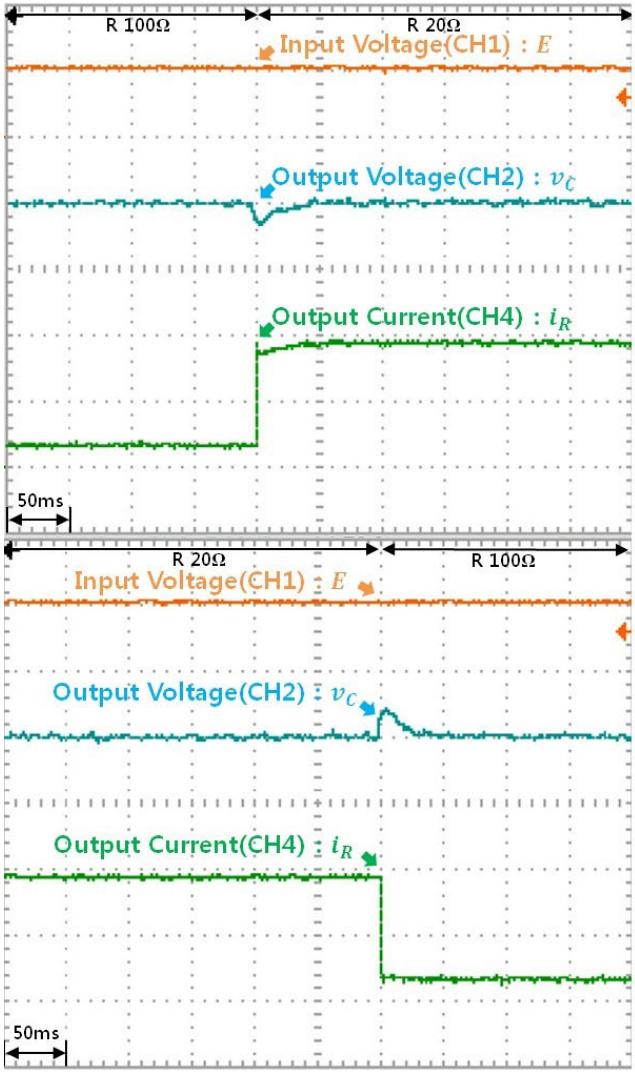

FIGURE 10. Experimental results by conventional method under C2. (Top)100[Ω] → 20[Ω]. (Bottom)20[Ω] → 100[Ω].

and $0 \leq 1-\lambda \ll 1$, then the above stability condition (30) can be easily satisfied.

IV. EXPERIMENTAL VERIFICATION

For experimental study, we consider a boost converter with $L = 200[\mu H]$ and $C = 200[\mu F]$. We assume that the nominal output load resistance and external source voltage are $R_0 = 100[\Omega]$ and $E_0 = 10[V]$, respectively. The sampling frequency f_s is set as $f_s = 1/T_s = 50[kHz]$. The parameter values used for experimental study are summarized in Table 1.

By using (4), $R_0 = 100[\Omega]$, $E_0 = 10[V]$, and the boost converter parameters given in Table I, we can derive the following boost converter model

$$\dot{z} = \begin{bmatrix} 0 & -2500 & 0 \\ 2500 & -50 & 0 \\ 0 & 1 & 0 \end{bmatrix} z + \begin{bmatrix} \frac{v_c}{L} \\ -\frac{i_L}{C} \\ 0 \end{bmatrix} v \qquad (31)$$

TABLE 1. Boost converter parameters for simulation and experiment.

External source voltage (E)	5 - 10 [V]
Current sensor	LTS 6-NP
Sampling frequency (f_s)	50[kHz]
Load resistance (R)	100 [Ω]
Output capacitance (C)	200 [μF]
Input inductance (L)	200 [μH]
Output diode (D)	CSD10060
Main switch (S)	IRFP26N60
Digital Signal Processor (DSP)	TMS320F28335

In order to verify the practical feasibility and effectiveness of the proposed method, we consider the following two cases C1-2:

C1: The external source voltage E changes from 10[V] → 5[V] → 10[V] while the output load resistor R and the reference voltage V_r are kept constant at the nominal values $R = 100[\Omega]$ and $V_r = 20[V]$, respectively.

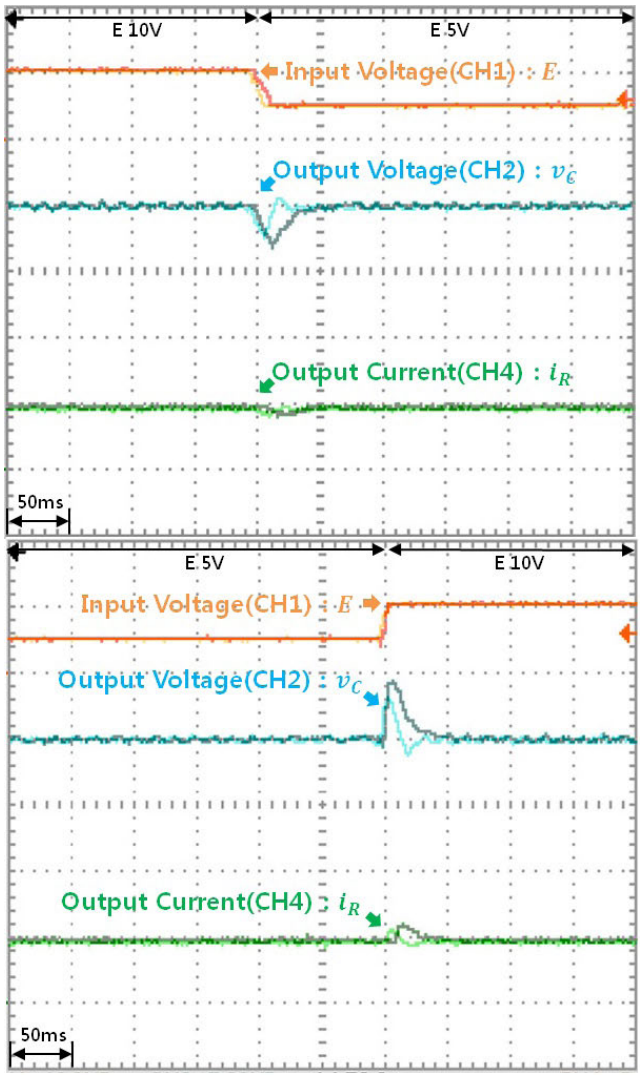

FIGURE 11. Experimental results under C1. (Top)10[V] → 5[V]. (Bottom)5[V] → 10[V].

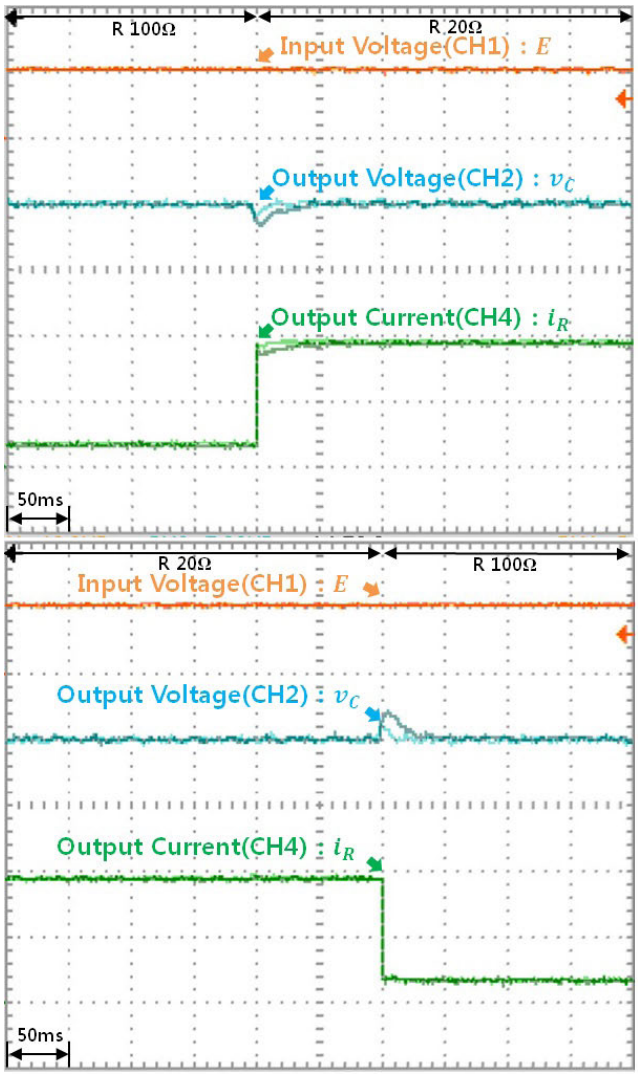

FIGURE 12. Experimental results C2. (Top)100[Ω] → 20[Ω]. (Bottom)20[Ω] → 100[Ω].

C2: The output load resistor R changes from 100[Ω] → 20[Ω] → 100[Ω] while the external source voltage E and the reference voltage V_r hold constant at the nominal values $E = 10[V]$ and $V_r = 20[V]$, respectively.

A Texas Instruments TMS320F28335 floating-point DSP with the clock speed of 150[MHz] is used to implement the proposed fractional order PID-type control algorithm. A 12-bit ADC module with a built-in sample-and-hold circuit is used for analog-to-digital conversion of the input inductor current i_L and the output capacitor voltage v_C. A Tektronix TDS5140B digital oscilloscope is employed to measure and plot the input voltage E, the output capacitor voltage v_C, and the output load resistor current i_R. Figure 4 shows the schematic diagram of the experimental testbed. Figure 5 depicts the circuit scheme of the power stage used for experimental study. Figure 6 illustrates the experimental setup. We assume that the desired time constant τ is 0.001 leading to a 3-dB bandwidth of 1000, a rise time of $2.2\tau = 0.0022$, and a 2% settling time of $4\tau = 0.004$. By referring to the method presented in the previous section, we find optimal $\lambda = 0.88$ and $\mu = 0.06$, and we obtain the proposed fractional order PID-type control law as follows:

$$v(k) = -0.1x_1(k) - 0.0399x_2(k) - 28.770a(k) - 3.968 \times 10^{-6}b(k) \quad (32)$$

where $a(k)$ and $b(k)$ are updated by the following recursive equations

$$a(k) = \left(\frac{2}{T_s}\right)^{0.06} [x_3(k) - 0.06x_3(k-1)] - 0.06a(k-1) \quad (33)$$

$$b(k) = \left(\frac{2}{T_s}\right)^{0.88} [x_2(k) - 0.88x_2(k-1)] - 0.88b(k-1) \quad (34)$$

Under the clock speed of 150[MHz], the maximum, minimum, and average calculation times of the above proposed fractional order control law $v(k)$ of (32) are 1.26 μsec, 0.86 μsec, and 1.06 μsec, respectively. Figure 7 shows the time trajectories of the external source voltage E, the output capacitor voltage v_C, and the output load resistor current i_R subject to E changing abruptly from $10[V] \rightarrow 5[V] \rightarrow 10[V]$ with $R = 100[\Omega]$ and $V_r = 20[V]$. Figure 8 illustrates the histories of E, v_C, and i_R when the output load resistor R changes abruptly from $100[\Omega] \rightarrow 20[\Omega] \rightarrow 100[\Omega]$ while E and V_r hold constant at $E = 10[V]$ and $V_r = 20[V]$.

By setting $\mu = 0$ and $\lambda = 1$, a conventional integer order PID-type controller can be obtained as follows:

$$v(k) = -0.1x_1(k) - 0.0399x_2(k) - 28.770x_3(k) - 3.968 \times 10^{-6}b(k) \quad (35)$$

where $b(k)$ are updated by the following recursive equations

$$b(k) = \frac{2}{T_s}[x_2(k) - x_2(k-1)] - b(k-1) \quad (36)$$

The maximum, minimum, and average calculation times of the above conventional integer order control law $v(k)$ of (35) are 0.98 μsec, 0.58 μsec, and 0.78 μsec, respectively. Figures 9 and 10 show the time trajectories by the above conventional integer order PID-type controller (35). Figure 9 illuminates the time trajectories of the external source voltage E, the output capacitor voltage v_C, and the output load resistor current i_R subject to E changing abruptly from $10[V] \rightarrow 5[V] \rightarrow 10[V]$ with $R = 100[\Omega]$ and $V_r = 20[V]$. Figure 10 depicts the histories of E, v_C, and i_R when the output load resistor R changes abruptly from $100[\Omega] \rightarrow 20[\Omega] \rightarrow 100[\Omega]$ while E and V_r hold constant at $E = 10[V]$ and $V_r = 20[V]$. In order to highlight the differences of the control performances, Figures 7 and 9 are superimposed into Figure 11, and Figures 8 and 10 are also superimposed into Figure 12. Figures 7 through 12 imply that the proposed controller achieves 25 % reduction in maximum output voltage error, 25 % reduction in maximum output current error, and 25 % reduction in recovery time for the case C1 compared to the conventional integer order controller (35). The proposed controller achieves 50 % reduction in maximum output voltage error, and about 70 % reduction in recovery time for the case C2 compared to the conventional controller. The increase in average calculation time caused by using the proposed fractional order PID-type controller instead of the conventional controller is 0.36 μsec. The maximum and average calculation times of the proposed fractional order PID-type controller are 1.26 μsec and 1.06 μsec. These are much less than the sampling period 20 μsec. Thus the execution time cannot be a constraint when the proposed controller is implemented on a DSP. And the experimental results given in Figures 7 to 12 imply that the proposed fractional order PID-type controller may require a slight increase in calculation time but it gives a much faster recovery time, less overshoot, smaller maximum output error compared to the conventional controller.

V. CONCLUSION

We proposed a fractional order PID-type control algorithm for a boost DC-DC converter. We also gave simulation and experimental results to verify the effectiveness and practicality of the proposed control system under several operating conditions. Via experimental study we verified that the proposed method can give a less overshoot and faster recovery time compared to the conventional integer order controller under abrupt load or input voltage variations. Finally, we remark that fractional order PID-type controllers for buck converters and buck-boost converters can also be designed using formulations similar to that provided in this paper.

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