Digital Microfluidic Biochips: Recent Research and Emerging Challenges

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ABSTRACT

Microfluidic biochips are replacing the conventional biochemical analyzers, and are able to integrate on-chip all the basic functions for biochemical analysis. The "digital" microfluidic biochips (DMFBs) are manipulating liquids not as a continuous flow, but as discrete droplets on a two-dimensional array of electrodes. Basic microfluidic operations, such as mixing and dilution, are performed on the array, by routing the corresponding droplets on a series of electrodes. The challenges facing biochips are similar to those faced by microelectronics some decades ago. To meet the challenges of increasing design complexity, computer-aided-design (CAD) tools are being developed for DMFBs. This paper provides an overview of DMFBs and describes emerging CAD tools for the automated synthesis and optimization of DMFB designs, from fluidic-level synthesis and chip-level design to testing. Design automations are expected to alleviate the burden of manual optimization of bioassays, time-consuming chip designs, and costly testing and maintenance procedures. With the assistance of CAD tools, users can concentrate on the development and abstraction of nanoscale bioassays while leaving chip optimization and implementation details to CAD tools.

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General Terms: Algorithms, Performance, Design, Reliability

Keywords: Microfluidics, biochips, design automation

1. INTRODUCTION

Microfluidic-based biochips are soon revolutionizing clinical diagnostics and many biochemical laboratory procedures due to their advantages of automation, cost reduction, portability, and efficiency [32]. Conventional technology depends on the manipulation of continuous liquid flow through microfabricated channels. However, actuation of flow is implemented with external assistance of micro-pump and micro-valve, which are complex and cumbersome. Moreover, permanently-etched channels greatly restrict the feasibility and versatility. Therefore, microfluidic research is witnessing a paradigm shift from the continuous-flow-based architecture to *droplet*-based architecture or, in particular, the *digital microfluidic biochip* (DMFB) [6, 12, 19, 32].

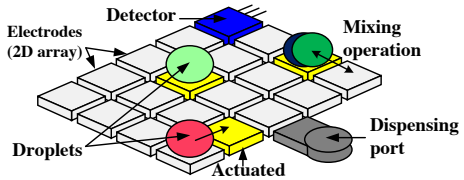

Figure 1: The schematic view of a DMFB.

Generally, a DMFB consists of a two-dimensional (2D) electrode array and peripheral devices such as optical detector and dispensing port, as schematically shown in Figure 1 [12, 32]. The sample carriers, *droplets*, being miniaturized and *discretized* liquids, are controlled by underlying electrodes using electrical actuations (i.e., a principle called electrowetting-on-dielectric or EWOD) [25]. By assigning time-varying voltage values to turn on/off electrodes, droplets can be moved around the entire 2D array to perform fundamental operations (e.g., dispensing and mixing) [28]. These operations are carried out in a *reconfigurable* manner due to their flexibility in area and time domain [6]. Compared with continuous-flow-based biochips, DMFBs offer various advantages including more flexible control mechanism and higher throughput and sensitivity as well as lower sample/reagent volume consumption.

Due to these advantages, DMFBs have attracted many efforts being devoted to marketplace demands, ranging from healthcare, environmental sensing, and point-of-care-testing applications. As reported in Figure 2, the global market value for biochip products was estimated to be $2.6 billion in 2009, but it is expected to increase to nearly $6 billion in 2014, for a 5-year high compound-annual-growth-rate (CAGR) of 17.7% [2]. Continuing growth of various applications have dramatically complicated chip/system integration and design complexity [7, 12], rendering traditional manual designs infeasible, especially under time-to-market constraints. Hence, it is necessary to develop high-quality computer-aided-design (CAD) tools for efficient design automation. Design automations are expected to reduce the burden associated with manual optimization of bioassays, time-consuming chip designs, and costly testing and maintenance procedures. Moreover, the assistance of CAD tools will facilitate the integration of fluidic components with a microelectronic component in next-generation system-on-chips (SOCs) [6, 7, 12, 32].

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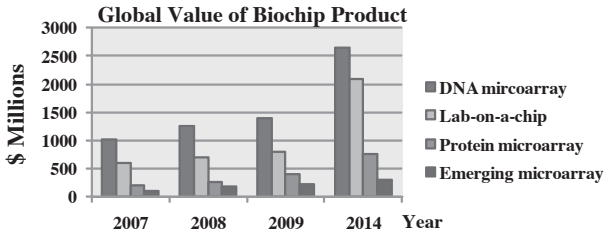


Figure 2: Global-value estimate of biochip products.

In this paper, we provide a survey of recent research and emerging challenges in design and optimization for DMFBs. We show how CAD approaches can be used to automate and optimize the design of DMFBs in fluidic domain and chip (i.e., hardware) domain. The goal in this paper is to give a holistic perspective on top-down system-level CAD tools, and discuss several associated combinatorial and geometric optimization problems. Having these CAD tools, users and designers will be able to describe bioassays at a high-level of abstraction. CAD tools will generate an optimized schedule of bioassay operations, a suitable chip layout for best fluidic performance, and well-planed signal connections for low-cost manufacturing process. Therefore, biochip users and designers can concentrate on innovations at the application level, leaving implementation details to CAD tools. These CAD tools will reduce human effort and enable high-volume production. The remainder of the paper is organized as follows: Section 2 reviews the typical CAD flow of DMFB that consists of fluidic-level synthesis and chip-level design. Section 3 and section 4 discuss the related optimization problems and CAD approaches in fluidic-level synthesis and chip-level design, respectively. Section 5 examines defects, fault models, and testing techniques.

Section 6 describes the design challenges and several open problems that remain to be tackled in the future. Finally, conclusion is drawn in Section 7.

2. CAD FLOW OF DMFBS

A regular CAD flow of DMFBs consists of two stages, *fluidic-level synthesis* and *chip-level design* [12], as illustrated in Figure 3. Fluidic-level synthesis describes an automated scheduling of assays and a generation of a mapping of assay operations to resources in a time-multiplexed manner. Fluidic-level synthesis is divided into two major phases, referred to as architectural-level synthesis (i.e., high-level synthesis) and geometry-level synthesis (i.e., physical design) [29, 30, 32]. Optimizations here are guaranteeing high-performance fluidic behaviors as well as a suitable chip layout. On the other hand, the goal in chip-level design is determining the control-signal plan and electrical connections for the electrodes to execute the synthesized result. Chip-level design consists of two steps of electrode addressing followed by wire routing [12, 16]. This design stage is receiving increasing attention in recent years as it dominates the manufacturing complexity and fabrication cost of a DMFB.

In the following sections, we provide a progression of the related CAD problems and research on fluidic-level synthesis and chip-level design, respectively.

3. FLUIDIC-LEVEL SYNTHESIS

In this section, we discuss automated fluidic-level synthesis.

Hierarchical and cell-based design techniques from modern very-large-scale-integration (VLSI) automation has been utilized for architectural-level synthesis and geometry-level synthesis.

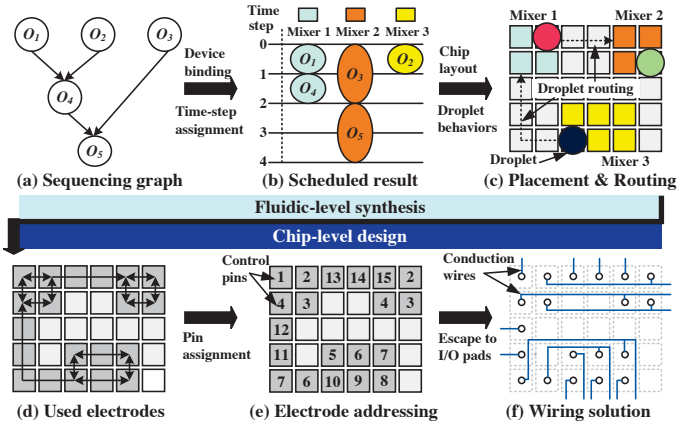


Figure 3: Regular CAD flow of DMFBs consists of two stages of fluidic-level synthesis followed by chip-level design.

3.1 Architectural-Level Synthesis

An assay is typically abstracted as a model of sequencing graph (see Figure 3(a)). The sequencing graph is directed, acyclic and polar (i.e., there is a source node without predecessors and a sink node without successors). Each node represents a specific assay operation (e.g., mixing, generation, and detection), while a directed edge indicates the dependency between two operations.

In architectural-level synthesis, both the resource-binding problem and the scheduling problem are addressed to generate a structural view of a biochip design. As analogous to high-level synthesis for integrated circuits, resource binding determines a mapping from assay operations to available functional resources. There may be several types of resources for any given assay operation. For example, a 2×2 mixer and a 2×3 mixer can be used for a mixing operation but with different mixing times. A resource binding procedure is applied to determine the selections with a minimized assay execution time. Once resource binding is carried out, the execution time for each assay operation can be roughly determined. In other words, scheduling of the start times and stop times of all assay operations is determined, subject to the precedence constraints by the given sequencing graph, as illustrated in Figure 3(b).

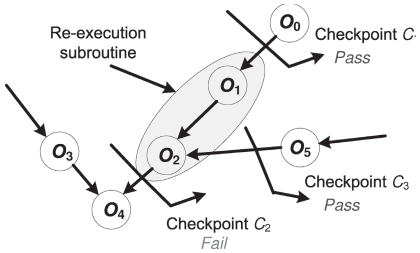


Figure 4: Checkpoint insertion and re-execution subroutine [47].

Several algorithms, such as tabu-search based synthesis [23] and ILP (integer-linear-programming) based synthesis [29], are proposed to handle the basic architectural-level synthesis of DMFBs. In addition, for some complex biomedical applications such as clinical diagnostics, it is necessary to verify the correctness of on-chip

fluidic operations. The status of an assay can be monitored by examining the volume of the droplet, sample concentration, or detector readout. If an error occurs during the execution of an assay, e.g., an unexpected volume of an intermediate droplet, the assay outcomes will be misleaded. Therefore, it is important to detect such errors as early as possible and re-execute the fluidic operations to obtain correct assay outcomes. Considering this issue, a control-path based design is recently integrated to the architectural-level synthesis of DMFBs [47]. In [47], they first calculate the possibilities of errors for each operation via an error-propagation estimates, and then insert a check point consisting of a storing operation and a error detection to the sequencing graph, as shown in Figure 4. A simulated-annealing (SA) method is also proposed to optimize the execution time used for error recovery.

3.2 Geometry-Level Synthesis

A key problem in the geometry-level (i.e., physical-level) synthesis of DMFBs is the placement of fluidic modules such as different types of mixers and detection units. The major goal of the placement is to find the actual locations of different fluidic modules corresponding to different time intervals. Since DMFBs enable dynamic reconfiguration of the microfluidic array during run-time, they allow the placement of different modules on the same location during different time intervals [31, 33]. Therefore, the placement of modules can be modeled as a three-dimensional (3D) packing problem. Each fluidic module represents a 3D box, the base of which denotes the rectangular area of the module and the height denotes the time span of its execution, see Figure 5 for an example.

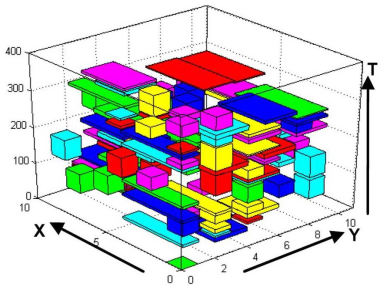


Figure 5: 3D packing diagram of a placement result.

The most important optimization objective of the placement problem is the minimization of chip area. Since solutions of the placement problem can provide the designers with guidelines on the chip size to be manufactured, area minimization frees up more unit cells for other fluidic functions such as sample preparation and collection. During the placement, some performance constraints including the upper limit on assay completion time and maximum allowable chip array should be satisfied, in order that the system reliability and integrity inherent from the architectural-level synthesis can be well-maintained. Besides, since the increasing assay density and area of DMFBs may potentially reduce yield, a critical issue of *fault tolerance* is also considered to avoid defective cells due to fabrication. Since we need time to ramp up the yield of DMFBs, it is desirable to perform a bioassay on a DMFB with the existence of defects (i.e., fabrication faults). How to integrate the defect tolerant issue into the placement problem with correct fluidic functions has become an important issue. To handle such a problem, some algorithms, such as SA-based optimization [30, 33] and T-tree-based placement formulation [44], are presented in recent years. Besides, a work in [4] further considers the control-path based synthesis with placement to minimize the operation variability.

Droplet routing on DMFBs is a key design issue in the physical-level synthesis, which schedules the movement of each droplet in a time-multiplexed manner. The major goal of droplet routing is constructing the connections between modules, and between modules and I/O ports (i.e., on-chip reservoirs) within different time intervals. This physical synthesis is one of the most critical design challenges due to design complexity as well as large impacts on correct assay performance. Since a microfluidic array is reconfigured dynamically at run-time, the inherent reconfigurability allows different droplet routes to share cells on the micorfluidic array during different time intervals. Besides, a series of 2D placement configurations of fluidic modules in different time intervals are obtained in the placement stage. Therefore, droplet routing is decomposed into a series of *sub-problems*, which establishes the connections for pre-placed fluidic modules between successive sub-problems. We can thus obtain a complete droplet routing solution by solving these sub-problems sequentially. In this sense, the routes on the microfluidic array can be viewed as *virtual routes* in a 3D manner, which make the droplet routing problem different from the classical wire routing in VLSI designs [34]. Systematic droplet routing methods have therefore been developed to minimize the number of cells used for droplet routing for better fault, while satisfying constraints imposed by performance goals and fluidic properties [13, 15, 34, 45, 49].

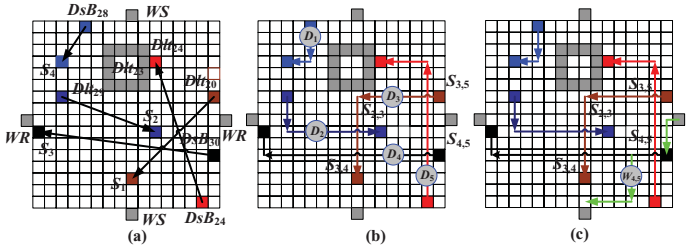


Figure 6: Synchronization of washing operations and droplet routing [48]. (a) A droplet routing result. (b) Washing operations on contaminated spot $S_{4,5}$.

Cross-contamination is likely to occur when multiple droplet routes intersect or overlap with each other. At the intersection site of two droplet routes, a droplet that arrives at a later clock cycle can be contaminated by the residue left behind by another droplet that passed through at an earlier clock cycle. To avoid assay execution error, washing operations (i.e., wash-droplet routing) are introduced to clean the contamination left on the surface [46, 14, 48]. In [46], a disjoint route algorithm is applied to avoid the overlap between different routes, with insertions of washing operations between successive droplet routing subproblems. In [14], a network-flow based algorithm is utilized to formulate simultaneous droplet routing and washing operations. The work in [48], synchronizes wash-droplet routing with sample/reagent droplet-routing steps by controlling the arrival order of droplets at cross-contamination sites. Figure 6 shows a synchronization result of washing operations.

Recently, the work in [21] considers the cross-contamination avoidance in earlier design stage of placement. As illustrate in Figure 7, it generates a placement topology with a minimized number of crossing routing paths by using a bipartite matching formulation. Therefore, the efforts spent on routing wash droplets can be minimized.

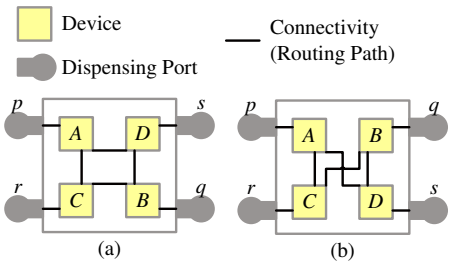


Figure 7: Different placement topology leads to different numbers of crossing routing paths [21]. (a) Zero crossing routing path. (b) One crossing routing path.

4. CHIP-LEVEL DESIGN

In this section, we discuss chip-level design, which consists of electrode addressing and wire routing [1], as shown in Figure 3(d)-(f). We first show the EWOD actuator of digital microfluidics and then discuss the electrode addressing and wire routing.

4.1 Architecture and Design Model of EWOD Chips

In performing various fluidic-handling functions, a primary issue is the manipulation of droplets. Although droplets can be controlled on many driving platforms [32], the EWOD chips, also referred to as EWOD actuators, have received much more attention due to their high accuracy and efficiency, and simple fabrication [10]. The EWOD chip generates electric potential by actuating electrodes to change the wettability of droplets, such that droplets can be shaped and driven along the active electrodes [25, 28]. To induce enough change of wettability for droplet motion, the voltage value applied to electrodes must exceed a threshold. This phenomenon enables a binary value (i.e., 1/0) to represent a relative logic-high/logic-low value of an actuation voltage, and thus the entire electrode controls can be modeled simply. Furthermore, by patterning electrodes to a general 2D array and adopting time-varying actuations, many droplet-based operations (e.g., mixing and cutting) can be well-performed on a 2D array in a *reconfigurable* manner [32].

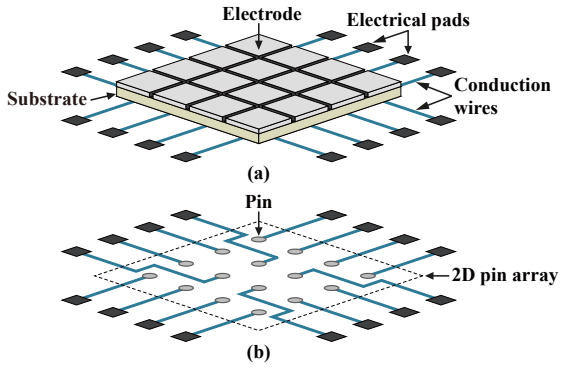
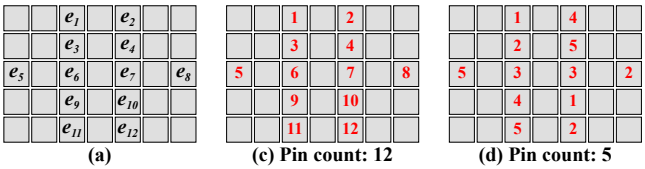


Figure 8: (1) Schematic view of an EWOD chip. (2) Design model on a 2D pin array.

As schematically presented in Figure 8(a), the general diagram of a 2D EWOD chip contains a patterned electrode array, conduction wires, electrical pads, and a substrate [10, 22, 28, 32]. In order to enable the fabrication of smaller and denser electrodes with high interconnect routing flexibility, a typical two-metal-layer design process of EWOD chips is presented in [3, 22]. It comprises two metal layers of 2D electrodes patterned in the first layer and conduction wires routed in the second layer, as well as an inter-insulator of silicon dioxide for via holes patterning. Based on this architecture, design model for EWOD chips can be specified to a 2D pin array, in which signal plan and electrical connections between these pins and electrical pads (i.e., signal ports) are established, as illustrated in Figure 8(b). As a result, the majority of existing efforts can be roughly grouped into two main design steps: 1) electrode addressing and 2) wire routing.

4.2 Electrode Addressing

Electrode addressing is a method whereby electrodes are addressed with control pins to identify input signals. Early EWOD-chip designs relied on *direct addressing* [10], where each electrode is directly addressed with an independent control pin. This addressing scheme maximizes the flexibility of electrode controls. However, since the control pins are actuated by an external controller which supplies a limited number of signal ports, it is infeasible to actuate a large number of control pins especially for high-density electrode array. For example, the controller in a recently developed chip with over 1000 electrodes for multiplex immunoassay can only actuate 64 control pins [1]. To comply with the limited pin-count supply, *pin-constrained* design of electrode addressing has been introduced as a solution to this problem, which utilizes a limited number of pins to control a large number of electrodes in EWOD chips. A promising solution, *broadcast addressing*, has been presented in [42]. The droplet-controlling information is stored in the form of electrode actuation sequences, where each bit in a sequence represents a signal status ("1" (actuated), "0" (de-actuated), or "X" (don't-care)) of the electrode at a specific time step [42]. Note that the don't-care symbol "X" can be either "1" or "0" which has no impact on scheduled fluidic controls. Examples of an electrode set and their actuation sequences are presented in Figure 9(a) and (b).



Electrode	e_1	e_2	e_3	e_4	e_5	e_6	e_7	e_8	e_9	e_{10}	e_{11}	e_{12}
Activation Sequence	1	1	0	0	0	X	X	0	X	X	X	X
	0	0	1	1	1	0	0	1	X	X	X	X
	0	0	0	0	0	1	1	0	0	0	X	X
	X	X	0	0	0	0	0	0	1	1	0	0
	X	X	X	X	1	0	0	1	X	X	1	1

(b)

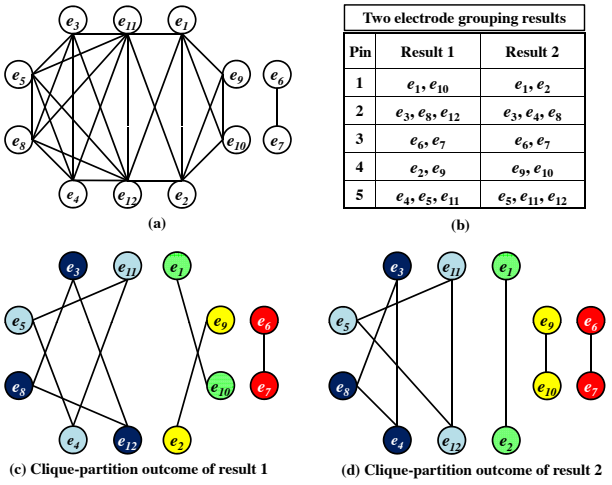
Figure 9: (a) Electrodes that are used for handling fluidic functions. (b) Scheduled fluidic functions in the form of actuation sequences. (c) Applies the direct-addressing scheme. (d) Applies the broadcast-addressing scheme.

Unlike direct addressing, where each electrode is assigned by an independent control pin, broadcast addressing focuses on electrode grouping and control signal merging through the compatibility of actuation sequences. Specifically, each electrode actuation sequence may contain several don't care terms. By carefully replacing these don't care terms with "1" or "0", multiple actuation

[1]Note that in chip-level design, routing refers to wire routing, which is different from droplet routing in the fluidic domain.

sequences can be merged to an identical outcome, which is also referred to as the *common compatible sequence* of these electrodes. Therefore, these electrodes can be assigned by the same control pin to receive the same control signal.

Take electrodes e_4 and e_5 in Figure 9(b) for example. By replacing "X" in the actuation sequence of e_4 with "1", we can merge the actuation sequences of e_4 and e_5 to "01001". Therefore, e_4 and e_5 can be addressed with the same control pin due to their mutually compatible actuation sequences. The example in Figure 9 (c) and (d) demonstrate the direct-addressing and broadcast-addressing outcomes, respectively. Compared with the direct-addressing result in (c), the broadcast-addressing result in (d) significantly reduces the required control pins from 12 to 5. This reduction requires fewer electrical devices and connections to perform the same fluidic functions, thus improving chip reliability as well as reducing fabrication cost [42].



Two electrode grouping results

Pin	Result 1	Result 2
1	e_1, e_{10}	e_1, e_2
2	e_3, e_8, e_{12}	e_3, e_4, e_8
3	e_6, e_7	e_6, e_7
4	e_2, e_9	e_9, e_{10}
5	e_4, e_5, e_{11}	e_5, e_{11}, e_{12}

Figure 10: (a) A compatibility graph G_c derived from Figure 9(b). (b) Two possible electrode grouping results. (c)-(d) Corresponding clique-partition results of (b).

Researchers have utilized the *compatibility graph* to specify the broadcast addressing [42], where the vertex set represents the electrode set and an edge between two electrodes indicates their corresponding activation sequences are compatible. For example, Figure 10(a) demonstrates a compatibility graph G_c derived from Figure 9(b). Based on the compatibility graph, the electrode grouping can be mapped to the *clique partition problem*, which is a well-known example of an intractable problem in graph theory. Since each clique represents an electrode group with mutually compatible control signals, we can individually assign each clique with a dedicated control pin. Two feasible electrode grouping results can be shown in Figure 10(b), with corresponding clique-partition results in Figure 10(c)-(d). Accordingly, by recognizing a minimum clique partition in the compatibility graph, the required number of control pins can be optimally minimized. However, the general minimum clique partition is known to be NP-hard [11] and thus is computationally expensive.

To tackle the computational cost, many heuristics have been proposed in the literature [39, 42, 43]. The work by [39] proposes an array-partition based method to group the electrode set without introducing unexpected fluidic-level behaviors. The work by [42] presents a greedy method of iterative clique recognitions with maximum cardinality on the compatibility graph. Recent work by [43] applies a connect-5 algorithm to group the electrode set with maximum controlling freedom of a single droplet. Moreover, several works further integrates various pin-count saving techniques into fluidic-level synthesis to achieve design convergence, thereby facilitating pin-count reduction effectively [15, 49]. Moreover, a work in [20] proposes a dedicated pin-count aware design methodology and explores the properties that are favorable for pin-count reduction along the fluidic-level synthesis. It classifies the usage of electrodes into three categories of reaction, branching, and routing corresponding to the design steps of resource binding, placement, and droplet routing. ILP-based pin-count saving formulations are applied to these three design steps, respectively.

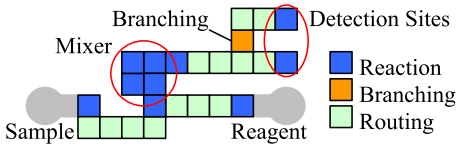


Figure 11: Categorization of electrodes corresponding to different pin-count demand [20].

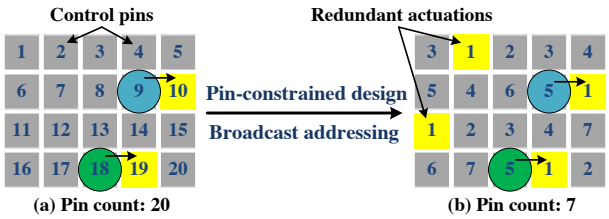


Figure 12: (a) A direct-addressing result uses two pins (pin 10 and pin 19) to generate two exact actuations for moving the two droplets. (b) A broadcast-addressing result uses one pin (pin 1) to generate two exact actuations, plus two redundant actuations, for moving the two droplets.

Although broadcast addressing serves as a promising solution to pin-constrained designs, yet the redundant actuations during signal merging have potentially caused a power-consumption problem. For example, in Figure 12(a), the direct-addressing result needs two exact actuations for moving the two droplets. In Figure 12(b), after applying the broadcast addressing, the pin count is greatly reduced from 20 to 7. Nevertheless, the addressing result needs two exact actuations, plus two *redundant* actuations, for moving the two droplets. As electrodes are controlled in a series of actuation steps, if control pins are not carefully assigned to electrodes, the addressing result will introduce a great number of redundant actuations. Hence, executing a bioassay may incur a high power-consumption problem which is critical to many battery-driven hand-held applications. Regarding this power-consumption problem, one work has been recently proposed to deal with the power-consumption problem incurred from the pin-constrained design [17]. The work in [17] formulates the electrode addressing and power saving into an effective minimum-cost maximum-flow network, with a progressive electrode-addressing scheme for reducing design complexity.

4.3 Wire Routing

After electrodes are addressed with control pins, conduction wires must be appropriately routed to establish the correspondence between the control pins (i.e., electrodes with the same pin must be wired together) and the signal pads with a total minimum wirelength. Since signal pads of EWOD chips generally locate outside

the component (defined as the 2D pin array) boundary the routing problem that connects these inside terminal pins to outsides signal ports is similar to the typical escape routing problem appearing in many VLSI designs [5]. However, in pin-constrained EWOD-chip designs, multiple electrodes may share the same control pin and therefore a single control signal may actuate multi-terminal pins. To realize the electrical connections, multi-terminal pins with the same control signal must be routed together, and then escape to the component boundary. This feature makes the typical escape router, which is based on the connection of two-terminal pins, unsuitable for the EWOD-chip routing problem. However, readily available CAD tools targeting this type of routing problem are still critically lacking.

Regarding the pin-constrained design, a critical problem comes from the interdependence of broadcast addressing and routing. Different broadcast-addressing results lead to different wiring connections and this problem occurs even with the same pin count. If broadcast addressing and routing cannot be considered together, the feasibility and quality of the routing solution may be inevitably limited.

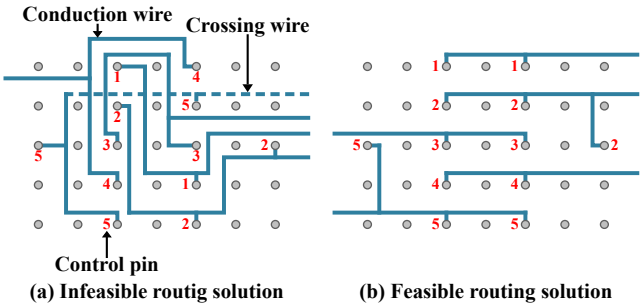


Figure 13: Consideration of electrode addressing and routing: (a) separately; (b) simultaneously.

For example, Figure 13 illustrates two routing solutions under two different design methods that perform the same fluidic controls (the corresponding electrode groups and addressing results can refer to the result 1 and result 2 in Figure 10(b), respectively). In (a), the separate consideration of electrode addressing and routing confronts many back detours for pins 3-4, and thus blocks the routing for pin 5. On the other hand, in (b), simultaneous consideration of electrode addressing and routing provides a higher feasibility and quality routing solution in terms of routability and wirelength. In the case of (a), additional post processes such as electrode readdressing and rerouting or even a multi-layer routing structure should be considered. Regarding this, an effective design to low-cost manufacturing of electrical connections cannot be realized [10].

There is only one existing work proposed in [15] that considers the automated design of EWOD-chip routing. The work by [15] simultaneously solves the electrode addressing and routing by adopting a two-stage technique of global routing followed by progressive routing. In global routing, a set of horizontal/vertical global routing tracks is constructed using a maximum-flow formulation. By guiding straight routes on these tracks, the pin count and wirelength can be simultaneously minimized in a global view. Then, the progressive routing iteratively completes the addressing and routing with respect to these tracks using a minimum-cost maximum-flow model, while maintaining a minimum growth of pin count and wirelength between successive iterations.

5. TESTING AND FAULT MODELS

In this section, we describe recent advances in the testing of digital microfluidic biochips and fault localization techniques.

5.1 Fault Modeling

As in microelectronic circuits, a defective DMFB is said to have a failure if its operation does not match its specified behavior. In order to facilitate the detection of defects, fault models that efficiently represent the effect of physical defects at some level of abstraction are required. Faults in digital microfluidic systems can be classified as being either catastrophic or parametric. Catastrophic faults lead to a complete malfunction of the system, while parametric faults cause degradation in the system performance. A parametric fault is detectable only if this deviation exceeds the tolerance in system performance.

Table I lists some common failure sources, defects and the corresponding fault models for catastrophic faults in DMFB. Examples of some common parametric faults include the following:

- Geometrical parameter deviation: The deviation in insulator thickness, electrode length and height between parallel plates may exceed their tolerance value.
- Change in viscosity of droplet and filler medium. These can occur during operation due to an unexpected biochemical reaction, or changes in operational environment, e.g., temperature variation.

5.2 Structure Test Techniques

A unified test methodology for DMBF has been presented, whereby faults can be detected by controlling and tracking droplet motion electrically [35]. Test stimuli droplets containing a conductive fluid (e.g., KCL solution) are dispensed from the droplet source. These droplets are guided through the unit cells following the test plan towards the droplet sink, which is connected to an integrated capacitive detection circuit. Most catastrophic faults result in a complete cessation of droplet transportation. Therefore, we can determine the fault-free or faulty status of the system by simply observing the arrival of test stimuli droplets at selected ports. An efficient test plan ensures that testing does not conflict with the normal bioassay, and it guides test stimuli droplets to cover all the unit cells available for testing. The microfluidic array can be modeled as an undirected graph, and the pathway for the test droplet can be determined by solving the Hamiltonian path problem [36]. With negligible hardware overhead, this method also offers an opportunity to implement self-test for microfluidic systems and therefore eliminate the need for costly, bulky, and expensive external test equipment. Furthermore, after detection, droplet flow paths for bioassays can be reconfigured dynamically such that faulty unit cells are bypassed without interrupting the normal operation.

Even though most catastrophic faults lead to a complete cessation of droplet transportation, there exist differences between their corresponding erroneous behaviors. For instance, to test for the electrode-open fault, it is sufficient to move a test droplet from any adjacent cell to the faulty cell. The droplet will always be stuck during its motion due to the failure in charging the control electrode. On the other hand, if we move a test droplet across the faulty cells affected by an electrode-short fault, the test droplet may or may not be stuck depending on its flow direction. Therefore, to detect such faults, it is not enough to solve only the Hamiltonian path problem. In [37], a solution based on Euler paths in graphs is described for detecting electrode shorts.

Despite its effectiveness for detecting electrode shorts, testing based on an Euler path suffers from long test application time. This

TABLE I: EXAMPLES OF FAULT MODELS FOR DIGITAL MICROFLUIDIC BIOCHIP

Cause of defect	Defect type	Number of cells	Fault model	Observable error
Excessive actuation voltage applied to an electrode	Dielectric breakdown	1	Droplet-electrode short (a short between the droplet and the electrode)	Droplet undergoes electrolysis, which prevents its further transportation
Electrode actuation for excessive duration	Irreversible charge concentration on an electrode	1	Electrode-stuck-on (the electrode remains constantly activated)	Unintentional droplet operations or stuck droplets
Excessive mechanical force applied to the chip	Misalignment of parallel plates (electrodes and ground plane)	1	Pressure gradient (net static pressure in some direction)	Droplet transportation without activation voltage
Coating failure	Non-uniform dielectric layer	1	Dielectric islands (islands of Teflon coating)	Fragmentation of droplets and their motion is prevented
Abnormal metal layer deposition and etch variation during fabrication	Grounding Failure	1	Floating droplets (droplet are not anchored)	Failure of droplet transportation
	Broken wire to control source	1	Electrode open (electrode actuation is not possible)	Failure to activate the electrode for droplet transportation
	Metal connection between two adjacent electrodes	2	Electrode short (short between electrodes)	A droplet resides in the middle of the two shorted electrodes, and its transport along one or more directions cannot be achieved
Particle contamination or liquid residue	A particle that connect two adjacent electrodes	2	Electrode short	
Protein adsorption during bioassay [10]	Sample residue on electrode surface	1	Resistive open at electrode	Droplet transportation is impeded.
			Contamination	Assay results are outside the range of possible outcomes

approach uses only one droplet to traverse the microfluidic array, irrespectively of the array size. Fault diagnosis is carried out by using multiple test application steps and adaptive Euler paths. Such a diagnosis method is inefficient since defect-free cells are tested multiple times. Moreover, the test method leads to a test plan that is specific to a target biochip. If the array dimensions are changed, the test plan must be completely altered. In addition, to facilitate chip testing in the field, test plans need to be programmed into a microcontroller. However, the hardware implementations of test plans from [35] are expensive, especially for low cost, disposable biochips. More recently, a cost-effective testing methodology referred to as "parallel scan-like test" has been proposed [40]. The method is named thus because it manipulates multiple test droplets in parallel to traverse the target microfluidic array, just as test stimuli can be applied in parallel to the different scan chains in an integrated circuit.

A drawback of the above “structural” test methods is that they focus only on physical defects, and they overlook module functionality. Therefore, these methods can only guarantee that a biochip is defect-free. However, a defect-free microfluidic array can also malfunction in many ways. For example, a defect-free reservoir may result in large volume variations when droplets are dispensed from it. A splitter composed of three defect-free electrodes may split a big droplet into two droplets with significantly unbalanced volumes. These phenomena, referred to as malfunctions, are not the result of electrode defects. Instead, they are activated only for certain patterns of droplet movement or fluidic operations. Such malfunctions can have serious consequences on the integrity of bioassay results.

5.3 Functional Test Techniques

Functional testing involves test procedures to check whether groups of cells can be used to perform certain operations, e.g., droplet mixing and splitting. For the test of a specific operation, the corresponding patterns of droplet movement are carried out on the target cluster of cells. If a target cell cluster fails the test, e.g., the mixing test, we label it as a malfunctioning cluster. As in the case of structural testing, fault models must be developed for functional testing. Malfunctions in fluidic operations are identified and included in the list of faults; see Table II.

Functional test methods to detect defects and malfunctions have been developed. In particular, dispensing test, mixing test, splitting test, and capacitive sensing test have been described in [41] to address the corresponding malfunctions.

Functional test methods were applied to a PCB microfluidic platform for the Polymerase Chain Reaction (PCR). The platform consists of two columns and two rows of electrodes, three reservoirs, and routing electrodes that connect the reservoirs to the array. An illustration of the mixing and splitting test is shown in Figure 14. The bottom row was first targeted and five test droplets were dispensed to the odd electrodes, as shown in Figure 14(a). Next, splitting test for the even electrodes was carried out. Droplets were split and merged on the even electrodes. In Figure 14(b), we see a series of droplets of the same volume resting on the even electrodes, which means that all the odd electrodes passed the splitting test, and merging at the even electrodes worked well. However, when the splitting test was carried out on the even electrodes, a large variation in droplet volume was observed on the 3rd and 5th electrodes; see Figure 14(c). This variation implied a malfunction, leading to unbalanced splitting on the 4th electrode. The malfunction was detected when the droplets were routed to the capacitive sensing circuit. The 4th electrode on the bottom row was marked as an unqualified splitting site.

Recently, the design of microfluidic logic gates implementing Boolean functions such as AND, OR, and NOT has been reported [50]. Logic values “0” or “1” are defined as follows: the presence (absence) of a droplet of 1x volume at an input or output port indicates a logic value of “1” (“0”). Unlike other microfluidic logic designs [24, 26], the same interpretations at inputs and outputs ensure that logic gates can be easily cascaded. A 2-input OR gate (Z = X1+X2) is shown in Figure 15. A detector can be placed at Electrode 9 to determine the output value. Such capacitive or optical

TABLE II: FUNCTIONAL FAULT MODELS

Cause of malfunction	Malfunction type	Number of cells	Fault model	Observable error
Electrode actuation for excessive duration	Irreversible charge concentration on the dispensing electrode	3	Dispensing-stuck-on (droplet is dispensed by not fully cut off from the reservoir)	No droplet can be dispensed from the reservoir
Electrode shape variation in fabrication	Deformity of electrodes	3	No overlap between droplets to be mixed and center electrode	Mixing failure
Electrode electrostatic property variation in fabrication	Unequal actuation voltages	3	Pressure gradient (net static pressure in some direction)	Unbalanced volumes of split droplets
Bad soldering	Parasitic capacitance in the capacitive sensing circuit	1	Oversensitive or insensitive capacitive sensing	False positive/negative in detection

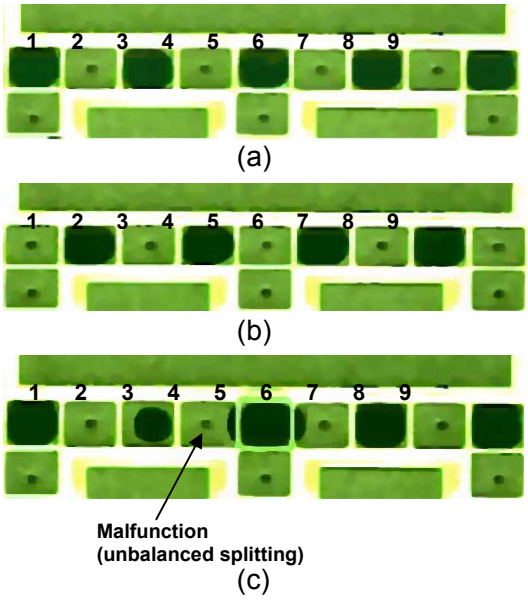


Figure 14: Mixing and splitting test for a fabricated PCR chip.

detectors to indicate the presence of a droplet can be easily implemented [50]. The sequence of control voltages is independent of the input logic values, which allows easy implementation. Such logic gates have been used for the design of response compactors for built-in self-test.

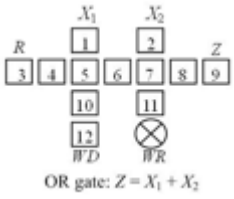


Figure 15: A microfluidic OR gate.

6. FUTURE DESIGN CHALLENGES

Future design challenges lie in the incorporation of chip reliability into the CAD flow of DMFB. One significant problem is the reliability problem incurred from pin-constrained designs. Control-pin/-signal sharing might introduce additional and unnecessary electrode actuations, which has the potential to make an electrode confront excessive actuations in case of a naive design. Studies on EWOD chips have reported this kind of problem accelerates the extent of trapping charge, leading to a permanent degradation of dielectric layer [9, 18, 38]. This scenario inevitably impedes complete and correct fluidic controls and therefore degrades the chip reliability. Thus, it becomes desirable and crucial to strike a balance between control-pin/-signal sharing and reliability preservation when the chip size and assay functionality grow, especially under the circumstance of pin-constrained design.

Reliability-aware placement needs to be incorporated. Current design automations place the modules with unrestricted sharing of cells/electrodes to minimize the chip size. For some applications such as point-of-care testing, on-chip fluidic modules, for example the fluidic modules of incubations, are associated with relatively long execution durations than other counterparts such as simple mixing and dilution. If cells are overly shared by these modules, the underlying electrodes many suffer from excessive actuations thereby decreasing the lifetime of electrodes, which degrades the chip reliability. Therefore, it is desirable to develop a reliability-aware placement algorithm for this kind of applications.

Optimization across energy domains also needs to be investigated. Such optimization problems that span several energy domains (e.g., electrical, circuit, fluidic, and thermal domains) appear to be extremely difficult due to the further involvements of energy-related constraints or objectives. For example, in pin-constrained design, we should limit the fanout of a single control pin to avoid overly charge sharing, which might cause problems such as high power dissipation and trapped charge. Moreover, thermal-aware signal planning is also important for the prevention of fluidics from overheating in some area that has congested electrical connections.

Biochip operation execution is in the order of seconds, whereas specialized heuristics for the synthesis problems can potentially obtain good results in milliseconds [27]. An interesting possibility in this context is to perform the synthesis online, while the biochemical application is running, and not offline, as it has been done so far. Such an online approach has the advantage of adaptivity, to faults in the architecture or variations in the operation execution. In addition, it opens up the possibility of fully portable point-of-care devices. Although no research has been done so far in this area, recent research [4, 47] has shown how an implementation can react to faults by switching online to recovery schedules pre-synthesized offline.

7. CONCLUSIONS

In this paper, we have provided a survey on recent research in the design and optimization of DMFBs. We show how CAD tools are involved to automate the design of DMFBs. Several optimization problems appearing in the design stages, fluidic-level synthe-

sis, chip-level design, and testing, are also presented. In addition, we have pointed out a set of open problems and design challenges that remain to be tackled in the future. The authors believe this paper will spark more research interests being devoted into the developments of CAD tools for DMFBs, which are expected to pave the way for the deployment and use of biochips in the emerging marketplace.

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