Digital Microfluidic Logic Gates and Their Application to Built-in Self-Test of Lab-on-Chip

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***Abstract*—Dependability is an important system attribute for microfluidic lab-on-chip. Robust testing methods are therefore needed to ensure correct results. Previously proposed techniques for reading test outcomes and for pulse-sequence analysis are cumbersome and error prone. We present a built-in self-test (BIST) method for digital microfluidic lab-on-chip. This method utilizes digital microfluidic logic gates to implement the BIST architecture; AND, OR and NOT gates are used to compress multiple test-outcome droplets into a single droplet to facilitate detection with low overhead. These approaches obviate the need for capacitive sensing test-outcome circuits for analysis. We also apply the BIST architecture to a pin-constrained biochip design. A multiplexed bioassay protocol is used to evaluate the effectiveness of the proposed test method.**

***Index Terms*—Dependability, lab-on-chip, logic gates, microfluidics, testing.**

I. Introduction

MICROFLUIDICS lab-on-chip technology has made great strides in recent years [1], [2]. It has enabled on-chip immunoassays, clinical diagnosis, environmental toxicity monitoring, and high-throughput DNA sequencing. An especially promising technology platform is based on the principle of electrowetting-on-dielectric. Discrete droplets of nanoliter volumes can be manipulated in a "digital" manner on a 2-D array of electrodes ("unit cells"). Hence, this technology is referred to as "digital microfluidics" [2].

Droplets are moved by applying a control voltage to a unit cell adjacent to the droplet and, at the same time, deactivating the one under the droplet. Fluid-handling operations, such as droplet merging, splitting, mixing, and dispensing can be executed in a similar manner. Droplet routes and operation schedules are programmed into a microcontroller that drives the electrodes.

Another application of microfluidics lies in the use of droplets for implementing logic gates [13]. Microfluidic logic gates can be implemented in various ways, such as electrochemical reactions [29], relative resistance [26], and bubbles in electronic channels [14]. However, a drawback of these methods is that they assign different interpretations to inputs and outputs, which makes the cascading of gates difficult. Digital microfluidics provides a promising alternative technique for on-chip logic functionality, and for integrating sensing and computing. In this paper, we design and demonstrate digital microfluidic logic gates, and use them for testing a lab-on-chip.

Notable advances have been reported recently in lab-on-chip design by using digital microfluidics [1], [8], [17], [27], [32]. A prototype has been developed for gene sequencing through synthesis [1], which targets the simultaneous execution of 106 fluidic operations and the processing of billions of droplets. In [27], the multiplexed sample preparation is realized on a digital microfluidic chip. Other lab-on-chip systems are being designed for protein crystallization, which requires the concurrent execution of hundreds of operations [32]. For example, a prototype for clinical diagnostics includes more than 5 000 electrodes [4], and a commercial chip embeds more than 600 000 20 by 20-μm electrodes with integrated optical detectors [17]. Recent years have therefore seen a growing interest in design-automation and test techniques for the digital microfluidic platform [7], [9], [11], [15], [16], [20]–[22], [28], [30]–[35]. Test techniques for other microfluidic platforms have also been developed [10], [12].

Dependability is an important system attribute for lab-on-chip, especially for safety-critical applications such as point-of care diagnostics, health assessment, and screening for infectious diseases. Some manufacturing defects may lead to erroneous assay outcomes. Therefore, structural test is needed to detect these defects. For instance, a single defective electrode can be detected/located via the traversal of a test droplet. In [30], a parallel scan-like testing methodology has been proposed for digital microfluidic devices.

Many fluidic operations must be repeatedly executed with high precision using a group of unit cells in compact microfluidic arrays. Structural test methods, which use test droplets to traverse the target array, are not sufficient to ensure that these fluidic operations can be performed reliably. For instance, some unit cells may function correctly during droplet transportation, but they might malfunction during droplet dispensing from reservoirs. As indicated in [31], the defects that lead to errors in splitting are different from defects that lead to errors in mixing. For example, when there is electrode-shape variation in fabrication, the possibility arises of no overlap between droplets to be mixed and the center electrode, which leads to mixing failure. When unequal voltages are applied to two electrodes adjacent to the center electrode where the droplet stays, there is an unwanted pressure gradient, which leads to unbalanced volumes of split droplets. Therefore, a group of cells, which can be reliably utilized to operate as a mixer, may malfunction when they are used for droplet splitting. Therefore,

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it is important to carry out functional testing to verify the functionality of the underlying microfluidic platform. In [31], several techniques are proposed for the functional testing of droplet-based microfluidic biochips. These techniques address fundamental biochip operations, such as droplet dispensing, transportation, mixing, splitting, and capacitive sensing.

Previous test methods for digital microfluidic platforms use capacitive sensing circuits to read and analyze test outcomes [30], [31]. After reading the test-outcome droplets in a consecutive manner, the capacitive-sensing circuit generates a pulse sequence corresponding to the detection of these droplets. This approach requires an additional step to analyze the pulse sequence to determine whether the microfluidic array under test is defective. The reading of test outcomes and the analysis of pulse sequences increase test time; the latter procedure is especially prone to errors arising from inaccuracies in sensor calibration. The complexity of the capacitive-sensing circuit and the need for pulse-sequence analysis make previously proposed testing methods less practical, especially for field operation.

In this paper, we propose a built-in self-test (BIST) method for digital microfluidic lab-on-chip. Microfluidic logic gates are utilized to implement the "compactor" in the BIST architecture. A compactor is a hardware block that is used to compress test responses to a short signature [6]. Using the principle of electrowetting-on-dielectric, we implement AND, OR, NOT, and exclusive-or (XOR) gates through basic droplet-handling operations, such as transportation, merging, and splitting. The microfluidic compactor can compress the test-outcome droplets into the droplet signature in a very short amount of time, and the signature can be detected by using a simple photodiode detector, thereby avoiding the need for a capacitive-sensing circuit and complicated pulse-sequence analysis. We also apply the BIST method to a pin-constrained design in order to support the execution of testing and the target bioassay steps. A practical application, namely, a multiplexed bioassay, is used to evaluate the effectiveness of the proposed method.

The rest of this paper is organized as follows. In Section II, logic gates, such as AND, OR, NOT, and XOR gates are proposed based on digital microfluidics. They are implemented through basic droplet-handling operations. Section III utilizes microfluidic logic gates to implement the "compactor" in BIST architectures for the structural test and functional test. In Section IV, the BIST architecture is applied to a pin-constrained design. A multiplexed bioassay is used to evaluate the effectiveness of the proposed method. Finally, conclusions are drawn in Section V.

II. Digital Microfluidic Logic Gates

In this section, we propose logic gates based on digital microfluidics. Nontrivial computing systems can be created by cascading the microfluidic logic gates that have the same input–output interpretation. These microfluidic logic gates are configured on the fabricated biochip for experimental validation.

A. Definitions and Experimental Setup

In the digital microfluidic platform, droplets of unit volume ($1\times$) or larger can be easily moved [3]. A droplet of $0.5\times$ volume is not large enough to have sufficient overlap with an adjacent electrode; hence, it cannot be moved with a nominal actuation voltage. It has been verified experimentally that the times required for dispensing one droplet, splitting a droplet into two, merging two droplets into one, and transporting a droplet to an adjacent electrode are nearly identical [3]. This duration is defined as one time frame (clock cycle).

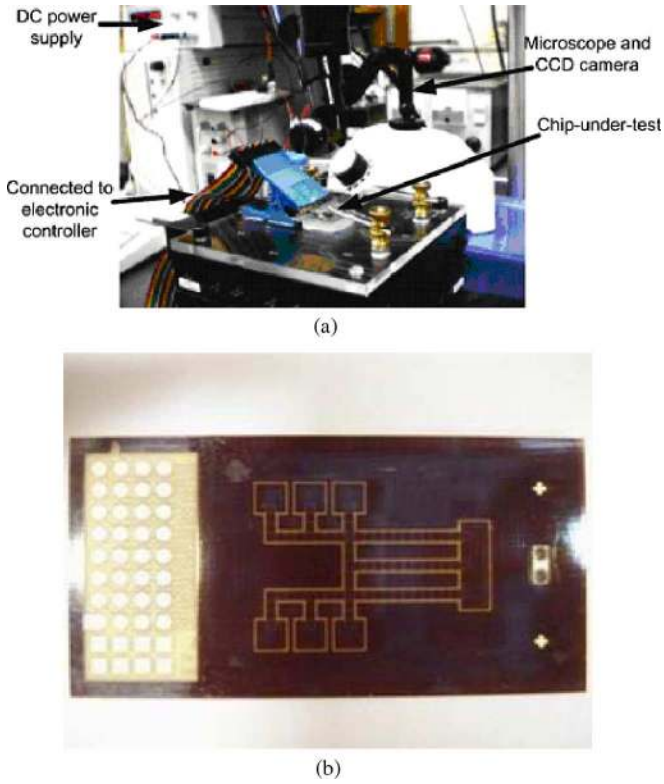

Fig. 1. Experimental setup from [3] and fabricated biochip. (a) Experimental setup [3]. (b) Fabricated chip used for experiments.

The definitions for logic values "0" or "1" are as follows: the presence of a droplet of $1\times$ volume at an input or output port indicates a logic value of "1." The absence of a droplet at an input or output port indicates the logic value "0." The same interpretations at inputs and outputs enable the output of one gate to be fed as an input to another gate; thus, logic gates can be easily cascaded.

To experimentally verify a microfluidic logic gate, we configured it on a fabricated biochip, then activated the corresponding electrodes to perform on-chip cycle-by-cycle operations in the laboratory. In the experiment, we use a biochip with an electrode pitch of 1.5 mm and a gap spacing of 0.475 mm. The droplets are dispensed from the on-chip reservoirs that are filled by DI water with black dye. The voltage setup for the splitting process is 250 V [input voltage for the printed-circuit board (PCB)]. Under this voltage setup, the droplet with a volume equal to or larger than $1\times$ can be split into two droplets with equal volumes. The voltage setup for transportation is in the range of 80 V to 90 V (input voltage for PCB). Under this voltage setup, only droplets with a volume equal to or larger than $1\times$ can be moved to the adjacent activated electrode.

A typical experimental setup is shown in Fig. 1(a). The chip-under-test is mounted on a custom-assembled platform. We use

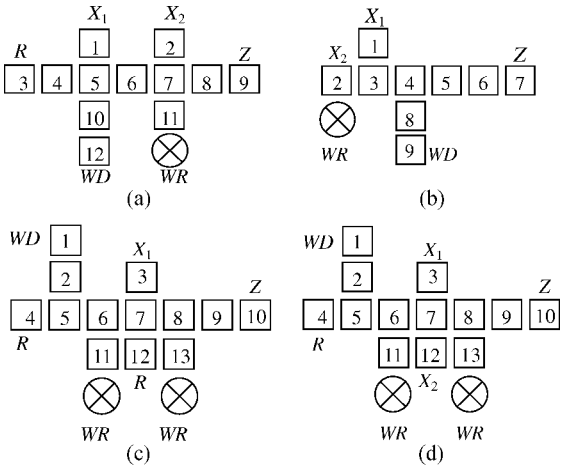

Fig. 2. Schematics of microfluidic logic gates. (a) OR gate $Z = X_1 + X_2$. (b) AND gate $Z = X_1 \cdot X_2$. (c) NOT gate $Z = \overline{X_1}$. (d) XOR gate $Z = X_1 \cdot \overline{X_2} + X_2 \cdot \overline{X_1}$.

a custom-made electronic unit developed by others in the laboratory to independently control the voltages of each control electrode in the array by switching them between ground and a dc actuation voltage. The chip-under-test is a PCB microfluidic prototype for protein crystallization (from Advanced Liquid Logic, Inc.), as shown in Fig. 1(b).

Next, we present the schematics and actuation-voltage sequences for various microfluidic logic gates. The cycle-by-cycle operations of gates are also presented.

B. Microfluidic OR *Gate*

Fig. 2 shows the schematics of the two-input OR, two-input AND, NOT, and XOR gates. The OR gate in Fig. 2(a) incorporates a waste reservoir (WR) and 12 indexed electrodes. Electrodes 1 and 2 are the two input ports X_1 and X_2; Electrode 3 is the reference port (R), from which one reference droplet is injected into the OR gate. Electrode 9 is the output port (Z) where a detector can be placed to determine the output logic value of the OR gate. These detections indicate that the presence or absence of a droplet can be easily implemented using photodiodes [18]. Electrode 12 is the washing port (WD) from which a washing droplet is injected after the logic operation to collect the residual droplets and move them to the waste reservoir.

The sequence of control voltages applied to each electrode is shown in Table I. A "1" ("0") entry in the table indicates a high (low) voltage to the corresponding electrode in that clock cycle. An "x" entry indicates a "don't-care," (i.e., the corresponding electrode can be either high or low). The sequence of control voltages is independent of the input logic values.

Fig. 3 describes the cycle-by-cycle operation of the OR gate for $X_1X_2 = 11$. At clock cycle 0, two $1\times$ droplets stay at two input ports (electrodes 1 and 2). At clock cycle 9, there is a $1\times$ droplet on electrode 9; hence, the output value is 1.

Fig. 4 illustrates the cycle-by-cycle operation of the OR gate for $X_1X_2 = 10$. At clock cycle 0, one $1\times$ droplets stay at the first input port (electrode 1), while there is no droplet on the second input port (electrode 2). At clock cycle 9, there is also a $1\times$ droplet on electrode 9, showing that the output value of this OR gate is 1.

TABLE I
ACTUATION-VOLTAGE SEQUENCE FOR THE OR GATE

Clock cycle	Electrode number											
	1	2	3	4	5	6	7	8	9	10	11	12
0	1	1	1	0	0	x	0	x	x	0	x	1
1	0	0	1	0	1	0	1	0	x	0	0	1
2	0	0	1	0	0	1	0	0	x	0	0	1
3	0	0	1	0	1	0	1	0	x	0	0	1
4	0	0	0	1	0	0	0	0	x	0	1	1
5	0	x	0	0	1	0	0	x	x	0	0	1
6	0	x	x	0	0	1	0	x	x	0	x	1
7	x	0	x	x	0	0	1	0	x	0	0	1
8	x	0	x	x	0	1	0	1	0	0	0	1
9	x	x	x	x	0	1	0	0	1	0	x	1

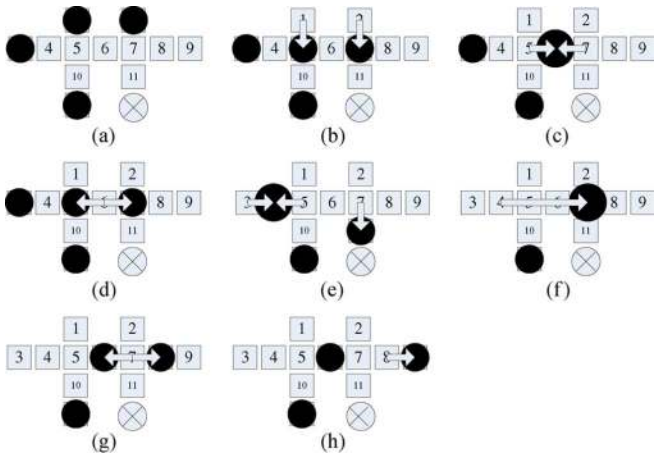

Fig. 3. Operation of the OR gate for input 11. (a) $t = 0$, two $1\times$ droplets stay at input ports. (b) $t = 1$, two $1\times$ droplets move downwards. (c) $t = 2$, two $1\times$ droplets are merged into a $2\times$ droplet. (d) $t = 3$, a $2\times$ droplet is split into two $1\times$ droplets. (e) $t = 4$, a $1\times$ droplet is merged with reference droplet into a $2\times$ droplet. (f) $t = 5$ to 7, a $2\times$ droplet moves right from electrode 4 to 7. (g) $t = 8$, a $2\times$ droplet is split into two $1\times$ droplets. (h) $t = 9$, a $1\times$ droplet moves right to the output port.

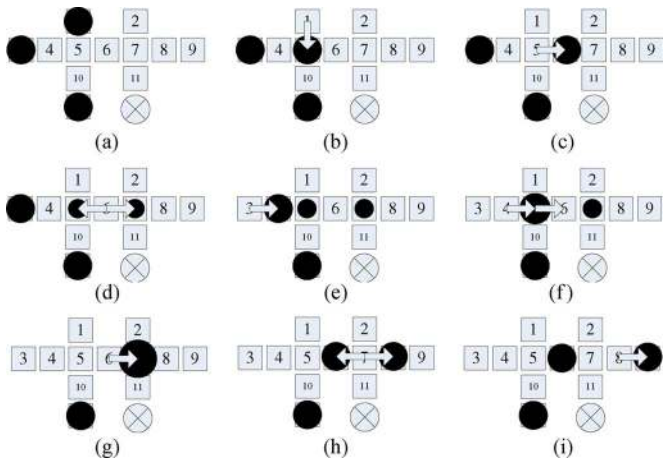

Fig. 4. Operation of the OR gate for input 10. (a) $t = 0$, one $1\times$ droplet stays at the input port 1. (b) $t = 1$, one $1\times$ droplet moves downwards. (c) $t = 2$, one $1\times$ droplet moves right from electrode 5 to 6. (d) $t = 3$, a $1\times$ droplet is split into two $0.5\times$ droplets. (e) $t = 4$, reference droplet moves right from electrode 3 to 4. (f) $t = 5$ to 6, reference droplet is merged with a $0.5\times$ droplet into a $1.5\times$ droplet, then continues moving. (g) $t = 7$, a $1.5\times$ droplet is merged with a $0.5\times$ droplet into a $2\times$ droplet. (h) $t = 8$, a $2\times$ droplet is split into two $1\times$ droplets. (i) $t = 9$, and a $1\times$ droplet moves right from electrode 8 to 9.

The delay of the OR gate is nine clock cycles, independent of the inputs. At the beginning of clock cycle 10, the droplet

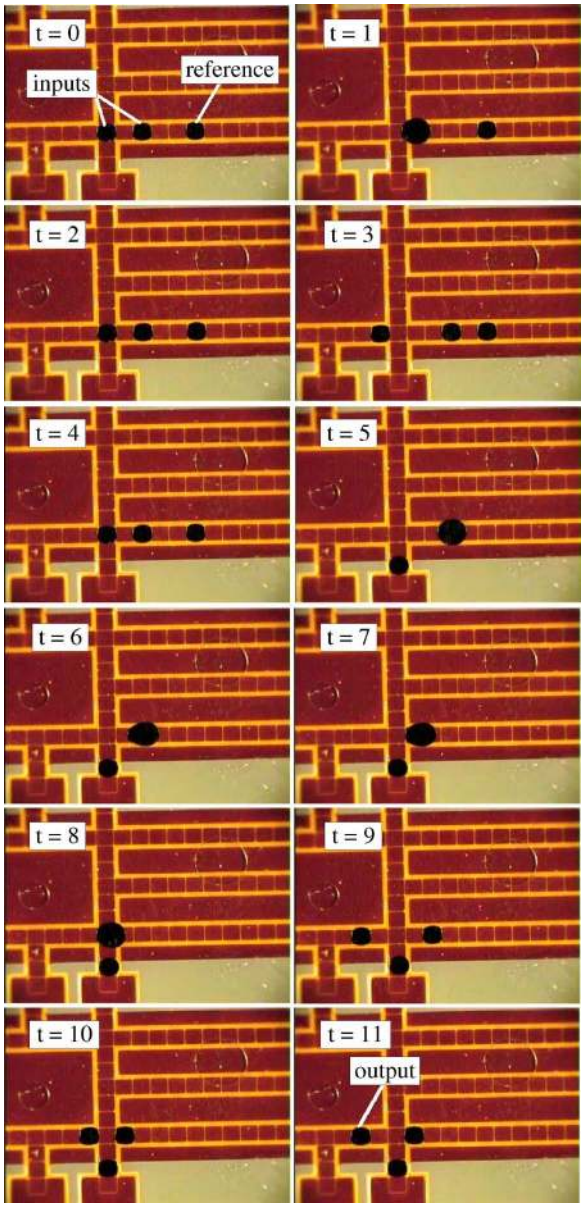

Fig. 5. On-chip cycle-by-cycle operation on a fabricated chip for the OR gate with input 11.

on the washing port (Electrode 12) is routed to merge with the residual droplets, and the result is transported to the waste reservoir. After this washing process, no droplet is left on the electrodes, and this gate is clean for the next operation.

Fig. 5 shows photographs of actual on-chip operation of the OR gate for $X_1X_2 = 11$. When $t = 0$, two $1\times$ droplets stay on the electrodes representing two inputs, while one $1\times$ droplet stays on the electrode representing the reference port. Operations from $t = 1$ to 10 are the same as that in Fig. 3. Note that the splitting step in the experiment occupies five electrodes and lasts for three clock cycles, as shown from $t = 2$ to 4. This is because we want to ensure even and thorough splitting, to acquire two split droplets with equal volume. At $t = 11$, there is one $1\times$ droplet on the electrode representing the output. Experimental results demonstrate the feasibility of the OR gate for different input values.

TABLE II
ACTUATION-VOLTAGE SEQUENCE FOR THE AND GATE

Clock cycle	Electrode number								
	1	2	3	4	5	6	7	8	9
0	1	1	0	x	x	x	x	0	1
1	0	0	1	0	x	x	x	0	1
2	0	1	0	1	0	x	x	0	1
3	x	0	0	0	1	0	x	0	1
4	x	x	x	0	0	1	0	0	1
5	x	x	x	x	0	0	1	0	1

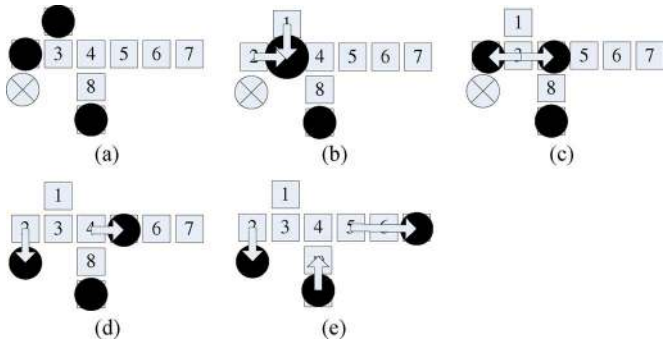

Fig. 6. Operation of the AND gate with input 11. (a) $t = 0$, two $1\times$ droplets stay at the input ports. (b) $t = 1$, two $1\times$ droplets are merged into a $2\times$ droplet. (c) $t = 2$, a $2\times$ droplet is split into two $1\times$ droplets. (d) $t = 3$, a $1\times$ droplet moves right from electrode 4 to 5. (e) $t = 4$ to 5, a $1\times$ droplet moves right from electrode 5 to 7, while the wash droplet moves upwards.

C. *Microfluidic* AND *Gate*

Fig. 2(b) illustrates the schematic of a two-input microfluidic AND gate. The AND gate in Fig. 2(b) incorporates a waste reservoir (WR) and nine indexed electrodes. Electrodes 1 and 2 are the two input ports X_1 and X_2. Electrode 7 is the output port (Z) and Electrode 9 is the washing port (WD).

The sequence of control voltages applied to each electrode is shown in Table II. Fig. 6 describes the cycle-by-cycle operation of the AND gate for $X_1X_2 = 11$. At clock cycle 0, two $1\times$ droplets stay at two input ports (Electrodes 1 and 2). At clock cycle 5, there is a $1\times$ droplet on electrode 9, showing that the output value of this AND gate is 1.

Fig. 7 illustrates the cycle-by-cycle operation of the AND gate for $X_1X_2 = 01$. At clock cycle 0, one $1\times$ droplet stays at the second input port (electrode 2), while there is no droplet on the first input port (electrode 1). At clock cycle 2, the $1\times$ droplet on electrode 3 is split into two $0.5\times$ droplets. The $0.5\times$ droplet cannot be moved even if the adjacent electrode is activated at clock cycle 3. Therefore, at clock cycle 5, there is no droplet on electrode 7, showing that the output value of this AND gate is 0. Due to symmetry, $X_1X_2 = 10$ yields the same output value.

The delay of the AND gate is five clock cycles, independent of the inputs. At the beginning of clock cycle 6, the droplet on the washing port (Electrode 9) is routed into the AND gate to clean the residuals and transport them to the waste reservoir.

Fig. 8 shows photographs of actual on-chip operation of the AND gate for $X_1X_2 = 10$. When $t = 0$, one $1\times$ droplet stays on the electrode representing one input port, while no droplet stays on the other input port. Operations from $t = 1$ to 4 are the same as that in Fig. 7. Note that during splitting, we apply a sufficiently high voltage to electrodes in order to move the $0.5\times$

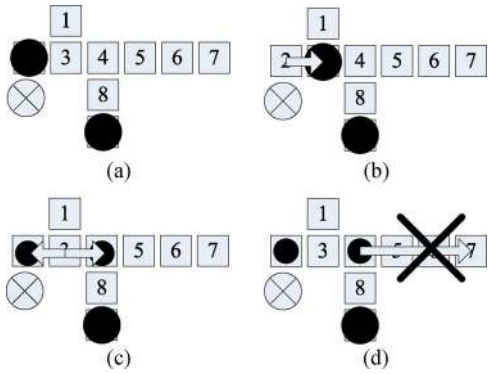

Fig. 7. Operation of the AND gate with input 10. (a) $t = 0$, a $1\times$ droplet stays at the input port 1. (b) $t = 1$, a $1\times$ droplet moves right from electrode 2 to 3. (c) $t = 2$, a $1\times$ droplet is split into two $0.5\times$ droplets. (d) $t = 3$ to 5, a $0.5\times$ droplet on electrode 4 cannot be moved to electrode 7.

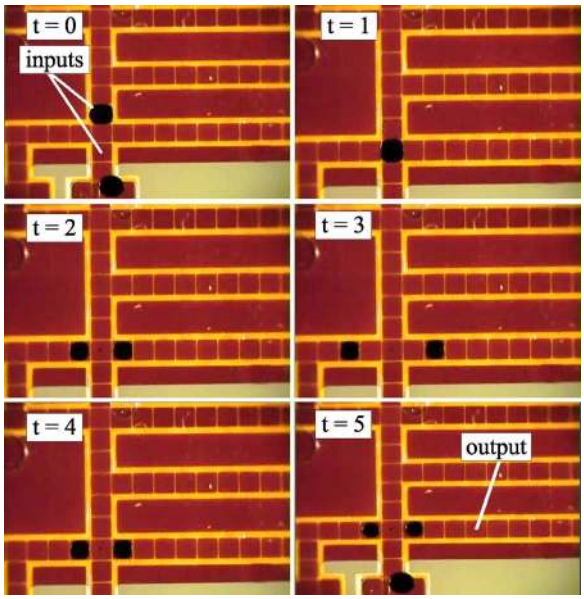

Fig. 8. On-chip cycle-by-cycle operation on a fabricated chip for the AND gate with input 10.

droplets, as shown from $t = 1$ to 4. After the splitting, when $t = 5$, we set the voltage low, so the $0.5\times$ droplet cannot be moved to the output port, while the $1\times$ droplet can be moved.

D. Microfluidic Inverter and XOR Gate

Fig. 2(c) shows a microfluidic inverter. The inverter incorporates two waste reservoirs (WR) and 13 indexed electrodes. Electrode 3 is the input port X_1; electrode 10 is the output port (Z); electrodes 4 and 12 are two reference ports (R), each of which one reference droplet is injected into the inverter; and electrode 1 is the washing port (WD).

The sequence of actuation voltages applied to each electrode is shown in Table III. Fig. 9 describes the cycle-by-cycle operation of the inverter for $X_1 = 1$. At clock cycle 0, one $1\times$ droplet stays at the input port (electrode 3). At clock cycle 9, no droplet is shown on electrode 10, indicating that the output value of this inverter is 0. The delay of the inverter is nine clock cycles.

Fig. 10 illustrates the cycle-by-cycle operation of the inverter for $X_1 = 0$. At clock cycle 0, no droplet stays at the input port

TABLE III
ACTUATION-VOLTAGE SEQUENCE FOR THE INVERTER/XOR GATE

Clock cycle	Electrode number												
	1	2	3	4	5	6	7	8	9	10	11	12	13
0	1	0	1	1	0	x	0	x	x	x	0	1	0
1	1	0	0	1	0	0	1	0	x	x	0	0	0
2	1	0	0	1	0	1	0	1	0	x	0	0	0
3	1	0	x	1	0	0	0	0	0	x	1	0	1
4	1	0	x	0	1	0	x	0	x	x	0	0	0
5	1	0	x	0	0	1	0	x	x	x	0	x	x
6	1	0	0	x	0	0	1	0	x	x	0	0	x
7	1	0	0	x	x	0	0	1	0	x	x	0	0
8	1	0	0	x	x	0	1	0	1	0	x	0	0
9	1	0	0	x	x	0	1	0	0	1	x	0	x

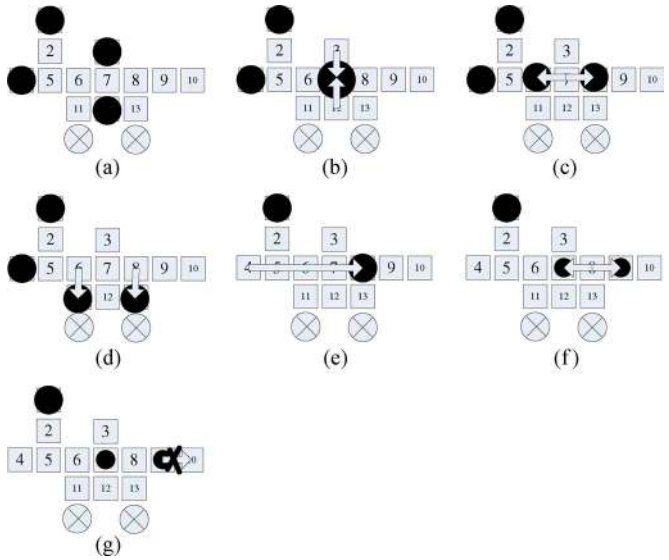

Fig. 9. Operation of the inverter with input 1. (a) $t = 0$, one $1\times$ droplet stays at the input port 1 (electrode 3). (b) $t = 1$, input droplet is merged with the reference droplet into a $2\times$ droplet. (c) $t = 2$, a $2\times$ droplet is split into two $1\times$ droplets. (d) $t = 3$, two $1\times$ droplets move downwards to waste reservoirs. (e) $t = 4$ to 7, reference droplet moves right from electrode 4 to 8. (f) $t = 8$, reference droplet is split into two $0.5\times$ droplets. (g) $t = 9$, the $0.5\times$ droplet on electrode 9 cannot be moved to electrode 10.

(electrode 3). At clock cycle 9, there is a $1\times$ droplet on electrode 10, showing that the output value of this inverter is 1.

Fig. 2(d) shows a two-input microfluidic XOR gate. The only difference between the schematics of the inverter and the XOR gate is that the second input port X_2 of the XOR gate is used as a reference port (R) in the inverter. It is experimentally verified that the function of the XOR gate can be performed correctly by using the same actuation-voltage sequence as the inverter.

III. BUILT-IN SELF TEST

In this section, we utilize microfluidic logic gates to implement the "compactor" in a BIST architecture. The microfluidic compactor can compress the test-outcome droplets into one droplet in a very short amount of time, and the droplet can be detected using a simple photodiode detector, thereby avoiding the need for a capacitive-sensing circuit and complicated pulse-sequence analysis. Reconfiguration is used to achieve low area overhead. Here, we utilize the microfluidic compactor in BIST architectures for two types of test: 1) a parallel scan-like test and 2) a functional test.

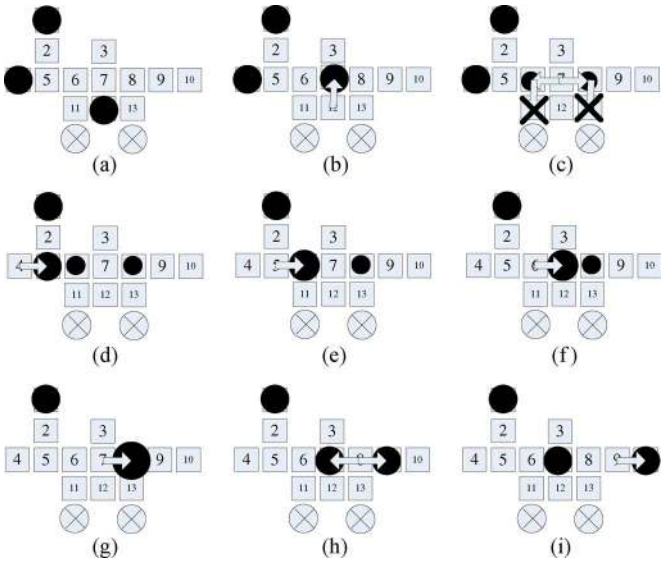

Fig. 10. Operation of the inverter with input 0. (a) $t = 0$, no droplet stays at the input port. (b) $t = 1$, reference droplet moves upwards from electrode 12 to 7. (c) $t = 2$ to 3, reference droplet is split into two 0.5× droplets, which cannot be moved downwards. (d) $t = 4$, reference droplet moves right from electrode 4 to 5. (e) $t = 5$, reference droplet is merged with a 0.5× droplet into a 1.5× droplet. (f) $t = 6$, a 1.5× droplet moves right from electrode 6 to 7. (g) $t = 7$, a 1.5× droplet merged with a 0.5× droplet into a 2× droplet. (h) $t = 8$, a 2× droplet is split into two 1× droplets. (i) $t = 9$, a 1× droplet moves right from electrode 9 to 10.

A. BIST for Parallel Scan-Like Test

In [30], a cost-effective testing methodology, referred to as "parallel scan-like test," has been proposed for the fault detection of catastrophic faults for droplet-based microfluidic devices. The "parallel scan-like test" implements the fault detection by using test droplets to traverse the microfluidic array. All of the defects listed in [30] (e.g., dielectric breakdown, irreversible charge concentration on an electrode, droplet electrolysis, and metal connection between two adjacent electrodes) can be detected by manipulating test droplets to traverse the candidate faulty electrodes. In order to detect defects involving single unit cells, defects involving two cells (e.g., shorts between two adjacent electrodes) and defects involving multiple unit cells, four iterations of test applications are needed to test the microfluidic array: two iterations for the vertically connected pairs and two iterations to traverse all of the horizontal connections. In each iteration, a test droplet is moved from its start electrode (referred to as pseudosource) along the row/column-under-test to its end electrode (referred to as pseudosink). Test droplets are routed in parallel along the corresponding rows/columns under test.

For a fault-free biochip, test droplets, which start simultaneously at the corresponding pseudosources, traverse the target rows/columns and reach their pseudosinks at the same time. If there is at least one fault in a row/column, the corresponding droplet will not arrive at its pseudosink. Therefore, after one iteration of the parallel scan-like test, we have to analyze whether there is one 1× droplet on each pseudosink.

After each iteration, to evaluate the test results, the test-outcome droplets are routed serially from "pseudosinks" to a capacitive-sensing circuit connected to the electrode for the sink reservoir. The capacitive-sensing circuit can produce a pulse-sequence corresponding to the detection of multiple test droplets.

After the test-outcome droplets are read serially, the capacitive-sensing circuit generates a pulse sequence corresponding to the detection of these droplets. An additional evaluation step is required to analyze these pulse sequences to determine whether the microfluidic array under test has a defect. For example, if a row/column of an array is faulty, there is no generated pulse in the corresponding position of the pulse sequence. The complexity of the capacitive-sensing circuit and the need to analyze the complex pulse sequence is a major drawback of [30]. Moreover, there is a need to calibrate the pulse-analysis system and errors are likely due to the lack of a "noise margin."

To solve the aforementioned problem, we propose a microfluidic compactor to compress multiple test-outcome droplets into one test-outcome droplet, which can be easily read and detected by a simple detector composed of a photodiode and LED [18]. The microfluidic compactor consists of a tree of microfluidic 2-input AND gates. The input ports of the AND gates in the first layer are connected one-by-one to the pseudosinks of the parallel scan-like row/column test, while the output ports of these AND gates are connected one by one to the input ports of AND gates in the second layer. The output of the single AND gate in the last layer is connected to the photodiode detector located at the sink of the microfluidic array. The structural test and functional test are performed in the area where logic gates are configured in the microfluidic array, before we actually use the logic gates as the compactor to compress the test outcome droplets.

Fig. 11 illustrates the schematic of the microfluidic compactor for the parallel scan-like test of odd rows/columns in a 16 × 16 microfluidic array. The electrodes represent the last row/column where the pseudosinks are located. The compactor consists of three layers of microfluidic 2-input AND gates. The output of the AND gate in the third layer is connected to the photodiode detector located in the sink reservoir of the microfluidic array.

In Fig. 11(a), after the parallel scan-like test for odd rows/columns, each of the odd pseudosinks has one 1× droplet on it, indicating that there is no defect in any odd rows/columns. The arrows show the direction of the droplet routing through the AND gates. The number at each arrow indicates the logic value of the input or output, according to the definitions for logic values in microfluidic systems. The input to each AND gate in the first layer is "1," so its output is "1." A 1× droplet finally appears on the output port (electrode) of the microfluidic compactor, indicating that the output value of the compactor is "1." Instead of routing all of the droplets in odd pseudosinks one-by-one to the capacitive-sensing circuit and analyzing the resulting pulse sequence, we use the photodiode detector to check for the presence of the 1× droplet on the output of the compactor. We conclude that there is no defect in the odd rows/columns of the microfluidic array.

In Fig. 11(b), there is no droplet on the fifth electrode, indicating that the corresponding row/column has a defect. Therefore, the left input of the second AND gate in the first layer is "0," while other input values are "1." The output of the AND gate with a "0" input value is "0." No droplet appears on the output port (electrode) of the microfluidic compactor; therefore, the output value of the compactor is "0." Since no droplet is detected by

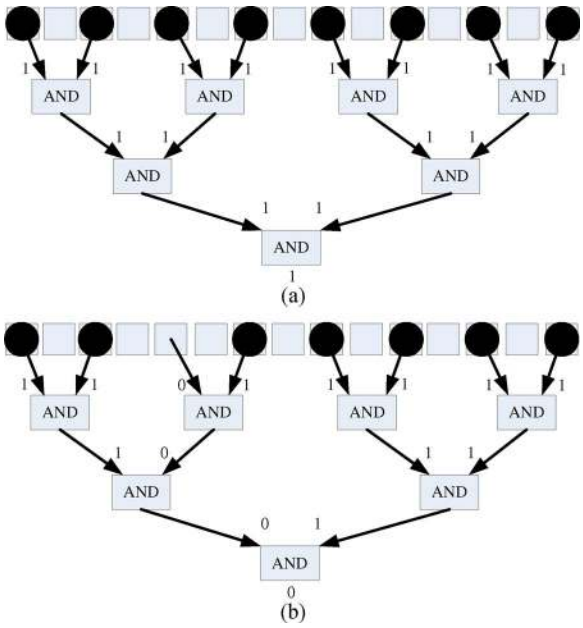

Fig. 11. Schematic of a microfluidic compactor for parallel scan-like testing. (a) compactor output = `1'; (b) compactor output = `0'.

the photodiode detector, we conclude that there is a defect in the odd rows/columns under test.

Fig. 12 shows the placement of the microfluidic compactor whose schematic is shown in Fig. 11. The 16 × 16 microfluidic array is also shown. The last three rows of electrodes are used to construct the microfluidic compactor. Note that we use a simplified design of the AND gate, which consists of only four electrodes. In order to reduce the size of the AND gate, the washing port and waste reservoir are not included in the AND gate. The microfluidic compactor consists of three layers of two-input AND gates. Only one washing port and one waste reservoir are needed for the compactor. After the compaction of the test-outcome droplets, a droplet from the washing port is routed through each electrode in the compactor, merged with the waste droplets, and routed to the waste reservoir.

The microfluidic array has only one source reservoir and one sink reservoir where the photodiode detector is located. This simplifies chip packaging and reduces fabrication cost. Dispensed from the single source, test droplets are aligned one by one and routed in sequence as components in an assembly line, along the periphery nodes to their pseudosources in the first row of all the odd columns. Beginning with these pseudosources, the test droplets are routed in parallel to the nodes at the other end of the corresponding odd columns. Finally, these test outcome droplets on the pseudosinks are compressed by the microfluidic compactor into one test-outcome droplet. As in Fig. 11, the arrows in Fig. 12 show the direction of the droplet flow. The output port of the compactor is directly connected to the photodiode detector.

For the parallel scan-like test for even rows/columns of the 16 × 16 microfluidic array, the microfluidic compactor is simply reconfigured by shifting it one column. The complete parallel scan-like test procedure with the microfluidic compactor reconfiguration is shown in Fig. 13.

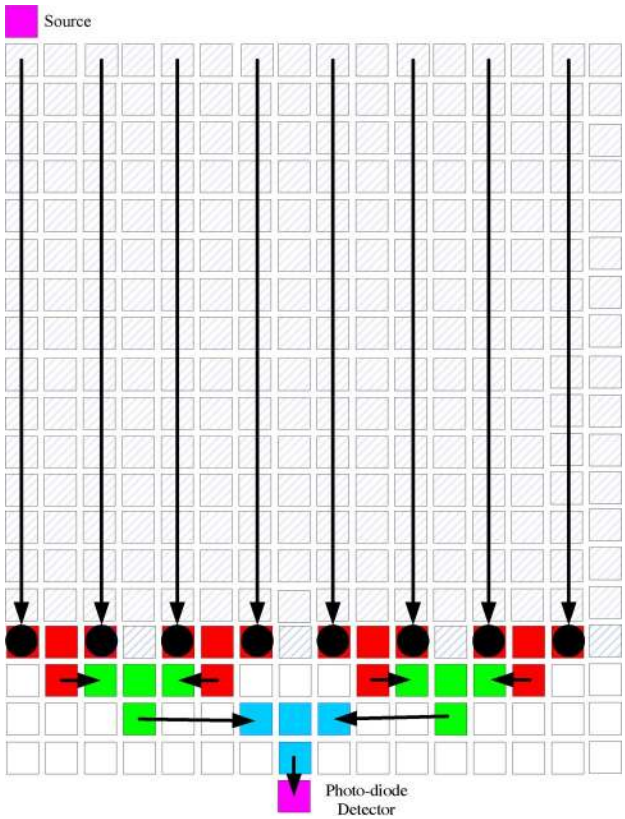

Fig. 12. Placement of a microfluidic compactor for parallel scan-like testing.

1) **Step 1.** Peripheral Test: A test droplet is dispensed from the source. It is routed to traverse all the peripheral electrodes, and the droplet finally returns to the sink;
2) **Step 2.** Column Test:
   i) 2(a): Parallel scan-like test of odd columns, where the test outcome droplets are compressed using microfluidic compactor, then the output of the compactor is read by the photo-diode detector;
   ii) 2(b): Parallel scan-like test of even columns, where the microfluidic compactor is reconfigured with one column shift-right from odd columns.
3) **Step 3.** Row Test: Repeat parallel scan-like test for both the odd and even rows to detect defects. The microfluidic compactor is reconfigured with one row shift during the two iterations.

Fig. 13. Parallel scan-like test procedure with reconfiguration of the microfluidic compactor.

For the parallel scan-like test without a compactor, an $N \times N$ microfluidic array needs N clock cycles to route all test-outcome droplets consecutively to the sink node connected to the capacitive-sensing circuit. The time needed for capacitive sensing is negligible [24]. For a parallel scan-like test with a compactor, we need $3 \times (\log_2 N - 1)$ clock cycles to compress the test-outcome droplets to one droplet. The detection of the droplet at the compactor output takes 30 s using the photodiode detector [18]. This duration is comparable to the compaction time; therefore, it must be taken into account when calculating the total time cost for result evaluation. The comparison of the

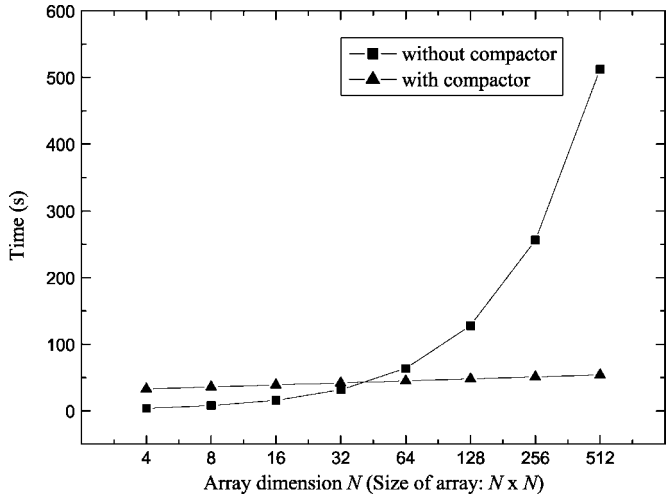

Fig. 14. Comparison of result-evaluation time with and without the microfluidic compactor.

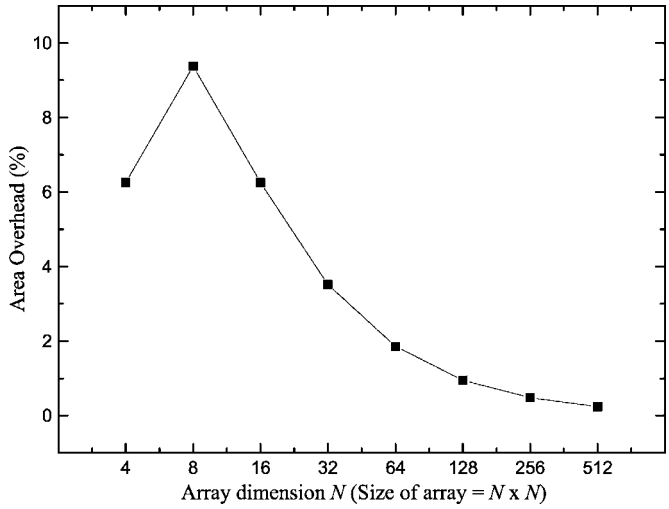

Fig. 15. Area overhead of a microfluidic compactor for a parallel scan-like test.

result-evaluation time for the two methods, assuming a typical clock frequency of 1 Hz, is shown in Fig. 14.

For an $N \times N$ microfluidic array, we need $(5 \times 2^{\log_2 N-2} - 4)$ electrodes to construct the compactor. For example, for $N = 16$, we need $(5 \times 2^{\log_2 16-2} - 4) = 16$ electrodes. The area overhead of the compactor is shown in Fig. 15. Since each AND gate in the first layer of the compactor utilizes three electrodes of the last row of the $N \times N$ microfluidic array under test, the area overhead for $N = 4$ is less than that for $N = 8$.

B. BIST for Functional Testing

Functional testing for digital microfluidics was first introduced in [31]. It targets the testing for fluidic operations, such as droplet dispensing, droplet transportation, mixing, and splitting. The proposed method allows functional testing using parallel droplet pathways. The functional test for the droplet-mixing operation is equivalent to the testing of the merging and routing operations within the target cell cluster. A mixing test can be reduced to a droplet merging test, which checks a series of three adjacent electrodes to determine whether two droplets can be merged on them. The fluidic splitting operation involves three adjacent electrodes, and can be viewed as the reverse of droplet merging. Therefore, the splitting test can be carried out by applying the merging test methods in a reverse manner.

These two tests can be combined into a unified test application procedure. The key idea is to carry out mixing and splitting test for all of the electrodes in a row/column concurrently. First, we carry out the horizontal splitting test for all of the even electrodes in a row concurrently. The split droplets get merged at the odd electrodes; therefore, the merging test is performed at the same time. Second, by carrying out the splitting test for all of the odd electrodes in a row concurrently, we can easily complete the horizontal merging test for all of the even electrodes. Thus, we can carry out all the horizontal tests (merging and splitting) in one row using only two manipulation steps. The test-outcome droplets on the electrodes after two manipulation steps are routed to the capacitive-sensing circuit. Similarly, all of the vertical tests in one column can be completed in two manipulation steps.

Only one capacitive-sensing circuit is used in [31] to reduce hardware cost. Moreover, in order to minimize the number of droplet manipulations, test results are read out after splitting and merging are carried out. Therefore, a complicated test-result interpretation scheme is required. The complexity of the capacitive-sensing circuit and the test-result interpretation scheme make the functional test method impractical for field operation.

To address the aforementioned problem, a microfluidic compactor is used here to compress multiple test-outcome droplets into only one test-outcome droplet. This test-outcome droplet can be easily detected by a photodiode detector. Assume that during mixing/splitting test, a droplet undergoes an unbalanced split. Since all other droplets are split evenly, this malfunction results in a pair of test droplets of abnormal volume—one bigger and the other smaller. The bigger droplet (volume larger than $1\times$) at the input ports of the AND gate is propagated to the output port, and it may lead to a malfunction of the AND gate. However, the bigger droplet does not affect the functionality of the NOT gate. Therefore, instead of AND gates, we use the combination of NOT gates and OR gates to construct the microfluidic compactor for functional testing.

The compactor consists of one layer of NOT gates and several layers of two-input OR gates; see Fig. 16. The first layer consists of NOT gates, and the input port of each NOT gate is connected to each electrode on which the droplets stay after the mixing and splitting test for one row/column. Other layers of the compactor tree consist of OR gates. The output of the OR gate in the last layer (root node of the compactor tree) is connected to the photodiode detector located in the sink of the microfluidic array.

Fig. 16 illustrates the microfluidic compactor for functional testing of 16 rows/columns. In Fig. 16(a), after the two-manipulation-step merging and splitting test in the row, each of the odd electrodes has a $1\times$ droplet on it, indicating that there is no malfunction in this row. According to the definitions of microfluidic logic values, we infer that the output value of the compactor is "0," indicating that there is no droplet on the electrode corresponding to the output port of the compactor. Instead of serially routing all of the droplets in the row under test to the capacitive-sensing circuit for detection, the photodiode detector

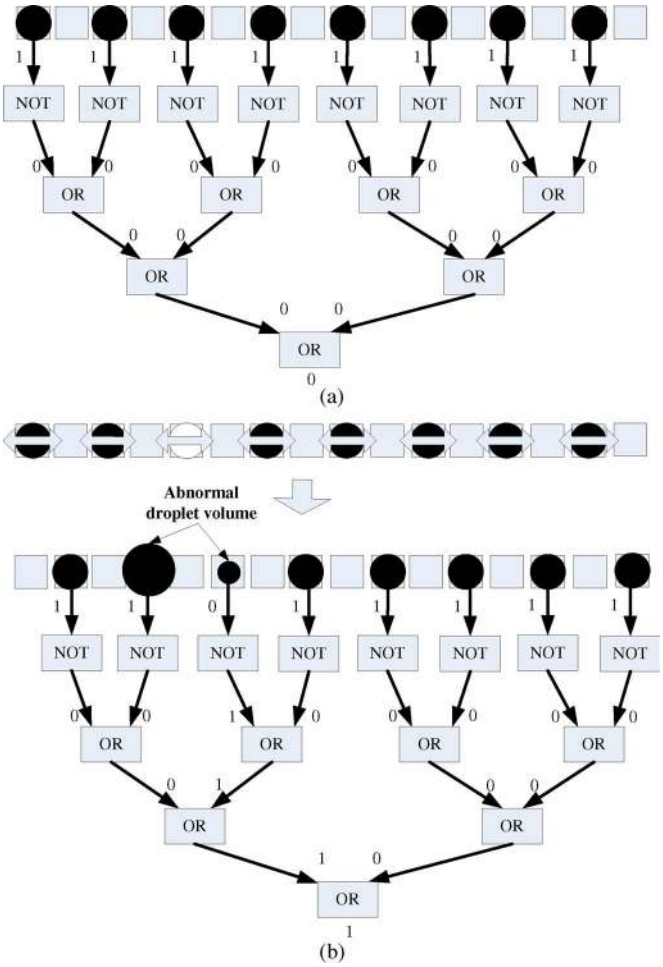

Fig. 16. Schematic of the microfluidic compactor for functional testing.

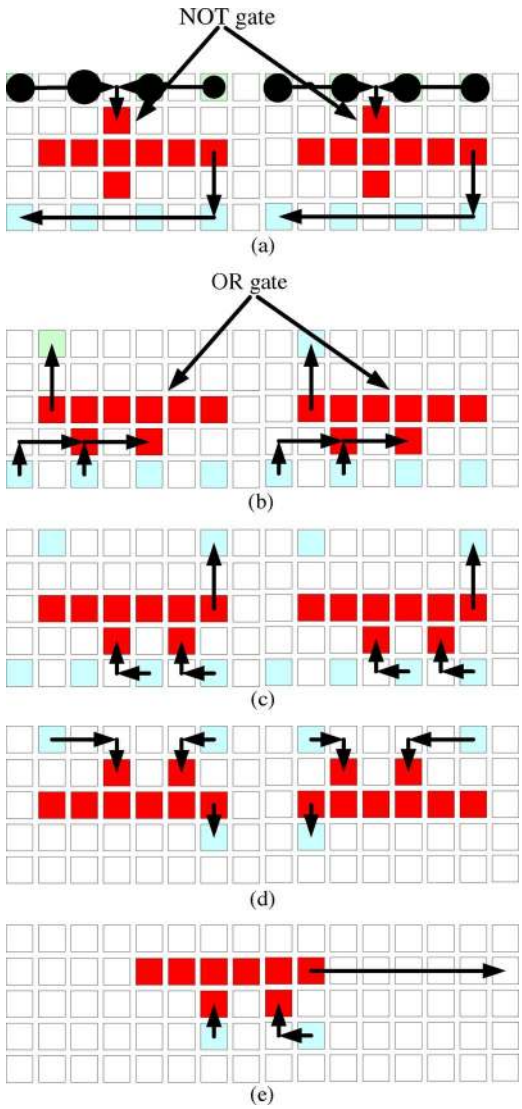

Fig. 17. Placement of the microfluidic compactor for functional testing.

indicates the absence of a droplet as in [18] at the output of the compactor; therefore, there is no malfunction in this row.

In Fig. 16(b), the droplet on the fifth electrode undergoes a unbalanced split during the functional test. Since all other droplets are split evenly, this malfunction results in a pair of test droplets of abnormal volume–one bigger and the other smaller. Note that the smaller droplet is too small (less than $0.5\times$) to be moved into the corresponding microfluidic NOT gate, so the input of this NOT gate is "0." The output of the compactor is "1," indicating the presence of a $1\times$ droplet on the output port of the compactor. The photodiode detector detects this droplet, indicating a malfunction in the row under test.

Fig. 17 shows the placement of the microfluidic compactor for a 16-electrode row under test. Note that we use simplified designs of the NOT gate, consisting of eight electrodes, and the OR gate, consisting of eight electrodes. The washing port and waste reservoir are not included in order to reduce the size of the gates. The reference droplets used by the NOT and OR gates are preloaded into the array. Only one washing port and one waste reservoir are needed for the entire compactor. After the compaction of the test-outcome droplets, a droplet from the washing port is routed through each of the electrodes in the compactor, merged with the waste droplets, and routed to the waste reservoir. Dynamic reconfiguration is utilized to construct the microfluidic compactor in order to use only a small amount of electrodes. In Fig. 17(a), there are two NOT gates (shown in red) in the array. At the left side of the row, four droplets are routed through the first NOT gate one by one, while the other four droplets are routed through the second NOT gate one by one. The eight electrodes (shown in gray) are the destinations where the outputs of the NOT gates are connected.

Using the aforementioned routing procedure, only two NOT gates are needed instead of eight NOT gates in the schematic in Fig. 16. In Fig. 17(b), the electrodes are reconfigured into two OR gates. Two pairs of droplets are routed concurrently through the OR gates. The same procedure is repeated for other two pairs, as shown in Fig. 17(c). Therefore, we only need two OR gates instead of four OR gates in the second layer of the compactor. In Fig. 17(d), the electrodes are reconfigured into two OR gates to implement the function in the third layer of the compactor. In Fig. 17(e), the electrodes are reconfigured into one OR gate to implement the function in the last layer of the compactor. The complete mixing and splitting test procedure with a reconfigurable microfluidic compactor is shown in Fig. 18.

1) Route 1x droplets to all the odd electrodes in a row;
2) Carry out splitting test for all the odd electrodes concurrently (1x droplets are now on even electrodes);
3) Carry out splitting test for all the even electrodes concurrently (1x droplets are now on odd electrodes);
4) Compress the droplets using microfluidic compactor, which is implemented by reconfiguring inverters and OR gates, then route the output of the compactor to the photodiode detector for test readout;
5) Repeat the test procedure for the next row;
6) Repeat steps 1-5 for columns.

Fig. 18. Procedure of complete mixing and splitting test procedure with reconfiguration of the microfluidic compactor.

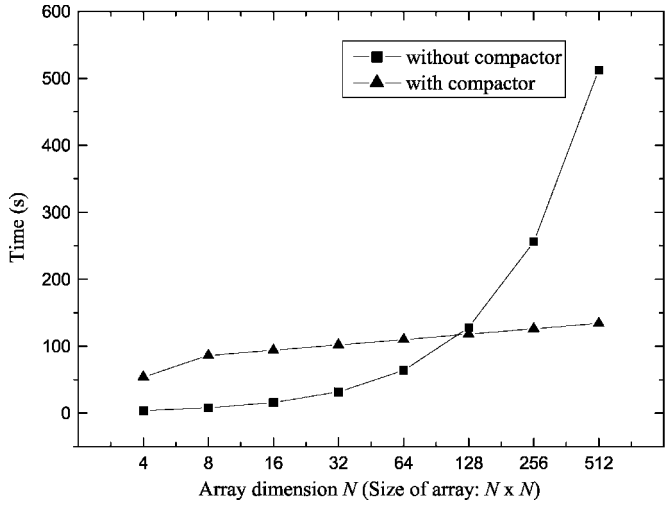

Fig. 19. Comparison of droplet-routing time with and without the microfluidic compactor.

For functional testing without using a compactor, an $N \times N$ microfluidic array needs N clock cycles to route all test-outcome droplets serially to the sink node with the capacitive-sensing circuit. For functional testing with a compactor, we need $8 \times (\log_2 N + 4)$ clock cycles to compress the test-outcome droplets to one droplet. The comparison of result-evaluation time for the two methods, taking into account the 30 s needed for optical sensing and assuming a typical 1-Hz clock frequency, is shown in Fig. 19.

The proposed microfluidic compactor requires $4 \times N$ electrodes for an $N \times N$ array. The area overhead of the compactor as a function of N is shown in Fig. 20.

IV. Application to Pin-Constrained Chip

In the discussion of the BIST method in Section III, we have assumed that the chip is controlled by using the direct-addressing method. To reduce product cost for disposable chips, pin-assignment methods [7], [19], [34], [35] have been proposed to design pin-constrained biochips. These methods allow us to use a small set of control pins to activate the electrodes in large microfluidic arrays. In [19], the number of control pins is minimized by using a multiphase bus for the fluidic pathways. Every nth electrode in an n-phase bus is electrically connected, where n is a small number (typically $n = 4$). An alternative

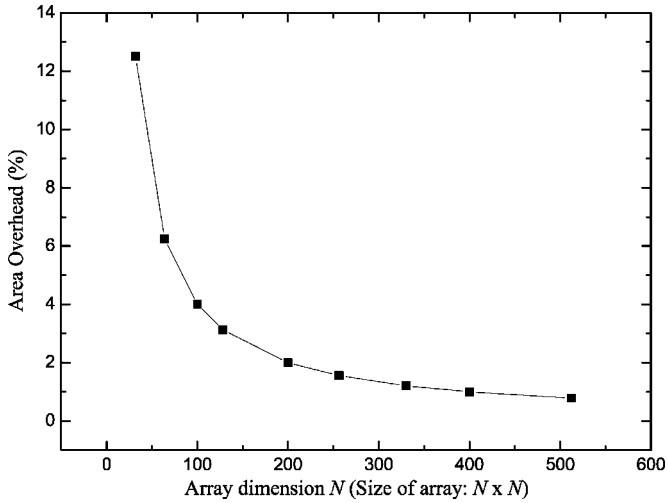

Fig. 20. Area overhead of the microfluidic compactor for functional testing.

design uses row and column addressing, which is referred to as "cross referencing." Each electrode is connected to two pins, corresponding to a row and a column, respectively [7]. A broadcast-addressing-based design technique is proposed in [34].

In this section, we investigate the application of the proposed BIST method to pin-constrained biochips. A practical application, a multiplex immunoassay, is used as an example to evaluate the proposed method.

A. BIST Architecture in the Pin-Constrained Chip

The BIST architecture proposed in Section III consists of microfluidic logic gates. The fluidic operations of the microfluidic logic gates can be easily implemented without any pin-actuation conflict on a direct-addressable chip. However, for a pin-constrained chip, due to constraints introduced by the sharing of input control pins by electrodes, carrying out these logic-gate operations on some electrodes can result in unintentional droplet manipulations. Here, we use an example to explain this problem.

Fig. 21 shows a part of the pin-constrained chip design. The number on each electrode indicates the control pin that is used to activate it. We attempt to perform the cycle-by-cycle operation of the microfluidic logic AND gate on it. First, two $1\times$ input droplets mix with each other into a $2\times$ droplet. Next, the $2\times$ droplet is split according to the operation of the microfluidic AND gate. Two adjacent electrodes of the $2\times$ droplet should be activated to perform the split operation, which requires that Pins 2 and 4 should be activated concurrently. However, another electrode that is controlled by Pin 2 is also activated. As a result, the split droplet that is supposed to be seated on the electrode of Pin 4 will be moved unintentionally to the boundary of the electrodes of Pins 4 and 2. This type of problem is referred to as electrode interference. Therefore, the BIST architecture that consists of microfluidic logic AND gates cannot be implemented correctly on this part of the pin-constrained chip. Since the pin-constrained chip is designed for a specific bioassay protocol and the number of electrodes are minimized in order to reduce the chip area, it is difficult to find a group of electrodes where the

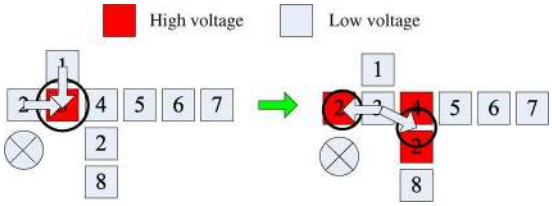

Fig. 21. Example of the malfunction of microfluidic logic AND gate on a pin-constrained chip.

microfluidic logic gates can be mapped correctly without any pin-actuation conflict.

Note that the failure of implementation of the BIST architecture is due to the conflicts between the fluidic operation steps required by the BIST architecture and the constraints on droplet manipulations introduced by the mapping of pins to electrodes. Therefore, we can conclude that the key to implementing the BIST architecture on a pin-constrained chip is to generate a BIST-friendly pin assignment that results in the successful implementation of the bioassay and the BIST architecture.

B. BIST-Aware Pinconstrained Chip Design

A testability-aware pin-constrained chip design is proposed in [33]. The resulting pin-constrained chip design guarantees a test-friendly pin assignment that supports all of the fluidic operations required for functional test and the target bioassay. However, it does not take the compaction of test-outcome droplets on a pin-constrained chip into consideration.

The proposed BIST-aware pin-constrained chip design can generate the pin assignment that guarantees the implementation of the bioassay and the BIST architecture (i.e., the compaction of test-outcome droplets using microfluidic logic gates).

Fig. 22 illustrates the steps of the BIST-aware pin-constrained chip design. The fluidic operations required by the test procedure (e.g., catastrophic test and functional test) merge with the fluidic operations of the droplet manipulation steps needed for the target bioassay. The merging can be carried out by attaching the electrode-actuation sequences for the test procedure to the electrode-actuation sequences for the target bioassay. For each electrode in the array, its actuation sequence during the test procedure is appended to that for the target bioassay to form a longer sequence. Next, fluidic operations required by the test-outcome-droplet compaction (i.e., microfluidic logic gates) are merged with the target bioassay and the test procedure by appending the corresponding electrode-actuation sequences in the same manner. The outcome long electrode-actuation sequences are provided as input to the broadcast-addressing method [34]. The resulting pin-constrained chip design supports not only the target bioassay, but also the BIST architecture, including test procedures and the test-outcome-droplet compaction.

C. Example: Multiplexed Immunoassay

We evaluate the proposed BIST method and the BIST-aware pin-constrained design method by applying it to a multiplexed immunoassay. We have two samples S_1 and S_2, and two reagents R_1 and R_2. Four pairs of droplets (i.e., $\{S_1, R_1\}$, $\{S_1, R_2\}$, $\{S_2, R_1\}$, $\{S_2, R_2\}$) are routed together in sequence

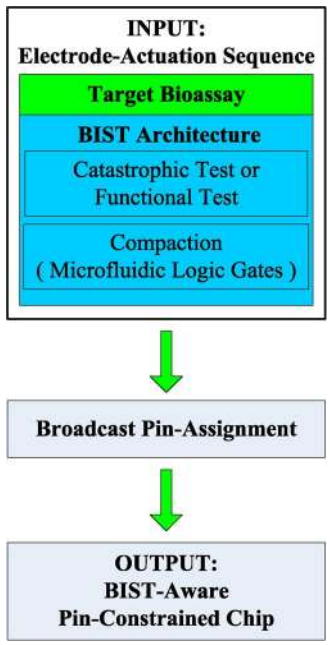

Fig. 22. Steps in the BIST-aware pin-constrained chip design.

for the mixing operation. Thereby, four mixing operations are performed. Finally, each of the mixed droplets is routed to the detection site for analysis. A 15×15 microfluidic array is used here to perform the fluidic operations in the bioassay.

Since the multiplexed immunoassay is implemented only on a group of electrodes in the microfluidic array, rather than the whole array, only this group of electrodes is required for test procedures to validate that they are defect free or malfunction free. The group of electrodes results in an irregular chip layout, where the conventional parallel scan-like test [30] and the functional test [31] cannot be performed directly. In addition, the use of a single test droplet to traverse the group of electrodes leads to high test duration, which is not practical during the field test. Thereby, we use the droplet-trace partitioning method [35] to partition the microfluidic array for the multiplexed bioassay into nine spatial nonoverlapping parts (from P1 to P9), as shown in Fig. 23.

In each partition, one test droplet is used to traverse all of the electrodes in the partition. For simplicity, we focus on the catastrophic test (i.e., move a test droplet across all of the electrodes to detect the physical defects). We also assign an electrode within each partition as the output site where the test-outcome droplet locates. After the catastrophic test in each partition, if there is a test-outcome droplet on the output site, it indicates that there is no defect in the corresponding partition. Otherwise, it indicates that one or multiple electrodes within the partition have physical defects. The output site also serves as the input of the compaction tree of the BIST architecture. The compaction tree of the BIST architecture discussed in Section III-A is implemented to compress all of the nine test-outcome droplets into a single droplet signature. As shown in Fig. 24, the compaction tree consists of several layers of microfluidic logic AND gates, and each of its inputs is connected to an output site of one partition. The compaction tree will be reconfigured by using the

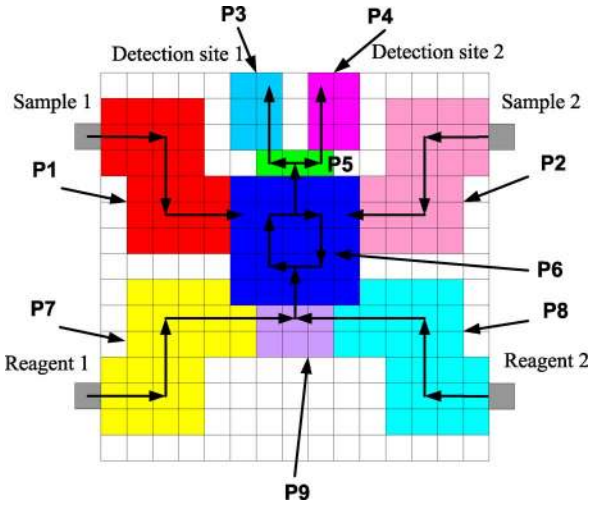

Fig. 23. Microfluidic array partition for the multiplexed bioassay.

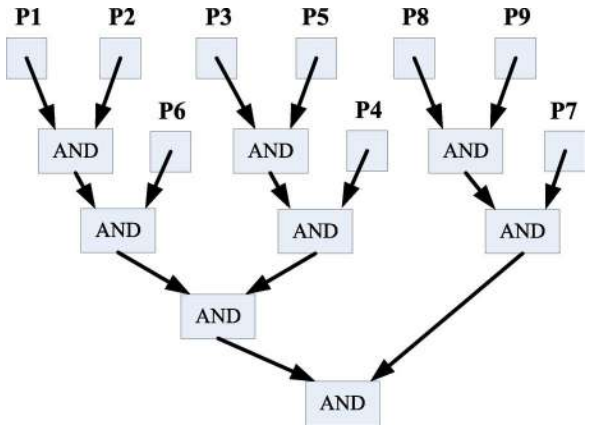

Fig. 24. Schematic of the microfluidic compactor for the multiplexed bioassay.

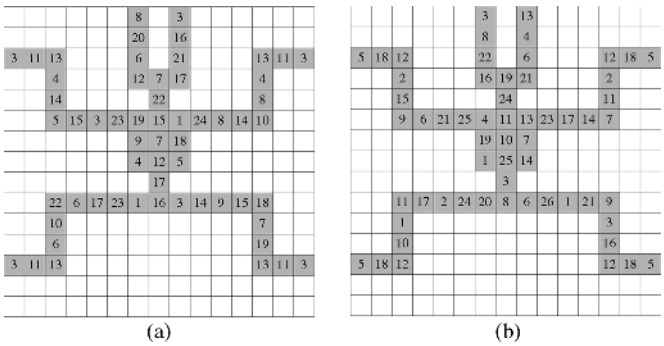

Fig. 25. Pin assignment using broadcast addressing for the multiplexed bioassay: (a) target bioassay and (b) target bioassay and BIST architecture.

electrodes of the irregular chip layout for the multiplexed immunoassay.

We assume a representative clock frequency of 1 Hz [33] (i.e., the droplets are transported at the rate of 1 electrode/s). Given the multiplex bioassay protocol and the module placement in Fig. 23, we can obtain the pin-assignment (using the pin-assignment method in [34]) for the target multiplexed immunoassay, as shown in Fig. 25(a). A total of 24 control pins are needed to perform the bioassay.

Next, we generate the electrode-actuation sequences for the target multiplexed immunoassay, the catastrophic test of each partition, and the implementation of the microfluidic compactor of the BIST architecture. For each electrode in the irregular chip layout for the multiplexed immunoassay, its actuation sequence during the bioassay, the test procedure, and the compaction procedure will be concatenated serially in order to form a longer sequence. The long sequences for all of the electrodes are provided as input to the broadcast-addressing method [34] in order to generate the pin-constrained chip design that supports not only the target bioassay but also the BIST architecture. As shown in Fig. 25(b), a total of 26 control pins are needed to perform the bioassay with the BIST architecture, only two more pins than that for the target bioassay.

We compare the result-evaluation time with and without a compactor. For result-evaluation without a compactor, the test-outcome droplets in all partitions are serially routed to the detection site in either partition 3 or partition 4 for result evaluation. The total time cost for result evaluation without a compactor is 71 clock cycles. For the result evaluation with a compactor, as shown in Fig. 24, the compactor consists of four layers of logic AND gates, and all of the logic operations within one layer can be executed concurrently. Therefore, the total time cost for result evaluation with a compactor is 20 clock cycles.

V. Conclusion

Using the principle of electrowetting on dielectric, we have implemented AND, OR, and NOT and XOR logic gates in the digital microfluidic biochips. We have presented a new built-in self-test (BIST) method for two types of tests: the parallel scan-like test and the functional test. This method utilizes digital microfluidic logic gates to implement various compactors for fault detection. We have also applied the BIST architecture to the pin-constrained chip design to ensure that the target bioassay and the BIST method can be implemented without any pin-actuation conflict. A multiplexed bioassay has been utilized to evaluate the effectiveness of the proposed BIST-aware pin-constrained biochip design method. In our future work, we will investigate the design of a digital microfliudics-based mechanical computer, along the lines of the MEMS-based mechanical computer reported in [5].

Acknowledgment

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