Digital Multimode Buck Converter Control With Loss-Minimizing Synchronous Rectifier Adaptation

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***Abstract*—This paper develops a multimode control strategy which allows for efficient operation of the buck converter over a wide load range. A method for control of synchronous rectifiers as a direct function of the load current is introduced [1]. The function relating the synchronous-rectifier timing to the load current is optimized on-line with a gradient power-loss-minimizing algorithm. Only low-bandwidth measurements of the load current and a power-loss-related quantity are required, making the technique suitable for digital controller implementations. Compared to alternative loss-minimizing approaches, this method has superior adjustment speed and robustness to disturbances, and can simultaneously optimize multiple parameters. The proposed synchronous-rectifier control also accomplishes an automatic, optimal transition to discontinuous-conduction mode at light load. Further, by imposing a minimum duty-ratio, the converter automatically enters pulse-skipping mode at very light load. Thus, the same controller structure can be used in both fixed-frequency pulsewidth modulation and variable-frequency pulse-skipping modes. These techniques are demonstrated on a digitally-controlled 100-W buck converter.**

***Index Terms*—Adaptive control, dead-time, digital control, gradient methods, multimode control, optimization methods, pulse skipping, pulsewidth modulated (PWM) power converters, pulsewidth modulation (PWM), synchronous rectifier (SR), variable frequency control.**

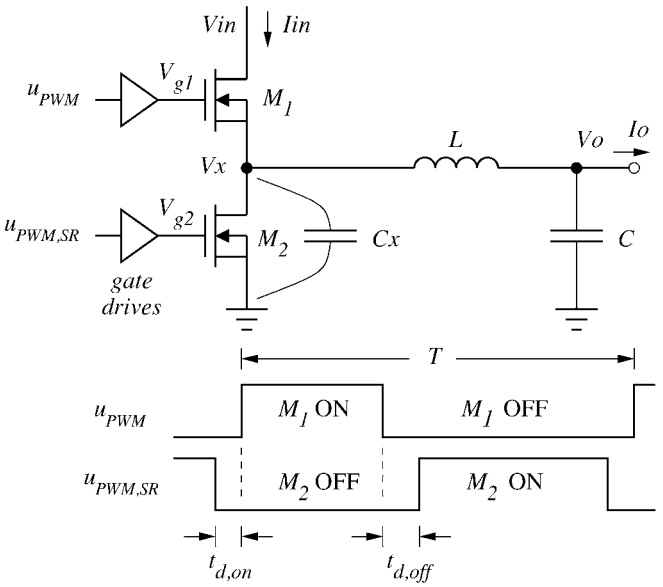

Fig. 1. Buck converter with SR (M_2), and the corresponding MOSFET control signals.

I. Introduction

THE proliferation of digital consumer electronics, coupled with its growing power demands, underscore the importance of improving power-conversion efficiency in both battery-operated and line-connected digital applications. The synchronous buck converter (Fig. 1) and its multiphase version (see, e.g., [3]) are commonly used in voltage regulators (VRs) for microprocessors. Under different load conditions there are different optimal gating patterns for the switches. For large load currents the converter runs in continuous-conduction mode (CCM) characterized by strictly positive steady-state inductor current. At light load, the converter can run in discontinuous conduction mode (DCM), where the inductor current is zero during part of the switching period. At no load or very light load the switching losses dominate, and thus it is advantageous to decrease the switching frequency by entering a variable-frequency mode (e.g., pulse-frequency modulation (PFM), burst mode, or pulse skipping). Finally, the synchronous rectifier (SR) switch (M_2 in Fig. 1) has to be gated appropriately, so as to minimize power losses while the inductor current is circulating through the ground loop.

Multimode control of VRs for hand-held portable electronics, such as cellular phones and PDAs, is quite common since high efficiency is required over a wide load range (typically tens of mA to a few A). Most designs operate in CCM at heavy load with fixed-frequency pulsewidth modulation (PWM) control, and in DCM with PFM control [4]. The transition between the low-power and high-power modes is typically implemented based on some estimate of the load current. Multimode control in higher-power portables such as laptops is less frequently used, however it is becoming increasingly relevant. A laptop power-management method proposed in [5] turns off the SR based on a command from the host microprocessor indicating low-current state. On the other hand, the FAN5093 microprocessor voltage-regulator IC [6] turns off the SR when negative inductor current is detected, allowing the converter to automatically switch to DCM at light load. This part also allows disabling one of its two phases for improved light-load efficiency.

The majority of existing methods for SR control in buck converters rely on high-bandwidth sensing of the gate and drain

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voltages of the switch MOSFETs, using these signals to adjust the SR timing in order to emulate an ideal diode [7]. For example, an ideal diode can be emulated by turning on the low-side MOSFET when its drain-source voltage collapses to zero, and turning off the low-side MOSFET when its drain current decays to zero. The drain current can be sensed via the MOSFET on-state drain-source resistance. Direct implementations of this approach (e.g., in [7]) could suffer from undesirable body-diode conduction intervals due to control and MOSFET switching delays.

Adaptive SR methods have been introduced to overcome control and MOSFET switching delays by predictively setting the SR timing edges based on information from previous cycles [8]–[10]. This technique has been used in a commercial digital implementation [11]. It still relies on MOSFET gate and drain voltage sensing, which has to be done on each phase leg in a multiphase converter, and may require an estimate of the MOSFET threshold voltage. Further, this method might force the converter in CCM at light load, instead of allowing it to enter DCM which is more power efficient.

Since the ultimate objective of SR control is to decrease losses, an alternative approach is to adjust SR timing so as to directly minimize some measure of the power loss. This basic idea is behind the method developed here, and has been pursued in a number of other works as well. In power electronic systems the perturbation naturally introduced by the switching action can be used to optimize the system operation online [12], [13], and it has been suggested to use this approach for SR control [14]. However, this technique cannot successfully adjust parameters which are not directly related to the switching action, such as the SR dead-times. More recently, a method proposed in [15] steps the SR dead-time and measures the resulting change in the converter input current which is related to the efficiency. The dead-time is adjusted in direction of increasing efficiency. Only turn-on dead-time optimization is demonstrated, with the turn-off dead-time kept fixed. A similar method proposed in [16] adjusts the SR dead-times so that the duty-ratio command is minimized, corresponding to maximized efficiency. Each dead-time is initially set to some large value and gradually decreased until the duty-ratio command starts to increase, at which point the algorithm stops. The algorithm is run subsequently for the turn-on and turn-off dead-times. The adaptive algorithm is turned off until a "large" transient is detected, after which it is run again. It is suggested that after a transient the algorithm starts from the point it reached during the previous optimization run. Using the duty-ratio command as a cost function for the dead-time optimization has the major benefit of not requiring sensing and analog-to-digital conversion of any additional quantities besides the output voltage.

Unfortunately, the search algorithms in both [15] and [16] have little robustness to transients and can easily converge to a sub-optimal SR timing pattern in the presence of even minor disturbances. Further, the optimization of the turn-on and turn-off dead-times cannot be done simultaneously. Finally, the speed of convergence to the new optimum after a load transient is limited by feedback stability constraints of the adaptive loop. These could be considerable disadvantages in microprocessor VR applications where the load current may change rapidly and frequently over a wide range [17].

We present an alternative approach based on controlling (scheduling) the SR timing as a direct function of load current, since the optimal SR timing depends strongly on the load current. A load current measurement or estimate is typically available to the controller since it is used for load-line control in VRs [18]. The function relating the optimal SR gating to the load current can be determined off-line and programmed in the controller. Alternatively, it can be obtained on-line by dynamically minimizing the converter power loss via multiparameter extremum seeking. The latter approach is pursued in this work, since it can track drifts in circuit parameters over time. Extremum-seeking control is discussed in [19]–[22]. The extremum-seeking method introduces perturbations in the parameters which are to be optimized (SR dead-times in this case) and measures the gradient of a cost function (power loss, or related quantities). The gradient information is used to adjust the parameters in direction of improving cost function. Quantities besides the power loss which could be used as cost functions are the input current, temperature, or the closed-loop duty ratio, as suggested in [16].

This method does not suffer from the sensitivity to transients and the speed limitations of the algorithms in [15] and [16]. The speed of dead-time response to load-current changes can be set independently of the speed of the loss-minimizing adaptation loop. The load current adjusts the SR dead-times in a direct, feedforward manner, which is not limited by feedback stability constraints, and can therefore provide rapid response to load transients. Thus, the rate of adjustment of the SR timing as a function of the load current can be made as fast as practical (e.g., close to the bandwidth of the main voltage control loop). This capability could be very important in applications such as microprocessor supplies, where the load current can change with a high frequency and slew rate. On the other hand, the loss-minimizing adaptation of the dead-time function can be designed to be much slower, to reduce sensitivity to disturbances caused by transients. The sensitivity to transients is also decreased by demodulating the cost function with the perturbation signal, thus sharply attenuating disturbances at other frequencies. This method can optimize multiple variables (such as the turn-on and turn-off dead-times) simultaneously using a set of orthogonal perturbations. It requires only coarse sampling of the scheduling variable (e.g., the output current) at a rate commensurate with the desired speed of SR timing adjustment. The inductor current can be used as a scheduling variable instead of the load current. Slow variations of other converter parameters on which the power loss depends, such as input voltage and ambient temperature, are compensated for by the extremum-seeking algorithm. Only low-bandwidth sensing of the quantity characterizing the converter power loss is required for the extremum-seeking adaptation. This method is particularly well-suited for a digital controller implementation, since it uses low-rate computations and data storage, thus not requiring analog-to-digital sampling rates beyond the converter switching frequency, which is typically in the range of hundreds of kHz to a MHz.

Importantly, with the proposed SR control method, the converter automatically enters DCM at light load by virtue of the fact that the power-loss in DCM is lower than that in CCM, and the extremum-seeking algorithm converges there. Further,

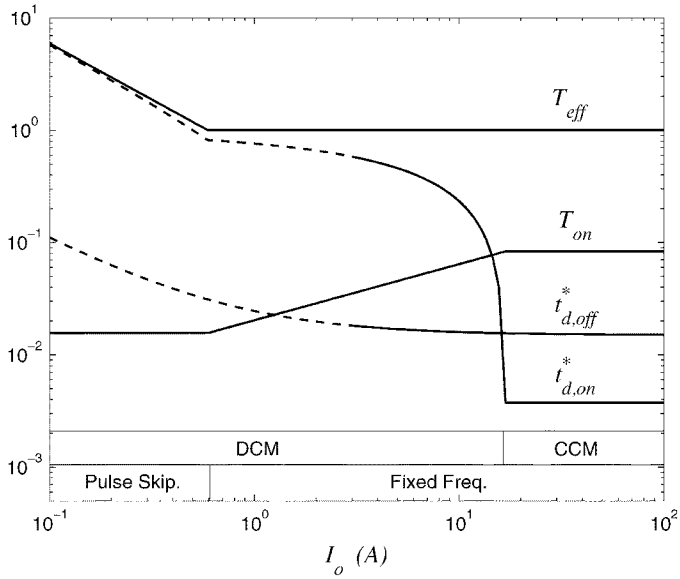

Fig. 2. Timing parameters of the buck-converter control switch and SR for different modes of operation. All parameters are normalized by the fixed-frequency switching period T, and both axes are logarithmic.

by imposing a minimum duty-ratio, which is straightforward to implement in a digital controller, the converter will automatically enter pulse-skipping mode at very light load, effectively decreasing the switching frequency and the associated switching losses. Thus, the same controller structure is used in both fixed-frequency PWM and variable-frequency pulse-skipping modes.

Multimode operation of buck converters is discussed in Section II. Section III develops load-current-scheduled SR control with loss-minimizing adaptation. Section IV demonstrates loss-minimizing scheduled SR control and multimode operation on a digitally-controlled 100-W four-phase buck converter. Section V discusses the proposed techniques in view of the experimental results. Finally, Section VI concludes the paper.

II. Multimode Buck Converter Control

As discussed in Section I, to ensure high efficiency over a wide load range, the buck converter can be operated in different modes depending on the load current. A representative mode diagram, giving the switches' timing parameters as a function of load, is shown in Fig. 2. Parameter T_{eff} is the effective switching period, which is equal to T in fixed-frequency operation (refer to Fig. 1). Parameter T_{on} is the on-time of control (high-side) switch M_1. Parameters $t^*_{d,\text{on}}$ and $t^*_{d,\text{off}}$ are the optimal turn-on and turn-off dead-times, respectively, of the SR (low-side) switch M_2. The modes of operation of the buck converter are cataloged below as follows.

1) Fixed-Frequency CCM: At heavy load the converter operates in CCM with a fixed switching period T. The control switch on-time is $T_{\text{on}} = DT = MT$, where D is the duty ratio, $M = V_o/V_{\text{in}}$ is the conversion ratio, and V_{in} and V_o are the input and output voltages, respectively. The optimal turn-off dead time $t^*_{d,\text{off}}$ depends on the intrinsic turn-off delay $t_{d,\text{off}0}$ of the control switch M_1, and the time it takes to discharge the switching node capacitance C_x

$$t^*_{d,\text{off}} = \frac{V_{\text{in}} C_x}{I_o} + t_{d,\text{off}0} \tag{1}$$

where I_o is the load current. Further, the optimal turn-on dead time $t^*_{d,\text{on}}$ is a small constant, preventing conduction overlap between the control switch and the SR. The power losses in CCM are typically dominated by conduction losses caused by the load current and the inductor current ripple flowing through the switches and the inductor [10], [23, Ch.5].

2) Fixed-Frequency DCM: At lighter load, the converter enters DCM if the SR is gated so that it does not allow negative inductor currents. This happens below load current

$$I_{o,\text{crit}} = \frac{V_{\text{in}} T M(1-M)}{2L} \tag{2}$$

where L is the total inductance (all inductors in parallel in a multiphase converter). The duty ratio now depends on the load current

$$D = \sqrt{\frac{2LI_oM}{V_{\text{in}}T(1-M)}}. \tag{3}$$

The optimal turn-off dead time still follows (1). The optimal $t_{d,\text{on}}$, on the other hand, varies substantially as a function of the load current

$$t^*_{d,\text{on}} = T\left(1 - \frac{D}{M}\right). \tag{4}$$

In DCM, this parameter corresponds to the time the inductor current is zero.

3) Variable-Frequency Pulse Skipping: At very light load the converter loss is dominated by switching losses which are proportional to the switching frequency [23, Ch.5]. Thus, it is advantageous to allow variable frequency operation at very light load. This can be implemented in a straightforward way with a digital controller by limiting the minimum duty ratio to a value D_{min}. [Note that there is a fundamental minimum duty-ratio limit of one DPWM hardware least significant byte (LSB).] The duty ratio limit results in pulse-skipping behavior, effectively reducing the switching frequency. The converter is pulse skipping for

$$I_o < \frac{D^2_{\text{min}} V_{\text{in}} T(1-M)}{2LM} \tag{5}$$

with the average switching period following approximately

$$T_{\text{eff}} \approx \frac{V_{\text{in}} T^2_{\text{on}}(1-M)}{2LI_oM}. \tag{6}$$

The pulse width T_{on} depends on the digital proportional–integral–derivative (PID) parameters and the integrator state. The integral term forces the average error to zero, thus driving the output voltage periodically among the -1, 0, and $+1$ error

bins, resulting in a V_o limit cycle centered at the zero-error bin.[1] Hence, the V_o limit cycle typically has an amplitude of about two analog-to-digital converter (ADC) bins (for example see Fig. 7(d)–(f) in Section IV).

Finally, in a multiphase buck converter, which is the architecture typically used in microprocessor VR's, additional power savings can be realized at light load by disabling some of the phases [6]. This approach completely eliminates the switching losses which would otherwise be contributed by the disabled phase legs. Further, some low-power converter designs gate the SR in very-light-load variable-frequency operation, while others turn it off altogether. The choice depends on the efficiency contribution of the SR. For a particular design, it is beneficial to use the SR at light load if the energy saved by it is more than the energy dissipated to drive it [2, Ch.4].

It should be noted that, at light load there is a design trade-off among the different possible modes of operation: Pulse skipping and reducing the number of phases can decrease power loss, at the price of increased output voltage ripple. Fixed-frequency DCM, on the other hand, has lower ripple, at the expense of higher switching losses. Both of these alternatives are substantially more efficient than CCM operation.

III. Load-Scheduled Loss-Minimizing Synchronous-Rectifier Control

A. Dead-Time Adjustment as Function of Load Current

As suggested by Fig. 2, the SR dead-times can be scheduled as a function of the load current. The functions $t_{d,\mathrm{on}}(I_o)$ and $t_{d,\mathrm{off}}(I_o)$ can be derived from theoretical equations, such as (4) and (1), or obtained from off-line power-loss measurements, and programmed into a look-up table. However, these approaches do not compensate for parameter variability with time and ambient conditions. For example, the optimal SR timing could change with input (e.g., battery) voltage, temperature, component drift, etc. In this section we present an adaptive algorithm which resolves these issues by determining the optimal SR scheduling on-line.

The objective is to adjust the SR timing parameters $t_{d,\mathrm{on}}$ and $t_{d,\mathrm{off}}$ so as to minimize the converter power loss P_{loss} for each load current value. The algorithm is identical for $t_{d,\mathrm{on}}$ and $t_{d,\mathrm{off}}$, and will therefore be presented for a general variable t_d. We parameterize each of the dead-time functions

$$t_d = t_d(I_o, \mathbf{\Theta}) \tag{7}$$

with parameter vector $\mathbf{\Theta} = [\theta_1, \cdots, \theta_m]$. In this work we use a piecewise linear function to implement (7), where θ_j is the jth vertex of the function (Fig. 3). The m vertices are positioned at every $\Delta I_{o,\mathrm{lin}}$ increment of I_o. They are weighted by a vector $\mathbf{W}(I_o) = [w_1(I_o), \cdots, w_m(I_o)]$ toward $t_d(I_o)$

$$t_d(I_o, \mathbf{\Theta}) = \mathbf{W}(I_o)\, \mathbf{\Theta}^T. \tag{8}$$

[1]For a discussion of quantization and limit cycling in digitally-controlled PWM converters see [2, Ch.3] and [24].

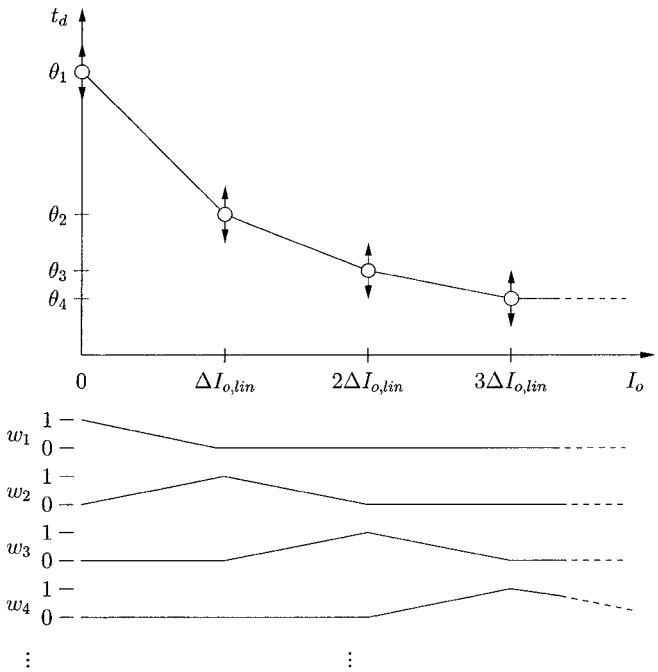

Fig. 3. Piecewise linear function modelling dead-time $t_d(I_o)$ (top), and associated vertex weighting functions (bottom).

The weighting functions $w_j(I_o)$ characterize the fractional distance of I_o to the two neighboring vertices of the piecewise linear function $t_d(I_o, \mathbf{\Theta})$, as shown in Fig. 3. The weighting functions are defined as

$$w_j(I_o) = \begin{cases} 0, & j < \left\lfloor \frac{I_o}{\Delta I_{o,\mathrm{lin}}} \right\rfloor \\ \left\lfloor \frac{I_o}{\Delta I_{o,\mathrm{lin}}} \right\rfloor + 1 - \frac{I_o}{\Delta I_{o,\mathrm{lin}}}, & j = \left\lfloor \frac{I_o}{\Delta I_{o,\mathrm{lin}}} \right\rfloor \\ \frac{I_o}{\Delta I_{o,\mathrm{lin}}} - \left\lfloor \frac{I_o}{\Delta I_{o,\mathrm{lin}}} \right\rfloor, & j = \left\lfloor \frac{I_o}{\Delta I_{o,\mathrm{lin}}} \right\rfloor + 1 \\ 0, & j > \left\lfloor \frac{I_o}{\Delta I_{o,\mathrm{lin}}} \right\rfloor + 1 \end{cases} \tag{9}$$

where $\lfloor x \rfloor$ is the floor function giving the greatest integer less than or equal to x. Thus, the value of $t_d(I_o)$ is obtained by linear interpolation between the two vertices bracketing I_o. The increment size $\Delta I_{o,\mathrm{lin}}$ can be constant or can depend on I_o to suit a particular shape of the fitted function. In the latter case, the indexing in (9) should be adjusted appropriately. Other parametrization approaches could be used, such as realizing (7) with a smooth function, and adjusting its parameters (e.g., a polynomial with tunable coefficients).

B. Dead-Time Function Optimization

To determine the optimal value of the parameter vector, a perturbation-based extremum seeking algorithm is used. Fig. 4 gives a block diagram of the adaptive controller. The controller introduces small, zero-mean perturbations $\tilde{t}_d$ in t_d, at frequency f_d, resulting in modulation of the converter power loss P_{loss}. The power loss can be computed directly from measurements of the input voltage and current, and output voltage and current. Alternatively, other quantities related to the power loss can be used in the optimization, such as the input current [15], temperature [2, Ch.4], or closed-loop duty ratio [16]. The measurement

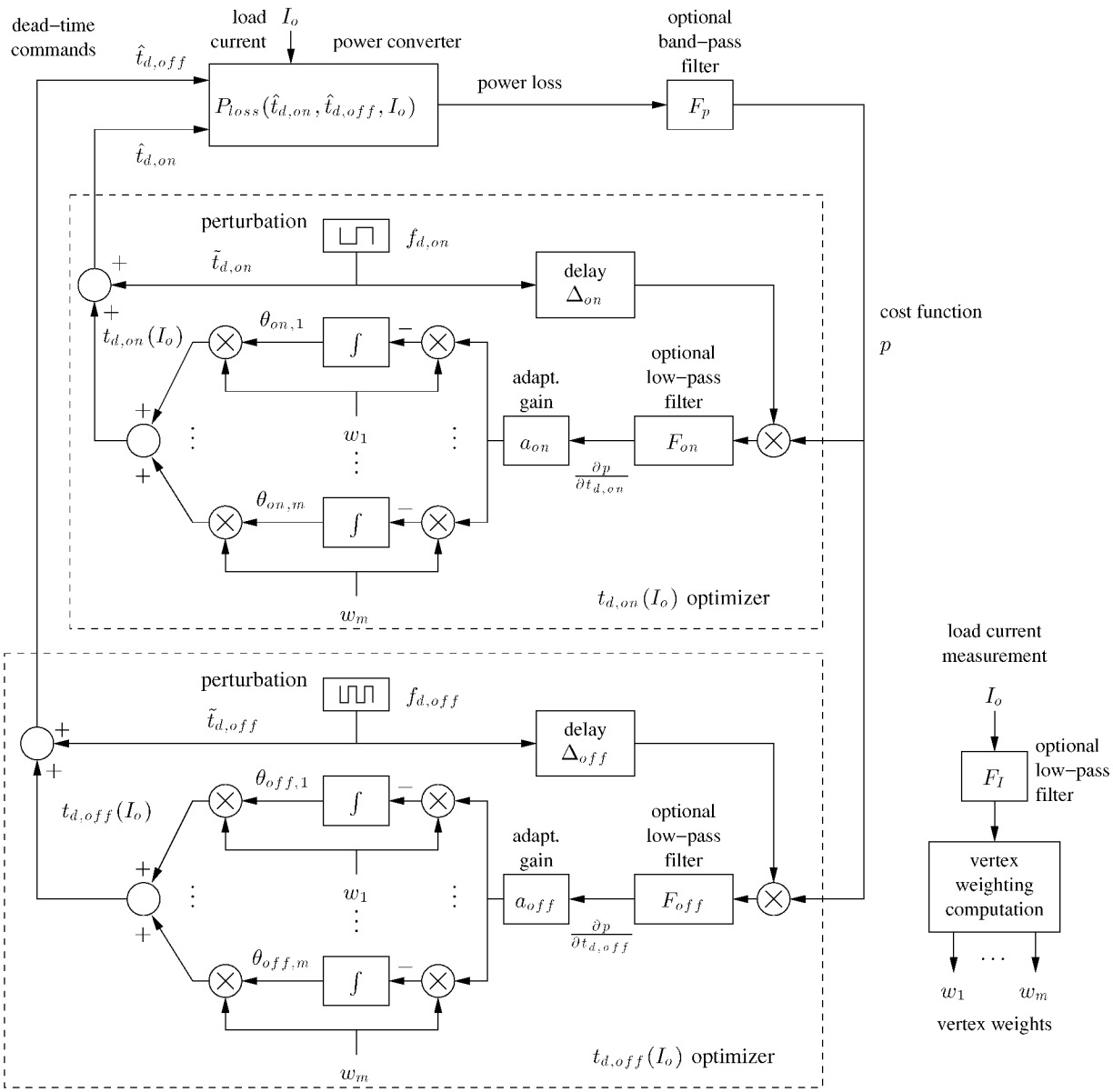

Fig. 4. Block diagram of SR adaptive control using multiparameter extremum seeking. The SR dead-times are scheduled as direct functions of the converter load current. Perturbations at two distinct frequencies are added to the dead-time commands, and the resulting modulation of the converter power loss is used in a gradient-descent algorithm to estimate the two dead-time functions.

of power loss or a related quantity is passed through an optional filter F_p yielding signal (cost function) p which is to be minimized. Filter F_p can be band-pass, blocking the dc levelof the signal, since only the AC components of the signal at the perturbation frequencies are needed for the gradient estimation algorithm [20], [21]. Note that since the power loss signal p can be ac-coupled, window ADC structures, which have high resolution only in a small window around the zero signal level, could be used to quantize it [3]. The power-loss gradient with respect to the dead-time $\partial p/\partial t_d$ can be obtained by demodulating the power-loss signal p with the perturbation signal $\tilde{t}_d$ time-delayed by Δ s [20], [21]

$$p(t)\tilde{t}_d(t-\Delta) \propto \frac{\partial p}{\partial t_d}. \tag{10}$$

The delay Δ models the lag of the converter and sensor response, and the data acquisition and processing delay. Optionally, the gradient estimate can be filtered through a low-pass filter F to reduce the $2\times f_d$ ripple resulting from the perturbation signal [21]. The vertices of $t_d(I_o)$ are updated with a gradient-descent law, which adjusts them in the direction of decreasing power loss

$$\frac{d\mathbf{\Theta}(t)}{dt} = -a\mathbf{W}(I_o(t))p(t)\tilde{t}_d(t-\Delta). \tag{11}$$

Parameter a determines the speed of adaptation. The weighting functions constituting vector $\mathbf{W}(I_o)$ are given by (9), and are hence non-zero only for the two vertices neighboring I_o. Thus, at each iteration the two vertices of $t_d(I_o, \mathbf{\Theta})$ which bracket the load current are adjusted according to the vertex distance from

I_o.[2] As a result, each vertex is adjusted based on gradient information from a $2\times\Delta I_{o,\mathrm{lin}}$ current bracket, resulting in robustness to sensing noise and small undulations of the power loss characteristic due to parasitic ringing. The load current measurement could be low-pass filtered with F_I before the vertex weighting computation implementing (9), to control the speed of response of the dead-times to load changes. The two perturbation signals $\tilde{t}_{d,\mathrm{on}}$ and $\tilde{t}_{d,\mathrm{off}}$ are chosen to be zero-mean and mutually orthogonal to allow independent estimation of $t_{d,\mathrm{on}}(I_o)$ and $t_{d,\mathrm{off}}(I_o)$, respectively. The perturbation signals can be sine or square waves at two different frequencies, for example. Importantly, this algorithm does not need to run fast, since it computes optimal curves for $t_{d,\mathrm{on}}(I_o)$ and $t_{d,\mathrm{off}}(I_o)$, thus requiring only identification of the constant or slowly varying parameter vectors $\mathbf{\Theta}_{\mathrm{on}}$ and $\mathbf{\Theta}_{\mathrm{off}}$, and not the rapidly changing parameters $t_{d,\mathrm{on}}$ and $t_{d,\mathrm{off}}$ themselves. The speed of response of the SR timing parameters is independent of the speed of the perturbation-based adaptation, and is set by F_I which can be made as fast as practical.

In the adaptation problem discussed above there are four time scales: the converter dynamics, the load current dynamics, the parameter-tuning perturbation frequencies, and the parameter optimizer loop time constant. To ensure parameter convergence to a small neighborhood of their optimal values, the system has to be designed so that the parameter optimizer is slower than the perturbation signals, which should be slow compared to the converter dynamics [21]. In some applications, such as microprocessor supplies, the load current can vary at speeds comparable to the converter dynamics. However, high-frequency load-current variations tend to be rejected by the optimization algorithm since these variations are not correlated with the perturbation signals.

IV. Experimental Results

A. Prototype Implementation

The multimode control strategy with adaptive SR scheduling was tested on a digitally-controlled 100-W buck converter. The switching controller with a PID feedback law was implemented with a Xilinx FPGA board. Table I gives the power-train and voltage-controller parameters. The digital control law was implemented as in [3]. Since the converter has four phases, the output voltage is sampled at 1.5 MHz, which is four times the switching frequency, and the duty-ratio command is updated at the same rate. If the duty-ratio command is less than $D_{c,\min} =$ 2 LSB, both the high-side switches and the low-side switches are forced off, to effect pulse-skipping.

The adaptive SR algorithm of Fig. 4 was implemented with a DSPACE real-time control board. Table II lists the adaptive controller parameters. The controller samples the converter input voltage and current, and output voltage and current with 12-b ADCs at a rate of $f_{\mathrm{samp,adapt}} = 11.7$ kHz. The optimized $t_{d,\mathrm{on}}$ and $t_{d,\mathrm{off}}$ commands are sent to the FPGA at the same rate. The piecewise linear curves for $t_{d,\mathrm{on}}(I_o)$ and $t_{d,\mathrm{off}}(I_o)$ have seven vertices each: six of them at 4-A steps between 0 and 20 A, and another vertex at 75 A. The gain of filter F_p lumps the signal conditioning gain before the gradient estimator. The power loss signal is normalized by the load current (above 1 A) to reduce the gain variation of the adaptive loop over the full load range, and to alleviate interference of load transients with the gradient estimation algorithm (see discussion in Section V). Since square-wave perturbations are used, following each perturbation-signal edge, N_{blank} samples of the power-loss signal $p(t)$ are discarded to reduce possible interaction between the voltage-loop dynamics and the gradient estimator.

The prototype also incorporated an option to sample the power-train MOSFETs' temperature and use it as an optimization cost function instead of the power loss computed directly from the input voltage and current, and output voltage and current. The temperature sensing was done with series-connected thermistors tightly mounted on the heat-sink tabs of all high-side and low-side power MOSFETs. One thermistor was mounted on each MOSFET. For brevity, the temperature optimization results are not reported here, but are presented in [2, Ch.4].

TABLE I
100-W Prototype Buck Converter Parameters

	Power Train	
N	number of phases	4
V_{in}	input voltage	12 V
r_s	input source impedance	1 mΩ
$r_{h\phi}$	high-side switch on-resistance	12 mΩ
$r_{l\phi}$	low-side switch on-resistance	3.6 mΩ
L_ϕ	phase inductors	330 nH
$r_{l,\phi}$	inductor ESR & trace resistance	1 mΩ
C	output capacitance (ceramic)	36×100 μF
τ_C	output capacitor ESR time constant	0.8 μs
	PID Controller	
V_{ref}	reference voltage	1.3 V
f_{sw}	switching frequency	375 kHz
f_{samp}	V_o sampling frequency	1.5 MHz
N_{adc}	effective ADC resolution	10 bit
N_{dpwm}	DPWM hardware resolution	7 bit
N_{dith}	dither resolution	4 bit
K_p	proportional gain	2^2
K_i	integral gain	2^{-4}
K_d	derivative gain	2^6
t_{delay}	controller delay	0.7 μs
f_e	error amplifier -3 dB bandwidth	160 kHz
$D_{c,min}$	minimum duty-ratio command	2 LSB (1.6%)
	Loop Gain	
PM	phase margin	40°
GM	gain margin	18 dB
f_c	unity gain frequency	18 kHz

[2]Since multiplication by the weighting vector $\mathbf{W}(I_o)$ is applied twice in the adaptive loop, in (8) and in (11), the adaptive loop gain is varied by a factor of two between the condition when I_o is centered between two vertices, and the condition when I_o coincides with a vertex. This gain variation does not affect significantly the operation of the algorithm, since the adaptation occurs at a slow rate. Further, the gain variation can be easily compensated for by appropriately adjusting the adaptation gain a.

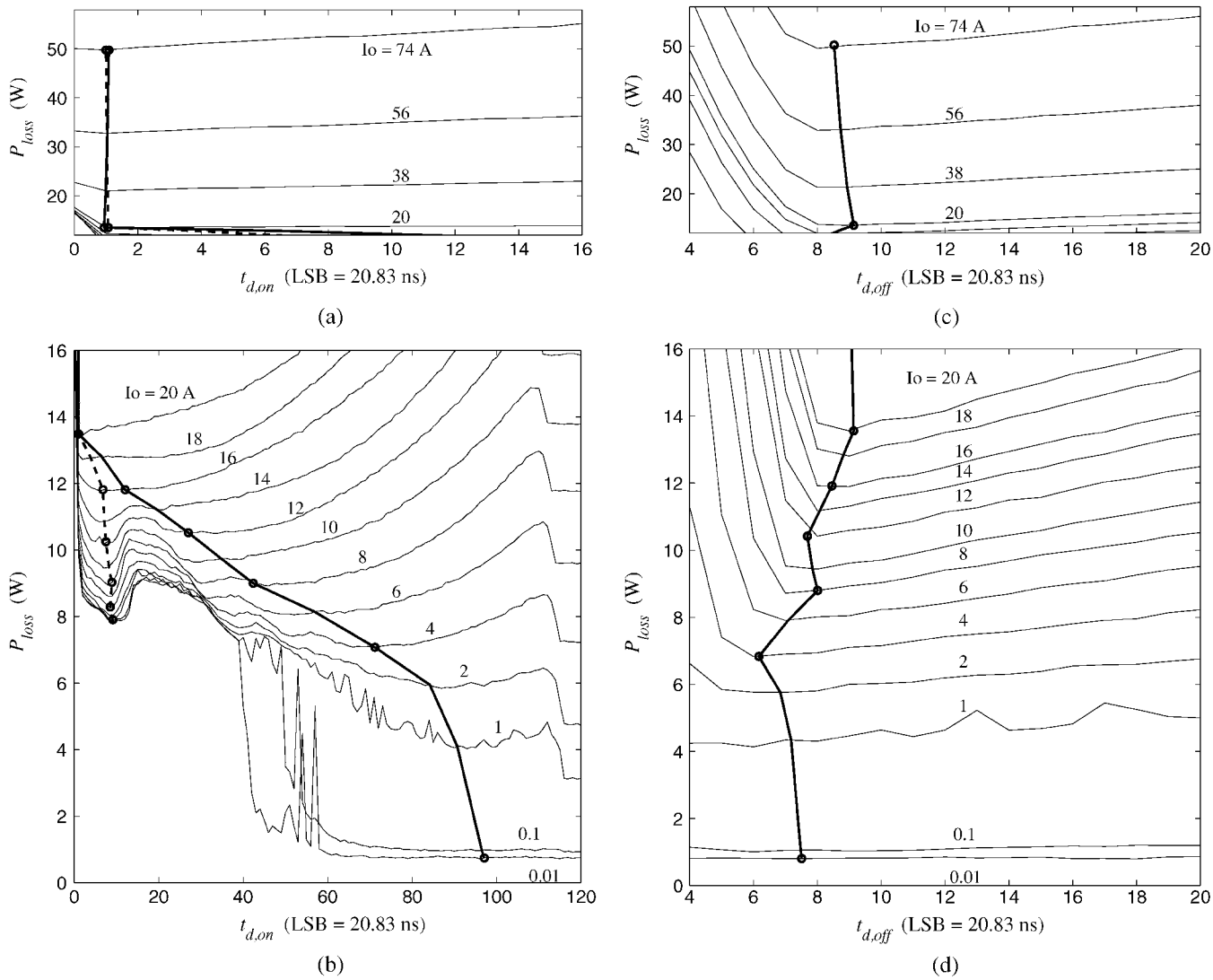

Fig. 5. Power loss as function of $t_{d,\mathrm{on}}$ (a)–(b) and $t_{d,\mathrm{off}}$ (c)–(d) parameterized by load current. Bold lines depict optimal dead-time locus, determined by on-line extremum seeking with power-loss minimization. The "o" symbols represent the vertices of the piecewise linear dead-time vs. load-current functions. In (a)–(b), solid bold line corresponds to optimal DCM operation, while dashed bold line reflects soft-switching behavior by load curent; (a,c) show heavy loads and (b,d) show light loads.

B. Power Loss Map

Fig. 5 shows the static converter power loss (horizontally-oriented curves), measured off-line, as a function of the SR dead-times and parameterized by load current. If the SR is kept off, the converter enters DCM for load currents below 19 A, consistent with (2) in Section II. As a result, at light load the global power loss minimum shifts to large $t_{d,\mathrm{on}}$ values [see Fig. 5(b)], corresponding to the SR turning on when the inductor is discharging, and turning off when the inductor current becomes zero. Under these conditions another local minimum is observed at $t_{d,\mathrm{on}} \approx 8$ LSB [see Fig. 5(b)], corresponding to the converter accomplishing soft-switching by letting negative inductor current charge up the switching node capacitance to V_{in} [8], [25, Ch.20]. This soft-switching behavior is experimentally illustrated in Fig. 7(b). Note that the abrupt dips in power loss at the right end of Fig. 5(b) correspond to the SR being off all the time and thus not contributing switching losses. Furthermore, the minimum duty-ratio command is limited to two LSBs, forcing the converter to enter pulse-skipping mode for load currents below about 2 A, consistent with (5). The abrupt drop in power loss for large $t_{d,\mathrm{on}}$ at very light load (0.1 A and 0.01 A), evident in Fig. 5(b), is due to the transition to pulse-skipping, since pulse-skipping results in substantially reduced switching losses. Finally, in Fig. 5(c)–(d) the optimum $t_{d,\mathrm{off}}$ is approximately constant at heavy load, and decreases by a small amount at light load, which appears to be due to reduced high-side switch turn-off delay.

C. Dead-Time Optimization

Power-loss minimization with the adaptive SR controller was tested while the load current was varied over time to allow for optimization of the complete $t_{d,\mathrm{on}}(I_o)$ and $t_{d,\mathrm{off}}(I_o)$ functions. The power loss was computed from the input voltage and current, and output voltage and current. Convergence of the dead-time functions to a small neighborhood of the power loss minima occurred within a few minutes, mostly limited by the speed of manual adjustment of the load. The initial

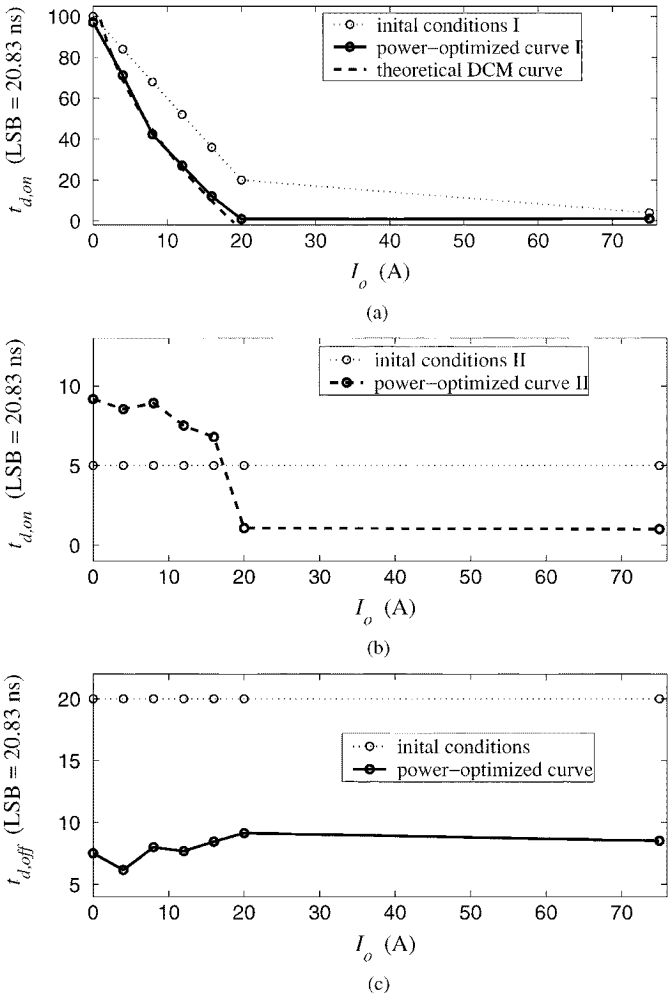

Fig. 6. Dead-times $t_{d,\mathrm{on}}$ (a-b) and $t_{d,\mathrm{off}}$ (c) versus I_o obtained in power-loss minimization experiments. For $t_{d,\mathrm{on}}$ two different initial conditions and the corresponding optimization outcomes are illustrated: (a) corresponds to DCM operation, while (b) reflects soft-switching behavior. This is an alternative representation of the vertically-oriented bold curves in Fig. 5.

conditions and the resulting optimized curves are plotted in Fig. 6(a)–(b) for $t_{d,\mathrm{on}}(I_o)$, and in Fig. 6(c) for $t_{d,\mathrm{off}}(I_o)$. Note that the initial conditions were deliberately set far from the expected optima, to test the effectiveness of the algorithm. Two different initial conditions for $t_{d,\mathrm{on}}$ are explored: With the $t_{d,\mathrm{on}}$ initial conditions in Fig. 6(a) the converter converges to optimal DCM operation for load currents below 20 A. Parameter $t_{d,\mathrm{on}}$ is constant for heavy load, but varies over a wide range for light load, since the optimal SR on-time is a strong function of the load current in DCM. This is predicted by (4) which is also plotted in Fig. 6(a), and matches the experimental data very well. Of course, the calculated curve requires the relevant power-train parameters to be known, which is not practical in general. In contrast, knowledge of the power train-parameters is not necessary for the on-line optimization. The alternative initial conditions in Fig. 6(b) result in an optimized $t_{d,\mathrm{on}}(I_o)$ function which yields soft-switching behavior below 20 A. This is due to the local minimum in the power-loss characteristic associated with soft-switching, which was discussed earlier in the section, and is clearly illustrated in Fig. 5(b). Finally, the optimal $t_{d,\mathrm{off}}(I_o)$ in Fig. 6(c) is dominated by the turn-off delay of the high-side switch, and is thus relatively flat.

TABLE II
ADAPTIVE SYNCHRONOUS-RECTIFIER CONTROLLER PARAMETERS

parameter	value	unit
$\lvert F_p \rvert$	$1/I_o$	LSB/W
F_p high-freq. -3 dB BW	3.4	kHz
F_I high-freq. -3 dB BW	3.4	kHz
$f_{d,on}$	100	Hz (sqr wave)
$\lvert \tilde{t}_{d,on} \rvert$	1	LSB (20.83 ns)
Δ_{on}	0.42	ms
F_{on} high-freq. -3 dB BW	2	Hz
a_{on}	469	
$f_{d,off}$	200	Hz (sqr wave)
$\lvert \tilde{t}_{d,off} \rvert$	1	LSB (20.83 ns)
Δ_{off}	0.42	ms
F_{off} high-freq. -3 dB BW	2	Hz
a_{off}	469	
$f_{samp,adapt}$	11.7	kHz
N_{blank}	10	

To better illustrate the optimality of the obtained $t_{d,\mathrm{on}}(I_o)$ and $t_{d,\mathrm{off}}(I_o)$ functions, they are also superimposed with bold vertically-oriented curves on the power-loss plots in Fig. 5. In Fig. 5(a)–(b), the optimized $t_{d,\mathrm{on}}(I_o)$ curves corresponding to DCM operation are denoted with a solid bold line, while the ones reflecting soft-switching behavior are denoted with a dashed bold line. Clearly, the optimized curves follow closely the power-loss minima over the whole operating range (assuming the SR is gated). Thus, it can be concluded that the algorithm successfully optimized the SR timing as a function of the load current. Depending on the initial condition for $t_{d,\mathrm{on}}(I_o)$, the optimization may converge to DCM operation or to soft-switching at medium and light load. The desired mode of operation can thus be chosen by setting appropriate initial conditions, and further enforced by adding a software limit on the values $t_{d,\mathrm{on}}(I_o)$ can take.

The time constant of the dead-time response to load-current changes was set to be much faster than the adaptation time constants, illustrating a distinct advantage of the presented SR control algorithm. The dead-time/load-current response time constant is determined by the first-order filter F_I, and hence had a value of 47 μs. No attempt was made to explore an even shorter time constant, but it seems that setting it to equal the voltage-loop time constant of 9 μs would be a feasible and suitable choice. In contrast, the parameter adaptation time constants, which depend on the gains a_{on} and a_{off}, are close to 1 s, due to the constraint that the adaptation time constants have to be slow relative to the perturbation frequencies $f_{d,\mathrm{on}}$ and $f_{d,\mathrm{off}}$ (see Table II).

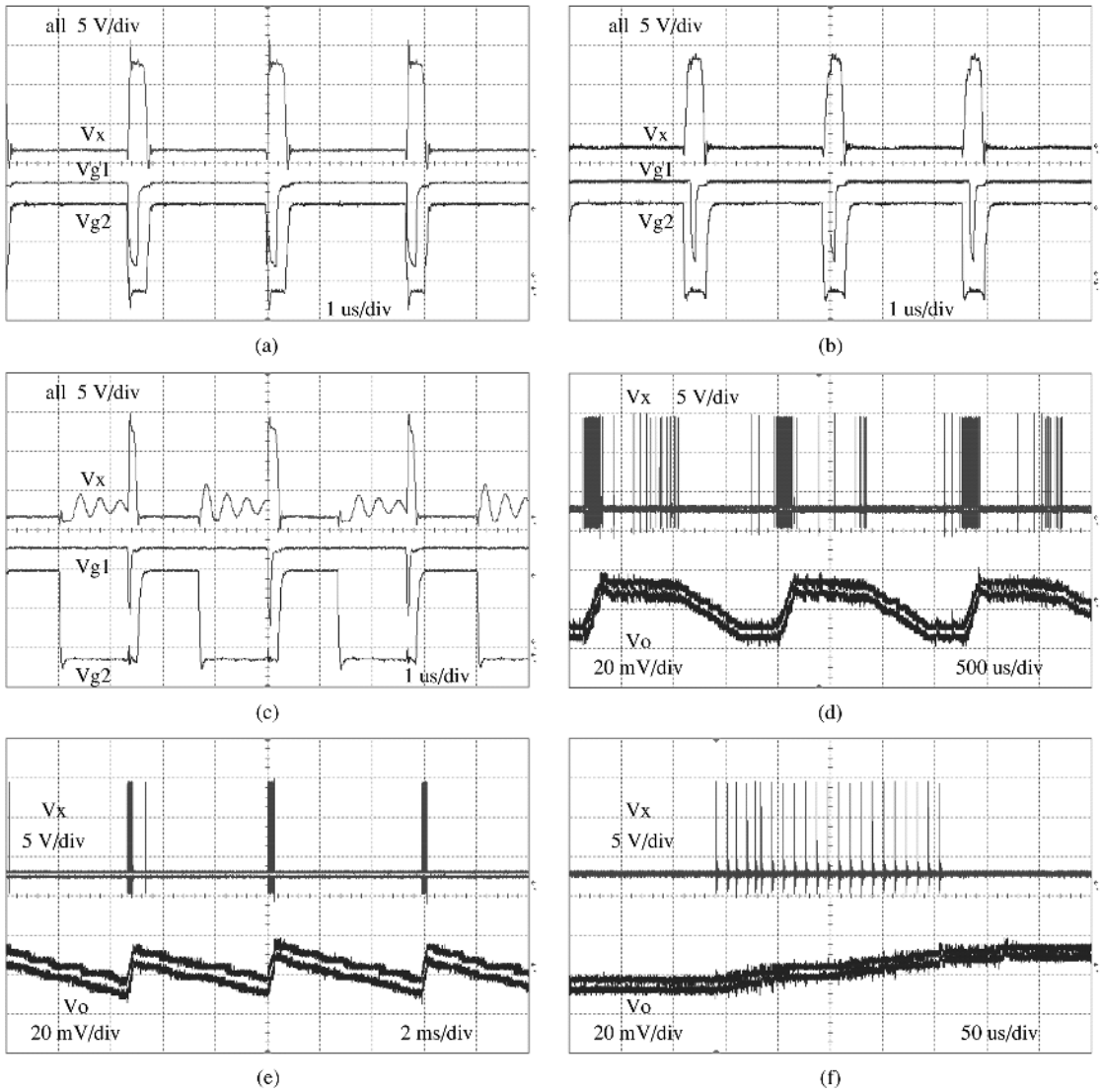

Fig. 7. Sample switching waveforms in DCM and CCM. Parameter V_{g1} is high-side (implemented with PMOS) gate voltage, V_{g2} is low-side (NMOS) gate voltage, and V_x is switching node voltage. In (d)–(f) oscilloscope is in peak-detect mode to capture narrow pulses: (a) CCM operation ($I_o = 35$ A), (b) soft-switching behavior ($I_o = 10$ A), (c) DCM operation with SR ($I_o = 5$ A), (d) pulse skipping ($I_o = 0.1$ A), (e) pulse skipping ($I_o = 0.01$ A); burst frequency $\sim$170 Hz, and (f) zoom of single burst in (e); pulse frequency $\sim$94 kHz.

D. Multimode Operation

Fig. 7 is a gallery of the switching waveforms of one of the four converter phases, illustrating behavior at different load currents with optimized SR timing. Oscillogram (a) shows the converter in CCM at heavy load. Waveform V_{g1} is the high-side(implemented with PMOS) gate voltage, V_{g2} is the low-side (NMOS) gate voltage, and V_x is the switching node voltage (refer to the buck converter diagram in Fig. 1). Oscillogram (b) illustrates soft-switching behavior ($I_o = 10$ A, $t_{d,\mathrm{on}} =$ 7 LSB). Notice the switch-node voltage V_x rising before the high-side switch V_{g1} is turned on, due to negative inductor current charging up the parasitic switch-node capacitance. It could be the case that for designs with very high switching frequencies, the soft-switching mode has better performance than DCM, since it reduces the switching losses. Oscillogram (c) shows DCM operation with gated SR. Oscillograms (d)–(f) illustrate pulse skipping at very light load. The converter settles into a quasi-limit-cycle behavior consisting of periodic switching bursts, followed by off periods. The average interpulse period is modeled by (6). Generally, the switching behavior within each burst is governed by the proportional and derivative terms of the PID control law. When V_o crosses from the zero-error ADC bin to the -1 error bin, an on-pulse is generated with width proportional to $K_p + K_d$. This pulse boosts V_o back into the zero-error bin. No pulses are generated there, since the error is zero, and eventually V_o droops back into the -1 error bin, thus repeating the sequence. The repetitive transitions to the -1 error bin cause the PID integrator to slew up, eventually driving V_o in the $+1$ error bin. This forces an off-state while the integrator is discharging. Thus, the alternation between burst and off state is determined by the integral term, which maintains the output voltage centered at the zero-error ADC bin. Note that the amplitude of the V_o variation is about two ADC bin sizes ($\Delta V_{\mathrm{adc}} = 11.7$ mV), confirming switching among the -1, 0, and $+1$ error bins,

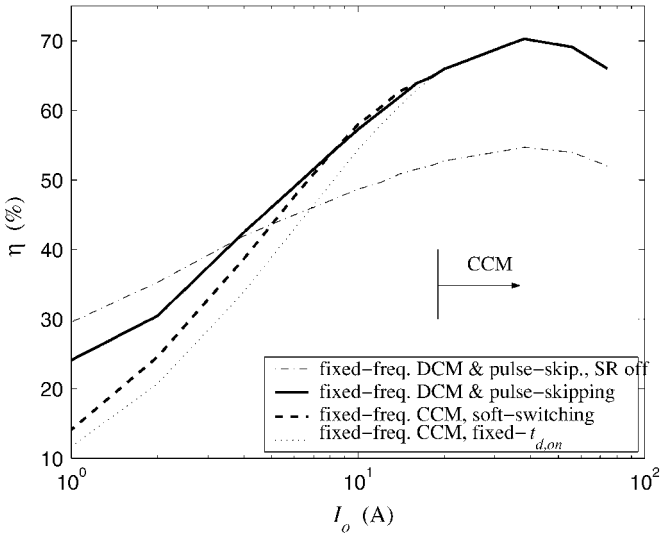

Fig. 8. Converter efficiency η versus load current I_o for various modes of operation. Above the critical load-current value of 19 A, indicated with an arrow, the converter operates in CCM for all control schemes. Below the critical load-current value, the modes of operation are identified in the legends, and explained in the text. The two bold curves represent the outcomes of the adaptive dead-time optimization for two sets of initial conditions.

which satisfies the zero average error condition enforced by the integral PID term.

Finally, Fig. 8 shows the efficiency of the converter in various modes. The overall efficiency is not very high, due to the particular power train used. Informative, however, is the difference in efficiency among the modes. For all control schemes, the converter operates in CCM above the critical load-current value of 19 A. Below the critical load-current value, the converter behavior depends on the control strategy used. For the optimization experiment with initial condition I given in Fig. 6(a), the converter operates in fixed-frequency DCM at intermediate load, and in pulse-skipping at very light load, as discussed above. The corresponding efficiency is plotted with a solid bold line in Fig. 8(a). The efficiency associated with CCM and soft-switching behavior, resulting from initial condition II in Fig. 6(b), is plotted with a dashed bold line. For comparison, the efficiencies associated with fixed-$t_{d,\mathrm{on}}$ CCM ($t_{d,\mathrm{on}} = 2$ LSB) and with the SR off ($t_{d,\mathrm{on}} = 120$ LSB) are plotted as well. These curves correspond to the two modes used in controllers which nominally operate in CCM with synchronous rectification, and turn off the SR completely at light load [5]. By converging into DCM at light-to-medium load (4 A $< I_o <$ 19 A), the SR optimizer improves the efficiency by up to 5% over the better of the fixed-$t_{d,\mathrm{on}}$ and SR-off alternatives. Below about 3.5 A, for this converter configuration it is optimal to turn off the SR altogether (see discussion in Section V). In this case, discontinuous-conduction pulse skipping increases efficiency to 30%, up from 12% for nominal CCM operation at 1 A.

V. Discussion

In the reported experimental results, the power loss used in the dead-time optimization algorithm was computed from the input voltage and current, and the output voltage and current. We have also implemented this algorithm with power-train MOSFETs' temperature minimization [2, Ch.4]. In practical implementations, temperature sensors could be integrated on the MOSFET switch dies, yielding fast thermal response, in which case high-frequency perturbations could be used. Integrating temperature sensors in power MOSFETs would enable other functionality, such as fault control and phase-current balancing based on adaptive thermal equalization among the phase legs, which could enhance the converter reliability [26], [27]. Integrated temperature sensing can be accomplished with a single diode, which has a temperature coefficient of -2 mV/°C, as is done in some modern high-performance microprocessors [28]. Since only the temperature components at the perturbation frequencies are needed for the optimization, the temperature measurement can be ac-coupled before the analog-to-digital conversion, reducing the dynamic range requirements on the ADC. Finally, other cost functions related to power loss can be used, such as the input current [15] or closed-loop duty ratio [16].

In Section IV, it was pointed out that the power loss signal is divided by I_o before being used in the gradient estimator. The reason behind this is that the conduction power loss can be approximated as a function of two multiplicative components: a resistive component which depends on the SR timing, and a component which is a function of only the load current. For example, the latter component is approximately I_o^2 in CCM and $I_o^{3/2}$ in DCM [2, Ch.4]. The purpose of the adaptive algorithm is to minimize the resistive component by adjusting the SR dead-times. The load-current component is not useful for the optimization, and introduces transients in the gradient estimator when I_o changes. Thus, dividing the power loss by I_o reduces gradient-estimator disturbances, as well as adaptive-loop gain variation. An implementation where the cost function is formed by dividing the power loss by I_o^2 and $I_o^{3/2}$ in CCM and DCM, respectively, could perform even better. Essentially, this is a method for extracting the quantity most relevant for the optimization.

It should be noted that the adaptive nature of the power optimization algorithm obviates the need for accurate measurement or estimation of the load current. As long as the scheduling quantity is a monotone increasing function of the load current, the algorithm can work. In fact, other quantities related to the load current, such as the inductor current or even the input current could be used for scheduling.

It was seen in Fig. 7(d)–(f) that at very light load, the converter exhibits pulse-skipping behavior characterized by bursts of switching, followed by periods of no switching. In existing applications, dedicated circuitry is required to implement "burst-mode" control, and to switch between burst-mode and fixed-frequency operation [29]. In contrast, the digital controller presented here automatically enters burst-mode operation at light load by imposing a minimum duty-ratio limit,without modifications of the controller structure. The amplitude of the pulse-skipping limit cycle depends on the resolution of the output-voltage ADC, and is typically about two ADC LSBs. The limit-cycle characteristics can be further controlled by adjusting the PID gains at light load.

The efficiency plot in Fig. 8 indicates that below 3.5 A it is better to turn off the SR altogether. The loss-minimizing gradient algorithm cannot determine this, since turning off the SR

at high values of $t_{d,\mathrm{on}}$ creates a discontinuous local power loss minimum, evident in Fig. 5(b). Therefore, for this configuration, the controller has to be pre-programmed to turn off the SR below 3.5 A. It should be noted, though, that if a more aggressive pulse skipping is used (i.e., $D_{c,\min}$ is made larger), gating the SR at light loads may provide superior efficiency, due to the large peak inductor current value. In such case, the extremum-seeking algorithm can be used to optimize the SR timing over the full load range, including light load.

To further improve the converter efficiency, some of the phases could be disabled at light and intermediate load [6]. For the experimental converter described in this paper, it was determined by measurement that below 38 A it is advantageous to run only two phases, and that below 17 A single-phase operation is optimal [2, Ch.4]. Transition among different numbers of phases can be easily scheduled as a function of the load current in a digital controller. This approach will work well with the adaptive SR control developed above, since the SR timing is scheduled by the load current as well. Further, the gradient SR optimization method can work with any number of phases.

The issues discussed in this section are mostly insights gathered during the development and testing of the experimental prototype, and could be applied toward future controller development, including IC implementations. The SR optimization framework presented in this paper is essentially a type of adaptive feedforward control. It consists of scheduling a control variable as a feedforward function of the load current (or any other measured exogenous parameter which varies rapidly over a wide range), and then adaptively estimating this function. This approach can be applied to a number of other control problems in power converters. For example, using an array of feedback integrators spanning the load range and selected according to the load current, can enhance the transient response associated with load transitions within DCM or between DCM and CCM [2, Ch. 4].

VI. Conclusion

This paper developed a multimode control paradigm which operates the buck converter in CCM at heavy load, in DCM at medium load, and in variable-frequency pulse-skipping mode at light load. The SR timing is scheduled as a function of the load current, and optimized online so as to minimize power loss. Various quantities related to the power loss can be used as cost functions in the optimization. The transition between CCM and DCM is automatically managed by the optimization algorithm. The transition to pulse skipping is effected with a simple limit on the minimum duty-ratio command. In an experimental 100-W buck converter, the adaptive algorithm was able to converge to optimal SR timing, without *a priori* knowledge of the circuit parameters, and starting from initial conditions for the dead-times which were far from the optimal. In both cases, the time constant of the dead-time response to load-current changes was set to be much faster than the adaptation time constant, illustrating the decoupling between the speed of dead-time response and the speed of parameter optimization. Operation in optimized DCM at medium load resulted in up to 5% efficiency improvement. In the experimental converter, it was most efficient to turn off the SR altogether at light load, which could not be determined by gradient-descent algorithm, and therefore has to be preprogrammed in the controller. Pulse skipping with the SR turned off improved the efficiency by 18% at very light load. Generally, whether it is more efficient to disable the SR at light load, depends on the power train and controller parameters. The control paradigm discussed in this paper can effect significant power savings in high-power digital applications, such as laptop and desktop computers. Further, the developed extremum-seeking algorithm, which can simultaneously optimize a number of parameterized functions while providing fast response to transients, can be useful in other power electronic applications.

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