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Digitally-Assisted Dual-Switch High Efficiency Envelope Amplifier for Envelope Tracking Base-Station Power Amplifiers

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***Abstract*—This paper presents a novel digitally-assisted dual-switch envelope amplifier used for wideband high efficiency envelope tracking base station power amplifiers. The proposed envelope amplifier comprises two switching buck converters to provide the high power envelope tracking signal to the RF stage and a wideband linear stage to maintain the envelope signal accuracy. The control technique utilizes digital signal processing in conjunction with analog hysteretic feedback to separately control two high efficiency switchers and thus successfully reduces power consumption of the linear stage, especially for applications requiring high peak-to-average ratio (PAPR) signals. The overall envelope tracking system was demonstrated using GaAs high voltage HBT PAs. For a variety of signals ranging from 6.6 dB to 9.6 dB PAPR and up to 10 MHz RF bandwidth, the overall system power added efficiency reached 50 % to 60 %, with a normalized root mean square error below 1 % and the first adjacent channel leakage power ratio (ACLR1) of -55 dBc after digital predistortion with memory mitigation, at an average output power above 20 W and 10 dB gain.**

***Index Terms*— Dynamic supply modulator, envelope tracking, digital predistortion, memory effects, peak-to-average power ratio, power amplifiers.**

I. Introduction

In order to deliver high speed data, complex modulation schemes are normally employed in modern wireless communication systems. Such modulation techniques lead to non-constant envelopes in radio frequency (RF) transmission signals, which often have a high peak-to-average power ratio (PAPR). Conventional linear power amplifiers (PAs), such as Class A/AB, are good candidates to keep high signal fidelity, however, the average efficiency of these amplifiers becomes very low when transmitting signals with a high PAPR. A number of efficiency enhancement techniques have been proposed in wireless transmitters [1][2]. Among them, envelope-tracking (ET) is one of the techniques that has demonstrated excellent power efficiency improvement for base-stations [3][4][5]. As shown in Fig. 1, ET utilizes an envelope amplifier to dynamically control the supply voltage of the RF PA on the drain/collector, according to the envelope variations of the input signal. This technique enables the RFPA to be operated close to its saturation region over a wide range of power levels, which significantly improves power efficiency of the transmitter, especially for transmitting modulation signals with a high PAPR. The overall efficiency of ET systems depends not only on the performance of the RF power amplifier but also on that of the envelope amplifier that provides an amplitude-varying supply voltage. The RF PA performance may be optimized for ET operation by choosing different device technologies and load impedances [6]. However, increasing demands of wide modulation bandwidths and high data rates pose severe challenges on designing high efficient and high linear envelope amplifiers [7].

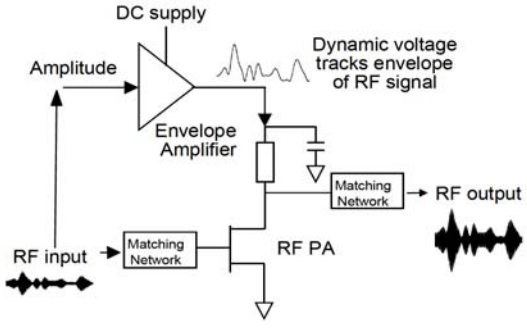

Fig. 1 Envelope tracking power amplifier architecture.

In [8], we demonstrated high efficiency performance of an envelope tracking system using a digitally-assisted dual-switch envelope amplifier that utilizes two high efficiency switch buck

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converters, coordinated with a linear stage, to efficiently provide the wideband envelope signal to the RF PA. Experimental results showed that, by employing this new architecture, the efficiency of the envelope amplifier was significantly increased and thus the efficiency of the overall ET system was increased. And this high performance was maintained for different PAPR signals. In [8], due to limited page space, only the basic concept of the approach was presented. In this paper, we give an in-depth description of the new envelope amplifier design. In particular, we will present the operation principles and the procedures of the digital control signal generation, the envelope amplifier system architecture and detailed design analysis and synthesis. Extensive measurement results and performance comparisons are also given.

The paper is organized as follows. Section II describes the operation methodology of the conventional envelope amplifier architecture. Section III presents the proposed dual-switch envelope amplifier, including digital switch control signal generation mechanism, system architecture and detailed design synthesis. The experimental results are presented in Section IV, with a conclusion in Section V.

II. Analog Single-Switch Envelope Amplifier

In much of the past work, envelope amplifiers are normally implemented with a linear stage in conjunction with a switching buck regulator (switcher), as shown in Fig. 2 [3][9][10]. This architecture includes two stages: a linear stage and a switcher stage. The linear stage is normally designed by using an operational amplifier. It provides a voltage output, V_{out}, that is an amplified envelope of the RF input, V_{in}, to ensure high tracking accuracy obtained at the output. The switcher provides a current output, i_{sw}, and it is controlled by a hysteretic controller that senses the current flowing out of the linear stage, i_{linear}, through a current-sense feedback resistor. The current to the load, i_{out}, is a combination of the current from the linear stage, i_{linear}, and the current from the switcher, i_{sw}. Since the switcher can be operated with higher efficiency than that of the linear stage, ideally and with a proper design, the hysteretic controller should enable i_{sw} to provide the majority of the output current to the PA.

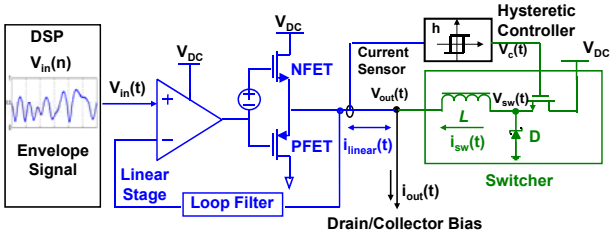

Fig. 2 Analog single-switch envelope amplifier architecture [3]

Fig. 3 shows the simulated output current while the amplifier is excited with a 200 kHz EDGE signal with 8-PSK modulation and 3.2 dB PAPR. In this example, the peak envelope voltage is scaled to 30 V, the load impedance is pure resistive and is set to 5 ohm, and the inductance value is set as 24 μH. We can see that almost all of the output current, i_{out}, is provided by the switcher. The linear stage is only responsible for correcting the switcher output noise and providing a small amount of current. The peak current, that the linear stage must provide, is less than 2 A and this happens only when the instantaneous slew rate of the switcher is lower than that of the output current. In this case, the hysteretic controller successfully controls the switcher to provide the current, i_{sw}, to track i_{out}. The average switching frequency of the switcher is around 1~2 MHz. Experimental results showed that the efficiency was higher than 80 % [11].

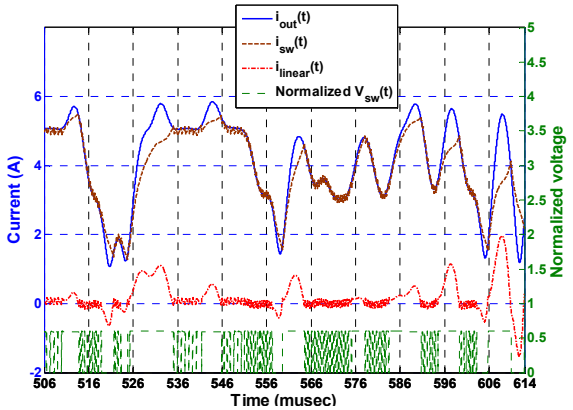

Fig. 3 Simulated envelope amplifier results with an EDGE signal as input.

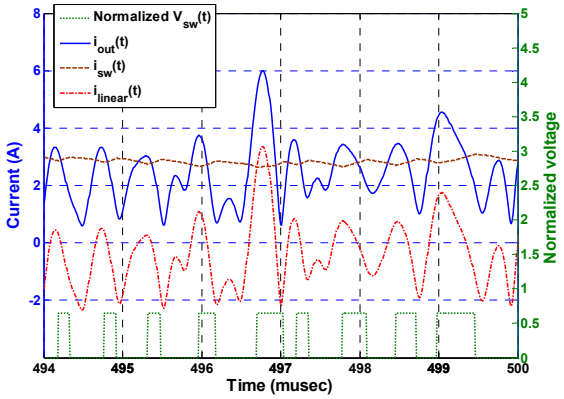

Fig. 4 Simulated envelope amplifier results with a W-CDMA signal as input.

TABLE I
SIMULTED SWITCHER LOSS AND LINEAR STAGE LOSS PERCENTAGE OVER THE ENTIRE DC INPUT POWER FOR AN EDGE AND A W-CDMA SIGNAL, RESPECTIVELY

PERCENTAGE	Linear stage loss	Switcher stage loss
EDGE (200KHz, 3.2 dB PAR)	1.4 %	4.8 %
W-CDMA (3.84 MHz, 7.7 dB PAR)	18.8 %	7.9 %

However, the limited slew rate of the switcher could lead to a different result for the same envelope amplifier excited by signals with a wider bandwidth and a higher PAPR. Fig. 4 shows simulation results using the same envelope amplifier but excited with a 3.84 MHz W-CDMA signal with 7.7 dB PAPR.

In this case, i_{sw} cannot track the envelope correctly, and only provides approximately the average current of i_{out}, due to the situation that the required average slew rate of envelope current is much higher than that of the switcher current [12]. This causes that i_{linear} must source and sink a large amount of the current. In this example, the peak current of the linear stage is around 3.5 A. This leads to high power dissipation in the linear stage, and the overall efficiency is degraded to around 70 % [3]. Table I summarizes the overall loss over the DC input power of the envelope amplifier excited by two different signals. In the case of the W-CDMA signal, the efficiency degradation is mainly due to the low slew rate of the switcher, causing mis-tracking that forces the linear stage to provide the majority of the output current.

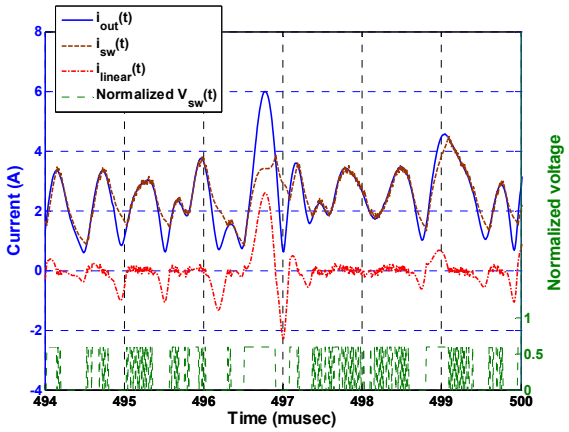

Fig. 5 Simulated envelope amplifier behaviors with 1.3 μH inductor, Hysteresis: 0.025, Test signal: W-CDMA 7.7 dB PAR; Peak envelope voltage: 30 V; Load: 5 ohm.

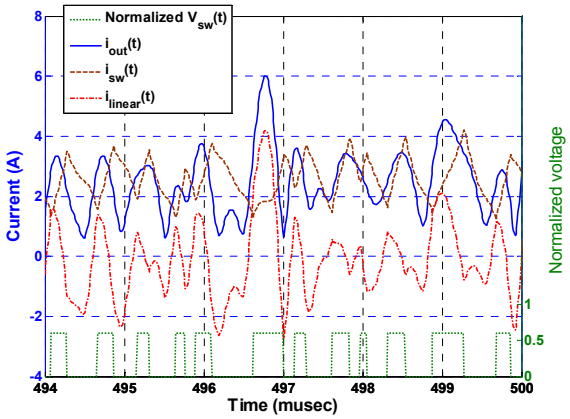

Fig. 6 Simulated envelope amplifier behaviors with 1.3 μH inductor: (a) Hysteresis: 0.025 V, (b) Hysteresis: 0.5 V; Test signal: W-CDMA 7.7 dB PAR; Peak envelope voltage: 30 V; Load: 5 ohm.

To resolve this problem, one possible solution is to use a smaller value of inductor for the switcher to boost the slew rate of i_{sw} to match the required slew rate of the envelope signal. Fig. 5 shows the results when the inductance is reduced to a 20 times smaller value than that used in Fig. 4. In this case, the slew rate of the switcher increases, so that the switcher can provide the majority of the output current now, which is similar to the case in which the envelope amplifier is excited with an EDGE signal, shown in Fig. 3. However, the average switching frequency of the switcher is also significantly increased, e.g., to over 10 MHz for a WCDMA signal. It leads that the power dispassion of the switcher increases due to higher switching loss, even though the current required from the linear stage is reduced.

To avoid increasing the switching frequency, we can choose a larger hysteresis value in the comparator. As shown in Fig. 6, by increasing the hysteresis value from 0.025 V to 0.5 V, the slew rate of the switcher can be improved without increasing the switching frequency. However, a larger hysteresis value causes a long delay between the expected current, i_{out}, and the current provided by the switcher, i_{sw}, and this delay cannot be easily compensated in the analog circuits. Since the linear stage must provide i_{linear} to compensate for the difference between i_{out} and i_{sw}, in order to maintain high tracking accuracy. i_{linear} therefore becomes very large, as shown in Fig. 6, which then results in high power dispassion in the linear stage and thus reduces overall efficiency.

In summary, from the results shown above, we can see that in order to boost the slew rate of the switcher to accommodate wideband signals, a smaller inductor is required. However, this leads that the hysteresis value h must be set to a bigger value; otherwise the switching frequency of the switcher becomes very high, results in high switching loss. A large hysteresis value causes further delays between the expected current and the current provided by the switcher. That requires the linear stage to provide a large amount of current to compensate for the errors, which causes high power dissipation in the linear stage and thus reduces the overall efficiency. It is therefore very difficult to maintain high power efficiency when transmitting wideband signals using envelope tracking, which severely limits the adoption of ET techniques in future wideband wireless systems.

III. Digitally-Assisted Dual-Switch Envelope Amplifier

To cope with the difficulties in the analog hysteretic controller based envelope amplifier described above, in this work, we propose a digitally-assisted dual-switch envelope amplifier that is composed of one linear stage and two high efficiency switchers.

A. Digital Control Signal Generation

Before introducing the dual-switch envelope amplifier architecture, we first present the operation principles of the digitally-assisted switch control signal generation. Instead of using the analog hysteretic controller, in this work, we propose to generate the switch control signal for the switcher using external digital circuits. The principle of the digital signal generation is similar to the operation mechanism of the analog hysteretic controller.

From Fig. 2, we can find that

$$L\frac{\partial i_{sw}(t)}{\partial t} = V_{sw}(t) - V_{out}(t) \quad (1)$$

and

$$V_{out}(t) = g_1 \cdot V_{in}(t) \quad (2)$$

$$V_{sw}(t) = g_2 \cdot V_c(t) \quad (3)$$

where g_1 and g_2 is the equivalent voltage gain of the linear stage and the switcher, respectively. In the discrete time domain, (1) can be written as

$$i_{sw}(n) = i_{sw}(n-1) + \frac{\Delta t}{L}\left[g_2 \cdot V_c(n-1) - g_1 \cdot V_{in}(n-1)\right] \quad (4)$$

where Δt is the sampling interval. In the mean time, i_{linear} also can be expressed in the discrete time domain as

$$i_{linear}(n) = i_{out}(n) - i_{sw}(n) \quad (5)$$

In the analog controller, the current sensor compares i_{linear} with the hysteresis value h to generate the switch control signal, $V_c(t)$, to turn on/off of the switcher. In the same way, we can use (4) and (5), and the following conditions in the digital domain to generate the switch control pulse V_c(n),

If $i_{sw}(n) < i_{out}(n)$-h,
  V_c(n) = 1 (turn on);
else if $i_{sw}(n) > i_{out}(n)$+h,
  V_c(n) = 0 (turn off);
else
  V_c(n)= V_c(n-1).

This means that the envelope amplifier in Fig. 2 can be replaced by the circuit architecture illustrated in Fig. 7, where the switch control signal is directly generated in the discrete time domain by using a digital circuit rather than an analog hysteretic controller.

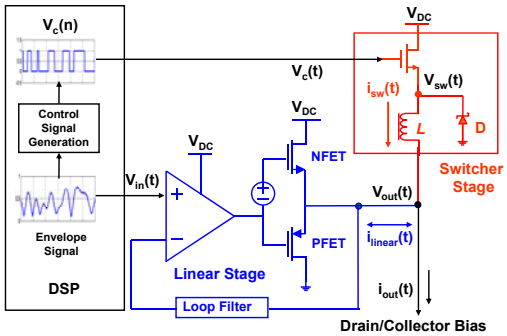

Fig. 7 Envelope amplifier with digital control

Ideally, V_c(t) should force the switcher to provide the current $i_{sw}(t)$ to follow $i_{out}(t)$, the required ideal output envelope signal. However, the approach above suffers the same difficulties as in the analog controller because delay unavoidably occurs in producing the output of the switcher, since the control signal V_c(n) is generated based upon the present envelope signal $V_{in}(n)$. For example, Fig. 8 shows a simulated switching control signal generated using the approach above, and the output current from the switcher and the targeted tracking signal (the envelope waveform). We can see that there are substantial delays between the switcher current and the tracking signal, similar to that occurs in the analog controller shown in Fig 6. This misalignment between the required tracking signal and the actual current supplied by the switcher leads to large errors in the output of the switch. This will require the linear stage to provide a large amount of current to correct the errors, which leads to very low efficiency of the linear stage, and thus reduces the overall efficiency.

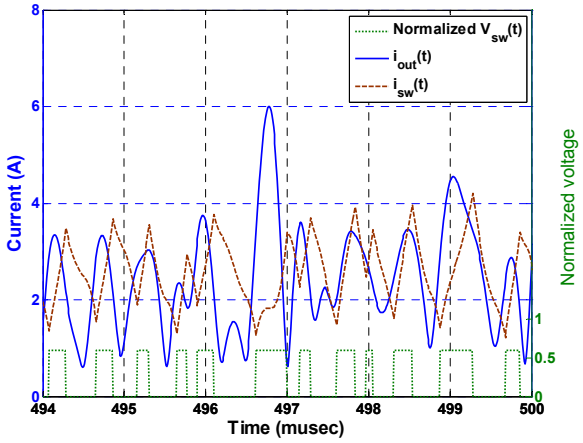

Fig. 8 Transient simulation of envelope signal, corresponding switching control waveform without delay correction (dot), and the switcher current from the main switcher (dash).

Fortunately, unlike the analog controller where the delay is very difficult to compensate, with the digital control, the delay can be easily removed by changing the conditions of the switch signal generation. To compensate for the delay in the hysteretic controller, instead of using the present envelope waveform, we can use the future envelope samples as the reference to generate the switching pulse. If we assume the number of delay samples is k, the pulse generation conditions become

If $i_{sw}(n) < i_{out}(n+k)$-h,
  V_c(n) = 1 (turn on);
else if $i_{sw}(n) > i_{out}(n+k)$+h,
  V_c(n) = 0 (turn off);
else
  V_c(n)= V_c(n-1).

By adjusting the delay k, the dynamic response of the current generated from the main switcher can be aligned with the targeted waveform. Fig. 9 shows the simulated switcher current and the load current after properly adjusting delay of the control signal.

With the digital delay compensation, the slew rate and efficiency problems occurred in the conventional analog envelope amplifier can be resolved, because it allows us to use small inductors and large hysteresis values to accommodate high dynamic wideband signals without decreasing power efficiency. For example, by using the same inductor and hysteresis values for a WCDMA signal, as those used in Fig. 6,

the linear stage output current is significantly reduced, as shown in Fig. 9.

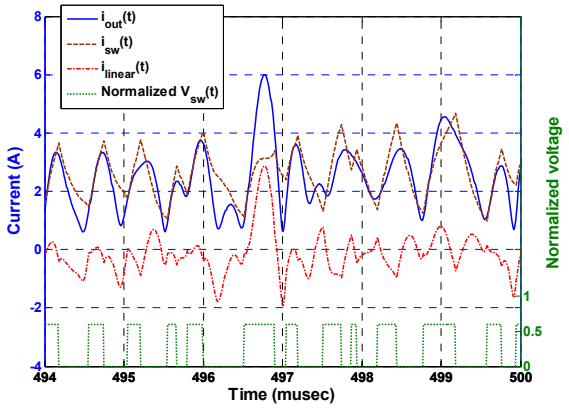

Fig. 9 Simulated envelope amplifier behaviors with 1.3 μH inductor and switcher control delay adjustment.

Unlike other digital signal generation mechanisms using linear modulations, such as pulse width modulation (PWM) [10] where the frequency of the digital signal generated is often much higher than the envelope rate which leads to high switching loss in the switchers and thus reduces the overall efficiency, in this work, the switch control signal is generated by using the same principle of the analog hysteretic control approach, that involves nonlinear process and thus dramatically reduces the switching frequency of the switcher. For example, for a 3.84 MHz WCDMA signal, the average switching frequency is only around 2~3 MHz.

B. Dual-switch Envelope Amplifier Architecture

Ideally, the DSP-assisted envelope amplifier in Fig. 7 can achieve high efficiency for wideband signals by properly designing the switch control signal to force the switcher to provide the majority of the required output current. However, because the digital switch control is an open loop structure, in practice, it cannot be guaranteed that the DC level provided by the switcher always matches the one required by the output. For example, Fig. 10 shows a simulation result for the scenario that the switcher generates DC energy imbalanced with the required output. In this case, the linear stage must provide more DC current to compensate for the errors. High DC current in the linear stage can cause overheating and possibly damage the circuit.

One way to compensate for the DC errors between the open loop switcher and the linear stage is to employ another switcher, called auxiliary switcher, to provide DC current. The structure of the auxiliary switcher can be made as the same as that one employed in the conventional single-switch envelope amplifier but using different transistor/inductor components. This auxiliary switcher can also be controlled by a current-sense analog feedback, where the feedback signal is the magnitude difference between the load current and the total current provided by two switchers. Once the magnitude of feedback signal exceeds a certain level, which is in the case that the linear stage has to provide more power to compensate for the offset, the current-sense stage will trigger the auxiliary switcher to turn on to support the DC imbalance current. Due to the fact that the DC imbalance signal is in low frequency, the auxiliary switcher is not required to have a high speed, or to have a high slew rate, which eases the switcher driver design.

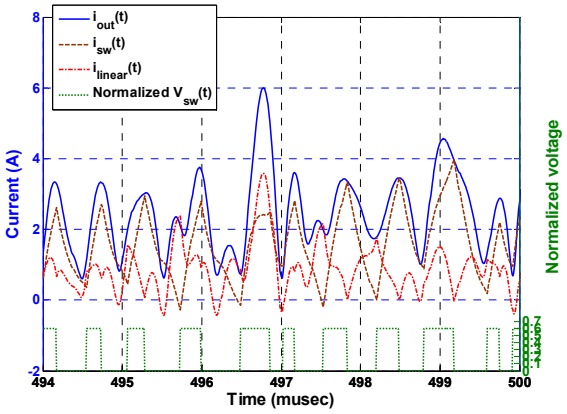

Fig. 10 Simulated DC current imbalance at the output of envelope amplifier

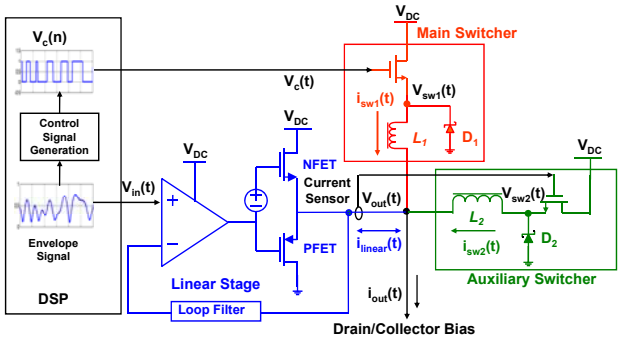

Fig.11 Digitally-assisted dual-switch envelope amplifier.

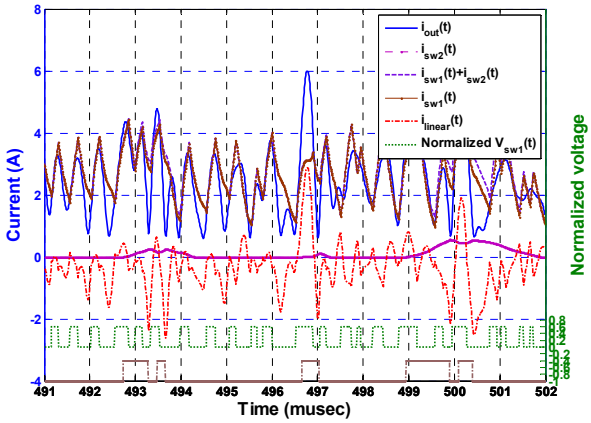

Fig. 12 Simulated dual-switch envelope amplifier behavior.

This finally leads that the proposed complete envelope amplifier comprises one linear stage and two switcher stages in parallel, called digitally-assisted dual-switch envelope amplifier, as shown in Fig. 11. The current supplied to the collector/drain of the RF power amplifier results from the

combined outputs of the linear stage and the two switchers. The main switcher is digitally controlled by a DSP unit while the auxiliary switcher employs an analog current-sense hysteretic controller. The main switcher provides the majority of the current, including a large portion of high frequency parts, to the RF power amplifier, while the auxiliary switcher acts as an assistant switcher to provide part of low frequency current and to compensate DC current imbalances between the linear stage and the main switcher. The linear stage is still functioned as a voltage source to correct any disturbances between the expected output and the one provided by two switcher stages with an internal loop filter, so that the tracking error is minimized. Fig. 12 shows simulation results of the dual-switcher envelope amplifier, where we can see that the majority current is provided by the main switcher while the auxiliary switcher only occasionally turns on to produce low current to compensate for the DC imbalance.

IV. Experimental Results

A. Envelope Amplifier Tests

To evaluate the performance of the proposed design, a dual-switch envelope amplifier was assembled for envelope tracking with the peak voltage at 30 V. The load impedance of the envelope amplifier was 4 Ω. The hysteresis control voltage is chosen as 0.5 V. And 1.6 µH and 25 µH inductor was used in the main and the auxiliary switcher, respectively. A fast switch-FET transistor IRLR120N from International Rectifier was selected for the main switcher and IRFR3518 was used for the auxiliary switcher. The picture of the assembled envelope amplifier is shown in Fig. 13.

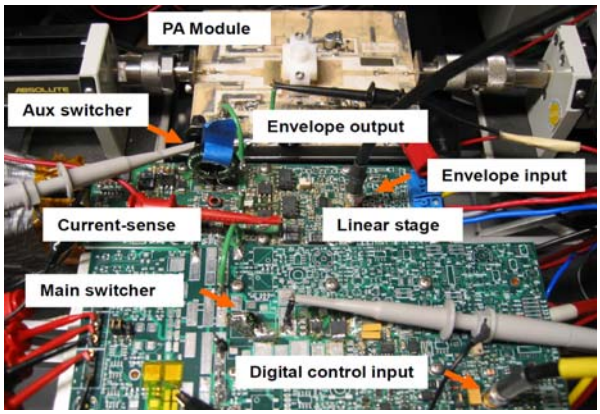

Fig. 13 Dual-switch envelope amplifier hybrid integration on PCB

The two switchers were first tested with periodic pulse signals with roughly 50 % duty ratio as input for the main switcher and 20 % duty ratio for the auxiliary switcher. The efficiency and power loss results are shown in Fig. 14. The main switcher can reach over 80 % efficiency at around 2~3 MHz switching frequency with 50~60 W average output power, while the efficiency of the auxiliary switcher can reach over 90 % with the switching frequency below 1 MHz and with 10 W output power. The full envelope amplifier was then tested with a single carrier WCDMA signal. Fig. 15 (a) and (b) shows the measured waveforms before and after delay adjustment in the main switcher control, respectively, where we can see that, with a proper adjustment, the current from the main switcher can be aligned with the expected current, i.e., the load current.

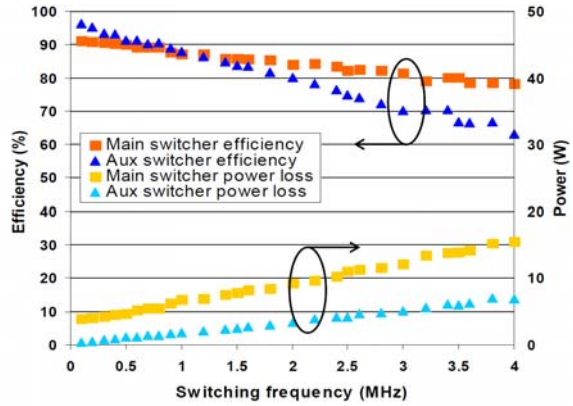

Fig. 14 Measured switcher power loss and efficiency performance versus switching frequency

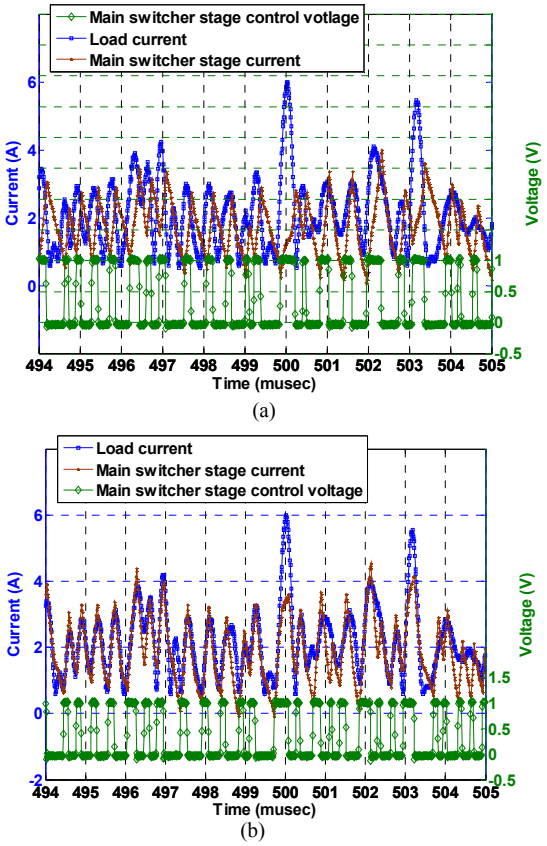

Fig. 15 Measured waveforms of dual-switch envelope amplifier (a) before and (b) after delay adjustment on V_{sw2}

Fig. 16 shows the switching frequency distributions for the main and auxiliary switchers recorded from the experiment. For comparison, the switching frequency distribution of the single switcher in the conventional envelope amplifier, excited with the same W-CDMA input signal, is also shown in Fig. 16. All the distributions are scaled to their peak values. We can see

that the switching frequencies are spitted among the two switchers in the new design that allows us to maximize the efficiency of the switchers separately to effectively handle different frequency components in the tracking signal, so that the optimum efficiency can be obtained for the overall system. However, in the single-switch system, only one switching frequency can be optimized.

Fig. 17 shows efficiency measurements of two envelope amplifiers over different PAPRs for single-carrier W-CDMA signals. Each amplifier was configured for its optimal efficiency with a fixed load impedance during the experiments. The results show that the efficiency of the digitally-assisted dual-switch envelope amplifier is much higher than that of the single-switch envelope amplifier, especially when excited with higher PAPR signals.

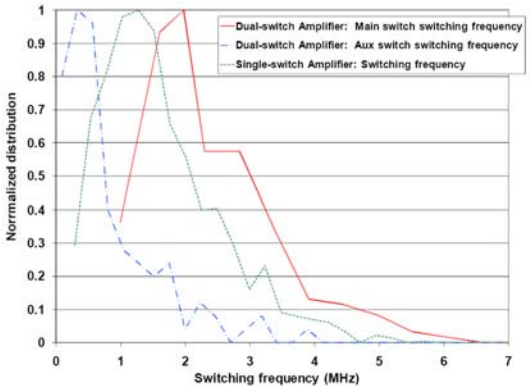

Fig. 16 Measured switching frequency distributions between different switcher stages

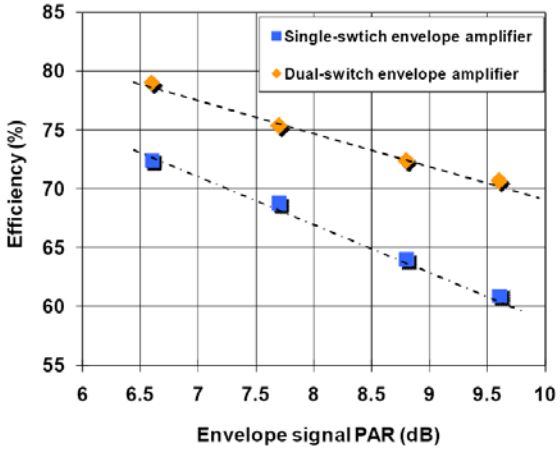

Fig. 17 Efficiency measurement and comparisons between two types of envelope amplifiers using single-carrier W-CDMA signals

B. *Envelope Tracking System Measurements*

To demonstrate the overall performance of the envelope tracking system, the proposed envelope amplifier was tested with two RF power amplifiers, which were both designed by using high voltage InGaP/GaAs HBTs from TriQuint Semiconductor. Two different sizes of devices were used: the first PA employs a Gen 1 device that can produce 130 W peak CW output power, while the second PA uses a Gen 2 device that can achieve more than 250 W at the output. Detailed information about the device technology can be found in [5][13][14] .

The block diagram of the overall measurement system is shown in Fig. 18. The original I/Q baseband signal, the envelope and the digital switch control signal were generated in the digital domain with a clock frequency at 107.52 MHz. The RF up-conversion path used a digital IF frequency of 26.88 MHz. The power amplifier was operated at 2.14 GHz frequency band, excited with 3.84 MHz WCDMA and 10 MHz WiMAX signals. Decresting was performed digitally in baseband [3], which brought the PAPR of the WCDMA signal to a range of 6.6 to 9.6 dB and that of the WiMAX signal to 8.8 dB, respectively. The probe calibration and efficiency measurement setup was the same as that described in [3]. A memoryless digital predistortion and memory mitigation techniques [17] were used for improving linearity of the system.

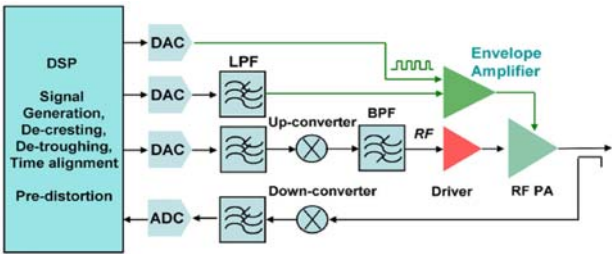

Fig. 18 Envelope tracking system diagram

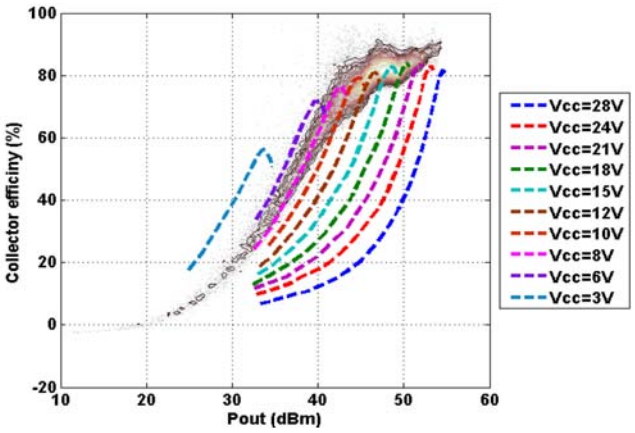

Fig. 19 ET TriQuint Gen 2 GaAs HVHBT RF device collector efficiency versus collector voltage measurement.

Fig. 19 shows the instantaneous collector efficiency measurement of the Gen 2 RF PA using envelope tracing with W-CDMA signals. The collector efficiency is more than 80 % over a broad range of output power (> 10 dB) and peak power is up to 54.5 dBm. The average efficiency after considerations of signal probability density distribution is up to 82% (see Table II). To verify this result, a separate measurement was conducted by using CW signals with constant voltage sweeping from 3 to 28 V on the collector bias. The result is also plotted in Fig. 19. The efficiency measurement matches with the result using envelope tracking at average output power (back off from

the peak about 6~10 dB). Some differences at peak output power level is due to thermal effect.

Table II summarizes the ET system performance before and after digital predistortion. For the HVHBT Gen 1 device [5][13], the average collector efficiency, including dissipation in the envelope amplifier, is as high as 64% with an average output power of 43.5 W for a 6.6 dB PAPR WCDMA signal, while the average collector efficiency of the Gen 2 RF power amplifier [14] is as high as 65.6 % with an average output power of 66.9 W with the same W-CDMA test signal and the corresponding power added efficiency (PAE) is as high as 61.7%. This is the highest efficiency among the reported W-CDMA base-station power amplifiers up to date [5] [8] [15]. For signals with higher PAPRs, such as up to 9.6 dB, the overall PAE is still maintained over 53 %. Table II also gives the measured performance of the ET amplifier with a WiMAX signal with 8.8 dB PAPR and 10 MHz bandwidth. Even though the switching loss of the envelope amplifier is increased [5] when excited with wider bandwidth signals, the overall PAE of the ET power amplifier remains higher than 52 %, which is a significant improvement from previously presented results [5][8]. The high efficiency can be maintained for higher PAPR signals is due to the fact that the slew rate of the DSP-controlled switcher can be made to match the slew-rate of the envelope signals at higher PAPRs, through proper adjustments during the digital control signal generation .

Fig. 20 shows the ACPR performance before and after DPD and memory mitigation for a WCDMA signal. The ACPR after memory mitigation [17] is down to below -55 dBc with the similar efficiency performance [15]. For a higher PAPR, 9.6 dB, W-CDMA signal, the overall ET system PAE maintains above 53 % for the HVHBT Gen 1 device. Fig. 21 shows the ACPR performance for a WiMAX signal. The ACPR after memory mitigation is down to below -48.3 dBc with the similar efficiency performance.

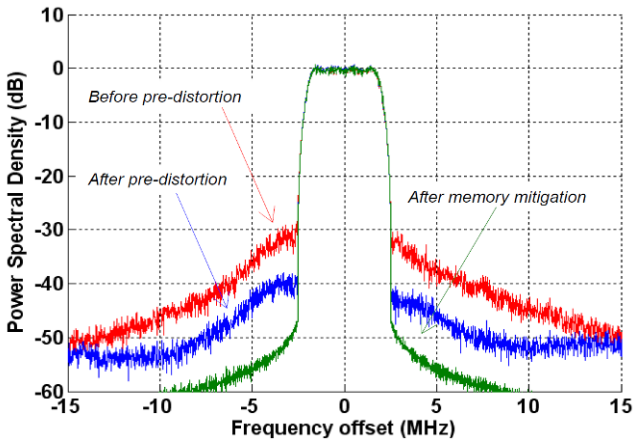

Fig. 20 Measured normalized output spectrum of ET power amplifier before, after DPD and after memory-mitigation using a W-CDMA 7.7 dB PAPR signal.

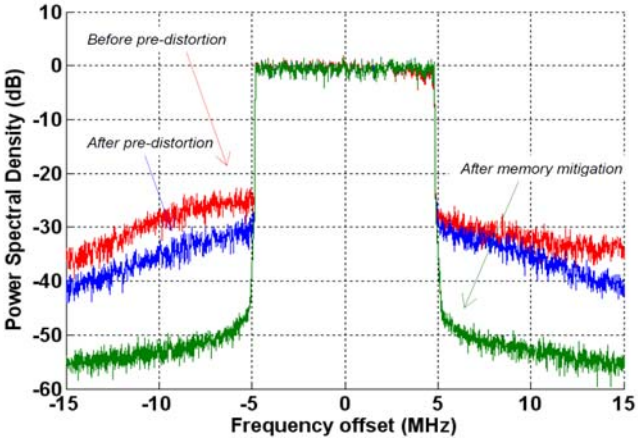

Fig. 21 Measured normalized output spectrum of ET power amplifier before, after DPD and after memory-mitigation using a Wi-MAX 8.8 dB PAPR signal.

TABLE II
PERFORMANCE WITH W-CDMA and Wi-MAX SIGNALS BEFORE AND AFTER DIGITAL PREDISTORTION

Signal Type	DPD	Gain (dB)	P_{out} (W)	CE[1] (%)	PAE[2] (%)	η(PA)[3] (%)	η(env)[4] (%)	EVM (%)	ACPR1 (dBc)	ACPR2 (dBc)
Gen 1 HVHBT										
W-CDMA 6.6 dB PAPR	Before	10.5	43.1	62.9	57.3			7.1	-35.6	-43.9
	After	10.3	43.5	64.2	58.2	82.1	78.2	1.9	-45.5	-50.3
	Memory[5]	10.3	43.4	64.1	58.1			0.5	-57.7	-61.2
W-CDMA 9.6 dB PAPR	Before	10.7	21.9	57.2	52.3			6.5	-35	-44
	After	10.6	22.2	58.1	53.0	82.2	70.7	2.0	-45	-50.1
	Memory	10.6	22.2	58.1	53.0			0.5	-57.8	-61.5
Wi-MAX 8.8 dB PAPR	Before	10.8	26.1	55.7	51.1			9.3	-28	-32
	After	10.6	26.4	57.0	52.0	81.3	70.1	4.9	-33.3	-38.6
	Memory	10.5	26.3	57.0	51.9			0.8	-48.3	-55.2
Gen 2 HVHBT										
W-CDMA 6.6 dB PAPR	Before	12.4	66.2	64.5	60.8			6.8	-35.6	-44.8
	After	12.3	66.9	65.6	61.7	82.1	79.9	2.4	-45.1	-50.5
	Memory	12.3	66.8	65.5	61.6			0.7	-55.5	-60.2

1 Collector efficiency ; 2 CE•(1-1/Gain); 3 RF PA efficiency ; 4 Envelope amplifier efficiency ; 5 Memory mitigation

VI. Conclusion

A novel digitally-assisted dual-switch envelope amplifier architecture has been presented to improve the efficiency of envelope tracking base station power amplifiers excited with wideband signals. The technique utilizes DSP circuits to generate a switch control signal to force the main switcher providing the majority of current required by the RF power amplifier, and use an auxiliary switcher to compensate for DC imbalance and provide low frequency current using analog hysteretic feedback. A wideband linear stage is used at low power to maintain the envelope signal accuracy. The technique significantly improves the efficiency of the envelope amplifier, especially for applications requiring high peak-to-average power ratio signals. The overall system was demonstrated by using GaAs high voltage HBT power amplifiers. For a variety of signals ranging from 6.6 dB to 9.6 dB PAPR and up to 10 MHz RF bandwidth, the overall system PAE exceeds 50%, with normalized root mean square errors below 0.8% and the first adjacent channel leakage power ratio (ACLR1) of -55 dBc after digital predistortion with memory mitigation, at an average output power above 20 W and over 10 dB gain.

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