Digitally Enhanced Software-Defined Radio Receiver Robust to Out-of-Band Interference

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Abstract—A software-defined radio (SDR) receiver with improved robustness to out-of-band interference (OBI) is presented. Two main challenges are identified for an OBI-robust SDR receiver: out-of-band nonlinearity and harmonic mixing. Voltage gain at RF is avoided, and instead realized at baseband in combination with low-pass filtering to mitigate blockers and improve out-of-band IIP3. Two alternative "iterative" harmonic-rejection (HR) techniques are presented to achieve high HR robust to mismatch: a) an analog two-stage polyphase HR concept, which enhances the HR to more than 60 dB; b) a digital adaptive interference cancelling (AIC) technique, which can suppress one dominating harmonic by at least 80 dB. An accurate multiphase clock generator is presented for a mismatch-robust HR. A proof-of-concept receiver is implemented in 65 nm CMOS. Measurements show 34 dB gain, 4 dB NF, and $+3.5$ dBm in-band IIP3 while the out-of-band IIP3 is $+16$ dBm without fine tuning. The measured RF bandwidth is up to 6 GHz and the 8-phase LO works up to 0.9 GHz (master clock up to 7.2 GHz). At 0.8 GHz LO, the analog two-stage polyphase HR achieves a second to sixth order $HR > 60$ dB over 40 chips, while the digital AIC technique achieves $HR > 80$ dB for the dominating harmonic. The total power consumption is 50 mA from a 1.2 V supply.

Index Terms—Adaptive interference cancellation, adaptive signal processing, baseband processing, blocker, blocker filtering, CMOS, cross-correlation, digitally assisted, digitally enhanced, harmonic mixing, harmonic rejection, interference mitigation, linearity, LMS, low-noise amplifier (LNA), low-noise transconductance amplifier (LNTA), mismatch, multiphase, multiphase clock, nonlinearity, out-of-band interference, passive mixer, polyphase, receiver, robust receiver, SAW-less, software radio (SWR), software-defined radio (SDR), switching mixer, wideband receiver.

I. INTRODUCTION

SOFTWARE-DEFINED RADIO (SDR) concepts have recently drawn considerable academic interest and increasingly also industrial interest. Limiting our discussion to RF transceivers, most work focuses on integrating the functionality of multiple dedicated narrowband radios into one radio, which is reconfigurable by software [1], [2]. This is hoped to bring cost and size reductions while supporting an ever increasing set of communication standards in a single device. The SDR concepts might also allow field upgradable radios to accommodate emerging standards and become an enabler for cognitive radio applications, to improve the efficiency of utilizing the scarce spectrum resources.

To support the reception of different radio standards, a wideband radio receiver seems an obvious solution. Some wideband receivers have been reported, e.g., for wideband TV receivers [3], [4], ultra-wideband receivers [5], [6], and SDR applications [1], [2]. However, *wideband receivers are not only wideband to desired signals but also wideband to undesired interference*.

Traditional wireless standards use dedicated radio bands, so that in-band interference (IBI) can be distinguished from out-of-band interference (OBI). For a SDR aiming at covering arbitrary frequencies, the definition of IBI and OBI may become fuzzy. Still, we will use the terms IBI and OBI in this paper as: 1) current SDR receivers often aim at covering multiple traditional radio standards which have clear band definitions; 2) even if this is not the case, e.g., for cognitive radio, a SDR still aims at implementing selectivity, i.e., receive a signal for which baseband bandwidth is much smaller than f_{RF}. In the latter case OBI can be interpreted as "out-of-baseband interference".

For popular mobile communication applications, the IBI can be as strong as -30 to -20 dBm while the OBI can be as strong as -10 to 0 dBm [7]. An RF band-selection filter is often employed to suppress OBI to below the IBI level, requiring high quality factor and sharp roll-off. These filters are difficult to integrate on-chip and are often dedicated to one specific band. In a SDR receiver, the dedicated RF filter is undesired owing to its poor flexibility. State-of-the-art multi-band receivers [8], [9] use multiple dedicated RF filters in parallel, which increases size and cost for every band that is added. This paper aims at improving the robustness of a radio receiver to OBI in order to relax the requirement on RF filters, exploiting fully integrated analog and digitally enhanced mixed-signal techniques.

At least two mechanisms generate in-band distortion due to OBI: 1) nonlinearity related mixing of strong OBI via, e.g., intermodulation or cross-modulation; 2) harmonic mixing of interferers with LO harmonics due to hard-switching mixers and/or the use of digital LO waveforms. We will explain these two mechanisms briefly below as well as review the state-of-the-art solutions for these problems.

A. Out-of-Band Nonlinearity

Nonlinearity may generate intermodulation and harmonic distortion falling on top of the desired signal, or may desensitize a receiver due to blockers and produce cross modulation [10]. Without sufficient RF band-selection filtering, the out-of-band linearity can become the bottleneck since OBI is much stronger than IBI. A wideband LNA as used in [1] and [2] amplifies the desired signal and undesired wideband interference with equal

gain. A low voltage gain of 6 dB can already clip a 0 dBm blocker to a 1.2 V supply. The amplified interference also challenges the nonlinear output impedance of an LNA and the linearity of a next-stage mixer.

LNA linearization techniques have been proposed [11], [12] to achieve an IIP3 in excess of $+15$ dBm but have drawbacks [13]: 1) they often rely on two nonlinearity mechanisms that compensate each other but do not automatically match, so that some kind of fine tuning is needed, compromising robustness to process spread; 2) they mostly rely on modeling of the weakly nonlinear region so that high IIP3 is only achieved for low input two-tone power while limited or no benefit for strong interference.

Recently, a blocker filtering technique has been presented [14], achieved by means of an auxiliary feedforward path, which conducts the undesired interferers and suppresses them by subtracting them from the main signal path at the output of LNA. However it comes with some drawbacks: 1) significant cost arises in terms of noise and power consumption in that auxiliary path; 2) the blocker filtering effect relies on the matching between the main path and the auxiliary path. We will see later in Section II that equivalent functionality can be achieved with much simpler hardware, i.e., without requiring additional signal path.

B. Harmonic Mixing

Linear time-variant behavior in a hard-switching mixer, or equivalently multiplication with a square wave, not only down-converts the desired signal but also interference around LO harmonics. This harmonic mixing is of much less concern in narrowband receivers, relying on RF band-selection filters. The 8-phase harmonic-rejection (HR) mixers as described in [15] can suppress RF signals around second to sixth LO harmonics but amplitude and phase mismatches limit the achievable HR ratio typically to 30-to-40 dB [2]–[4], [16]. However, a quick calculation shows that much more rejection is needed: if we want to bring harmonic responses down to the noise floor, e.g., -100 dBm in 10 MHz for $NF = 4$ dB, and cope with interferers of -40 to 0 dBm, a HR ratio of 60 to 100 dB is needed. State-of-the-art wideband TV tuners rely on RF tracking filters together with HR mixers [3], [4] to guarantee more than 65 dB HR ratio. We aim at removing such tracking filters or at least relaxing their requirements by making HR mixers more robust to mismatch.

C. Contribution of This Paper

Both out-of-band nonlinearity and harmonic mixing can severely degrade signal-to-distortion ratio.[1] Therefore, in our view *a practical SDR should not just be a wideband receiver, but also have enhanced out-of-band linearity and enhanced harmonic rejection.* This paper will propose an architecture to improve the wideband receiver's linearity, especially its IIP3 for OBI and its tolerance to blockers. Moreover, to dramatically improve HR performance, two alternative HR techniques are proposed: 1) a two-stage polyphase HR technique implemented

[1]Signal-to-distortion ratio is so important to software-defined radio that it can be viewed as another interpretation of "SDR".
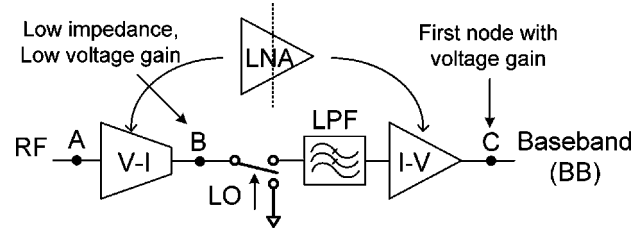

Fig. 1. Conceptual diagram of the low-pass blocker filtering.

purely in the analog domain [17], [18]; 2) a mixed-signal technique exploiting digital adaptive interference cancelling (AIC) [19]. Both improve HR by rejecting harmonics in two successive steps ("iterative"), and both share the same 8-phase RF-to-baseband downconverter as a first HR stage. Compared to [17]–[19], we greatly extend the analysis and show additional experimental results. Compared to [20], this work derives the interference estimate in another way, presents measurements and achieves better performance due to the better interference estimate.

The rest of the paper is organized as follows. Section II introduces a technique using low-pass filtering to mitigate blockers and improve out-of-band IIP3. Section III proposes a two-stage polyphase HR concept to improve amplitude accuracy obtaining high HR robust to mismatch. To improve both amplitude and phase accuracy, a digitally enhanced HR technique using AIC is presented in Section IV. The implementations of the analog front-end and the digital back-end are discussed in Sections V and VI respectively. The experimental results are presented in Section VII with a comparison of analog and digital HR techniques as well as benchmarking to other work. The conclusions are drawn in Section VIII.

II. LOW-PASS BLOCKER FILTERING

Traditionally, narrowband receiver front-ends use LNA-mixer combinations which can deliver good enough linearity, typically an IIP3 < 0 dBm, for in-band (IB) interference while an RF band-selection filter takes care of out-of-band (OB) interference. However, in a wideband receiver, since OBI is much stronger than IBI, the required OB IIP3 is much higher than the required IB IIP3 and even desensitization can occur due to strong OB blockers. Therefore, frequency selective amplification or attenuation is desired. Tunable bandpass filtering (BPF) is in principle a solution, but it is difficult to provide sufficient selectivity and tunability simultaneously with good noise and linearity, using CMOS on-chip filters. Here we approach the problem from another angle.

A. Concept

To guarantee low NF, we need amplification early in the receiver chain. Voltage amplification in an LNA is usually realized via V-I conversion using, e.g., the transconductance of a transistor, followed by I-V conversion via some impedance or transimpedance. We can separate the two functional blocks, V-I and I-V, and insert a passive zero-IF mixer and a low-pass filter (LPF) in between, as shown in Fig. 1. The LPF drawn is conceptually current-in current-out and internally with no voltage swing. However in practice, the functions of the LPF and the

I-V conversion can be merged by using a frequency-dependent impedance, such as a parallel R and C.

It is crucial to present a low impedance over a wide band to the output of V-I block, i.e., node B, so that little voltage gain occurs before filtering, leading to less distortion in the mixer and the nonlinear output impedance of the V-I block.[2] Therefore, the first voltage gain occurs only at baseband after low pass filtering, which provides selectivity to mitigate OBI.

To quantify the blocker filtering effect, we may compare the 1 dB compression point $(P_{1\mathrm{dB}})$ for desired signals to the 1 dB desensitization point $(B_{1\mathrm{dB}})$ for blockers,[3] both input-referred. Assume a third order Taylor series for nonlinearity with α_1 and α_3 for the first and third order coefficients respectively. Without any blocker filtering, it can be derived from [10] that $P_{1\mathrm{dB}} = 10\cdot\log(0.145\cdot|\alpha_1/\alpha_3|)$ and $B_{1\mathrm{dB}} = 10\cdot\log(0.0725\cdot|\alpha_1/\alpha_3|)$, if both in amplitude. Therefore, $B_{1\mathrm{dB}}$ can be calculated based on $P_{1\mathrm{dB}}$, and if without blocker filtering, $B_{1\mathrm{dB}} = (P_{1\mathrm{dB}} - 3\ \mathrm{dB})$.

The LPF in Fig. 1 can mitigate blockers, and its bandwidth (BW) and order (n) determines the blocker filtering effect. If desensitization happens after I-V conversion, which is often the case due to a high voltage gain and limited voltage headroom, the suppression of blockers in dB by the LPF corresponds to the improvement of $B_{1\mathrm{dB}}$.

However, for a wideband receiver the situation is more complicated, as one RF-blocker can be downconverted by different LO harmonics. For instance, a square-wave LO of 400 MHz converts a 1250 MHz RF signal to 850 MHz and 50 MHz via the first and third harmonic of the LO,respectively. The strongest downconverted signal depends on the blocker frequency (f_B) and the LO frequency (f_{LO}), i.e., which LO harmonic the blocker is closer to. Also it depends on the relative gain of the mth harmonic compared to the fundamental (first) harmonic, i.e., the mth harmonic rejection ratio (HR_m).

Assume for simplicity that one blocker component dominates after downconversion and determines $B_{1\mathrm{dB}}$. If $|f_B - m\cdot f_{\mathrm{LO}}| \leq BW$, i.e., the blocker is within the LPF BW after downconversion by the mth harmonic, we find

$$B_{1\mathrm{dB}} \approx (P_{1\mathrm{dB}} - 3\ \mathrm{dB}) + \min\left[HR_m\right]. \qquad (1)$$

If $|f_B - m\cdot f_{\mathrm{LO}}| > BW$, i.e., the blocker is outside the LPF BW after downconversion by the mth harmonic, assuming an asymptotic filter characteristic, we find

$$\begin{aligned} B_{1\mathrm{dB}} \approx &(P_{1\mathrm{dB}} - 3\ \mathrm{dB}) \\ &+ \min\left[n\cdot 20\log\left(\frac{|f_B - m\cdot f_{\mathrm{LO}}|}{BW}\right) + HR_m\right]. \end{aligned} \quad (2)$$

From (2) we can expect smaller bandwidth (BW) and higher order (n) of the LPF gives higher $B_{1\mathrm{dB}}$, if f_B, f_{LO} and HR_m are fixed. Besides, we can also improve $B_{1\mathrm{dB}}$ via improving $P_{1\mathrm{dB}}$, e.g., if compression happens at the receiver output, a lower receiver voltage gain or a larger output voltage headroom can improve the input-referred $P_{1\mathrm{dB}}$, and hence a higher $B_{1\mathrm{dB}}$.

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[2]Another motivation for low impedance at RF nodes is to widen the receiver's RF bandwidth as exploited in [5].

[3]$P_{1\mathrm{dB}}$ thus defines the desired input signal power at which the receiver gain drops by 1 dB without applying blockers, while $B_{1\mathrm{dB}}$ defines the undesired input interference (single-tone blocker) power where the receiver gain drops by 1 dB.
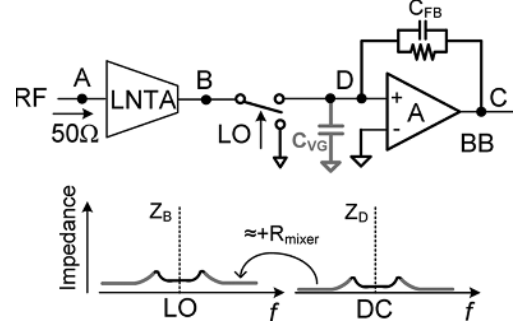

Fig. 2. Realization of the low-pass blocker filtering and illustration of impedance transfer effect.

The LPF can help to relax the OB linearity of the I-V conversion, however *not* for the V-I conversion. Therefore, the maximum achievable $B_{1\mathrm{dB}}$ is ultimately limited by the $P_{1\mathrm{dB}}$ of the V-I conversion minus 3 dB. Thus, linearity of the V-I conversion is very important and we will return to that point in Section V-A. Via a similar mechanism, the OB IIP3 can also be enhanced compared to the IB IIP3.

B. Realization

A specific realization of the general concept (Fig. 1) is presented in Fig. 2. Zero-IF receivers commonly use an LNA followed by a mixer with current output loaded by a LPF to suppress interference. We carry this approach one step further by entirely removing the voltage-gain LNA before the mixer and instead use a Low Noise Transconductance Amplifier (LNTA) as the first RF stage for the V-I conversion with input impedance matching. As mentioned before, maintaining a low impedance at node B over a wide band is important. This can be realized by using low-ohmic switches in the passive mixers followed by transimpedance amplifiers (TIA) built via negative feedback around operational transconductance amplifier (OTA). The feedback network consists of R & C in parallel to form a LPF. At high frequency, the feedback loop gain drops so the virtual-ground impedance rises. By putting a capacitor C_{VG} to ground or across the differential virtual-ground nodes, the impedance at high frequency is reduced. Both C_{VG} and C_{FB} contribute to the total LPF function.

Fig. 2 also shows, qualitatively, the impedance relationship between node B (Z_B) and node D (Z_D), i.e., Z_B is roughly equal to a certain scaling factor times Z_D plus the mixer switch-on resistance (R_{mixer}) and shifted in frequency. Applying an RF current input, it can be derived [21] that, for an N-phase mixer driven by 1/N-duty-cycle (non-overlapping) LO, the impedance Z_B at an RF around m^{th}-LO-harmonic frequency $(m = 1, 2, 3\ldots)$, i.e., with an offset frequency Δf from $m\cdot f_{\mathrm{LO}}(|\Delta f| \leq f_{\mathrm{LO}}/2)$, can be written as

$$Z_B(m\cdot f_{\mathrm{LO}} + \Delta f) \approx R_{\mathrm{mixer}} + \frac{N}{m^2\cdot\pi^2}\cdot\sin^2\left(\frac{m\cdot\pi}{N}\right)\cdot Z_D\left(\Delta f\right). \tag{3}$$

Please note that (3) holds given that Z_D presents strong filtering effect, e.g., a pole at a much lower frequency than f_{LO}, which is normally the case for a downconversion mixer. Consider $m = 1$: for $N = 2$ or 4 the coefficient of Z_D is about 0.2, and for
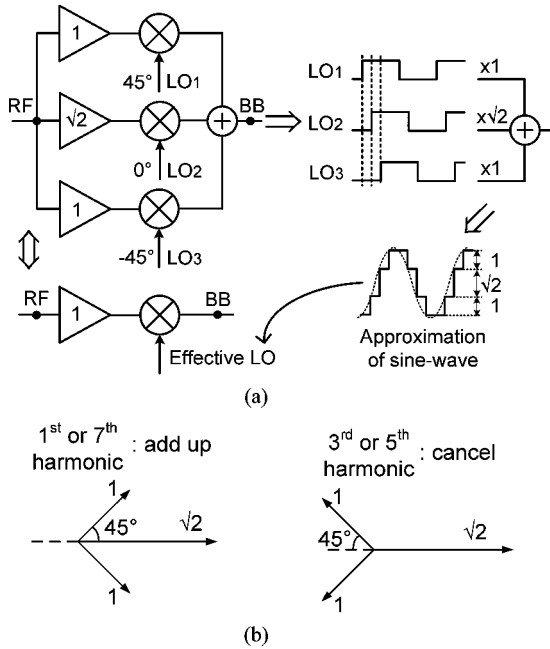
Fig. 3. (a) Block diagram of a traditional HR mixer, and (b) its vector diagram.

$N = 8$, it is about 0.12, showing R_{mixer} actually plays a much larger role in determining Z_B. For $m > 1$, the coefficient of Z_D is even smaller.

Besides delivering low impedance, this topology (Fig. 2) can also bring two other advantages exploited in some *narrowband* receivers [22]–[24]: 1) good *in-band* linearity in the I-V conversion due to the negative feedback; 2) low 1/f noise from the mixer switches working in the linear region which carry little DC current. This work [17] exploits this topology in a *wideband* receiver to enhance *out-of-band* linearity. If the LPF suppresses the OBI well, the main contributor to the OB nonlinearity will come from the V-I conversion of the LNTA, which can be quite linear as we will see later.

Although voltage amplification is avoided at RF, if the transconductance of LNTA is big, the receiver-input-referred noise of the following stages, i.e., mixer and TIA, can be relatively small, so that the overall receiver NF can still be good and dominated by LNTA itself. As an example, the whole receiver in [24] achieves an NF of 2.2 dB based on a similar topology but in a narrowband configuration.

III. TWO-STAGE POLYPHASE HARMONIC REJECTION

The low-pass blocker filtering technique presented in the previous section acts after mixing, so it cannot prevent the harmonic mixing already occurring in the mixer stage. It is known that using balanced LO can suppress all even-order harmonics. To also suppress odd-order harmonics, harmonic-rejection (HR) mixers using multi-phase square-wave LOs driving parallel operating mixers have been proposed before [15], [16]. Fig. 3(a) shows an example, where the weighted current outputs add up to approximate mixing with a sine-wave LO. The combination of an amplitude ratio of $1:\sqrt{2}:1$ and an 8-phase LO[4] (equidistant $45°$) can reject the third and fifth harmonics, as shown in the

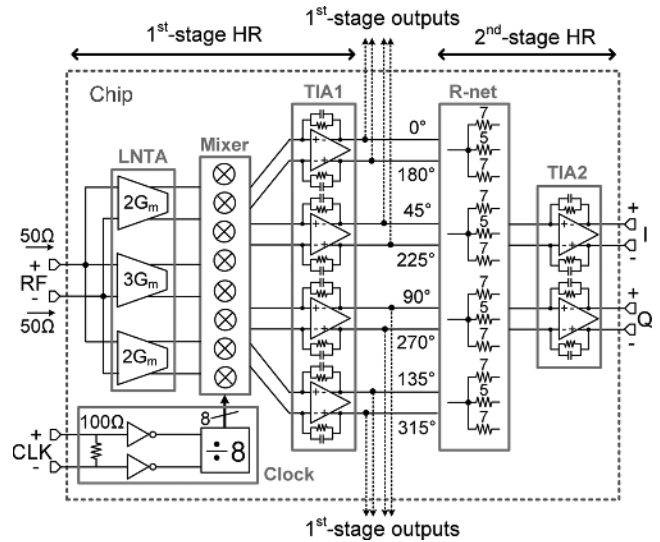[4]Using more LO phases can reject more harmonics, but it complicates LO generation.

vector diagram of Fig. 3(b). The seventh harmonic is not rejected and still needs to be removed by filtering, but the filter requirement is strongly relaxed compared to the case of a normal I/Q mixer whose first un-rejected harmonic is the third order. However, the achievable HR ratio is limited by the accuracy of the amplitude ratios and the LO phases.

To achieve high HR ratio we need to accurately implement the desired weighting ratios, in this case the irrational ratio $1:\sqrt{2}$ accurately on chip. There are at least two challenges here: 1) realizing the right nominal (average) ratio; 2) keeping random variations due to mismatch small enough. To address these issues we propose a two-stage polyphase HR concept (see Fig. 4) in which two-stage iterative weighting and summing results in much higher HR than traditional HR mixers with only one stage. We will show that this iterative weighting results in a small product of relative errors for random variations, whereas the use of suitably chosen integer ratios results in sufficient accuracy to achieve a HR well above 60 dB.

A. Block Diagram

Fig. 4 shows the block diagram of the two-stage polyphase HR system, implemented on chip. The irrational ratio $1:\sqrt{2}:1$ is realized in two iterative steps with integer ratios: a first step with 2:3:2 and a second step with 5:7:5. The first-stage weighting is realized via 7 unit-LNTAs interconnected in 3 parallel groups to form the 2:3:2 ratio. The second-stage weighting is realized via a baseband resistor network "R-net" between the TIA1 and TIA2 stages. The 5:7:5 amplitude ratio corresponds to the 7:5:7 resistance ratio. The passive mixer array is driven by 8-phase 1/8-duty-cycle (non-overlapping) LO. Via the combination of the LNTA, mixer and TIA with LPF, the first voltage gain occurs at baseband after LPF for good OB linearity. Since harmonics can be as strong as blockers, it is important to have significant HR before the first voltage gain, especially because the antiblocker filtering does not reduce harmonic images close to harmonics of the LO, as shown in (1). The additional more accurate HR follows in the second stage, aiming to bring residual harmonic images below the noise floor.

Fig. 4. Chip block diagram implementing the two-stage polyphase HR and the low-pass blocker filtering.

Fig. 5. Weighting factors for the first-stage HR outputs versus time.
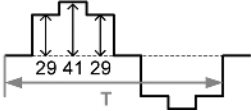
Fig. 6. Approximation of $1:\sqrt{2}:1$ as 29:41:29 via integer ratios.
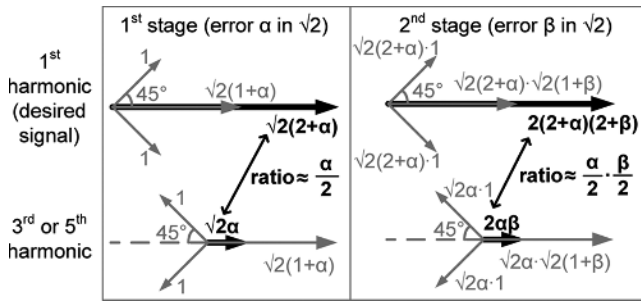
Fig. 7. Error reduction principle in the two-stage polyphase HR (error $\alpha/2$ becomes a much smaller product of errors: $\alpha\beta/4$).

B. Working Principle

We will now show how we accurately approximate $1:\sqrt{2}:1$ via 2:3:2 and 5:7:5. A key point is that the output of the TIA1 stage has 8 IF-outputs with equidistant phases, i.e., $0°$ to $315°$ with $45°$ step, instead of the conventional 4 phases, i.e., quadrature. This enables iterative HR by adding a second stage. Fig. 5 shows the weighting factor for the 8 outputs of the first-stage HR versus time (t) for one complete period of the LO (T). If we weight and sum three adjacent-phase outputs of the first-stage HR via the second-stage weighting factors 5:7:5, as shown in Fig. 6, we find 29:41:29. The ratio 41:29 is equal to 1.4138, which represents only a 0.028% error from $\sqrt{2}$. This amplitude error corresponds to a HR ratio of more than 77 dB, if no phase error.

The two-stage polyphase HR not only can approximate $1:\sqrt{2}:1$ very closely, but it is also robust to amplitude mismatch, as illustrated in Fig. 7 via vector diagrams of the two stages. It shows how, for the desired signal, polyphase contributions from three paths add up, while for the third and fifth harmonics, they cancel nominally. Assume now that the error in realizing $\sqrt{2}$ dominates and model it as a relative error β for the first stage and α for the second stage. Also for simplicity, assume that the desired signal and the third and fifth harmonics
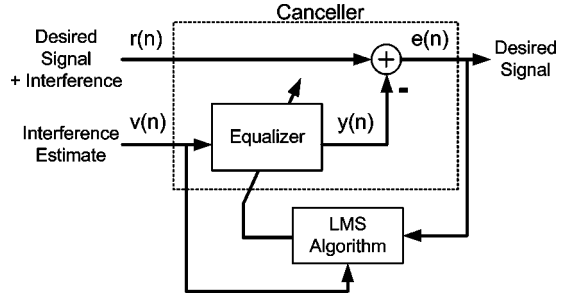

Fig. 8. A block diagram showing the concept of adaptive interference cancelling.

are equally strong at the receiver input and neglect the relative strength of different LO harmonics due to a certain LO duty cycle. After the first stage, the desired signal is multiplied by $\sqrt{2} \cdot (2 + \alpha)$ and the third and fifth harmonics by $\sqrt{2} \cdot \alpha$, leading to a relative error (interference-to-signal ratio) of $\alpha/2$ if $\alpha \ll 2$. For the second stage the same derivation holds. *As the two stages are cascaded, the product of the gains determines the result*, i.e., the total gain for the desired signal becomes $[\sqrt{2} \cdot (2 + \alpha)] \cdot [\sqrt{2} \cdot (2 + \beta)]$ and for the third and fifth harmonics it is $[\sqrt{2} \cdot \alpha] \cdot [\sqrt{2} \cdot \beta]$. This renders a total relative error (interference-to-signal ratio) of

$$\frac{2\alpha\beta}{2 \cdot (2 + \alpha) \cdot (2 + \beta)} \approx \frac{\alpha}{2} \cdot \frac{\beta}{2} \qquad (4)$$

if $\alpha \ll 2$ and $\beta \ll 2$. Therefore, the total relative error is the *product* of the relative errors for the two stages, $\alpha/2$ and $\beta/2$. If the second stage has an error $\beta = 1\%$, ideally this improves HR by $(\beta/2)^{-1}$, i.e., 46 dB, which has also been confirmed by simulation.

Please note that the product of errors, as shown in (4), holds for both third and fifth harmonics. Moreover, it not just works for mismatch induced errors but for any amplitude errors, e.g., errors introduced by parasitic capacitance or finite LNTA output impedance.

Theoretically, more than two stages can achieve even better amplitude accuracy, but practically phase accuracy will often dominate. To also address the phase error, next we will propose an alternative HR concept that exploits digital techniques.

IV. DIGITALLY ENHANCED HARMONIC REJECTION

Even for the concept proposed in the previous section, the HR performance can still be limited by the amplitude and especially phase mismatches between the paths. In this section, we propose a digitally enhanced HR architecture exploiting digital adaptive interference cancelling (AIC). Simply put, this concept adapts an estimate of the third or fifth order harmonic image in such a way that after subtraction from the received signal the HR ratio is increased.

The AIC concept is shown in Fig. 8: the interference estimate, v(n), is aligned (in phase and amplitude) with the interference in the received signal, r(n), by an adaptive digital equalizer. Thus, the equalizer removes the amplitude *and* phase differences of the interference between v(n) and r(n). The equalized interference estimate is subtracted from the received signal, which cancels the interference and produces the output signal, e(n).
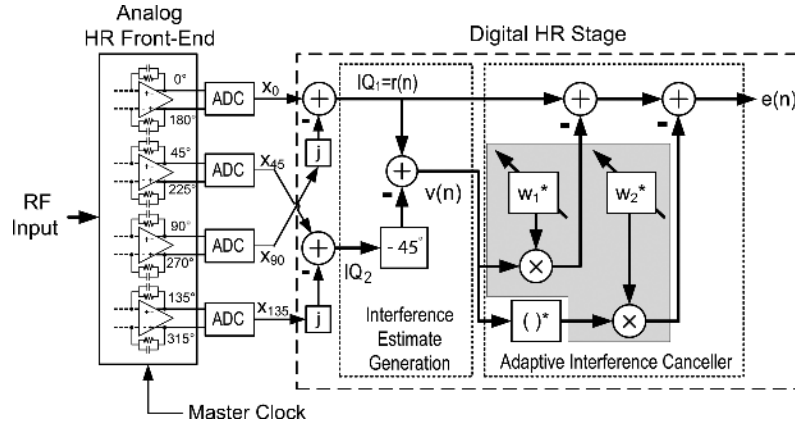
Fig. 9. A system-level block diagram of the analog front-end, the interference estimate generation and the AIC. The equalizer of the AIC is shown in grey.

Fig. 9 shows a system-level block diagram of the proposed system. The analog front-end used is identical to the first stage of the two-stage analog HR architecture proposed earlier. It produces four fully differential signals, which are converted into the digital domain using four A/D converters, to form signals x_0, x_{45}, x_{90} and x_{135}. The HR of the analog down-mixer, typically in the range of 30 to 40 dB, reduces the required dynamic range of the aforementioned A/D converters.

Two complex-valued IQ pairs are formed using the four real-valued baseband signals:

$$IQ_1(n) = x_0(n) - j \cdot x_{90}(n)$$
$$IQ_2(n) = x_{45}(n) - j \cdot x_{135}(n)$$

where IQ_1 can be considered as the received signal and IQ_2 is an additional I/Q pair, needed to generate the interference estimate.

The baseband signals, x_0, x_{45}, x_{90} and x_{135}, produced by the analog front-end are subject to component mismatches and LO timing errors, which cause amplitude and phase uncertainty. As a result, the amplitude and phase difference between the received signal, r(n), and the interference estimate, v(n), are subject to this uncertainty.

Perfect cancelling of the interference requires two conditions to be met: first, the interference estimate must be a perfect representation of the interference and second, the amplitude and phase difference between the interference estimate and the interference in the received signal must be completely removed by the equalizer.

Given the above, the equalizer must be adaptive to be able to cope with the uncertainty in the phase and amplitude in order to obtain the maximum amount of interference canceling.

The equalizer consists of two single-tap FIR filters, which are formed by the complex coefficients, w_1, w_2 and the two associated multipliers shown in the grey portion of Fig. 9. The coefficients are adapted by applying the power-normalized LMS algorithm [25].

For the single interferer case (only a third or fifth order harmonic image is present), the signal-to-interference ratio (SIR)

TABLE I
THE NORMALIZED (TO THE DESIRED SIGNAL) RF-TO-BASEBAND TRANSFER CHARACTERISTICS OF IQ_1, IQ_2 AND THE INTERFERENCE ESTIMATE v(n)

Signal	IQ_1		IQ_2		Interference estimate, v(n)	
	Gain	Phase	Gain	Phase	Gain	Phase
Desired	1.000	0°	1.000	45°	0.000	0°
3rd	0.024	-90.0°	0.024	135°	0.048	-90.0°
5th	0.014	90°	0.014	-45°	0.028	90.0°

at the output, e(n), of the digital AIC stage is determined by the inverse SIR of the interference estimate, v(n) [26]:

$$SIR_{e(n)} \approx \frac{1}{SIR_{v(n)}}. \qquad (5)$$

To maximize the SIR at the output of the canceller, the SIR of the interference estimate must be minimized. Therefore, the aim is to generate an interference estimate that contains the least amount of desired signal energy and the maximum amount of harmonic image energy.

A. Generating the Interference Estimate

The analog baseband outputs of the front-end, x_0, x_{45}, x_{90} and x_{135}, are formed by 8-phase 1/8-period-shifted LO waveforms that approximate a sinusoid, as explained in Section III. An N/8-period time shift results in a $N \cdot 45°$ phase shift for the desired signal and three and five times as much for the third and fifth harmonic images.[5] This property is exploited in the generation of the interference estimate.

Considering only the relatively large (6%) approximation error of $1{:}\sqrt{2}{:}1$ by 2:3:2 (weighting ratio of the three LNTAs), the theoretical RF-to-baseband gain and rotation of the desired and third and fifth order signals are given in Table I. For instance, it shows that the third harmonic image is attenuated by $-20 \cdot \log_{10}(0.024) = 32.4$ dB, with respect to the desired signal.

[5]A time-shift is a linear phase operation. Thus, the resulting phase shift scales linearly with frequency.

The data for IQ_1 and IQ_2 in Table I can be derived using the mixer modeling technique used in [20], which uses the Fourier series of the effective LO waveforms and the LNTA weighting ratio. Note that the phase and amplitude relations between IQ_1 and IQ_2 are *independent of the actual RF signals*, i.e., modulation schemes.

By examining Table I, it follows that the interference estimate, v(n), can be generated by a $-45°$ rotation of IQ_2, which aligns the desired signal with respect to IQ_1. Subtracting the rotated IQ_2, i.e., IQ_2', from IQ_1 results in the cancelling of the desired signal but leaves the interference:

$$v(n) = IQ_1(n) - \underbrace{IQ_2(n) \cdot \exp\left(-j \cdot \pi \cdot \frac{45}{180}\right)}_{IQ_2'(n)}. \quad (6)$$

The resulting signal components in the interference estimate, also shown in Table I, can be derived using (6). For instance, it shows that the third harmonic image is attenuated by $-20 \cdot \log_{10}(0.048) = 26.4$ dB. This attenuation is solely due to the analog HR front-end and the application of (6). The third harmonic image, in the interference estimate, is 6 dB stronger compared to IQ_1 or IQ_2 owing to a doubling of its amplitude by (6). This also holds for the fifth harmonic image. In addition, the desired signal is completely cancelled, despite the 6% error in $1:\sqrt{2}:1$. Thus, in theory, v(n) can be a good interference estimate.

B. The Adaptive Interference Canceller

In practical systems, however, the rejection of the desired signal in v(n) is limited by matching, just like the HR in the analog down-mixer. Fortunately, the AIC technique does not require perfect rejection of the desired signal to give good results. Consider a third harmonic interferer and a desired signal that are equally strong after passing through the analog HR down-mixing stage. Given a realistic (matching limited) desired signal rejection of 40 dB during the interference estimate generation by way of (6), the SIR of the estimate, $\text{SIR}_{v(n)}$, is -40 dB. Using (5), the theoretical SIR after the AIC, $\text{SIR}_{e(n)}$, is 40 dB. Then the total harmonic rejection is 40 dB plus the rejection obtained by the analog first stage (typically in the range of 30 to 40 dB).

Given the above, it should be clear that the additional harmonic rejection provided by the AIC is dependent on the SIR of the baseband signals IQ_1 and IQ_2, which is equal to the signal-to-harmonic ratios of the RF antenna signal minus the HR of the analog front-end.

Interestingly, the performance of the AIC shows a favorable trend with respect to the interference power: if the interference power increases, the quality (1/SIR) of the interference estimate *increases*, which leads to an increased SIR at the output of the canceller. In practice, the benefit of this trend is limited by the nonlinearity of the front-end, including the A/D converters.

Consider again the block diagram of the digital HR stage in Fig. 9. The interference estimate, v(n), and its complex conjugate,[6] $v^*(n)$, are equalized via multiplying by w_1^* and w_2^*, re-

[6]The complex conjugate is needed to remove the I/Q imbalance image [27] of the harmonic image in addition to the harmonic image itself.

spectively. The equalized signals are subtracted from the received signal, r(n), which removes the interference and produces the output signal, e(n). The filter weights, w_1^* and w_2^*, are adapted with every new output value of e(n) by means of the LMS update rule [25]:

$$w_1(n+1) = w_1(n) + \mu \cdot v(n) \cdot e^*(n)$$
$$w_2(n+1) = w_2(n) + \mu \cdot v^*(n) \cdot e^*(n) \quad (7)$$

where μ is the power-normalized step-size, normalized to the power of the interference estimate v(n), i.e., P_v:

$$\mu = \frac{1 \cdot 10^{-4}}{P_v} \quad (8)$$

and the canceller output, e(n), is calculated from the received signal, r(n), by

$$e(n) = r(n) - w_1^*(n) \cdot v(n) - w_2^*(n) \cdot v^*(n) \quad (9)$$

as shown in Fig. 9.

The LMS update rule as in (7) is an iterative process that aims to minimize the cross-correlation between the output of the canceller, e(n), and the interference estimate, v(n). Cross-correlation is a measure of similarity, thus, minimizing it results in the output of the canceller being as *dissimilar* to the interference estimate as possible: the interference at the output, e(n), is reduced.

The step-size parameter μ in (8) is chosen somewhat arbitrarily. Generally speaking, choosing μ too small results in slow convergence and choosing it too big increases the (time-varying) error of the filter weights [25], which reduces the harmonic rejection.

The optimum equalizer coefficients, w_1 and w_2, for cancelling the third harmonic image may differ from the optimum coefficients for cancelling the fifth harmonic image, owing to different phase and amplitude mismatches for each image. The dominating interference largely determines the cross-correlation. Therefore, the dominating harmonic image will be cancelled by the AIC stage. Note that the preceding analog HR down-mixer stage rejects both images.

The optimum coefficients are independent of the RF signal modulation scheme, owing to the fact that the amplitude and phase *differences* between r(n) and v(n) are independent of the actual RF signals. Thus, once the filter coefficients to cancel a specific harmonic image have been found (by application of the iterative LMS algorithm), they remain valid until the mismatch introduced by the front-end changes, for instance, when making large changes in the LO frequency.

V. IMPLEMENTATION OF THE ANALOG FRONT-END

A SDR receiver chip has been implemented in 65 nm CMOS to verify the three concepts proposed in previous sections. The digital AIC algorithm is realized in software and will be discussed later. The block diagram of the chip has been shown in Fig. 4. The signal path consists of LNTAs, passive mixers, and two-stage TIAs with second-stage HR-weighting via a resistor network (R-net). The first voltage gain should be at baseband after LPF for good OB linearity, as discussed in Section II, and the realization of two-stage polyphase HR has been described in
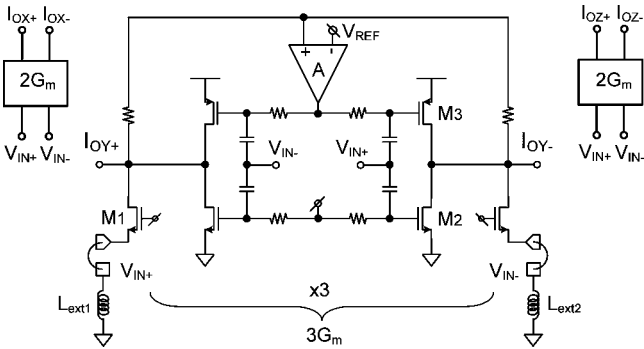
Fig. 10. Low-noise transconductance amplifiers (LNTA) implementing $3G_m$ (shown on transistor level) and two blocks of $2G_m$ (identical schematic).

Fig. 11. Simulated LNTA IIP3 versus load impedance (R_L for *each* of the three LNTAs) at different process corners (sn: slow-NMOS, sp: slow-PMOS, fn: fast-NMOS, fp: fast-PMOS).

Section III. The 8-phase LO is derived via a divide-by-8 from an off-chip signal CLK, i.e., the master clock. The receiver can be reconfigured to deliver either 8-phase outputs from TIA1 or I/Q outputs from TIA2. The 8-phase outputs interface to off-chip ADCs for digitally enhanced HR measurements while the TIA2 stage is switched off. To better understand the implementation, a more detailed description for some key blocks follows.

A. Linear LNTA

Fig. 10 shows the schematic of a pseudo-differential unit-LNTA, of which there are 7 units in parallel to form three LNTAs with 2:3:2 ratio, sharing the same external (large-value) inductor to GND for DC bias. The common-gate (CG) transistor M1 provides input matching while the input is also connected to the AC-coupled inverter consisting of common-source (CS) transistors M2 and M3. For each single-ended half, all 7 unit-LNTAs together deliver an impedance matching with the source impedance $R_S = 50\ \Omega$ and a total transconductance $g_{m,tot} = 100$ mS ($g_{m,CG} = 20$ mS, $g_{m,CS} = 80$ mS). A common-mode feedback (CMFB) loop using high-ohmic resistors and an amplifier "A" controls the PMOS transistors and ensures all three LNTA outputs are biased around $V_{REF} = 600$ mV. In total the three differential LNTAs draw 14 mA from a 1.2 V supply.

The noise behavior of the LNTA can be understood by studying a single-ended half, which consists of a CG transistor M1 and two CS transistors M2/M3, sharing the same input V_{in+}. Considering the LNTA output noise in the current domain, the noise factor can be written as

$$F = 1 + \frac{kT\gamma g_{m,CG} \cdot (1 - R_S \cdot g_{m,CS})^2}{kTR_S \cdot g_{m,tot}^2} + \frac{4kT\gamma g_{m,CS}}{kTR_S \cdot g_{m,tot}^2}. \tag{10}$$

The second term considers the partial noise cancelling of the CG transistor noise [28] and the third term considers the noise from the CS transistors. If take $R_S = 50\ \Omega$, $g_{m,CG} = 20$ mS, $g_{mCS} = 80$ mS, and $g_{m,tot} = 100$ mS into (10), we get $F = 1 + 9\gamma/25 + 16\gamma/25 = 1 + \gamma$. If γ is in the range of 2/3 to 1, the noise figure (NF) would be 2.2 to 3 dB.

For wideband operation, minimum-length transistors are used to achieve $S_{11} < -10$ dB to more than 6 GHz RF (simulation). Since the input impedance of a CG transistor depends on its drain impedance [29], a wideband low impedance at its output,
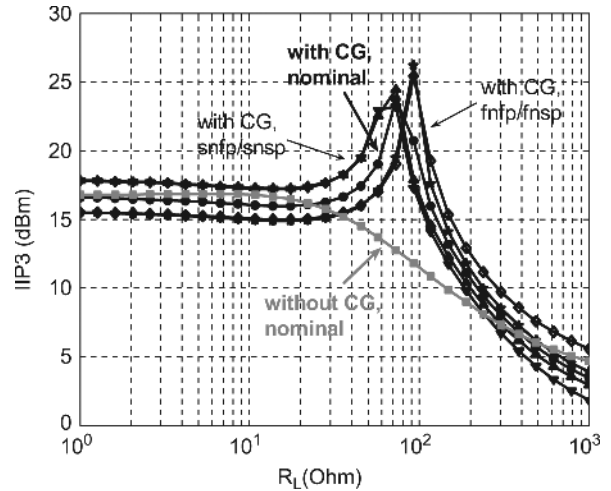
i.e., node B in Fig. 2, is desired for wideband input matching. This fits well to what is desired for linearity as discussed in Section II.

Since the LPF improves the OB linearity of I-V conversion (Fig. 1), the V-I linearity sets the ultimate limit of OB linearity. To obtain a good V-I linearity, high $(V_{GS} - V_{TH})$ and high V_{DS} is desired. In our $VDD = 1.2$ V design, $(V_{GS} - V_{TH})$ is larger than 250 mV and V_{DS} is 600 mV. Fig. 11 shows IIP3 simulation results (considering process spread), where each of the three LNTAs is loaded by a pair of resistors R_L to model the input impedance of the next stage mixers. To average out the effect of different LNTA transconductance (2:3:2), the simulation is carried out with all three LNTAs combined together as well as their individual R_L. The two input tones are at 801 MHz and 802 MHz. Simulations predict an IIP3 of more than $+15$ dBm if $R_L < 100\ \Omega$ and only ± 1 dB variation over different process corners, indicating that high LNTA linearity robust to process spread is possible if we keep voltage gain low (small R_L).

Actually, it turns out that the addition of the CG-stage in parallel to the inverters has a nonlinearity cancellation effect that improves IIP3 for R_L between about $20\ \Omega$ and $200\ \Omega$, which determines the V_{ds}-related distortion terms (for the case without a CG-stage, see the grey curve in Fig. 11). Simulation and analysis indicate that it is mainly the pre-distortion at the inverter inputs introduced by the CG-stage via its source current, to cancel the distortion generated by inverter itself. Nevertheless, since we are interested in using a low R_L value, produced by mixer switches, to deliver signal current into the TIA stage, here we do not discuss this effect further.

A differential LNTA requires an off-chip balun if a single-ended antenna or RF filter is used. Compared to an LNTA with single-ended input, although the differential one may double the power consumption [30], it can render better IIP2. Besides, the input voltage swing on each of the differential inputs is lowered by 3 dB, which improves LNTA IIP3 and P_{1dB} by 3 dB.

Using the same setup as for Fig. 11, simulations with an ideal balun and $R_L = 50\ \Omega$ (the designed input impedance of the mixer) show input-referred $P_{1dB} = +4$ dBm, NF < 3 dB (only

including noise from LNTA), and voltage gain $= -1$ dB for each single-ended output (low gain as desired for good linearity) with -3 dB bandwidth > 7 GHz. This wide RF bandwidth benefits from the low impedance (real part) at the output of LNTA, which means the dominant pole is located at a very high frequency given a certain capacitance.

B. Passive Mixer

Each of the three LNTAs with 2:3:2 ratio connects to 8 passive current-commutating mixers driven by 8-phase LO, as shown in Fig. 4. The mixers are DC-coupled to the LNTAs for wider bandwidth compared to AC-coupled, which introduces parasitic capacitance. Each mixer receives 3 differential inputs from LNTAs and together they deliver 4 differential outputs to TIA1, i.e., 8-phase signals with $45°$ interval.

The passive mixer simply consists of NMOS switches, with bulk tied to source. The gate of the mixer switch is AC-coupled to a clock driver and biased so that the maximum $V_{GS} = \text{VDD}$. The mixer switch-on resistance R_{mixer} is in the order of $50 \ \Omega$ and all mixer switches have the same dimension for good phase accuracy. Besides, the same R_{mixer} and different LNTA output impedance (3:2:3) also introduce a current division effect which brings the actual first-stage weighting ratio different from 2:3:2 but closer to the ideal $1:\sqrt{2}:1$ ratio, good for the overall amplitude accuracy.

For good NF, we need to minimize clock overlap to avoid a low-ohmic path between TIA inputs that will amplify TIA noise [22]. For the case with 8 TIA inputs this leads to a maximum LO duty cycle of 1/8. Both sides of the mixer, i.e., the output of LNTA and the input of TIA, are biased at the same DC level (around half VDD) ensuring that little DC current flows for a low 1/f noise from the mixer switches.

C. Accurate Multiphase Clock

Since the amplitude accuracy can be ensured by the two-stage polyphase HR, the phase inaccuracy is likely to dominate. Based on the Appendix, if the LO duty cycle is "d", the resulting third HR (1σ) is

$$HR3 = 10 \log \left(\frac{\sin^2(\pi \cdot d)}{\sin^2(3\pi \cdot d)} \cdot \left[\left(\frac{\sigma_A}{12} \right)^2 + \left(\frac{\sigma_\varphi}{4} \right)^2 \right]^{-1} \right) \quad (11)$$

where σ_A and σ_φ are the standard deviation in the amplitude and phase respectively. For $d = 1/8$ and negligible amplitude error $(\sigma_A \to 0)$ due to the two-stage technique as in (4), to reach 60 dB HR (3σ), the required phase error is $\sigma_\varphi = 0.03°$.

To build a multiphase clock generator with low phase mismatch, two design principles are applied: 1) to use a common master clock to derive all phases; 2) to minimize the path from the common master clock to the mixer switches therefore to minimize mismatch accumulation.

Fig. 12 shows a divide-by-8 ring counter using eight dynamic transmission-gate (TG) flip-flops (FF). The same master clock (CLK), with 8 times the LO frequency, drives all FFs. Only one inverter (INV2) is used as a buffer to minimize the path from CLK to mixer.

A preset data pattern is required to deliver the wanted 1/8 duty cycle. Each LO phase controls six mixer switches connecting to
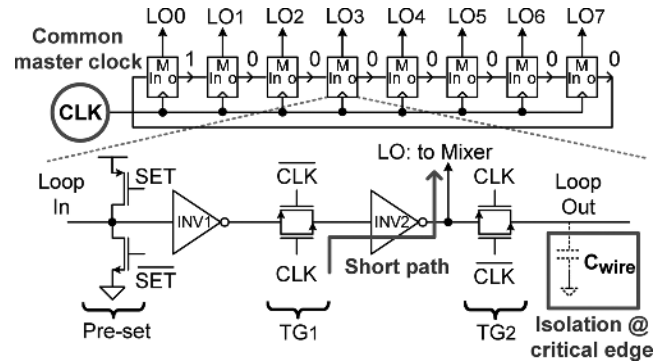

Fig. 12. An 8-phase clock generator with low phase mismatch (with one cell shown on transistor level).
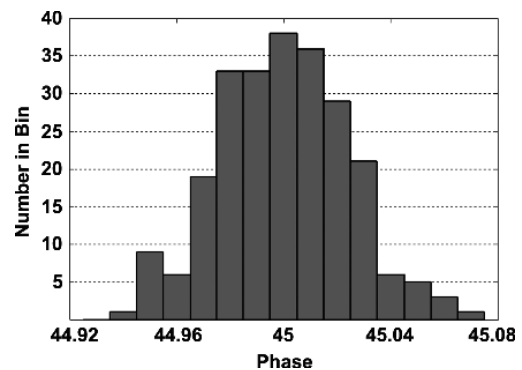

Fig. 13. Histogram of the simulated phase difference between two adjacent LO outputs (240 Monte Carlo results).

differential outputs of three LNTAs. The gates of all six switches are connected together and driven by the same buffer, i.e., INV2, to minimize buffer mismatch.

In a ring counter, all flip-flops "see" the same environment. However, a loop is not convenient in layout and it may need different wiring lengths between each two flip-flops, degrading phase accuracy. A careful layout strategy is adopted to minimize the wiring differences. Moreover, when the critical LO edges occur, the largest part of the wiring is isolated from the output of INV2 via TG2, decreasing rise and fall times and reducing the effect of wiring mismatch.

The phase error reported in [17] is found to be too pessimistic due to an incorrect simulation test-bench. Fig. 13 presents the simulated phase deviation from $45°$ between two adjacent 0.8 GHz LO phases due to mismatch, including the contribution from mixer switches. The histogram shows a maximum phase error of only $0.07°$ and it yields $\sigma = 0.024°$, i.e., 0.08 ps for 0.8 GHz. This clock performance is hence compatible with $HR > 60$ dB (3σ).

The master clock CLK comes from an off-chip generator followed by a pair of inverters as on-chip buffer. Simulation shows, at 0.8 GHz LO, the power consumption of the divider is 5.4 mA at 1.2 V supply and the input buffers consume 8.9 mA driven by 6.4 GHz differential input clock.

In simulation, the divide-by-8 can work up to 1.25 GHz LO (10 GHz CLK) in nominal case although it can vary with process corners. The up-side LO frequency is mainly limited by the large

division ratio, i.e., 8. If a higher LO frequency is wanted, a divide-by-2 may be used to generate 4-phase (quadrature) LO instead of the divide-by-8, and then the receiver in Fig. 4 can be reconfigured to a quadrature wideband receiver without HR [21], when harmonic mixing is less to be a problem at higher bands.

D. High-Swing TIA and Baseband R-net

Since the voltage gain occurs at the outputs of the TIA1 stage where interference is only partly suppressed, we choose an OTA topology [21] being able to handle large voltage swing, which helps tolerate large blockers. It is a two-stage class-AB-output OTA based on [31]. The input pair uses NMOS transistors in weak inversion for high g_m/I_{DC} and a big size leading to low 1/f noise. For the OTA second stage, a class-AB push-pull output stage is used, which can handle more than 2 V peak-to-peak differential output voltage swing. Each OTA draws 3 mA from 1.2 V supply.

A parallel RC feedback network implements a simple first order LPF to perform blocker filtering (Fig. 4). Each TIA stage has a LPF -3 dB bandwidth of 20 MHz and together they determine the receiver IF bandwidth of 12 MHz, which may accommodate most mobile communication standards. The virtual-ground impedance of the TIAs is about $4\,\Omega$ around DC and peaks to $60\,\Omega$ around 700 MHz. The simulated gain after the TIA1 stage is 27 dB and after the TIA2 stage 34 dB.

The resistor network (R-net) provides the second-stage weighting for HR. It also converts 8-phase outputs of the TIA1 stage into quadrature inputs of the TIA2 stage. To form a 5:7:5 amplitude ratio, 19 unit-resistors form a resistance ratio of 7:5:7 in three paths. Harmonic rejection at baseband (via R-net) can also reduce errors due to parasitic capacitance compared to at high frequency.

VI. Implementation of the Digital Back-End

The analog front-end used in the digitally enhanced HR architecture consists of the first stage HR mixer driven by the multi-phase clock generator of the two-stage analog HR architecture. The reader is referred to the previous section for the implementation details of the analog circuits.

The four fully differential baseband outputs provided by the TIA1 stage (Fig. 4) are converted into the digital domain using a commercial A/D board comprising four 14-bit ADCs (Fig. 9). Unfortunately, the input range of the used A/D board was more than 15 times greater than the output swing provided by the front-end, resulting in less than 10 effective bits.

The baseband processing, including the interference estimate generation and the adaptive interference canceller were implemented in software on a PC and use floating-point arithmetic. To allow real-time processing, a sampling rate of 4 MS/s was chosen. This gives 2 MHz bandwidth for each analog baseband signal and 4 MHz bandwidth in the digital domain using quadrature signals. Fig. 9 gives a system-level overview of the setup.

The interference estimate generation is implemented using two real adders and the phase shifter, shown in Fig. 14. This reduced-complexity shifter exploits the fact that the cosine and sine of a 45° angle are of equal magnitude. Thus, it needs two real multipliers (instead of four) and two real adders. Thus, the

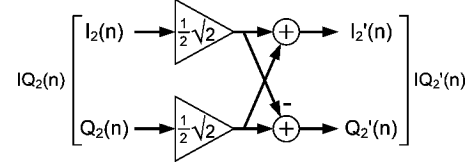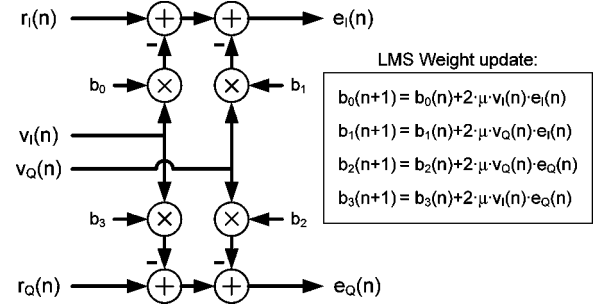Fig. 14. Reduced complexity $-45°$ phase shifter.

Fig. 15. Reduced complexity interference canceller.

total complexity of the interference estimate generation is two real multipliers and four real adders.

The complexity of the canceller indicated by (9) can be reduced from eight multipliers and eight adders to four multipliers and four adders, by applying the following substitutions:

$$b_0 = w_{1,I} + w_{2,I} \quad b_1 = w_{1,Q} - w_{2,Q}$$
$$b_2 = w_{1,I} - w_{2,I} \quad b_3 = -w_{1,Q} - w_{2,Q}$$

where the filter coefficients, w_1 and w_2, are split in their real and imaginary parts, $w_{1,I}, w_{1,Q}$, etc. The resulting canceller and the new LMS update rules are shown in Fig. 15. If the step-size μ is rounded to the nearest power of 2, four multipliers in the "LMS Weight update" become a shift operation. As a result, the update mechanism only needs four multipliers and four adders. Then, the total arithmetic complexity of the digital HR stage is 10 multiplications and 12 additions per sample.

While the digital algorithm was implemented only in software, a fixed-point VHDL version was synthesized using a 65 nm CMOS standard cell library. The tools reported a dynamic power of less than 10 mW at 100 MS/s and 1.2 V supply voltage.

VII. Experimental Results

The circuit shown in Fig. 4 is fabricated in 65 nm CMOS and the micrograph is shown in Fig. 16. The total area, excluding bond-pads, is about $1\,\text{mm}^2$. Capacitors (C_{FB} and C_{VG} in Fig. 2) take a large portion of area in the TIA, and also the OTA input pair is big to achieve a low 1/f noise corner. With 1.2 V supply, the analog power consumption is 33 mA (LNTA: 14 mA, TIA1-stage: 12.8 mA, TIA2-stage: 6.4 mA) while the clock power consumption is 8 mA at 0.4 GHz LO and 17 mA at 0.9 GHz LO, including the clock input buffers.

The chip is packaged in a 32-pin heat-sink very-thin quad flat-pack no-leads (HVQFN) package. To prove the receiver is robust to OBI, all measurements are performed on PCB without any external filter. Two SMD inductors are mounted on the PCB to bias the LNTA (Fig. 10). Both the receiver inputs and clock
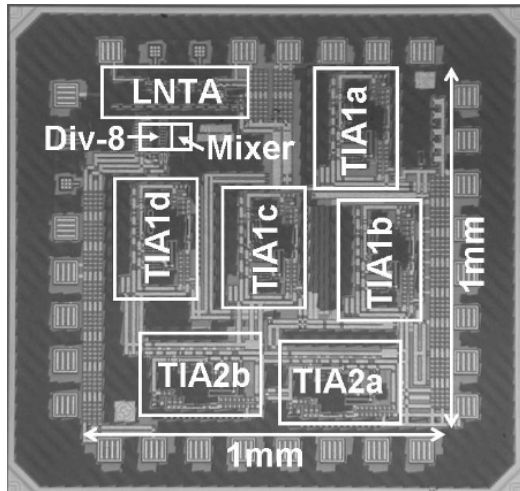
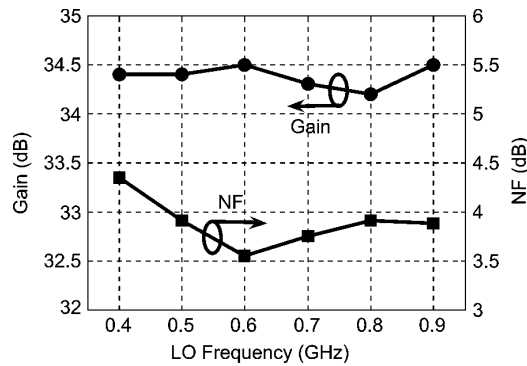Fig. 16.   65 nm CMOS chip micrograph indicating some functional blocks.

Fig. 17.   Measured voltage gain and DSB NF of the two-stage receiver as a function of the LO frequency.

inputs are differential and wideband hybrids (balun) were used to interface to single-ended $50\,\Omega$ measurement equipments. The IF-output voltages are sensed by a differential active probe that performs differential to single-ended conversion and impedance conversion to $50\,\Omega$. The characteristics of all components and cables for testing are de-embedded from the results.

The divide-by-8 works up to 0.9 GHz LO, and the measured S_{11} is lower than -10 dB up to 5.5 GHz. This means the HR measurement is valid for 0.9 GHz LO up to its sixth harmonic. The measured IF bandwidth is 12 MHz and the baseband 1/f noise corner is 30 kHz thanks to the passive mixer with little DC current and the OTA with a large-sized input pair.

A. Gain, NF, RF Bandwidth, and In-Band IIP2/IIP3

Fig. 17 shows the measured voltage gain and DSB NF over an LO frequency of 0.4 to 0.9 GHz. The voltage conversion gain, measured for an IF of 1 MHz from the input of the balun to the differential outputs of receiver, is above 34 dB over the whole band and is quite flat (± 0.2 dB variation), indicating a much wider RF bandwidth. The NF is measured for an IF of 10 MHz since the available NF analyzer (Agilent N8973 A) starts from that frequency. The DSB NF is below 4 dB except for 0.4 GHz where 1/f noise from the LNTA starts to dominate.
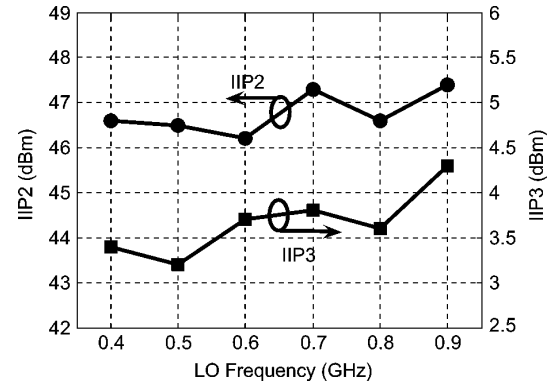

Fig. 18.   Measured in-band IIP2 and IIP3 versus LO frequency.

The divide-by-8 limits the LO frequency range up to 0.9 GHz (master clock @ 7.2 GHz), but the signal-path -3 dB RF bandwidth is much wider, up to 6 GHz. To verify it, we conducted a gain measurement for the seventh harmonic, i.e., the first non-canceled high-order harmonic. Ideally, using 1/8 duty-cycle LO, the strength of the seventh harmonic should be 1/7 of the fundamental harmonic, so we expect the seventh harmonic should ideally have a gain that is 16.9 dB (1/7) lower from 34 dB, i.e., 17.1 dB. Indeed, the gain drops from 17 dB at 0.7 GHz RF to 14.3 dB at 6 GHz RF (LO: 0.1 to 0.85 GHz), which means the OBI will only be attenuated a little by the frequency roll-off at RF. It also indicates that the receiver can be readily expanded to cover higher bands by extending the LO range as discussed in Section V-C.

Fig. 18 shows the measured in-band (IB) IIP2 and IIP3 over LO frequency, with two tones close to the LO frequency so that they are not affected by IF filtering (IIP2: $f_{LO} + 3$ MHz and $f_{LO} + 6.01$ MHz; IIP3: $f_{LO} + 3$ MHz and $f_{LO} + 3.01$ MHz). After downconversion, the IM2 component at 3.01 MHz and the IM3 component at 2.99 MHz are measured. The IB IIP3 is around $+3.5$ dBm, which is good given the high gain of 34 dB, thanks to only voltage gain at baseband with negative feedback. The IB IIP2 is above $+46$ dBm.

B. Out-of-Band IIP2/IIP3

We also measured the out-of-band (OB) IIP2 and IIP3. Due to the LPF behavior, the measured OB linearity depends on the distance from f_{LO} to the two RF tones used. For sufficient distance, the LPF will suppress the downconverted two-tone interference so the OB nonlinearity is mainly contributed by the V-I of the LNTA.

The OB IIP3 is tested via two tones at 1.61 GHz and 2.40 GHz with an LO at 819 MHz, so that the IM3 is at 820 MHz RF and 1 MHz IF. The results of both IB (0.8 GHz LO) and OB IIP3 are shown in Fig. 19. Without fine tuning, the measured OB IIP3 is $+16$ dBm, which agrees with the simulated results in Fig. 11. Compared to the IB IIP3 of $+3.5$ dBm, the OB IIP3 is dramatically improved because the TIA was dominating the IB IIP3, due to the high voltage gain at the output. As shown in the figure, the range for which IM3 follows the extrapolation line is also improved by almost 20 dB (upper limit of -30 dBm
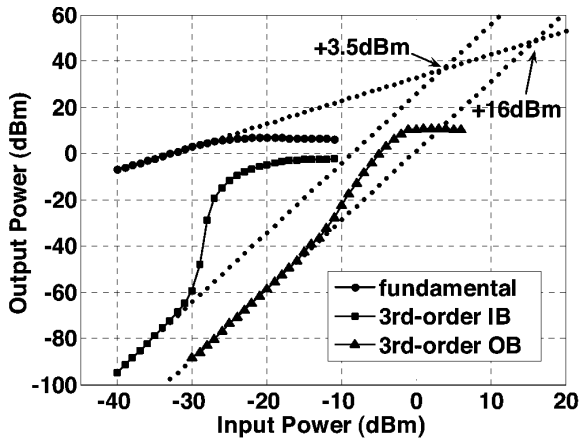
Fig. 19. Measured in-band (IB) and out-of-band (OB) IIP3 for 800 MHz LO demonstrating OB linearity improvement.

Fig. 20. Measured input-referred 1 dB desensitization point (B_{1dB}) versus blocker frequency.

Fig. 21. Measured HR ratio versus LO frequency: Comparison between HR with only one-stage and total two-stage (two-stage polyphase HR).

for IB versus -10 dBm for OB). This is crucial to tolerate large OB interference.

The OB IIP2 is $+56$ dBm, tested via two tones at 1.80 GHz and 2.40 GHz while LO at 601 MHz, so that the IM2 is at 600 MHz RF and 1 MHz IF.

C. 1 dB Compression Point and Blocker Filtering

To quantify the effect of the blocker filtering, we measured the 1 dB compression point (P_{1dB}) and the 1 dB desensitization point (B_{1dB}), both input-referred.

First we measured the P_{1dB} without applying any blockers, which is -22 dBm. The result is reasonable since -22 dBm input power plus 34 dB gain is equal to 12 dBm output power (referring to $50\ \Omega$), differentially. The single-ended voltage swing is about 1.27 V peak to peak, just exceeding the 1.2 V supply. This means the limitation is at the receiver output and the P_{1dB} can be improved by automatic gain control (AGC).

A more serious problem is to receive a weak signal at the same time with a strong interferer: a so-called blocker test. In this situation AGC does not help since the maximum gain is required to maintain sensitivity. The measurement was carried out with the LO at 400 MHz and the desired RF signal at 401 MHz with -50 dBm input power. The blocker frequency is varied from 402 MHz to 4.002 GHz. Fig. 20 shows B_{1dB} versus the blocker frequency. As predicted by (1) and (2), we see two effects in the figure: 1) the tolerable blocker power depends on the frequency distance between the LO and the blocker, due to the LPF behavior;[7] 2) HR also plays a role in blocker filtering, as two dips occur around seventh and ninth harmonic of the LO frequency, both of which are not rejected well by the 8-phase HR. From the figure, we can observe that B_{1dB} is better than P_{1dB} (-22 dBm) except very close-by blockers (402 MHz) and the maximum B_{1dB} is more than 0 dBm, showing the blocker filtering is indeed effective.

D. Two-Stage Polyphase HR

We will verify the analog two-stage polyphase HR here and the digitally enhanced HR in Section VII-E. These two alternative approaches will be compared in Section VII-F.

[7]The actual behavior of the LPF is more complicated than (2), since our baseband filter is cascaded in two stages, which does not follow a simple first order or second order filtering behavior.
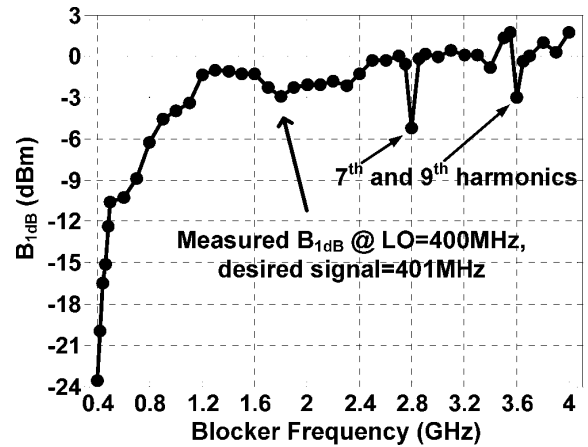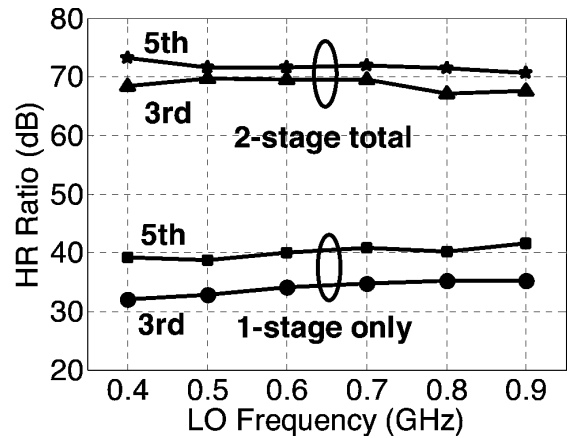
First we look at the two-stage polyphase HR. The HR ratio can be measured by comparing the gain difference between the desired signal and the harmonic image. At the receiver input, the desired signal power was -50 dBm while the harmonic image power was -30 dBm.

Fig. 21 shows, for one chip, the HR of one-stage, at the outputs of the TIA1, and the total two-stage HR, at the outputs of the TIA2, versus LO frequency. The HR of one-stage is between 30 and 40 dB and the HR of two-stage is around 70 dB, representing a 30 dB improvement for both third and fifth HR thanks to the two-stage polyphase HR technique. Generally, the HR improvement from one-stage to two-stage is in the range of 20 to 40 dB as observed from multiple chips. The large improvement also shows that it is the amplitude error dominating the first-stage HR.

To identify the effect of mismatch, we measured the HR of two-stage for 40 chips at 0.8 GHz LO, as shown in Fig. 22. The minimum third order HR is 60 dB and the minimum fifth order HR is 64 dB. The second, fourth, and sixth HR is also measured, over 20 chips. The minimum second order HR is 62 dB, while the minimum fourth and sixth order HR are both 67 dB. These results are achieved without calibration, trimming, or RF filtering.
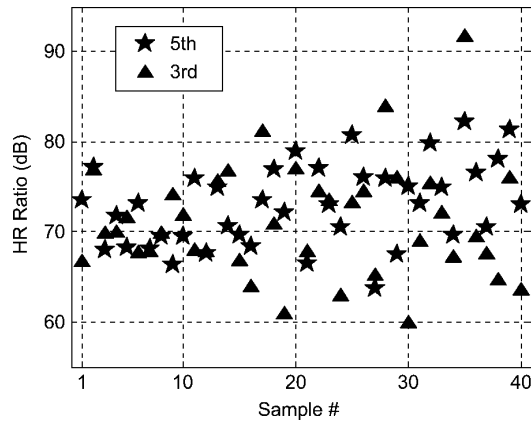
Fig. 22. Measured HR ratio of 40 randomly selected chips at 800 MHz LO (two-stage polyphase HR).

Fig. 24. The measured third and fifth order HR of the analog stage and combined stages, for 10 randomly selected chips, at 800 MHz LO (digitally enhanced HR).
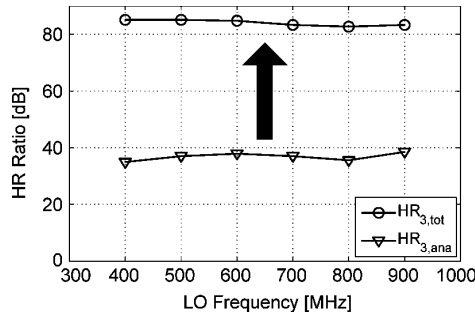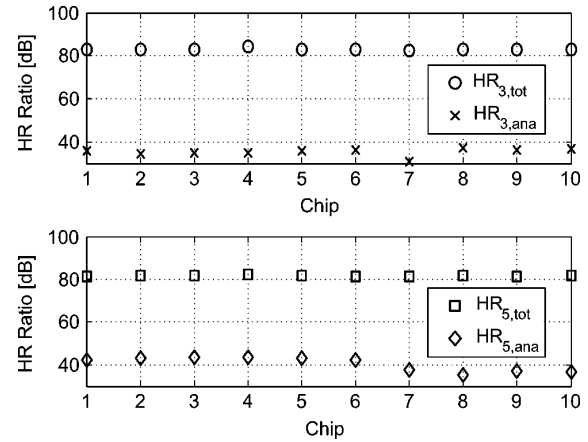

Fig. 23. The measured third order HR of the analog stage and the combined stages versus the LO frequency. Desired: -66.1 dBm RF power, third harmonic image: -20.1 dBm RF power (digitally enhanced HR).

Since the signal-path -3 dBm RF bandwidth has been characterized to be up to 6 GHz, the contribution of the frequency roll-off to the HR result should be small. According to (11), the simulated phase error $\sigma = 0.024°$ means a minimum HR (3σ) of 62 dB if the amplitude error is eliminated, fitting well with the measured HR as well as the Monte Carlo simulation results. This also suggests that phase error can indeed be the limitation now.

E. Digitally Enhanced HR

Consider now the digitally enhanced HR architecture. The harmonic rejection for the third harmonic image versus LO tuning range (0.4 to 0.9 GHz) was measured, see Fig. 23. At the receiver input, the desired signal RF power was -66.1 dBm and the harmonic image RF power was -20.1 dBm. The analog HR mixer provides more than 36 dB HR for the third harmonic image, which is higher than the 32.4 dB predicted by Table I. We attribute this difference to the finite output impedance of the three LNTAs. Thus, the effective weighting of the 2:3:2 ratio is closer to the ideal $1:\sqrt{2}:1$, resulting in a higher measured HR.

Given a SIR of -46 dB at RF, the digital AIC increases the harmonic rejection provided by the analog HR mixer from 36 dB to over 80 dB across the entire LO tuning range. The HR measurements are calculated based on the difference in power between the desired signal and the harmonic image. At the output

of the digital canceller, the harmonic image is below the noise floor. Instead of the harmonic image power, the noise floor was taken. Thus, the actual HR is greater than what is shown in Fig. 23.

A second indicator that the HR is higher comes from the SIR of the interference estimate, v(n), which was measured to be over 52 dB (limited by noise floor of equipment) across the entire LO tuning range. Given (5), the (theoretical) SIR at the output of the canceller is also 52 dB. The power ratio between the desired signal and the harmonic image (at RF) is -46 dB, which makes the theoretical HR greater than 98 dB! Unfortunately, the height of the noise floor at the output of the canceller, which is largely determined by the quantization noise of the A/D board, prevents this to be verified.

The third and fifth order harmonic rejection for multiple (randomly selected) chips is shown in Fig. 24. The desired signal RF power was -66.1 dBm at 800 MHz LO. The RF power of the third and fifth order harmonic images was -20.1 dBm. The results show more than 36 dB of analog harmonic rejection and more than 80 dB of combined harmonic rejection, for all chips. Thus, the digitally enhanced AIC technique performs well under varying mismatch conditions.

To show the effectiveness of the AIC technique against a modulated interferer, an FM modulated third harmonic image interferer was applied to the system. Fig. 25 shows the baseband spectrum of the received signal (top), r(n), and the AIC output (bottom), e(n).

In the received signal (Fig. 25, top), the third harmonic image signal at -1.25 MHz (baseband) causes interference to a (sinusoidal) desired signal at -1.45 MHz (baseband). The I/Q imbalance image of the third harmonic interferer is also visible at $+1.25$ MHz (baseband).

At the output of the canceller (Fig. 25, bottom), the third harmonic interferer is below the noise floor, which is a suppression of more than 40 dB. Assuming at least 36 dB of analog harmonic rejection, the combined harmonic rejection is thus more than 76 dB. This is less than 80 dB because the FM modulated interferer was weaker than the sinusoidal interferer used during the previous measurements.
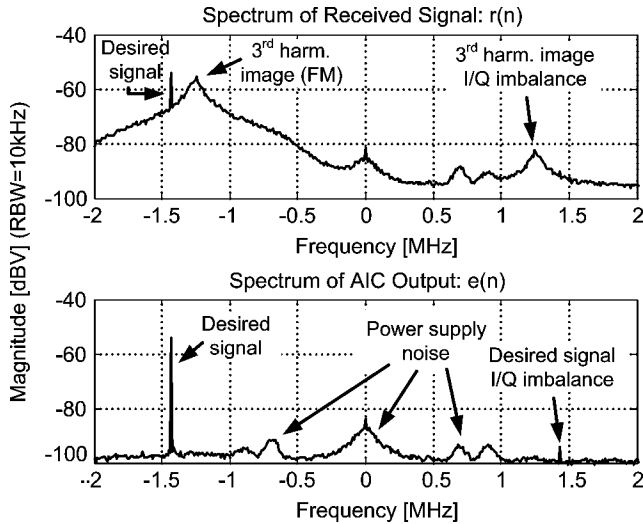
Fig. 25. (top) The measured baseband spectrum of the (discrete-time) received signal, r(n), and (bottom) the output of the canceller, e(n).

Fig. 25 also shows signals which are caused by ground loop problems and spurs emanating from the switching power supply of the PC, which housed the A/D converter board.

Note that the I/Q imbalance image of the third harmonic interferer, see Fig. 25 (top), is suppressed to below the noise floor, revealing the I/Q imbalance image of the desired signal, see Fig. 25 (bottom), at $+1.45$ MHz (baseband).

After convergence of the LMS algorithm, which takes around 50000 samples (12.5 ms), the equalizer coefficients were $w_1 = 0.4852 - j \cdot 0.0086$ and $w_2 = 0.0221 + j \cdot 0.0122$.

The measurements show that the digitally enhanced HR approach is indeed a powerful one; it produces unprecedented HR figures, irrespective of (small) analog mismatches that exist in the analog front-end.

F. Comparing the Alternatives

The two-stage polyphase HR implemented in analog approach helps *both* third *and* fifth HR via improved amplitude accuracy and achieves a minimum rejection of 60 dB and 64 dB respectively. The digitally enhanced HR based on AIC algorithm consistently shows more than 80 dB of HR for a single harmonic image (*either* the third *or* the fifth) by correcting both amplitude and phase of that harmonic image. The other harmonic image is rejected by at least 36 dB, not improved from the analog first stage. They share a similar limitation on even-order HR.

On the implementation level, compared to the two-stage polyphase HR, the digitally enhanced HR architecture requires two additional A/D converters, which may increase the power considerably. Fortunately, the converters for x_{45} and x_{135} (Fig. 9) may be switched off when the analog HR stages can provide enough harmonic rejection.

Table II summarizes the results and properties of the two alternative approaches.

G. Performance Summary and Benchmark

Table III summarizes the measured performance. As a benchmark, Table IV shows a comparison to other recently published

TABLE II
COMPARISON OF TWO ALTERNATIVE HR TECHNIQUES ROBUST TO MISMATCH

	Analog 2-stage	Digital AIC
Rej. strongest	>60 dB	>80 dB [a]
Rej. other odd	>64 dB	>36 dB
Rej. even	>62 dB	>64 dB
Power front-end	50 mA @ 1.2 V (excl. ADCs)	44 mA @ 1.2 V (excl. ADCs)
Power DSP (100 MS/s)	N/A	<8.5 mA @ 1.2 V (simulated)
# ADCs	2	4

[a] If one harmonic interference image band is dominating.

TABLE III
SUMMARY OF MEASURED KEY PERFORMANCE

LO Frequency		0.4 to 0.9GHz
Gain		34.4dB±0.2dB
DSB NF		4dB±0.5dB
S_{11} < -10dB		80MHz to 5.5GHz
-3dB RF Bandwidth		Up to 6GHz
In/Out-of-band IIP3		+3.5dBm / +16dBm
In/Out-of-band IIP2		+46dBm / +56dBm
-3dB IF Bandwidth		12MHz
1/f noise		30kHz corner
Harmonic Rejection	Analog 2-stage	2nd-6th: >60dB
	Digital AIC	1 strongest: >80dB
Technology		65nm CMOS
Supply Voltage		1.2V
DC Current		50mA max.

wideband receivers with HR. Since it is difficult to characterize the exact overhead of the part implemented in software (digital AIC), here we only compare the part implemented on chip (Fig. 4) to other work.

There are two outstanding parameters of this work, i.e., linearity and harmonic rejection. Comparing all work including an LNA, [2], [4], and [33] shows an IIP3 around -15 dBm while this work shows an IIP3 of $+3.5$ dBm and a competitive NF. The OB IIP3 of our work is even higher ($+16$ dBm), but we did not find a good way to benchmark it. For HR, only [32] and [33] reported numbers comparable to this work. However, [32] only reported results from one chip while consuming large power due to a different structure of the HR mixer. [33] reported results for 10 chips, but relying on hand calibration, and the calibration is only effective for either third or fifth HR but not for both at the same time. Thus, we conclude that our design has both good linearity and good HR at moderate power consumption, thanks to the proposed techniques.

VIII. CONCLUSION

This paper identified out-of-band (OB) nonlinearity and harmonic mixing as two main problems for *out-of-band interference* (OBI), and proposed solutions to reduce their effects. First,

TABLE IV
BENCHMARK WITH OTHER RECENT WORK

Benchmark	CMOS Tech.	Freq. (MHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	HR3 (dB)	HR5 (dB)	Chip #	Cal.	Power (mW)
This Work	65nm	400-900 a)	34	4	+3.5	60	64	40 min.	No	60
			LNA + Mixer + Divider							
Bagheri, JSSC06 [2]	90nm	800-5000	36	5	-15 b)	38	40	1	No	51
			LNA + Mixer + Divider, performance at 900MHz							
Lerstaveesin, JSSC08 [4]	180nm	48-860	83	4 to 7	-14	42 c)	?	1	No	468 c)
			LNA + Mixer + BB filter + VGA + ADC + PLL							
Ru, ISSCC08 [16]	65nm	200-900	2	19	+11	41	44	10 av.	No	19
			No LNA, only mixer & multiphase clock							
Maxim, ISSCC08 [32]	130nm	40-1000	?	16	+20	63	64	1	No	450
			No LNA, only mixer & multiphase clock							
Cha, MWCL08 [33]	180nm	48-862	35	8	-15	72	45	10 min.	Yes	189
			LNA + Mixer + Divider							

a) Only LO frequency range, while the measured RF bandwidth is up to 6GHz.
b) IIP3 is derived for the full-gain setting which is required to match the 5dB NF.
c) Both the HR3 and the power data exclude the contribution of RF tracking filter.

OB nonlinearity can be improved by implementing low-pass filtering, simultaneously with voltage gain only after downconversion, to improve the OB IIP3 and the desensitization point due to blockers. Second, two "iterative" harmonic-rejection (HR) techniques are presented to reduce harmonic mixing in a way which is robust to mismatch. An analog two-stage polyphase HR concept is proposed to greatly enhance the amplitude accuracy for both third and fifth harmonics so that the total amplitude error becomes product of errors. Alternatively, digitally enhanced HR based on adaptive interference cancelling (AIC) can be applied to improve HR of the analog first-stage further by correcting both amplitude and phase errors for one dominant harmonic, either third or fifth. To guarantee a mismatch-robust HR for both analog and digital approaches, a simple but accurate ring counter is presented to generate the multiphase clocks driving the HR mixer.

We have verified the proposed techniques via a SDR receiver in 65 nm CMOS, with RF bandwidth up to 6 GHz and 8-phase LO frequency up to 0.9 GHz (master clock up to 7.2 GHz). The 1 dB compression point is -22 dBm while the maximum 1 dB desensitization point is more than 0 dBm, showing the low-pass blocker filtering is effective. In terms of IIP3, $+16$ dBm for OBI is measured without fine tuning for sufficient frequency spacing, e.g., LO at 819 MHz while two-tone at 1.61 G and 2.40 GHz, versus an in-band IIP3 of $+3.5$ dBm. Without any trimming or calibration, the two-stage polyphase HR technique achieves 60 dB minimum HR ratio at 0.8 GHz LO for both third and fifth harmonics over 40 randomly selected chips, and all even-order HR ratios are measured above 60 dB as well. The digital AIC HR achieves a steady 80 dB HR for either third or fifth harmonic for 10 chips, indicating the power of adaptive digital techniques to solve analog problems.

APPENDIX

Effect of Random Amplitude and Phase Errors to Harmonic Rejection: This Appendix aims at estimating the HR ratio and its sensitivity to amplitude and phase errors. These effects have been partly considered in [2] and [15], however, the statistical nature of mismatch and the effect of using balanced RF or balanced LO have not been included so far. We will also consider the effect of LO duty cycle "d".

Suppose we have three signal paths to the output (as in Fig. 3 to Fig. 7) and the signals are represented by vectors as in Figs. 3(b) and 7. The resulted first and third harmonics can be respectively written as

$$H_1 = R_{H1} \cdot \left[A_1 \cos\varphi_1 + \sqrt{2}\cos 0° + A_2 \cos\varphi_2 \right]$$
$$H_3 = R_{H3} \cdot \left[A_1 \cos(3\varphi_1) + \sqrt{2}\cos 0° + A_2 \cos(3\varphi_2) \right]$$
(A.1)

where R_{H1} and R_{H3} are the Fourier series coefficients of a pulse-wave LO with duty cycle "d"

$$R_{H1} = \frac{2}{\pi}\sin(\pi \cdot d), \quad R_{H3} = \frac{2}{3\pi}\sin(3\pi \cdot d),$$
$$A_1 = (1 + \Delta A_1), \quad A_2 = (1 + \Delta A_2),$$
$$\varphi_1 = (45° + \Delta\varphi_1), \quad \varphi_2 = (-45° + \Delta\varphi_2).$$

If ΔA_1, ΔA_2, $\Delta\varphi_1$, $\Delta\varphi_2$ are small and uncorrelated, we can approximate the variance in H_3 as shown in (A.2), the first equation at the top of the next page. If $\sigma_{A1} = \sigma_{A2} = \sigma_A$ and $\sigma_{\varphi 1} = \sigma_{\varphi 2} = \sigma_\varphi$, then results (A.3), the second equation shown at the top of the next page. Since $H_1 \approx 2\sqrt{2} \cdot R_{H1}$, taking the ratio, we obtain

$$\left(\frac{\sigma_{H3}^2}{H_1^2} \right) \approx \frac{R_{H3}^2 \cdot [\sigma_A^2 + 9\sigma_\varphi^2]}{8R_{H1}^2}$$
$$= \frac{\sin^2(3\pi \cdot d)}{\sin^2(\pi \cdot d)} \left[\left(\frac{\sigma_A}{6\sqrt{2}} \right)^2 + \left(\frac{\sigma_\varphi}{2\sqrt{2}} \right)^2 \right]. \quad (A.4)$$

Please note that σ_A is the standard deviation of amplitude error in percentage and σ_φ is the standard deviation of phase error in radians.

For a double-balanced HR mixer, which creates the output during one half period from 0 to T/2 with the positive-sign RF-LNTA path then the other half from T/2 to T with the negative-sign RF-LNTA path, the first harmonic adds up in amplitude while the third harmonic adds up in power (as the

$$\sigma_{H3}^2 \approx R_{H3}^2 \cdot \left[\left(\frac{\partial H_3}{\partial A_1} \right)^2 \cdot \sigma_{A1}^2 + \left(\frac{\partial H_3}{\partial A_2} \right)^2 \cdot \sigma_{A2}^2 + \left(\frac{\partial H_3}{\partial \varphi_1} \right)^2 \cdot \sigma_{\varphi 1}^2 + \left(\frac{\partial H_3}{\partial \varphi_2} \right)^2 \cdot \sigma_{\varphi 2}^2 \right] \tag{A.2}$$

$$\sigma_{H3}^2 \approx R_{H3}^2 \cdot \left[2\cos^2 \left(3 \cdot 45^\circ \right) \cdot \sigma_A^2 + 18\sin^2 \left(3 \cdot 45^\circ \right) \cdot \sigma_\varphi^2 \right] = R_{H3}^2 \cdot \left[\sigma_A^2 + 9\sigma_\varphi^2 \right] \tag{A.3}$$

error is uncorrelated between two half periods for both amplitude and phase). Therefore, the ratio is improved by 3 dB for a double-balanced HR mixer compared to (A.4), i.e.,

$$\left(\frac{\sigma_{H3}^2}{H_1^2} \right)_{\text{diff}} \approx \frac{\sin^2(3\pi \cdot d)}{\sin^2(\pi \cdot d)} \left[\left(\frac{\sigma_A}{12} \right)^2 + \left(\frac{\sigma_\varphi}{4} \right)^2 \right]. \tag{A.5}$$

If the duty cycle of the LO is 50% or 25%, i.e., $d = 0.5$ or 0.25, we get

$$\left(\frac{\sigma_{H3}^2}{H_1^2} \right)_{\text{diff},50\%} \approx \left(\frac{\sigma_A}{12} \right)^2 + \left(\frac{\sigma_\varphi}{4} \right)^2. \tag{A.6}$$

If there is no amplitude error, 50% or 25% duty cycle results in a 3σ-HR3 of 70 dB if $\sigma_\varphi = 0.024^\circ$. If the duty cycle is 1/8, i.e., $d = 0.125$, as in our case, we get

$$\left(\frac{\sigma_{H3}^2}{H_1^2} \right)_{\text{diff},12.5\%} \approx 5.8 \cdot \left[\left(\frac{\sigma_A}{12} \right)^2 + \left(\frac{\sigma_\varphi}{4} \right)^2 \right]. \tag{A.7}$$

Without amplitude error, the 3σ-HR3 is now 62 dB.

A similar derivation for fifth order HR of a double-balanced HR mixer renders

$$\left(\frac{\sigma_{H5}^2}{H_1^2} \right)_{\text{diff}} \approx \frac{\sin^2 (5\pi \cdot d)}{\sin^2 (\pi \cdot d)} \cdot \left[\left(\frac{\sigma_A}{20} \right)^2 + \left(\frac{\sigma_\varphi}{4} \right)^2 \right] \tag{A.8}$$

where the phase term σ_φ would have been multiplied by 5 in (A.4) due to the 5-times phase shift of H_5 compared to H_1. Nevertheless, without amplitude errors, this leads to the same numerical result ($\sigma_\varphi = 0.024^\circ$): a 3σ-HR5 of 62 dB for 1/8 duty cycle LO.

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He holds several patents and has authored and co-authored more than 80 journal and conference papers. In 2006 and 2007, he served as Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II and since 2008 for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMSI.

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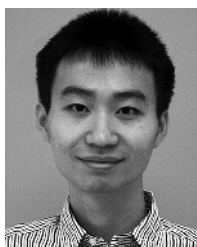
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In 1991 he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven, The Netherlands, where he worked on high-speed AD converters and analog key modules. In 1998 he returned to the University of Twente, as full Professor heading the IC Design group, which is part of the CTIT Research Institute. His current research interest is high-speed analog CMOS circuits. He is also a part-time consultant in industry, and in 2001 he co-founded Chip Design Works.

His Ph.D. thesis was published as a book: *Analog CMOS Filters for Very High Frequencies* (Springer, 1993) and he received the Shell Study Tour Award for his Ph.D. work. From 1997 until 1999 he served as Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II–ANALOG AND DIGITAL SIGNAL PROCESSING. After this, he served as Guest Editor, Associate Editor (2001–2006), and from 2007 as Editor-in-Chief for the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He is also a member of the technical program committees of the IEEE International Solid State Circuits Conference (ISSCC), the European Solid State Circuits Conference (ESSCIRC), and the Symposium on VLSI Circuits. He is a co-recipient of the ISSCC 2002 Van Vessem Outstanding Paper Award, a Distinguished Lecturer of the IEEE, an elected member of IEEE SSCS AdCom and an IEEE Fellow.