Direct-Current Measurements of Oxide and Interface Traps on Oxidized Silicon

Arnost Neugroschel, *Fellow, IEEE*, Chih-Tang Sah, *Fellow, IEEE*, K. Michael Han, *Student Member, IEEE*, Michael S. Carroll, Toshikazu Nishida, *Member, IEEE*, Jack Theodore Kavalieros, and Yi Lu, *Member, IEEE*

***Abstract*— A direct-current current-voltage (DCIV) measurement technique of interface and oxide traps on oxidized silicon is demonstrated. It uses the gate-controlled parasitic bipolar junction transistor of a metal-oxide-silicon field-effect transistor in a p/n junction isolation well to monitor the change of the oxide and interface trap density. The dc base and collector currents are the monitors, hence, this technique is more sensitive and reliable than the traditional ac methods for determination of fundamental kinetic rates and transistor degradation mechanisms, such as charge pumping.**

I. Introduction

IT IS WELL recognized that the electrical characteristics of metal-oxide-semiconductor transistors (MOST's) and bipolar junction transistors (BJT's) degrade during circuit operation due to channel-hot-electron (CHE) and substrate-hot-electron (SHE) stresses which increase oxide (Q_{OT}) and interface trap (Q_{IT}) densities [1], [2][1]. In MOST's, the trapped charges reduce the mobility ($\Delta\mu$) and shift the threshold gate voltage (ΔV_{GT}), both of which reduce drain saturation current (ΔI_D) which slows down the switching speed due to longer charging time of interconnect or load capacitances at lower currents. The trapped charges also shift the subthreshold gate voltage ($\Delta V_{GT-\mathrm{sub}}$), and decrease subthreshold slope of the drain-current versus gate-voltage curve, which reduces the current cut-off sharpness, thereby increasing leakage current or standby power and decreasing the noise margin. In BJT's, Q_{IT} and Q_{OT} will increase the minority carrier recombination rate in the base, thereby reducing its current gain, such as the common-emitter current gain, β_F [3]. Thus, a quantitative separation of the effects of Q_{OT} and Q_{IT} is necessary to delineate the location and physical origin of the degradation in order to design and manufacture highly reliable integrated circuits with ten-year or longer operating life.

Manuscript received January 25, 1995; revised May 15, 1995. The review of this paper was arranged by Associate Editor D. P. Verret. This work was supported by a MOS and a bipolar transistor reliability physics contracts awarded to the University of Florida by the Semiconductor Research Corporation (SRC), and by the National Science Foundation under Grant ECS-9220382. Materials and test transistors were provided by the SRC member companies and SRC mentors of the two contracts.

A. Neugroschel, C.-T. Sah, K. M. Han, M. S. Carroll, T. Nishida, and J. T. Kavalieros are with the Department of Electrical Engineering, University of Florida, Gainesville, FL 32611-6200 USA.

Y. Lu was with the Department of Electrical Engineering, University of Florida, Gainesville, FL 32611-6200 USA. He is now with the Intel Corporation.

IEEE Log Number 9413284.

[1]For a brief tutorial review, see pp. 323–325 and 674–678 of [1] and Appendix B of [2].

The separation of Q_{OT} and Q_{IT} is generally difficult. It has not been reliably separated using the traditional capacitance and conductance methods or the transient methods because the test structures are two-terminal capacitors, or very small test transistors which give extremely small capacitances due to the very small device area. Many traditional methods for separating Q_{OT} and Q_{IT} were reviewed [4], and a two-step method was demonstrated. However, it uses the subthreshold slope to monitor Q_{IT} which is reliable only when there is not an inhomogeneous or lateral distribution of Q_{IT} and Q_{OT}. Hence, it is not reliable for monitoring the highly nonuniform Q_{IT} and Q_{OT} generated by CHE stress.

A novel method is demonstrated in this paper which measures the *dc* base and collector *currents* versus the gate *voltage*, to be known as DCIV method (in analogy to the traditional usage such as HFCV for high-frequency capacitance-voltage or QSCV for quasi-static CV), to monitor the Q_{IT} and Q_{OT}. The novel DCIV method contains two features: 1) The base current (I_B) of the vertical BJT is used to measure the recombination current at the interface traps generated during fabrication or operation which avoids the error from lateral distribution or areal nonuniformity of Q_{IT} and Q_{OT} because I_B is directly proportional to N_{IT} or Q_{IT}/q. 2) The collector current (I_C) of the vertical BJT is used to measure the Q_{OT} because I_C increases sharply when the gate voltage passes the flat-band value toward depletion and inversion. The method will be described in this article using the nMOST and npnBJT of the BiMOS structure shown in Fig. 1. This BiMOS structure has been used previously to fabricate large test transistors with nearly 400 000 $\mu\mathrm{m}^2$ gate oxide area by Thompson ([8] and [9] cited in [4]), but it is also present in the submicrometer nMOST's in a p-well on n-substrate of production CMOS (Complementary MOS) inverter circuits. Thus, the novel DCIV method to be described can be easily applied to production test transistors and some examples to be given were data measured on micrometer and submicrometer MOST-BJT production structures.

With reference to Fig. 1, the BJT can be measured before and after a stress in two configurations: The top-emitter (top-E) or bottom-emitter (bottom-E) measurement configurations, with the n+drain/p-base or n+substrate/n-epitaxy/p-base as the forward biased emitter/base junction. Our geometrical terminology deviates from the traditional, emitter-up and emitter-down, which confuses the geometrical location of the emitter

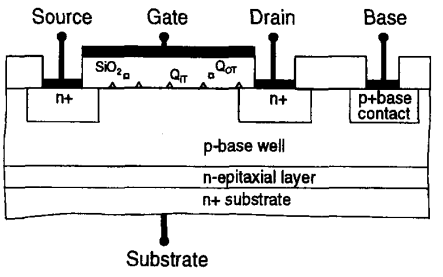


Fig. 1. The cross-sectional view of the BiMOS BJT-MOST transistor structure with a nMOST in a p-base well on a n-epitaxy/n+ substrate silicon wafer with the parasitic n+/p/n+ BJT.

with the emitted-charge flow direction. In both configurations, the shape of the I_B-V_{GB} curve and the magnitude of I_B at a constant V_{EB} will measure Q_{IT} [5], [6]. However, we recently anticipated that the shape and magnitude of I_C will also be a strong function of V_{GB} in both configurations because I_C increases sharply at the flat-band gate voltage, $V_{GB\text{-flatband}}$, from a low constant current to a high constant current at strong inversion voltage, $V_{GB\text{-threshold}}$. This sharp increase occurs when the *electron-channel* between the n+drain and n+source appears at $V_{GB\text{-flatband}}$ which abruptly increases the emitter/base area in the top-E configuration and the collector/base area in the bottom-E configuration.

The stress-induced base current, ΔI_B, is solely due to electron-hole recombination at the stress-generated interface traps [5], [6], hence, is a function of stress-induced interface charge and trap concentrations, ΔQ_{IT} and ΔN_{IT}, or the stress-induced density-of-states of the interface traps and surface recombination velocity, ΔD_{IT} and ΔS_0. However, the increase of the collector current with V_{GB} is nearly all from geometrical increase in the emitter or collector area contributed from the nMOST's electron channel. Therefore, the lateral shift in the I_C-V_{GB} curve, $\Delta V - GB$, is mainly a function of the stress-induced change of flatband gate voltage, $\Delta V_{GB\text{-flatband}}$, and hence is a very sensitive monitor of $\Delta Q_{OT} + \Delta Q_{IT}$. Thus, combining the $\Delta I_B - V_{GB}$ and $I_C - V_{GB}$ data will enable the separation of ΔQ_{OT} and ΔQ_{IT}. Experimental data in the following section will demonstrate this capability of the novel DCIV method.

Minority carrier surface recombination rate or velocity S_0 at the Si/SiO_2 interface was studied extensively since the use of MOS-gate-controlled BJT was demonstrated by one of us in 1961–1962 [5], [6]. In the early and follow-up experiments, I_B was measured in either the top-emitter configuration [5]–[9] or bottom-emitter configuration [10]–[13], to evaluate S_0. In [7] through [9], the BJT β_F degradation during emitter-base reverse-bias stress at the junction breakdown voltage was also studied. In many of these earlier measurements, the $I_B - V_{GB}$ curve was also displaced along the gate-voltage axis due to stress, but the peak in $I_B - V_{GB}$ was not very sharp. In some cases no peak was observed. In addition, the magnitude of I_B was greatly increased by the generated N_{IT}. Thus, an estimate of ΔQ_{OT} from the shift of V_{GB} at the peak ΔI_B in the $\Delta I_B - V_{GB}$ curve cannot be very accurate and reliable.

II. Description and Demonstration

Production n-channel MOST fabricated by state-of-the art CMOS process is measured to demonstrate the proposed DCIV method. The starting n-Si wafer has a p-base well with surface concentration of 1×10^{16} cm^{-3}, gate oxide thickness of $x_o \simeq 150$ Å, channel length $L = 1.6$ μm, and the gate area of $A_G = 1.6 \times 100$ μm^2. The cross-sectional view was shown in Fig. 1.

Fig. 2(a) and (b) shows the npn-BJT's $I_B - V_{GB}$ and $I_C - V_{GB}$ curves, measured in both the top-E and bottom-E configurations, before and after SHE stress as labeled. The oxide charges and interface traps were generated by areally uniform SHE stress with $V_{SB} = V_{DB} = 4$ V, and $V_{GB} = 7.5$ V. During the SHE stress, the bottom emitter junction (n+substrate/n-epitaxy/p-base shown in Fig. 1) was forward-biased to inject electrons into the p-base. Some of these electrons are accelerated (designated as hot electrons), by the reverse-biased surface space-charge layer ($V_{SB} = V_{DB} = 4$ V) of gate-induced collector/base junction area, to >3.2 eV kinetic energy. These hot electrons are then injected into the gate oxide over the 3.12 eV SiO_2/Si electron potential barrier. Some of the injected electrons are captured by the neutral oxygen vacancy centers [14]–[15], giving $V_O + e^- \rightarrow V_O^-$ and the negative Q_{OT} or positive ΔV_{GT}. Because of their high kinetic energy (~4 eV from $V_{DB} = V_{SB} = 4$ V) which is greater than the bond energy (~3 eV) of the strained Si-Si and Si-O interfacial bonds and the interfacial Si-H and Si-O bonds, the hot electrons also created some new interface traps, N_{IT} or D_{IT}, as indicated by the large increase of I_B in Fig. 2(a) measured in both the top-emitter and bottom-emitter configurations. The build-up of Q_{IT} also decreases the subthreshold slope of the nMOST's $I_D - V_{GB}$ curve shown in Fig. 2(c), however, the V_{GB} shift in $I_D - V_{GB}$ is due to the build-up of both Q_{OT} and Q_{IT}

$$\Delta V_{GB} = \Delta V_{GB-OT} + \Delta V_{GB-IT} \tag{1}$$

$$\equiv -(\Delta Q_{OT} + \Delta Q_{IT})/C_o \tag{1a}$$

which cannot be separated by this MOST $I_D - V_{GB}$ measurement alone unless additional properties of the interface traps are known or assumed, a limitation also present in Terman's method to obtain D_{IT} from HFCV characteristics. The two BJT measurements just described in Fig. 2(a) and (b) can help to separate the Q_{OT} and Q_{IT}, which are analyzed as follows.

The stress-generated increase of the I_B shown in Fig. 2(a) gives a direct measure of the surface recombination velocity S_0 and the density-of-the-state of the interface traps, D_{IT}, because it is proportional to the maximum of the stress induced $I_B, \Delta I_B \equiv I_B$ (post-stress) $-I_B$ (pre-stress). Its peak and shape can be distorted by areal nonuniformity of Q_{OT}, D_{IT}, or other device parameters, such as base dopant concentration and oxide thickness. But areal nonuniformity alone cannot produce a base current which must come from electron-hole recombination, unlike the HFCV ($C_{gb} - V_{GB}$) used in Terman's analysis and the $I_D - V_{GB}$ in the subthreshold slope analysis of the interface trap density, whose distortion could solely arise from areal inhomogeneity even when $D_{IT} = 0$.

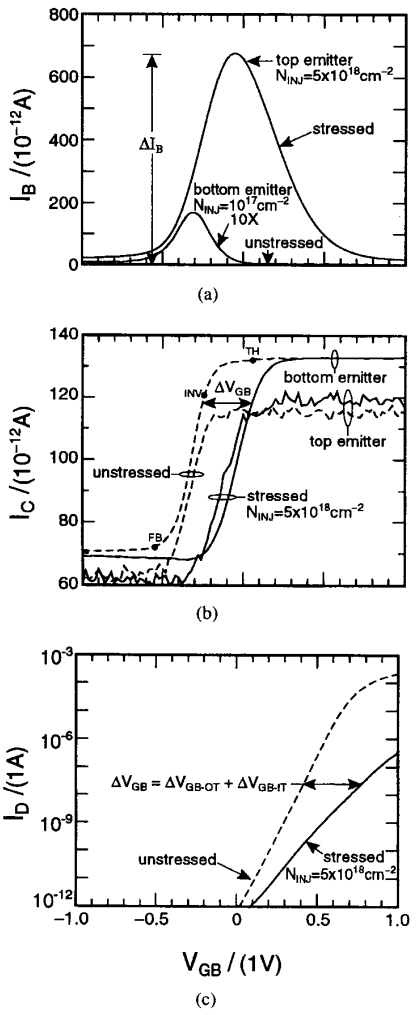


Fig. 2. The effect of areal-uniform SHEi stress on the npnBJT and nMOST characteristics as a function of the MOS gate voltage, V_{GB}. All stressed at 5×10^{18} electron/cm^2 fluence except bottom-EI_B in (a). Measured at $V_{EB} = -0.3$ V, $V_{CB} = 0$ V and 297 K. (a) Base current and (b) collector current in the top-emitter and bottom-emitter configurations. (c) Subthreshold $I_D - V_{GB}$ of the nMOST.

The V_{GB-IT} component can then be calculated from (2B) given below [5]

$$\Delta I_B \simeq (qA_G n_i \Delta S_O/2)\exp(qV_{BE}/2kT) \quad (2)$$

$$\Delta S_0 \simeq (\pi/2)\sigma_0 \Theta_{\text{th}} \bullet \Delta N_{IT} \quad (2a)$$

$$\Delta Q_{IT} \equiv -C_o \Delta V_{GB-IT} \equiv q\Delta N_{IT} \simeq q\Delta D_{IT} \bullet \Delta E_{IT}. \quad (2b)$$

The density-of-state, ΔD_{IT} (1/cm^2-eV), and carrier capture cross sections, $\sigma_n = \sigma_p = \sigma_0$ (cm^2), of the interface traps are assumed to be independent of the binding energy in the energy range ΔE_{IT} in the Si energy gap [16]. The calculation of ΔV_{GB-IT} is more complex than (2)–(2B) for an energy distribution of interface traps with energy-dependent density-of-state, $D_{IT}(E_{IT})$, and carrier capture cross sections, $\sigma_n(E_{IT})$ and $\sigma_p(E_{IT})$. However, S_0 calculated from measured ΔI_B after stress using (2), can still be used to monitor the build-up of the interface traps and the associated ΔV_{GB-IT}. In the example shown in Fig. 2(a), the numerical results are $\Delta S_0 \simeq 1600$ cm/s at the $I_{B\text{-peak}}$ which occurs at the gap energy position of $V_S - V_F = -0.24$ V below the midgap for the top-E curve stressed with a fluence of 5×10^{18} electron/cm^2, and $\Delta S_0 \simeq 40$ cm/s at $V_S - V_F = -0.26$ V for the bottom-E curve stressed at a fluence of 1×10^{17} electron/cm^2. For many devices measured, $I_{B\text{-peak}}$ of the bottom-E was about five times smaller than that of top-E.

The prestress-poststress $I_C - V_{GB}$ curves of both the top-E and bottom-E configurations shown in Fig. 2(b) give a very sensitive measure of the stress-generated V_{GB} shift. I_C is flat in the accumulation range and is proportional to the area of the n+drain/p-base well junction (or the sum of the area of n+drain and n+source if drain and source are tied together during the I_C measurement). When $V_{GB} \geq V_{FB} \simeq -0.55$ V (Greater sign is for nMOST.), an electron surface channel begins to form which will collect the electrons injected by the bottom-emitter and pass the collected electrons to the n+drain or/and n+source, causing an increase of I_C (or $I_D + I_S$). The I_C quickly reaches a higher plateau as V_{GB} increases further to about -0.15 V. This increase of I_C is proportional to the added collector area from the gate-induced electron-channel. The three characteristic Si surface potentials or Si energy band bendings (FB = flatband at $V_S = 0$ V, INV = inversion at equal electron-hole surface concentration $N_S = P_S$ or $V_S = V_F - V_{BE}/2$, and TH = threshold or strong inversion at $N_S = P_{\text{Base}}$ or $V_S = 2V_F - V_{BE}$) are marked by dots on the pre-stress $I_C - V_{GB}$ curve in Fig. 2(b). They show that I_C starts to rise sharply at $V_{FB} \simeq -0.55$ V at flatband in this example, reaching the higher plateau about halfway between inversion $V_{GB\text{-inversion}} \simeq -0.25$ V and the MOST threshold voltage, $V_{GB\text{-th}} \simeq +0.05$ V. Thus, the rise of I_C is sharp and occurs in a short range of V_{GB}, in this case, -0.05 V $-$ (-0.55 V) $= 0.5$ V.

It was asserted in the preceding discussion that I_C is not caused by carrier recombination or generation of the newly generated interface traps, but solely by the increase of the emitter or collector area from the gate-induced electron channel described above. This is now experimentally proven in Fig. 2(b) by the nearly parallel V_{GB} shift of the post-stress I_C from its pre-stress range with the nearly identical height for both the top-E and bottom-E measurement configurations, although this stress has generated a large N_{IT} to give the large increase of I_B shown in Fig. 2(a). This model is further supported by the observed and anticipated reduction of slope of the post-stress $I_C - V_{GB}$ at higher V_{EB} bias reflecting a larger negative Q_{IT} ($\simeq \Delta D_{IT} \bullet \Delta E_{IT}$). This is expected from the higher surface electron concentration injected by the emitter to charge the interface traps negatively due to i) the added stress-induced ΔD_{IT}, and ii) a larger energy range of N_{IT} towards the Si conduction band edge, estimated by $\Delta E_T \sim V_{BE}$.

A quantitative analysis of the Q_{IT} contribution to $I_C - V_{GB}$ shift in Fig. 2(b) can be made from

$$\Delta V_{GB-IT} = -\Delta Q_{IT}(V_F - V_{FN})/C_o \quad (3)$$

by using the fundamental property of intrinsic interface traps whose charge state is acceptor-like (negatively charged) near the conduction band edge and donor-like (positively charged) near the valence band edge, because they are localized or bound electron states which are split-off states from the respective band states by random atomic location perturbation of the crystalline periodic potential at the SiO_2/Si interface. This charge state assignment was implied by Bardeen when he introduced the concept of neutral Fermi level V_{FN} [17]. For Si, V_{FN} is at about $E_V + (1/3)E_G$ [17], [18]. Thus, $V_F - V_{FN} \simeq 0$ at flat-band for the p-Si used here which was doped with $N_{AA} \sim 10^{16}$ cm^{-3} of boron acceptors, and $C_o\Delta V_{GB} \simeq -\Delta Q_{OT}$. The stress induced V_{GB-FB} shift in the $I_C - V_{GB}$ curves of Fig. 2(b) then gives

$$\Delta N_{OT} = (C_o/q)\Delta V_{GB-OT} \tag{4}$$

$$\simeq (C_o/q)[-0.2 - (-0.55)] = 4.3 \times 10^{11}\ \text{cm}^{-2} \tag{4a}$$

which can then be used in (1) to separate Q_{IT} and Q_{OT}. In view of the nearly parallel shift of the $I_C - V_{GB}$ curves at low V_{BE} (~0.3 V in these examples), it is not necessary to locate the V_{GB-FB} point to get ΔV_{GB-OT} in practical applications.

The change of the subthreshold slope of the MOST $I_D - V_{GB}$ slope has been commonly used to monitor Q_{IT}. It is accurate if N_{IT} is areally constant. This is untenable in the practical CHE stress and can give erroneous results [4], [19].[2] In the present example, N_{IT} was generated by the areally uniform SHEi stress, thus, a decreasing slope of $I_D - V_{GB}$ shown in Fig. 2(c) gives an indication of a real stress-induced N_{IT} rather than inhomogeneity, analogous to the reasoning for the anticipated experimental post-stress slope reduction of the $I_C - V_{GB}$ just discussed. However, an important point is frequently overlooked: N_{IT} or $D_{IT}(E_{IT})\Delta E_{IT}$ from the $I_D - V_{GB}$ in Fig. 2(c) is in the strong inversion voltage range, $V_{GB} > V_{GB-TH}$ or in the Si-gap energy range $V_S > 2V_F - V_{BE} + (2kT/q)$ near the conduction band edge. In contrast, N_{IT} or $D_{IT}(E_{IT})\Delta E_{IT}$ in Fig. 2(b) is in the mid-range of the Si energy gap, from flat-band ($V_S = 0$) to strong inversion or threshold ($V_S = 2V_F - V_{BE}$). Thus, the subthreshold slope monitors an additional energy range of D_{IT} near the minority band edge, which is application-important because the MOST operates in this strong inversion range when it is turned on. But it is also fundamentally significant because the decreasing post-stress subthreshold slope [compressed by logarithmic I_D but still visible in the solid curve Fig. 2(c)] indicates an increasing D_{IT} with energy towards the conduction band edge, which is consistent with the commonly depicted U-shaped D_{IT} as anticipated by the fundamental microscopic-atomic model of interface states implied by Bardeen [17]. A qualitative estimate from the subthreshold slope change in Fig. 2(c), using the well known equation [20] gives

$$D_{IT} = (C_o/q)(q/2 \cdot 303kT)\ \Delta S \tag{5}$$

$$\simeq 10^{12}\ \text{cm}^{-2}\ \text{eV}^{-1}. \tag{5a}$$

[2] We are indebted to Professor Ma who insisted on this point which affects the numerical result evaluated from experimental data given in [4], but, does not alter the conclusions given in [4].

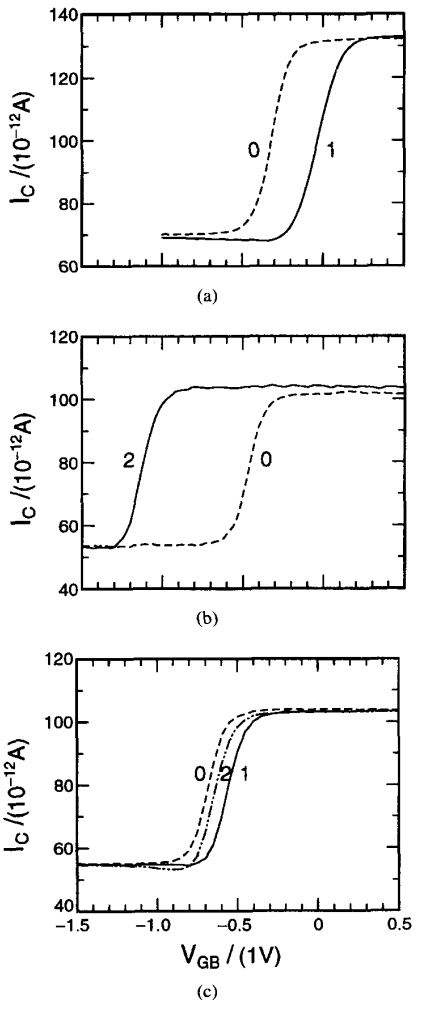


Fig. 3. The effect of stress on the collector current measured at V_{EB} (bottom-emitter) = −0.3 V, V_{CB} = 0 V, and 297 K. (a) 5 × 10^{18} cm^{-2} SHEi stress at V_{GB} = 7.5 V, V_{CB} = 4.0 V and I_G = 1 nA. (b) 1.4 × 10^{16} cm^{-2} SHEi stress at V_{GB} = 12 V, V_{CB} = 10 V, and I_G = 1 nA. (c) CHEi stress at $V_{GB} = V_{DB}$ = 16 V and floating V_{SB} and I_D = 1 μA for 1 s (curve 1) and 500 s (curve 2).

Additional examples are given in Fig. 3(a)–(c) for the bottom-Emitter configuration which use I_C to monitor negative, positive, and turn-around ΔQ_{OT} induced by stress. Fig. 3(a) is identical to Fig. 2(b) showing positive ΔV_{GB} from negative ΔQ_{OT}. Fig. 3(b) shows negative ΔV_{GB} after SHEi stress (curve 2) with V_{GB} = 12 V and $V_{DB} = V_{SB}$ = 10 V, due to positive ΔQ_{OT}, as anticipated [15] by the electron-impact emission of electrons trapped at the neutral oxygen vacancy, $V_O^0 + e^* \rightarrow V_O^+ + 2e^-$. Fig. 3(c) demonstrates the successive stresses that gave negative ΔQ_{OT} first and then positive ΔQ_{OT}, which is the so-called turn-around effect coined by Young [21]. Curve 1, showing positive ΔV_{GB}, was measured after a short (~1 s) CHEi stress at $V_{GB} = V_{DB} \simeq 15$ V with the source floating, indicating negative ΔQ_{OT} due to capture of the electrons injected into the oxide

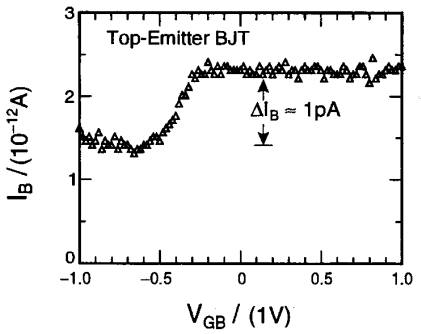


Fig. 4. Sensitivity test of the top-emitter I_B measurement of interface traps of an unstressed BiMOS with nMOST and npnBJT at $V_{EB} = -0.3$ V and 297 K.

along the entire length of the strongly inverted n-channel because $V_{GB} \gg V_{TH}$. Curve 2, showing negative ΔV_{GB}, was measured after an additional 500 s stress, indicating that some originally trapped electrons (not the captured electrons during the short stress) are emitted via a second pathway, the impact emission just described for Fig. 3(b).

The stress condition used in Fig. 3(c), with source floating or shorted to drain, approximates that in BJT under emitter-base junction reverse-bias stress. Thus, the bottom-emitter measurement configuration can be used to study the fundamental degradation mechanisms in BJT even without a separated gate over the emitter-base junction [3].

The sensitivity of this new DCIV is demonstrated experimentally in Fig. 4 which gives a sensitivity limit or minimum measurable $S_0 < \sim 1$ cm/s and $N_{IT} \leq 10^9$ cm^{-2}.

III. Summary

A new DCIV method for separating the oxide charge and interface traps in oxidized silicon is presented. It has several unique features difficult to attain previously. 1) It is a purely dc method resulting in ease of instrumentation and extremely high detection sensitivity. 2) It gives true D_{IT}, not affected by inhomogeneity and hence usable for profiling D_{IT} and Q_{IT}. 3) It has very high D_{IT} sensitivity in presence of large Q_{OT}. 4) It is applicable to submicrometer area devices in conventional production CMOS and nMOST junction well structure. 5) It can monitor the degradation kinetics of both MOST's and BJT's.

References

[1] C.-T. Sah, *Fundamentals of Solid-State Electronics.* River Edge, NJ and Singapore: World Scientific, Nov. 1991.

[2] ——, *Fundamentals of Solid-State Electronics—Study Guide.* River Edge, NJ and Singapore: World Scientific, Dec. 1993.

[3] A. Neugroschel, C.-T. Sah, and M. S. Carroll, "Current-acceleration for rapid time-to-failure determination of bipolar junction transistors under emitter-base reverse-bias stress," *IEEE Trans. Electron Devices,* vol. 42, no. 7, pp. 1380–1383, July 1995. (For a complete account of the original models proposed by Sah and Neugroschel, see SRC publication C94320.)

[4] K. M. Han and T. Nishida, "Sequential substrate and channel hot electron injection to separate oxide and interface traps in n-MOST," *Solid-State Electron.,* vol. 38, pp. 105–113, Jan. 1995; for a review of the BiMOS structure and measurement method, see T. Nishida, *Solid-State Electron.,* vol. 35, no. 3, pp. 357–369, March 1992.

[5] C.-T. Sah, "A new semiconductor tetrode-the surface-potential controlled transistor," in *Proc. of IRE,* vol. 49, Nov. 1961, pp. 1623–1634.

[6] ——, "Effect of surface recombination and channel on p-n junction and transistor characteristics," *IRE Trans. Electron Devices,* vol. ED-9, no. 1, pp. 94–108, Jan. 1962.

[7] J. F. Verwey, "On the mechanism of h_{FE} degradation by emitter-base reverse current stress," *Microelectronics and Reliability,* vol. 9, pp. 425–432, 1970.

[8] ——, "On the emitter degradation by avalanche breakdown in planar transistors," *Solid-State Electron.,* vol. 14, pp. 775–782, Sept. 1971.

[9] B. A. McDonald, "Avalanche degradation of h_{FE}," *IEEE Trans. Electron Devices* vol. ED-17, pp. 871–878, Oct. 1970.

[10] H. H. Berger, "The injection model-A structure oriented model for merged transistor logic," *IEEE J. Solid-State Circuits,* vol. SC-9, pp. 218–227, Oct. 1972.

[11] H. E. Wulms, "Base current of I^2L transistors," *IEEE J. Solid-State Circuits,* vol. SC-12, pp. 143–150, Apr. 1977.

[12] M. W. Hillen and J. Holsbrink, "The base current recombining at the oxidized silicon surface," *Solid-State Electron.,* vol. 26, pp. 453–463, May 1983.

[13] M. Y. Ghannam, R. P. Mertens, R. F. De Keersmaecker, and R. J. Van Overstraeten, "Electrical characterization of the boron-doped Si-SiO_2 interface," *IEEE Trans. Electron Devices,* vol. ED-32, pp. 1264–1271, July 1985.

[14] S. E. Thompson and T. Nishida, "Positive charge generation in SiO_2 by electron-impact emission of trapped electron," *J. Appl. Phys.,* vol. 72, pp. 4683–4695, Nov. 1992.

[15] C.-T. Sah and T. Nishida, "Mechanisms of electronic trapping in SiO_2 on Si," *The Physics of Semiconductors.* Singapore: World Scientific, vol. 1, pp. 28–40; also presented as the Plenary Presentation, 21th Int. Conf. Physics of Semiconductors, Beijing, Aug. 10–14, 1992.

[16] A. S. Grove and D. J. Fitzgerald, "Surface effects on p-n junctions: Characteristics of surface space-charge regions under non-equilibrium conditions," *Solid-State Electron.,* vol. 9, pp. 783–806, Aug. 1966.

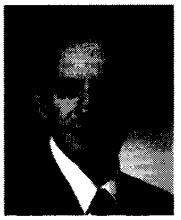
[17] J. Bardeen, "Surface states and rectification at a metal semiconductor contact," *Phys. Rev.,* vol. 71, pp. 717–727, May 15, 1947.

[18] C. A. Mead and W. G. Spitzer, "Fermi-level position at metal-semiconductor interfaces," *Phys. Rev.,* vol. 134, no. A713, 1964.

[19] T. P. Ma, private communication at the SRC Annual Project Review, April 13, 1994.

[20] C.-T. Sah, *Fundamentals of Solid-State Electronics.* River Edge, NJ and Singapore: World Scientific, Nov. 1991, 683.11, p. 666.

[21] D. R. Young, private communication to C.-T. Sah, 1975. See also D. R. Young, E. A. Irene, D. J. DiMaria, and R. F. DeKeersmaecker, *J. Appl. Phys.,* vol. 50, no. 6366, 1979.



Arnost Neugroschel (M'76–SM'80–F'90) received the degree in electrical engineering from the Slovak Polytechnical Institute, Bratislava, Czechoslovakia, in 1965, and the Ph.D. degree in electrical engineering from the Technicon–Israel Institute of Technology, Haifa, in 1973.

From 1973 to 1975, he was a Research Associate at the University of Illinois, Urbana. In 1975, he joined the Department of Electrical Engineering, University of Florida, Gainesville, where he is now a Professor of Electrical Engineering. He spent the summer of 1982 at the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, where he worked on the properties of polysilicon emitter contacts in bipolar transistors. During the academic year 1985–1986 he spent one semester at the Interuniversity Microelectronic Center (IMEC) in Leuven, Belgium, studying the properties of amorphous silicon. His current research interests are semiconductor device physics and reliability, and material and device characterization. He holds two U.S. patents.

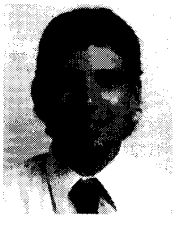
Dr. Neugroschel was elected a Fellow of the IEEE in 1990 for "contributions to material characterization for transistor and solar cell analysis and design."

Chih-Tang Sah (F'69) received two B.S. degrees, in electrical engineering and physics, in 1953 from the University of Illinois, Urbana-Champaign, and the M.S. and Ph.D. degrees from Stanford Univeristy, Stanford, CA, in 1954 and 1956, respectively.

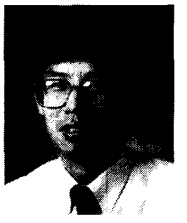
His industrial career began with William Shockley in 1956, and continued at the Fairchild Semiconductor Corporation from 1959 to 1964, where he directed and managed a 65-member physics department which developed the first-generation silicon integrated circuit manufacturing technology. He was a Professor of Electrical Engineering and a Professor of Physics at the University of Illinois, from 1961 to 1988, where he guided 40 doctoral theses to completion in physics or electrical engineering. He has been the Robert C. Pittman Eminent Scholar and a Graduate Research Professor at the University of Florida, Gainesville, since 1988. He has published about 300 journal articles and given more than 100 invited lectures in China, Europe, Japan, Taiwan, and the United States on transistor physics, technology, and evolution history. At the University of Florida, he taught the undergraduate device core course and wrote the textbook *Fundamental of Solid-State Electronics* in 1991 and its *Study Guide* in 1993. His recent research interests have focused on the fundamental degradation mechanisms in deep submicrometer silicon MOS and bipolar transistors.

Prof. Sah was the recipient of the IRE Browder J. Thompson Best Paper Prize for an author under 30, the J. J. Ebers and Jack Morton Awards from the IEEE Electron Device Society, the Franklin Institute Award for stable MOS transistor development, the first Achievement Award in High Technology from the Asian American Manufacturer Association, and the *Doctor Honoris Causa* from the University of Leuven, Belgium. He was listed as one of the 1000 most cited scientists during 1965–1978 in a survey by the Institute of Scientific Information. He is a fellow of the American Physical Society and a member of the U.S. National Academy of Engineering.

K. Michael Han (S'95) was born in Singapore in 1966. He received the B.S.E.E. degree (high honors) and the M.S.E.E. degree from the University of Florida, Gainesville, in 1990 and 1992, respectively. He is currently pursuing the Ph.D. degree in electrical engineering at the University of Florida. His research interests include reliability studies of advanced MOST/BJT devices, semiconductor device physics, advanced semiconductor processings, and analog circuit designs.



Michael S. Carroll was born in Madison, WI, in 1968. He received the B.S. degree in electrical engineering (high honors) from the University of Florida, Gainesville, in 1990. He received the M.S. degree in electrical engineering from Purdue University, West Lafayette, IN, in 1992. He is currently working toward the Ph.D. degree in electrical engineering at the University of Florida, Gainesville. He joined the Florida Solid-State Electronics Laboratory in August 1992. His doctoral research involves the modeling of reliability of advanced submicrometer silicon bipolar transistors. His interests are in submicrometer transistor technology development and reliability.



Toshikazu Nishida (S'84–M'88) was born in Urbana, IL, in 1963. He received the B.S. degree in engineering physics in 1984, the M.S. degree in 1985, and the Ph.D. degree in August 1988 in electrical engineering, all from the University of Illinois at Urbana-Champaign.

He is currently an Associate Professor of Electrical and Computer Engineering at the University of Florida, Gainesville. He has authored or co-authored more than 20 journal and conference articles, on topics such as the recombination properties of gold impurity centers in silicon, the effect of oxide trap generation on the reliability of a MOS inverter circuit, the threshold bond-breaking voltage and electric field of oxide traps, the electron and hole mobilities in the silicon surface inversion layer, profiling of thermal donors in Crochralski silicon, and hydrogenation of boron acceptor in silicon exposed to hydrogen-containing liquids and gases.

Dr. Nishida is a member of the American Physical Society, the Materials Research Society, and the American Association for the Advancement of Science.

Jack Theodore Kavalieros was born in Thessaloniki, Greece, on January 20, 1967. He received the B.S. and M.S. degrees in electrical engineering from the University of Florida, Gainesville, in 1989 and 1991, respectively. Since 1991, he has been working towards the Ph.D. degree at the University of Florida. His present interests include MOS device physics and in particular the reliability of the gate oxide layer.

He was the recipient of the Robert C. Pittman Fellowship in 1991. During the summers of 1989 and 1994, he interned at National Semiconductor Corporation and at the Intel Corporation, respectively.

Yi Lu (M'95) was born in China in 1964. He received the B.S. degree from the University of Science and Technology of China in 1986, the M.A. degree in physical chemistry from Washington University, St. Louis, MO, in 1988, and the M.S. and Ph.D. degrees in electrical engineering from the University of Florida, Gainesville, with an Intel Foundation Graduate Fellowship under the direction of Prof. Chih-Tang Sah.

He joined the Intel Corporation in February 1995.